SIT329: Advance Embedded Systems

Group Pass Task 10.1P
Sprint 3 Plan

Team members: Saksham Behal, Tushar Sharma, Manav Singh
Team name : The Boys

Sprint 2: Backlog:

- Serial communication.

Sprint 3 Planning:

In Sprint 2, the team made significant progress on their respective tasks related to FPGA development and image processing. Now, for Sprint 3, let's build on that foundation and outline the tasks and responsibilities for each team member:

1. **Saksham Behal:**
   - Continue working on the Verilog code to improve the code to directly convert binary pixels to RGB rather than hexadecimal binary image conversion to RGB format.
   - Optimize the code for simplicity and clarity.
   - Ensure the code functions correctly when controlling LEDs based on pixel values.
   - Created a 2D data array to map the pixels for easier display.
   - Made a test bench to feed the data and test the code for intended functionality.

2. **Tushar:**
   - Serial communication between DE10 Nano FPGA and the embedded Linux system.
   - Research and implement the necessary network configurations for proper communication between Linux and FPGA.
   - Develop a mechanism to send the RBF file from Linux to the DE10 Nano FPGA for flashing.

3. **Manav :**
   - Continue assisting Tushar with network setup.
   - Develop Python scripts to assist in mapping and data transfer between the Linux system and FPGA.

- Research any additional requirements or optimizations related to FPGA mapping.
- Provide support for hardware setup, especially for Arduino headers and LED connections.

Team Collaboration:

- Collaborate closely with each other to ensure seamless integration of the FPGA code, Linux system, and data transfer mechanisms.
- Regularly communicate and update progress on GitHub or another version control system.
- Compile the Verilog code in quartus prime.
- Test the overall system functionality using the physical hardware setup, as it provides a tangible demonstration of the code's output.

General Tasks:

- Keep detailed records of all work done, issues faced, and solutions implemented.
- Maintain regular communication through team meetings to discuss progress and address any challenges.
- Document the entire development process comprehensively, including code comments, documentation files, and user guides.

By the end of Sprint 3, the team should aim to have a fully functional system where the FPGA can receive Verilog code from the Linux system and display the corresponding pixel values on the connected LEDs. Additionally, ensure that the FPGA can be reprogrammed from Linux using the RBF file conversion.