ECE 382 Embedded Systems I

Conditional jumps support program branching relative to the PC and do not affect the status bits. The possible jump range is from –511 to +512 words relative to the PC value at the jump instruction. The 10-bit program-counter offset is treated as a signed 10-bit value that is doubled and added to the program counter:

$PC_{new} = PC_{old} + 2 + PC_{offset} \times 2$

Word Operations (W) = 0
Byte Operations (B) = 1

Table 1. Source Addressing Modes (As)

Address Mode	*As	Registers	Syntax	Operation
Register	00	R0-R2, R4-R15	R*n*	Register Contents.
0	00	R3	#0	0 Constant
Symbolic	01	R0	*addr*	(PC+next word) points to operand. (*x*(PC))
Indexed	01	R1, R4-R15	*x*(R*n*)	(R*n*+*x*) points to operand. *x* is next code word.
Absolute	01	R2	&*addr*	Next code word is the absolute address. (*x*(SR))
+1	01	R3	#1	+1 Constant
Indirect	10	R0-R1,R4-R15	@R*n*	R*n* points to operand.
+4	10	R2	#4	+4 Constant
+2	10	R3	#2	+2 Constant
Immediate	11	R0	#*N*	Next word is the constant *N*. (@PC+)
Indirect auto-inc	11	R1,R4-R15	@R*n*+	R*n* points to operand, R*n* is incremented (1 or 2).
+8	11	R2	#8	+8 Constant
-1	11	R3	#-1	-1 Constant

*Bits 4 and 5 in Single (Table 3) and Double (Table 5) Operand Instructions

Table 2. Destination Addressing Modes (Ad)

Address Mode	*Ad	Registers	Syntax	Operation
Register	0	R0-R2, R4-R15	R*n*	Register Contents.
0	0	R3	#0	Bit bucket
Symbolic	1	R0	*addr*	(PC+next word) points to operand. (*x*(PC))
Indexed	1	R1, R4-R15	*x*(R*n*)	(R*n*+*x*) points to operand. *x* is next code word.
Absolute	1	R2	&*addr*	Next code word is the absolute address. (*x*(SR))

*Bit 7 in (Table 5) Operand Instructions

Table 3. Single Operand Instructions

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
9-bit Opcode									b/w	As		D/S Register			

Mnemonic	Opcode									V	N	Z	C	Operation	Description
RRC	0	0	0	1	0	0	0	0	0	•	•	•	•	C→MSB→…LSB→C	Roll dst right through C
SWPB	0	0	0	1	0	0	0	0	1	–	–	–	–	Swap bytes	Swap bytes
RRA	0	0	0	1	0	0	0	1	0	0	•	•	•	MSB→MSB→…LSB→C	Roll destination right
SXT	0	0	0	1	0	0	0	1	1	0	•	•	z	bit 7→bit 8…bit 15	Sign extend destination
PUSH	0	0	0	1	0	0	1	0	0	–	–	–	–	SP-2→SP, src→@SP	Push source on stack
CALL	0	0	0	1	0	0	1	0	1	–	–	–	–	SP-2→SP, PC+2→@SP, dst→PC	Subroutine call
RETI	0	0	0	1	0	0	1	1	0	•	•	•	•	@SP+→SR, @SP+→PC	Return from interrupt

Table 4. Jump Instructions

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6-bit Opcode						10-bit, 2's complement PC Offset									

Mnemonic	Opcode						V	N	Z	C	Description
JNZ/JNE	0	0	1	0	0	0	–	–	0	–	Jump if not equal
JZ/JEQ	0	0	1	0	0	1	–	–	1	–	Jump if equal
JNC/JLO	0	0	1	0	1	0	–	–	–	0	Jump if carry flag equal to zero
JC/JHS	0	0	1	0	1	1	–	–	–	1	Jump if carry flag equal to one
JN	0	0	1	1	0	0	–	1	–	–	Jump if negative (N = 1)
JGE	0	0	1	1	0	1	•	•	–	–	Jump if greater than or equal (N = V)
JL	0	0	1	1	1	0	•	•	–	–	Jump if lower (N ≠ V)
JMP	0	0	1	1	1	1	–	–	–	–	Unconditional jump

Table 5. Double Operand Instructions

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4-bit Opcode				Source Register				Ad	b/w	As		Destination Register			

Mnemonic	Opcode				V	N	Z	C	Operation	Description
MOV	0	1	0	0	–	–	–	–	src→dst	Move source to destination
ADD	0	1	0	1	•	•	•	•	src+dst→dst	Add source to destination
ADDC	0	1	1	0	•	•	•	•	src+dst+C→dst	Add src and C to dst
SUBC	0	1	1	1	•	•	•	•	dst+.not.src+C→dst	Subtract src and NOT C from dst
SUB	1	0	0	0	•	•	•	•	dst+.not.src+1→dst	Subtract source from destination
CMP	1	0	0	1	•	•	•	•	dst-src	Compare source to destination
DADD	1	0	1	0	•	•	•	•	src+dst+C→dst(dec)	Decimal add src and C to dst
BIT	1	0	1	1	0	•	•	z	src.and.dst	Test bits in destination
BIC	1	1	0	0	–	–	–	–	.not.src.and.dst→dst	Clear bits in destination
BIS	1	1	0	1	–	–	–	–	src.or.dst→dst	Set bits in destination
XOR	1	1	1	0	•	•	•	z	src.xor.dst→dst	XOR source with destination
AND	1	1	1	1	0	•	•	z	src.and.dst→dst	AND source with destination

Status Register: • = bit affected, – = bit not affected, 0 = cleared, 1 = set, z = same as Z

Table 6. Source Operands Using Status (R2) and Constant Generator (R3) Registers

Register	As	Addr Mode	Syntax	Constant	Remarks
R2	00	Register	–	–	Register mode
R2	01	*x*(R2)	*addr*	(0)	Absolute address mode, next word contains address
R2	10	@R2	#4	0x0004	+4
R2	11	@R2+	#8	0x0008	+8
R3	00	R3	#0	0x0000	0
R3	01	*x*(R3)	#1	0x0001	+1, No extension word
R3	10	@R3	#2	0x0002	+2
R3	11	@R3+	#-1	0xFFFF	-1

Mnemonic		Description	Operation	V	N	Z	C
ADC(.B)	dst	Add C to destination	dst + C → dst	*	*	*	*
ADD(.B)	src,dst	Add source to destination	src + dst → dst	*	*	*	*
ADDC(.B)	src,dst	Add source and C to destination	src + dst + C → dst	*	*	*	*
AND(.B)	src,dst	AND source and destination	src .and. dst → dst	0	*	*	*
BIC(.B)	src,dst	Clear bits in destination	.not.src .and. dst → dst	-	-	-	-
BIS(.B)	src,dst	Set bits in destination	src .or. dst → dst	-	-	-	-
BIT(.B)	src,dst	Test bits in destination	src .and. dst	0	*	*	*
BR	dst	Branch to destination	dst → PC	-	-	-	-
CALL	dst	Call destination	PC+2 → stack, dst → PC	-	-	-	-
CLR(.B)	dst	Clear destination	0 → dst	-	-	-	-
CLRC		Clear C	0 → C	-	-	-	0
CLRN		Clear N	0 → N	-	0	-	-
CLRZ		Clear Z	0 → Z	-	-	0	-
CMP(.B)	src,dst	Compare source and destination	dst - src	*	*	*	*
DADC(.B)	dst	Add C decimally to destination	dst + C → dst (decimally)	*	*	*	*
DADD(.B)	src,dst	Add source and C decimally to dst	src + dst + C → dst (decimally)	*	*	*	*
DEC(.B)	dst	Decrement destination	dst - 1 → dst	*	*	*	*
DECD(.B)	dst	Double-decrement destination	dst - 2 → dst	*	*	*	*
DINT		Disable interrupts	0 → GIE	-	-	-	-
EINT		Enable interrupts	1 → GIE	-	-	-	-
INC(.B)	dst	Increment destination	dst +1 → dst	*	*	*	*
INCD(.B)	dst	Double-increment destination	dst+2 → dst	*	*	*	*
INV(.B)	dst	Invert destination	.not.dst → dst	*	*	*	*
JC/JHS	label	Jump if C set/Jump if higher or same		-	-	-	-
JEQ/JZ	label	Jump if equal/Jump if Z set		-	-	-	-
JGE	label	Jump if greater or equal		-	-	-	-
JL	label	Jump if less		-	-	-	-
JMP	label	Jump PC + 2 × offset → PC		-	-	-	-
JN	label	Jump if N set		-	-	-	-
JNC/JLO	label	Jump if C not set/Jump if lower		-	-	-	-
JNE/JNZ	label	Jump if not equal/Jump if Z not set		-	-	-	-
MOV(.B)	src,dst	Move source to destination src → dst		-	-	-	-
NOP		No operation		-	-	-	-
POP(.B)	dst	Pop item from stack to destination	@SP → dst, SP+2 → SP	-	-	-	-
PUSH(.B)	src	Push source onto stack	SP - 2 → SP, src → @SP	-	-	-	-
RET		Return from subroutine	@SP → PC, SP + 2 → SP	-	-	-	-
RETI		Return from interrupt		*	*	*	*
RLA(.B)	dst	Rotate left arithmetically		*	*	*	*
RLC(.B)	dst	Rotate left through C		*	*	*	*
RRA(.B)	dst	Rotate right arithmetically		0	*	*	*
RRC(.B)	dst	Rotate right through C		*	*	*	*
SBC(.B)	dst	Subtract not(C) from destination	dst + 0FFFFh + C → dst	*	*	*	*
SETC		Set C	1 → C	-	-	-	1
SETN		Set N	1 → N	-	1	-	-
SETZ		Set Z	1 → Z	-	-	1	-
SUB(.B)	src,dst	Subtract source from destination	dst + .not.src + 1 → dst	*	*	*	*
SUBC(.B)	src,dst	Subtract source and not(C) from	dst dst + .not.src + C → dst	*	*	*	*
SWPB	dst	Swap bytes		-	-	-	-
SXT	dst	Extend sign		0	*	*	*
TST(.B)	dst	Test destination	dst + 0FFFFh + 1	0	*	*	1
XOR(.B)	src,dst	Exclusive OR source and destination	src .xor. dst → dst	*	*	*	*

Legend: * = Status bit cleared or set on results - = Status bit not affected
0 = Status bit always cleared 1 = Status bit always set

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="3">Opcode</td><td>W=0/B=1</td><td colspan="2">As</td><td colspan="4">Dest Reg</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td colspan="3">Condition</td><td colspan="10">PC Offset (10-Bit)</td></tr>
<tr><td colspan="4">Opcode</td><td colspan="4">Source Reg</td><td>Ad</td><td>W=0/B=1</td><td colspan="2">As</td><td colspan="4">Dest Reg</td></tr>
</table>

3.4.4.3 Format-III (Jump) Instruction Cycles and Lengths

All jump instructions require one code word, and take two CPU cycles to execute, regardless of whether the jump is taken or not.

Table 3-15. Format-II Instruction Cycles and Lengths

	No. of Cycles				
Addressing Mode	RRA, RRC SWPB, SXT	PUSH	CALL	Length of Instruction	Example
Rn	1	3	4	1	`SWPB R5`
@Rn	3	4	4	1	`RRC @R9`
@Rn+	3	5	5	1	`SWPB @R10+`
#N	(See note)	4	5	2	`CALL #0F000h`
X(Rn)	4	5	5	2	`CALL 2(R7)`
EDE	4	5	5	2	`PUSH EDE`
&EDE	4	5	5	2	`SXT &EDE`

Table 3-16. Format 1 Instruction Cycles and Lengths

Addressing Mode					
Src	Dst	No. of Cycles	Length of Instruction	Example	
Rn	Rm	1	1	MOV	R5,R8
	PC	2	1	BR	R9
	x(Rm)	4	2	ADD	R5,4(R6)
	EDE	4	2	XOR	R8,EDE
	&EDE	4	2	MOV	R5,&EDE
@Rn	Rm	2	1	AND	@R4,R5
	PC	2	1	BR	@R8
	x(Rm)	5	2	XOR	@R5,8(R6)
	EDE	5	2	MOV	@R5,EDE
	&EDE	5	2	XOR	@R5,&EDE
@Rn+	Rm	2	1	ADD	@R5+,R6
	PC	3	1	BR	@R9+
	x(Rm)	5	2	XOR	@R5,8(R6)
	EDE	5	2	MOV	@R9+,EDE
	&EDE	5	2	MOV	@R9+,&EDE
#N	Rm	2	2	MOV	#20,R9
	PC	3	2	BR	#2AEh
	x(Rm)	5	3	MOV	#0300h,0(SP)
	EDE	5	3	ADD	#33,EDE
	&EDE	5	3	ADD	#33,&EDE
x(Rn)	Rm	3	2	MOV	2(R5),R7
	PC	3	2	BR	2(R6)
	TONI	6	3	MOV	4(R7),TONI
	x(Rm)	6	3	ADD	4(R4),6(R9)
	&TONI	6	3	MOV	2(R4),&TONI
EDE	Rm	3	2	AND	EDE,R6
	PC	3	2	BR	EDE
	TONI	6	3	CMP	EDE,TONI
	x(Rm)	6	3	MOV	EDE,0(SP)
	&TONI	6	3	MOV	EDE,&TONI
&EDE	Rm	3	2	MOV	&EDE,R8
	PC	3	2	BRA	&EDE
	TONI	6	3	MOV	&EDE,TONI
	x(Rm)	6	3	MOV	&EDE,0(SP)
	&TONI	6	3	MOV	&EDE,&TONI

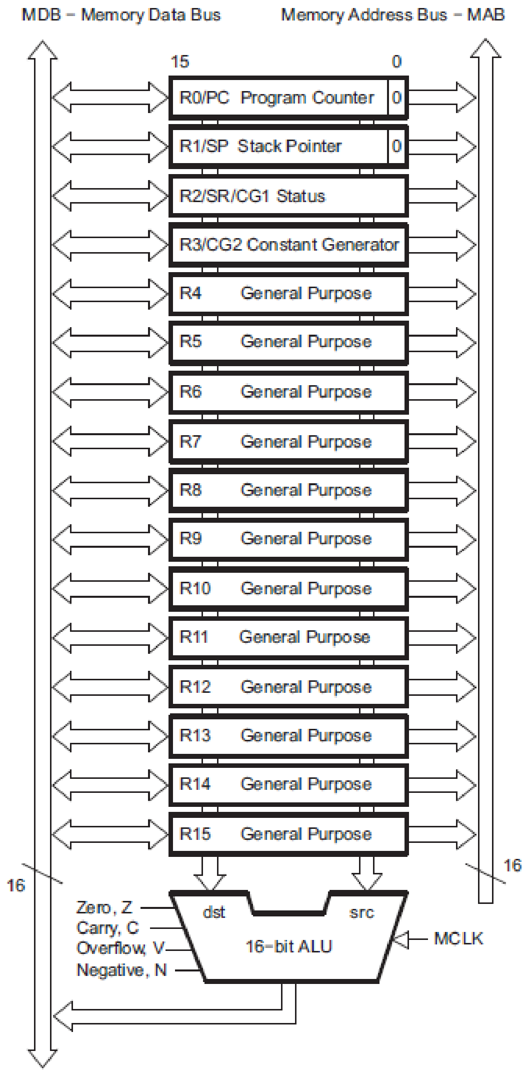


Figure 3-1. CPU Block Diagram

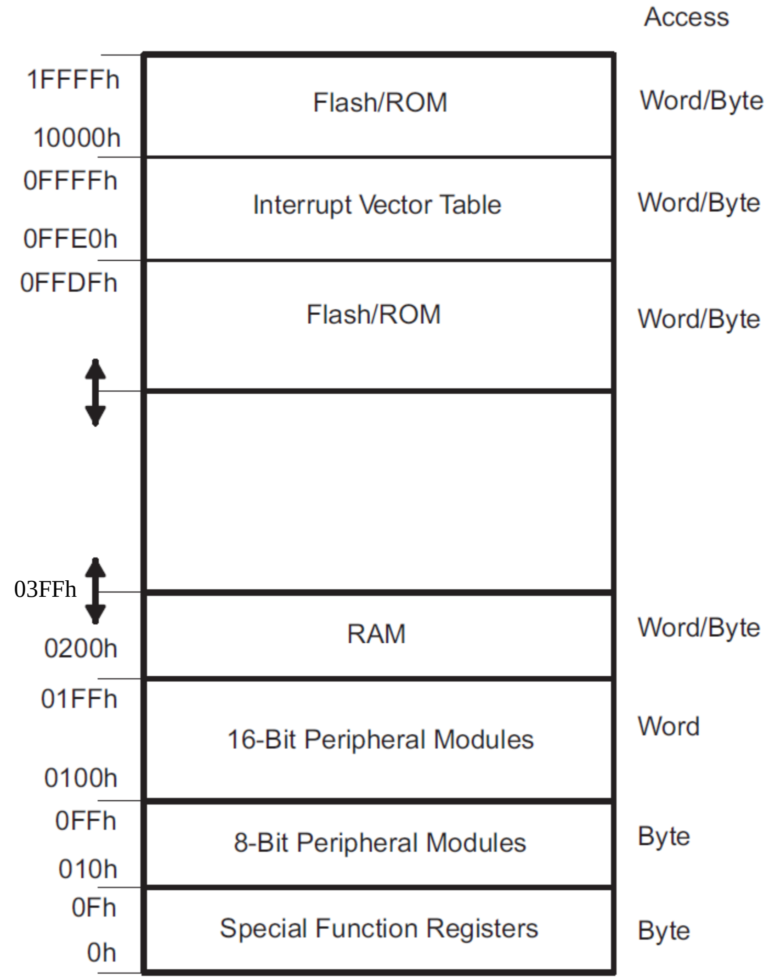
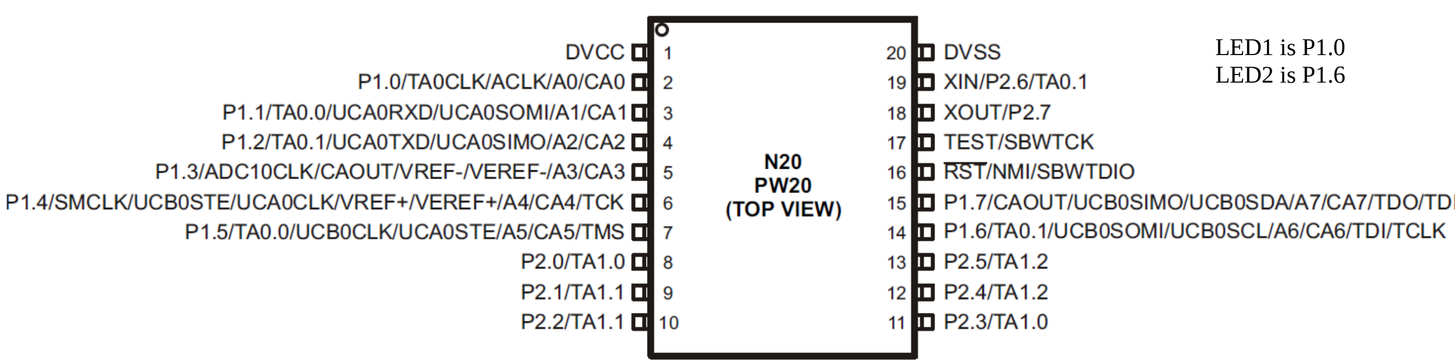


Figure 3-6. Status Register Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							V	SCG1	SCG0	OSC OFF	CPU OFF	GIE	N	Z	C
rw-0							rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0



LED1 is P1.0
LED2 is P1.6

8.2.1 Input Register PxIN

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function.

Bit = 0: The input is low

Bit = 1: The input is high

NOTE: Writing to Read-Only Registers PxIN

Writing to these read-only registers results in increased current consumption while the write attempt is active.

8.2.2 Output Registers PxOUT

Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function, output direction, and the pullup/down resistor is disabled.

Bit = 0: The output is low

Bit = 1: The output is high

If the pin's pullup/pulldown resistor is enabled, the corresponding bit in the PxOUT register selects pullup or pulldown.

Bit = 0: The pin is pulled down

Bit = 1: The pin is pulled up

8.2.4 Pullup/Pulldown Resistor Enable Registers PxREN

Each bit in each PxREN register enables or disables the pullup/pulldown resistor of the corresponding I/O pin. The corresponding bit in the PxOUT register selects if the pin is pulled up or pulled down.

Bit = 0: Pullup/pulldown resistor disabled

Bit = 1: Pullup/pulldown resistor enabled

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
CA0/		CA0	X	X	X	0	1 (y = 0)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0
		TA0.CCI0A	0	1	0	0	0
UCA0RXD/		UCA0RXD	from USCI	1	1	0	0
UCA0SOMI/		UCA0SOMI	from USCI	1	1	0	0
A1[2]/		A1	X	X	X	1 (y = 1)	0
CA1/		CA1	X	X	X	0	1 (y = 1)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Table 17. Port P1 (P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0	0	0	0
ADC10CLK[2]/		ADC10CLK	1	1	0	0	0
CAOUT/		CAOUT	1	1	1	0	0
A3[2]/		A3	X	X	X	1 (y = 3)	0
VREF-[2]/		VREF-	X	X	X	1	0
VEREF-[2]/		VEREF-	X	X	X	1	0
CA3/		CA3	X	X	X	0	1 (y = 3)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Table 18. Port P1 (P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
SMCLK/		SMCLK	1	1	0	0	0	0
UCB0STE/		UCB0STE	from USCI	1	1	0	0	0
UCA0CLK/		UCA0CLK	from USCI	1	1	0	0	0
VREF+[2]/		VREF+	X	X	X	1	0	0
VEREF+[2]/		VEREF+	X	X	X	1	0	0
A4[2]/		A4	X	X	X	1 (y = 4)	0	0
CA4		CA4	X	X	X	0	0	1 (y = 4)
TCK/		TCK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Table 19. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0	0
UCB0CLK/		UCB0CLK	from USCI	1	1	0	0	0
UCA0STE/		UCA0STE	from USCI	1	1	0	0	0
A5[2]/		A5	X	X	X	1 (y = 5)	0	0
CA5		CA5	X	X	X	0	0	1 (y = 5)
TMS		TMS	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0	0
UCB0SOMI/		UCB0SOMI	from USCI	1	1	0	0	0
UCB0SCL/		UCB0SCL	from USCI	1	1	0	0	0
A6[2]/		A6	X	X	X	1 (y = 6)	0	0
CA6		CA6	X	X	X	0	0	1 (y = 6)
TDI/TCLK/		TDI/TCLK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
UCB0SIMO/		UCB0SIMO	from USCI	1	1	0	0	0
UCB0SDA/		UCB0SDA	from USCI	1	1	0	0	0
A7[2]/		A7	X	X	X	1 (y = 7)	0	0
CA7		CA7	X	X	X	0	0	1 (y = 7)
CAOUT		CAOUT	1	1	0	0	0	0
TDO/TDI/		TDO/TDI	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

NOTE: Initializing or Re-Configuring the USCI Module

The recommended USCI initialization/re-configuration process is:

1. Set UCSWRST (BIS.B #UCSWRST,&UCxCTL1)
2. Initialize all USCI registers with UCSWRST=1 (including UCxCTL1)
3. Configure ports
4. Clear UCSWRST via software (BIC.B #UCSWRST,&UCxCTL1)
5. Enable interrupts (optional) via UCxRXIE and/or UCxTXIE

16.4.1 UCAxCTL0, USCI_Ax Control Register 0, UCBxCTL0, USCI_Bx Control Register 0

7	6	5	4	3	2	1	0
UCCKPH	UCCKPL	UCMSB	UC7BIT	UCMST	UCMODEx		UCSYNC=1
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	

UCCKPH Bit 7 Clock phase select.
- 0 Data is changed on the first UCLK edge and captured on the following edge.
- 1 Data is captured on the first UCLK edge and changed on the following edge.

UCCKPL Bit 6 Clock polarity select.
- 0 The inactive state is low.
- 1 The inactive state is high.

UCMSB Bit 5 MSB first select. Controls the direction of the receive and transmit shift register.
- 0 LSB first
- 1 MSB first

UC7BIT Bit 4 Character length. Selects 7-bit or 8-bit character length.
- 0 8-bit data
- 1 7-bit data

UCMST Bit 3 Master mode select
- 0 Slave mode
- 1 Master mode

UCMODEx Bits 2-1 USCI mode. The UCMODEx bits select the synchronous mode when UCSYNC = 1.
- 00 3-pin SPI
- 01 4-pin SPI with UCxSTE active high: slave enabled when UCxSTE = 1
- 10 4-pin SPI with UCxSTE active low: slave enabled when UCxSTE = 0
- 11 I^2C mode

UCSYNC Bit 0 Synchronous mode enable
- 0 Asynchronous mode
- 1 Synchronous mode

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.
- 00 UCLK
- 01 ACLK
- 10 SMCLK
- 11 SMCLK

UCRXEIE Bit 5 Receive erroneous-character interrupt-enable
- 0 Erroneous characters rejected and UCAxRXIFG is not set
- 1 Erroneous characters received will set UCAxRXIFG

UCBRKIE Bit 4 Receive break character interrupt-enable
- 0 Received break characters do not set UCAxRXIFG.
- 1 Received break characters set UCAxRXIFG.

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.
- 0 Not dormant. All received characters will set UCAxRXIFG.
- 1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.
- 0 Next frame transmitted is data
- 1 Next frame transmitted is an address

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.
- 0 Next frame transmitted is not a break
- 1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable
- 0 Disabled. USCI reset released for operation.
- 1 Enabled. USCI logic held in reset state.

15.4.3 UCAxBR0, USCI_Ax Baud Rate Control Register 0

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

15.4.4 UCAxBR1, USCI_Ax Baud Rate Control Register 1

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

UCBRx	7-0	Clock prescaler setting of the Baud rate generator. The 16-bit value of (UCAxBR0 + UCAxBR1 × 256) forms the prescaler value

15.4.5 UCAxMCTL, USCI_Ax Modulation Control Register

7	6	5	4	3	2	1	0
UCBRFx				UCBRSx			UCOS16
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCBRFx	Bits 7-4	First modulation stage select. These bits determine the modulation pattern for BITCLK16 when UCOS16 = 1. Ignored with UCOS16 = 0. Table 15-3 shows the modulation pattern.
UCBRSx	Bits 3-1	Second modulation stage select. These bits determine the modulation pattern for BITCLK. Table 15-2 shows the modulation pattern.
UCOS16	Bit 0	Oversampling mode enabled 0 Disabled 1 Enabled

15.4.7 UCAxRXBUF, USCI_Ax Receive Buffer Register

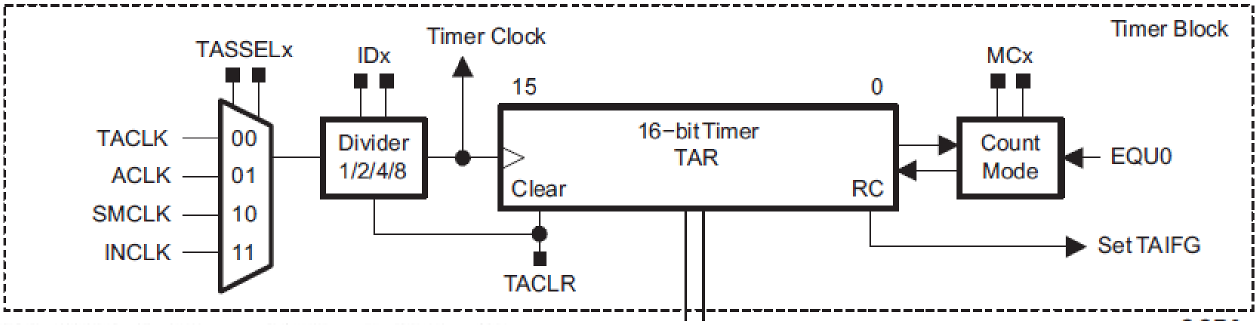
7	6	5	4	3	2	1	0
UCRXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCRXBUFx	Bits 7-0	The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCAxRXBUF resets the receive-error bits, the UCADDR or UCIDLE bit, and UCAxRXIFG. In 7-bit data mode, UCAxRXBUF is LSB justified and the MSB is always reset.

15.4.8 UCAxTXBUF, USCI_Ax Transmit Buffer Register

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCTXBUFx	Bits 7-0	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCAxTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.



12.3.1 TACTL, Timer_A Control Register

15	14	13	12	11	10	9	8
Unused						**TASSELx**	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
IDx		**MCx**		**Unused**	**TACLR**	**TAIE**	**TAIFG**
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Unused	Bits 15-10	Unused
TASSELx	Bits 9-8	Timer_A clock source select 00 TACLK 01 ACLK 10 SMCLK 11 INCLK (INCLK is device-specific and is often assigned to the inverted TBCLK) (see the device-specific data sheet)
IDx	Bits 7-6	Input divider. These bits select the divider for the input clock. 00 /1 01 /2 10 /4 11 /8
MCx	Bits 5-4	Mode control. Setting MCx = 00h when Timer_A is not in use conserves power. 00 Stop mode: the timer is halted. 01 Up mode: the timer counts up to TACCR0. 10 Continuous mode: the timer counts up to 0FFFFh. 11 Up/down mode: the timer counts up to TACCR0 then down to 0000h.
Unused	Bit 3	Unused
TACLR	Bit 2	Timer_A clear. Setting this bit resets TAR, the clock divider, and the count direction. The TACLR bit is automatically reset and is always read as zero.
TAIE	Bit 1	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0 Interrupt disabled 1 Interrupt enabled
TAIFG	Bit 0	Timer_A interrupt flag 0 No interrupt pending 1 Interrupt pending

12.3.4 TACCTLx, Capture/Compare Control Register

15	14	13	12	11	10	9	8
CMx		CCISx		SCS	SCCI	Unused	CAP
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r	r0	rw-(0)

7	6	5	4	3	2	1	0
OUTMODx			CCIE	CCI	OUT	COV	CCIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	r	rw-(0)	rw-(0)	rw-(0)

CMx Bit 15-14 Capture mode
- 00 No capture
- 01 Capture on rising edge
- 10 Capture on falling edge
- 11 Capture on both rising and falling edges

CCISx Bit 13-12 Capture/compare input select. These bits select the TACCRx input signal. See the device-specific data sheet for specific signal connections.
- 00 CCIxA
- 01 CCIxB
- 10 GND
- 11 V_{CC}

SCS Bit 11 Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock.
- 0 Asynchronous capture
- 1 Synchronous capture

SCCI Bit 10 Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit

Unused Bit 9 Unused. Read only. Always read as 0.

CAP Bit 8 Capture mode
- 0 Compare mode
- 1 Capture mode

OUTMODx Bits 7-5 Output mode. Modes 2, 3, 6, and 7 are not useful for TACCR0, because EQUx = EQU0.
- 000 OUT bit value
- 001 Set
- 010 Toggle/reset
- 011 Set/reset
- 100 Toggle
- 101 Reset
- 110 Toggle/set
- 111 Reset/set

CCIE Bit 4 Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag.
- 0 Interrupt disabled
- 1 Interrupt enabled

CCI Bit 3 Capture/compare input. The selected input signal can be read by this bit.

OUT Bit 2 Output. For output mode 0, this bit directly controls the state of the output.
- 0 Output low
- 1 Output high

COV Bit 1 Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software.
- 0 No capture overflow occurred
- 1 Capture overflow occurred

CCIFG Bit 0 Capture/compare interrupt flag
- 0 No interrupt pending
- 1 Interrupt pending

12.3.5 TAIV, Timer_A Interrupt Vector Register

15	14	13	12	11	10	9	8
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
0	**0**	**0**	**0**		**TAIVx**		**0**
r0	r0	r0	r0	r-(0)	r-(0)	r-(0)	r0

TAIVx Bits 15-0 Timer_A interrupt vector value

TAIV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
00h	No interrupt pending	-	
02h	Capture/compare 1	TACCR1 CCIFG	Highest
04h	Capture/compare 2[1]	TACCR2 CCIFG	
06h	Reserved	-	
08h	Reserved	-	
0Ah	Timer overflow	TAIFG	
0Ch	Reserved	-	
0Eh	Reserved	-	Lowest

[1] Not implemented in MSP430x20xx devices

Table 12-2. Output Modes

OUTMODx	Mode	Description
000	Output	The output signal OUTx is defined by the OUTx bit. The OUTx signal updates immediately when OUTx is updated.
001	Set	The output is set when the timer *counts* to the TACCRx value. It remains set until a reset of the timer, or until another output mode is selected and affects the output.
010	Toggle/Reset	The output is toggled when the timer *counts* to the TACCRx value. It is reset when the timer *counts* to the TACCR0 value.
011	Set/Reset	The output is set when the timer *counts* to the TACCRx value. It is reset when the timer *counts* to the TACCR0 value.
100	Toggle	The output is toggled when the timer *counts* to the TACCRx value. The output period is double the timer period.
101	Reset	The output is reset when the timer *counts* to the TACCRx value. It remains reset until another output mode is selected and affects the output.
110	Toggle/Set	The output is toggled when the timer *counts* to the TACCRx value. It is set when the timer *counts* to the TACCR0 value.
111	Reset/Set	The output is reset when the timer *counts* to the TACCRx value. It is set when the timer *counts* to the TACCR0 value.

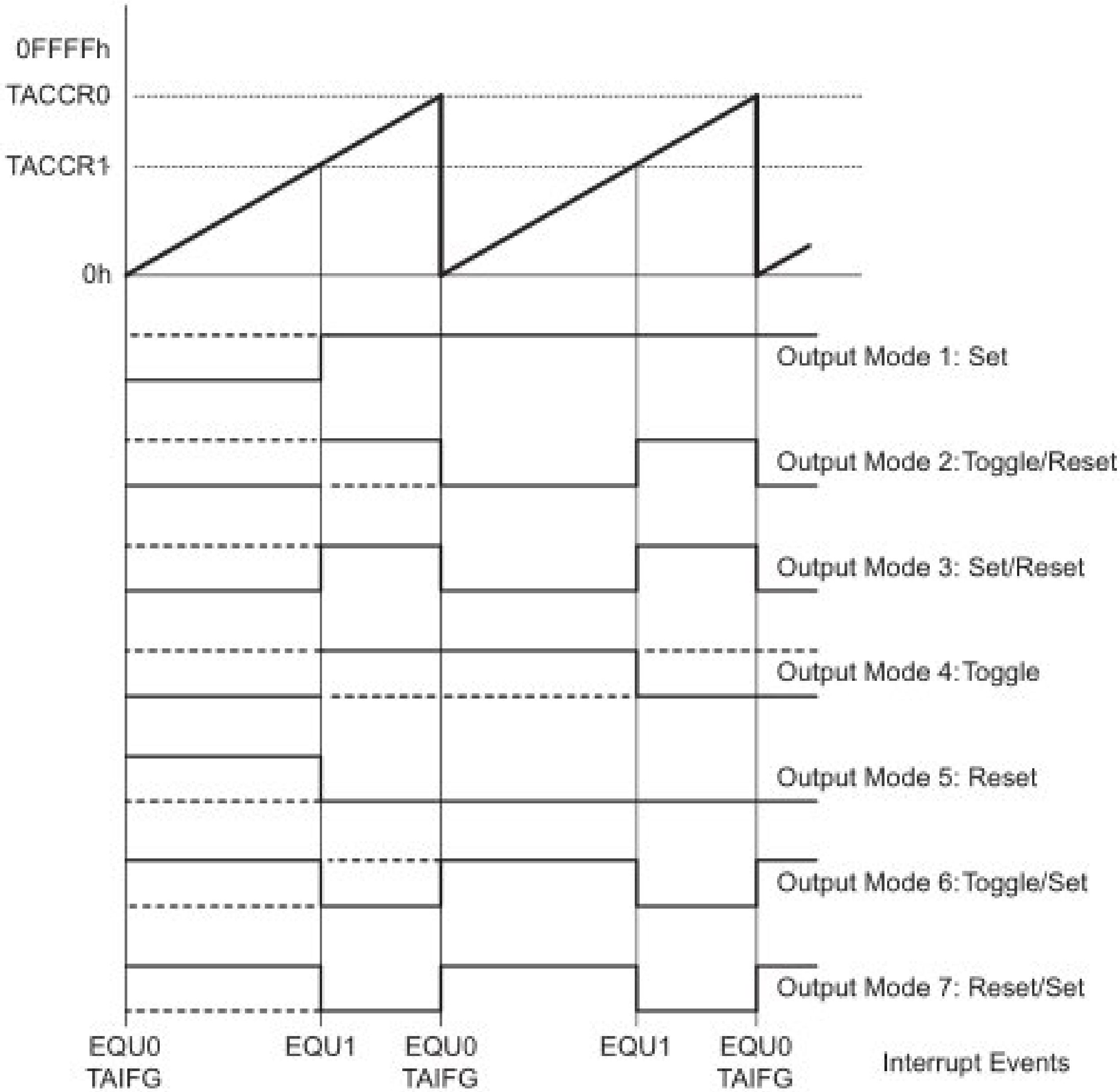


Figure 12-12. Output Example—Timer in Up Mode

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx			ADC10SHTx		ADC10SR	REFOUT	REFBURST
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC10ON	ADC10IE	ADC10IFG	ENC	ADC10SC
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ENC = 0

SREFx Bits 15-13 Select reference.
- 000 $V_{R+} = V_{CC}$ and $V_{R-} = V_{SS}$
- 001 $V_{R+} = V_{REF+}$ and $V_{R-} = V_{SS}$
- 010 $V_{R+} = V_{eREF+}$ and $V_{R-} = V_{SS}$. Devices with V_{eREF+} only.
- 011 V_{R+} = Buffered V_{eREF+} and $V_{R-} = V_{SS}$. Devices with V_{eREF+} pin only.
- 100 $V_{R+} = V_{CC}$ and $V_{R-} = V_{REF-}/ V_{eREF-}$. Devices with V_{eREF-} pin only.
- 101 $V_{R+} = V_{REF+}$ and $V_{R-} = V_{REF-}/ V_{eREF-}$. Devices with $V_{eREF+/-}$ pins only.
- 110 $V_{R+} = V_{eREF+}$ and $V_{R-} = V_{REF-}/ V_{eREF-}$. Devices with $V_{eREF+/-}$ pins only.
- 111 V_{R+} = Buffered V_{eREF+} and $V_{R-} = V_{REF-}/ V_{eREF-}$. Devices with $V_{eREF+/-}$ pins only.

ADC10SHTx Bits 12-11 ADC10 sample-and-hold time
- 00 4 × ADC10CLKs
- 01 8 × ADC10CLKs
- 10 16 × ADC10CLKs
- 11 64 × ADC10CLKs

ADC10SR Bit 10 ADC10 sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC10SR reduces the current consumption of the reference buffer.
- 0 Reference buffer supports up to ~200 ksps
- 1 Reference buffer supports up to ~50 ksps

REFOUT Bit 9 Reference output
- 0 Reference output off
- 1 Reference output on. Devices with V_{eREF+} / V_{REF+} pin only.

REFBURST Bit 8 Reference burst.
- 0 Reference buffer on continuously
- 1 Reference buffer on only during sample-and-conversion

MSC Bit 7 Multiple sample and conversion. Valid only for sequence or repeated modes.
- 0 The sampling requires a rising edge of the SHI signal to trigger each sample-and-conversion.
- 1 The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed

REF2_5V Bit 6 Reference-generator voltage. REFON must also be set.
- 0 1.5 V
- 1 2.5 V

REFON Bit 5 Reference generator on
- 0 Reference off
- 1 Reference on

ADC10ON Bit 4 ADC10 on
- 0 ADC10 off
- 1 ADC10 on

ADC10IE Bit 3 ADC10 interrupt enable
- 0 Interrupt disabled
- 1 Interrupt enabled

ADC10IFG Bit 2 ADC10 interrupt flag. This bit is set if ADC10MEM is loaded with a conversion result. It is automatically reset when the interrupt request is accepted, or it may be reset by software. When using the DTC this flag is set when a block of transfers is completed.
- 0 No interrupt pending
- 1 Interrupt pending

ENC Bit 1 Enable conversion
- 0 ADC10 disabled
- 1 ADC10 enabled

ADC10SC Bit 0 Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically.
- 0 No sample-and-conversion start
- 1 Start sample-and-conversion

22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
INCHx				SHSx		ADC10DF	ISSH
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
ADC10DIVx			ADC10SSELx		CONSEQx		ADC10BUSY
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0

INCHx Bits 15-12 Input channel select. These bits select the channel for a single-conversion or the highest channel for a sequence of conversions. Only available ADC channels should be selected. See device specific data sheet.

- 0000 A0
- 0001 A1
- 0010 A2
- 0011 A3
- 0100 A4
- 0101 A5
- 0110 A6
- 0111 A7
- 1000 V_{eREF+}
- 1001 V_{REF-}/V_{eREF-}
- 1010 Temperature sensor
- 1011 $(V_{CC} - V_{SS}) / 2$
- 1100 $(V_{CC} - V_{SS}) / 2$, A12 on MSP430F22xx devices
- 1101 $(V_{CC} - V_{SS}) / 2$, A13 on MSP430F22xx devices
- 1110 $(V_{CC} - V_{SS}) / 2$, A14 on MSP430F22xx devices
- 1111 $(V_{CC} - V_{SS}) / 2$, A15 on MSP430F22xx devices

SHSx Bits 11-10 Sample-and-hold source select.

- 00 ADC10SC bit
- 01 Timer_A.OUT1 [1]
- 10 Timer_A.OUT0 [1]
- 11 Timer_A.OUT2 (Timer_A.OUT1 on MSP430F20x0, MSP430G2x31, and MSP430G2x30 devices) [1]

ADC10DF Bit 9 ADC10 data format

- 0 Straight binary
- 1 2s complement

ISSH Bit 8 Invert signal sample-and-hold

- 0 The sample-input signal is not inverted.
- 1 The sample-input signal is inverted.

ADC10DIVx Bits 7-5 ADC10 clock divider

- 000 /1
- 001 /2
- 010 /3
- 011 /4
- 100 /5
- 101 /6
- 110 /7
- 111 /8

ADC10SSELx Bits 4-3 ADC10 clock source select

- 00 ADC10OSC
- 01 ACLK
- 10 MCLK
- 11 SMCLK

(1) Timer triggers are from Timer0_Ax if more than one timer module exists on the device.

22.3.3 ADC10AE0, Analog (Input) Enable Control Register 0

7	6	5	4	3	2	1	0
ADC10AE0x							
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

ADC10AE0x Bits 7-0 ADC10 analog enable. These bits enable the corresponding pin for analog input. BIT0 corresponds to A0, BIT1 corresponds to A1, etc. The analog enable bit of not implemented channels should not be programmed to 1.

- 0 Analog input disabled
- 1 Analog input enabled