```
1
     -- Name: Capt Jeff Falkinburg
 3
     -- Date: Spring 2016
 4
     -- Course: ECE 281
     -- File: ce2 ha structural.vhd
 5
     -- HW: Lecture 13
     -- Purp: Half Adder - Structural Implementation.
 7
 8
     -- Doc: None
 9
     -- Academic Integrity Statement: I certify that, while others may have
10
11
     -- assisted me in brain storming, debugging and validating this program,
12
     -- the program itself is my own work. I understand that submitting code
13
     -- which is the work of other individuals is a violation of the honor
     -- code. I also understand that if I knowingly give my original work to
14
15
     -- another individual is also a violation of the honor code.
16
17
     library IEEE;
                                    -- These lines are similar to a #include in C
18
     use IEEE.std_logic_1164.all;
                                    -- Use these libraries if you are using primitive
19
     library unisim;
     components
20
     use unisim.vcomponents.all;
21
22
     entity ce2_ha_structural is
23
       Port ( A : in STD LOGIC;
                B : in STD LOGIC;
2.4
                S : out STD LOGIC;
25
                Cout : out STD LOGIC);
2.6
     end ce2_ha_structural;
27
28
29
     architecture Structural of ce2_ha_structural is
30
        component AND2
31
           port ( i0, i1 : in std logic;
32
                           : out std logic);
33
        end component;
34
        component XOR2
35
           port ( i0, i1 : in std logic;
36
                           : out std logic);
37
        end component;
38
        signal s1, s2 : std logic; -- wires which begin and end in the component
39
     begin
40
        unit1:
                AND2
41
        port map ( -- s1 <= A AND B; (i.e. Cout)</pre>
42
           i0 => a,
43
           i1 \Rightarrow b,
           o => s1);
44
45
        unit2: XOR2
46
        port map ( -- s2 <= A XOR B; (i.e. Sum)</pre>
47
           i0 => a,
           i1 \Rightarrow b,
48
49
          o => s2);
50
        Cout <= s1;
51
52
        S \ll s2;
53
54
    end Structural;
```