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1  --------------------------------------------------------------------------------
2  -- Name: Capt Jeff Falkinburg
3  -- Date: Spring 2016
4  -- Course: ECE 281
5  -- File: minority.vhd
6  -- HW:   Lecture 13
7  -- Purp: Minority circuit - output is high if the minority of inputs
8  --       are high
9  --
10 -- Doc:  None
11 -- Academic Integrity Statement: I certify that, while others may have
12 -- assisted me in brain storming, debugging and validating this program,
13 -- the program itself is my own work. I understand that submitting code
14 -- which is the work of other individuals is a violation of the honor
15 -- code.  I also understand that if I knowingly give my original work to
16 -- another individual is also a violation of the honor code.
17 --------------------------------------------------------------------------------
18 library IEEE;                  -- These lines are similar to a #include in C
19 use IEEE.std_logic_1164.all;
20
21 entity minority_v2 is
22    port( a, b, c: in std_logic;
23                f: out std_logic);
24 end minority_v2;
25
26 architecture Behavioral of minority_v2 is
27    signal ABC: std_logic_vector(2 downto 0);
28 begin
29
30    ABC <= a & b & c; -- Concatenation of signals into a vector
31
32    f <=  '1' when ABC = "000" else --Double quotes for std_logic_vectors
33          '1' when ABC = "001" else
34          '1' when ABC = "010" else
35          '0' when ABC = "011" else
36          '1' when ABC = "100" else
37          '0' when ABC = "101" else
38          '0' when ABC = "110" else
39          '0'; -- for all others
40    -- essentially an enumeration of a truth table
41
42 end Behavioral;
```