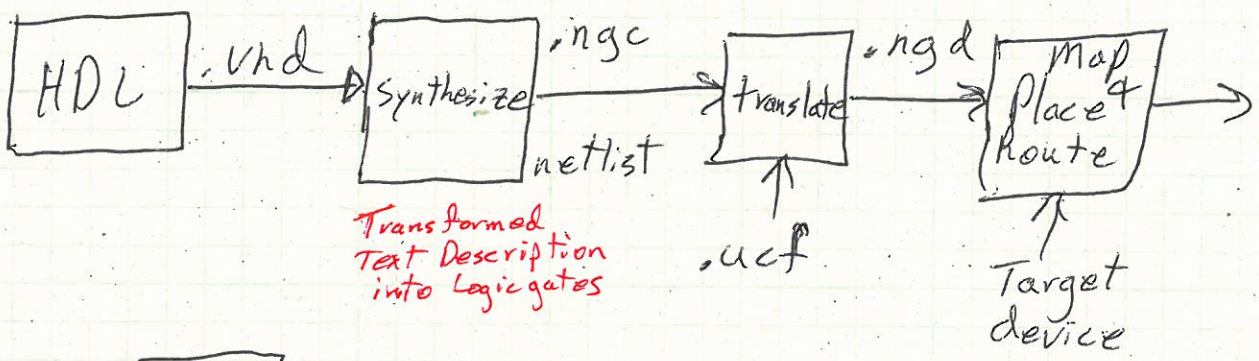
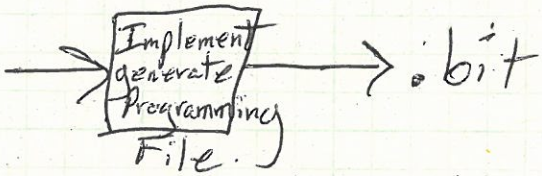
Overview:

- VHDL

VHDL - Very High speed Integrated Circuits (VHSIC) Hardware Description Language

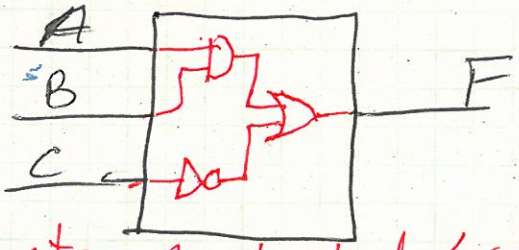




VHDL - is not sequential like (C, Java, & Python)
everything happens all at once

entity - defines inputs & outputs

architecture - describes what is inside the box



* Red indicates protected/reserved words!

```
entity ent_name is
    port ( port_name : mode signal_type );
                       (In, out)  (std_logic, std_logic_vector)
);

architecture arch_name of ent_name is
    signal declarations
    component declarations
begin
    connect your stuff;
end arch_name;
```

Behavioral vs Structural:

Signal Declarations – behavioral / structural

component Declarations – structural

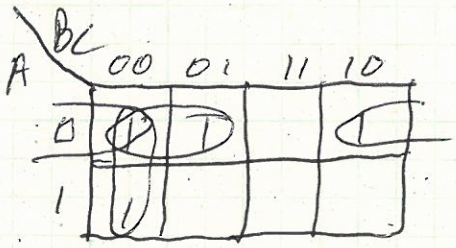
Behavioral – Describing a module in terms of the relationships between inputs & outputs

Structural – describing a module in terms of how it is composed of simpler modules

Exercise: 4.5

Minority

A B C	Y
0 0 0	1
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	0

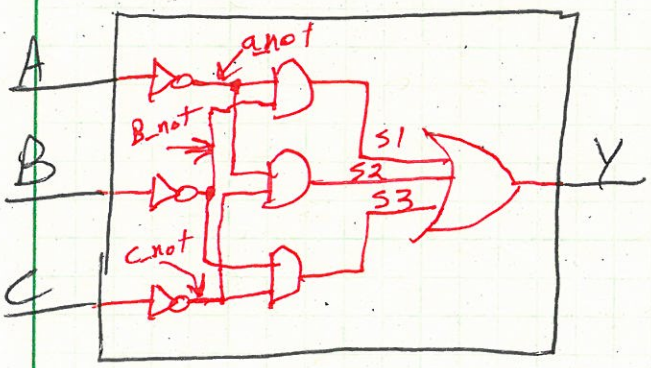


$Y = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$

First do an example of behavioral: implement in VHDL

How else can we do it?

Structural:



Create minority 2