```
1
     -- Name: Capt Jeff Falkinburg
 3
    -- Date: Spring 2016
 4
     -- Course: ECE 281
    -- File: Lsn20 muxFour.vhd
 5
    -- HW: Lecture 20
 7
    -- Purp: Structural implementation of a 4 to 1 Multiplexer
 8
     -- Doc: None
    -- Academic Integrity Statement: I certify that, while others may have
 9
    -- assisted me in brain storming, debugging and validating this program,
10
     -- the program itself is my own work. I understand that submitting code
11
12
     -- which is the work of other individuals is a violation of the honor
13
     -- code. I also understand that if I knowingly give my original work to
     -- another individual is also a violation of the honor code.
14
15
     ______
    library IEEE;
16
17
    use IEEE.STD LOGIC 1164.ALL;
18
     entity muxFour is
19
20
        Port ( A : in STD LOGIC;
21
               B : in STD LOGIC;
               C : in STD LOGIC;
2.2
23
               D : in STD LOGIC;
24
               S : in STD LOGIC VECTOR (1 downto 0);
               Y : out STD LOGIC);
2.5
26
     end muxFour;
2.7
28
     architecture Structural of muxFour is
        component muxTwo
29
           Port ( A : in STD_LOGIC;
30
               B : in STD LOGIC;
31
               S : in STD LOGIC;
32
               Y : out STD_LOGIC);
33
34
       end component;
35
36
       component and Two
           Port ( A : in STD LOGIC;
37
38
               B : in STD LOGIC;
               Y : out STD LOGIC);
39
       end component;
40
41
42
        signal top, bottom, anded : std logic;
43
44
45
    begin
46
47
       andGate: andTwo
48
        port map ( A => C,
49
                   B => D,
50
                   Y => anded);
51
     -- Can be written in short form like this:
     -- andGate: andTwo port map (C, D, anded);
52
53
               muxTwo
       mux1:
54
       port map ( A => A,
55
                   B => B,
56
                   S => S(0),
57
                   Y = > top);
```

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Lsn20_muxFour.vhd

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58
        mux2: muxTwo
59
        port map ( A => C,
60
                    B => anded,
                    S => S(0),
61
62
                    Y => bottom);
63
       mux3:
                muxTwo
        port map ( A => top,
64
65
                    B => bottom,
66
                    S \Rightarrow S(1),
67
                    Y => Y);
68
69
    end Structural;
70
```