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1  --------------------------------------------------------------------------------
2  -- Name: Capt Jeff Falkinburg
3  -- Date: Spring 2016
4  -- Course: ECE 281
5  -- File: minority.vhd
6  -- HW:   Lecture 13
7  -- Purp: Minority circuit - output is high if the minority of inputs
8  --       are high
9  --
10 -- Doc:  None
11 -- Academic Integrity Statement: I certify that, while others may have
12 -- assisted me in brain storming, debugging and validating this program,
13 -- the program itself is my own work. I understand that submitting code
14 -- which is the work of other individuals is a violation of the honor
15 -- code.  I also understand that if I knowingly give my original work to
16 -- another individual is also a violation of the honor code.
17 --------------------------------------------------------------------------------
18 library IEEE;                  -- These lines are similar to a #include in C
19 use IEEE.std_logic_1164.all;
20
21 entity minority is
22    port( a, b, c: in std_logic;
23                f: out std_logic);
24 end minority;
25
26 architecture Behavioral of minority is
27
28 begin
29    f <=  '1' when a='0' and b='0' and c='0' else
30          '1' when a='0' and b='0' and c='1' else
31          '1' when a='0' and b='1' and c='0' else
32          '0' when a='0' and b='1' and c='1' else
33          '1' when a='1' and b='0' and c='0' else
34          '0' when a='1' and b='0' and c='1' else
35          '0' when a='1' and b='1' and c='0' else
36          '0'; -- for all others
37    -- essentially an enumeration of a truth table
38
39 end Behavioral;
```