```
1   ----------------------------------------------------------------------------------
2   -- Name: Capt Jeff Falkinburg
3   -- Date: Spring 2016
4   -- Course: ECE 281
5   -- File: Flip_Flop.vhd
6   -- HW:   Lecture 19
7   -- Purp: Basic Flip-Flop
8   --
9   -- Doc:  None
10  -- Academic Integrity Statement: I certify that, while others may have
11  -- assisted me in brain storming, debugging and validating this program,
12  -- the program itself is my own work. I understand that submitting code
13  -- which is the work of other individuals is a violation of the honor
14  -- code.  I also understand that if I knowingly give my original work to
15  -- another individual is also a violation of the honor code.
16  ----------------------------------------------------------------------------------
17  library IEEE;
18  use IEEE.STD_LOGIC_1164.ALL;
19
20  entity Flip_Flop is
21      Port ( clk, D : in  STD_LOGIC;
22             Q : out  STD_LOGIC);
23  end Flip_Flop;
24
25  architecture Behavioral of Flip_Flop is
26
27  begin
28
29     process(clk)
30     begin
31        if (rising_edge(clk)) then -- Note:  Do not use *** clk'event and clk = '1'
32           Q <= D;
33        end if;
34     end process;
35
36  end Behavioral;
37
38
```