```vhdl
 1    ----------------------------------------------------------------------
 2    -- Name: Capt Jeff Falkinburg
 3    -- Date: Spring 2016
 4    -- Course: ECE 281
 5    -- File: Lsn20_muxTwo.vhd
 6    -- HW:   Lecture 20
 7    -- Purp: Structural implementation of a 2 to 1 Multiplexer
 8    -- Doc:  None
 9    -- Academic Integrity Statement: I certify that, while others may have
10    -- assisted me in brain storming, debugging and validating this program,
11    -- the program itself is my own work. I understand that submitting code
12    -- which is the work of other individuals is a violation of the honor
13    -- code.  I also understand that if I knowingly give my original work to
14    -- another individual is also a violation of the honor code.
15    ----------------------------------------------------------------------
16    library IEEE;
17    use IEEE.STD_LOGIC_1164.ALL;
18
19    entity muxTwo is
20        Port ( A : in  STD_LOGIC;
21               B : in  STD_LOGIC;
22               S : in  STD_LOGIC;
23               Y : out  STD_LOGIC);
24    end muxTwo;
25
26    architecture Behavioral of muxTwo is
27
28    begin
29
30       Y <= A when S = '0' else B;
31
32    end Behavioral;
33
34
```