FPGA Vertex 6 GTx Inteface

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1 GTx Transmitter

The FPGA TX interface is the FPGAs gateway to the TX datapath of the GTX transceiver.The GTx transmitter is fundamentally a parallel-to-serial converter. The incoming parallel data is fed through a small FIFO and can optionally be modified with the 8b/10B encoding. Applications transmit data through the GTX transceiver by writing data to the TXDATA port on the positive edge of TXUSRCLK2. The width of the port can be configured to be one, two, or four bytes wide. Port widths can be 8, 10,16, 20, 32, and 40 bits. The rate of the parallel clock (TXUSRCLK2) at the interface is determined by the TX line rate, the width of the TXDATA port, and whether or not 8B/10B encoding is enabled. In some operating modes, a second parallel clock (TXUSRCLK) must be provided for the internal PCS logic in the transmitter.

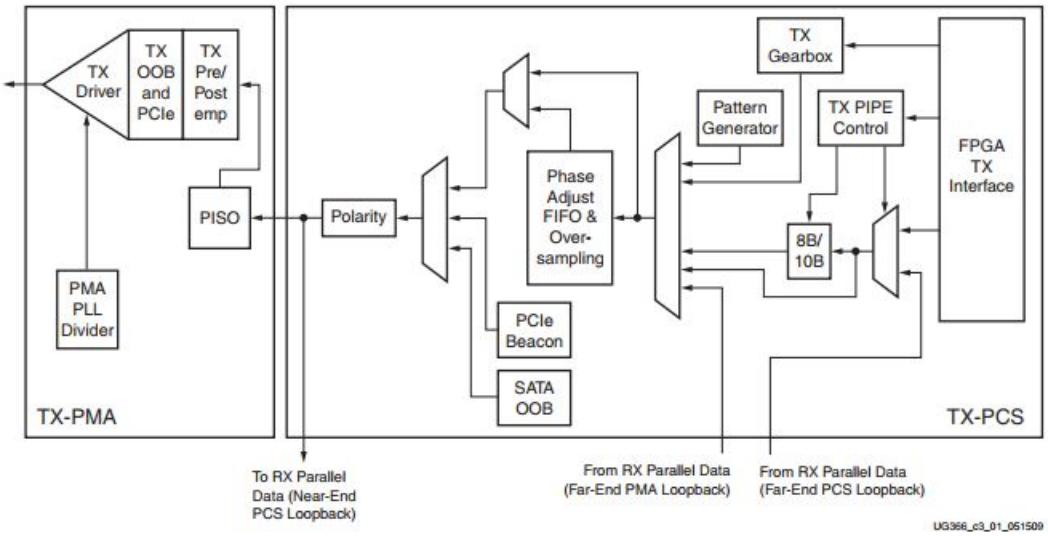

Figure 1.1: GTx Transciever Block Diagram

The FPGA TX interface includes two parallel clocks: TXUSRCLK and TXUSRCLK2. TXUSRCLK is the internal clock for the PCS (Physical Coding Sublayer) logic in the GTX transceiver transmitter. The required rate for TXUSRCLK depends on the internal datapath width of the GTXE1 primitive and the TX line rate of the GTX transceiver transmitter. Equation 1-1 shows how to calculate the required rate for TXUSRCLK. TXUSRCLK can be generated internally to the GTX transceiver. Figure 1-2 describes the situations in which the TXUSRCLK can be generated internally by the GTX transceiver.

$$TXUSRCLK\ RATE = \frac{Line\ Rate}{Internal\ Data\ Width} \tag{1.1}$$

TXUSRCLK2 is the main synchronization clock for all signals into the TX side of the GTX transceiver. Most signals into the TX side of the GTX transceiver are sampled on the positive

	TX_DATA_WIDTH	GTX Lanes in Channel(1)	GEN_TXUSRCLK
1-Byte	8, 10	1	TRUE
		2 or more	FALSE
2-Byte	16, 20	1 or more	TRUE
4-Byte	32, 40	1 or more	FALSE

Figure 1.2: TXUSRCLK Internal Generation Configuration

edge of TXUSRCLK2. TXUSRCLK2 and TXUSRCLK have a fixed-rate relationship based on the TX DATA WIDTH setting. Figure 1-3 shows the relationship between TXUSRCLK2 and TXUSRCLK per TX DATA WIDTH values.

	TX_DATA_WIDTH	TXUSRCLK2 Frequency
1-Byte	8, 10	$F_{TXUSRCLK2} = 2 \times F_{TXUSRCLK}$
2-Byte	16, 20	$F_{TXUSRCLK2} = F_{TXUSRCLK}$
4-Byte	32, 40	$F_{TXUSRCLK2} = F_{TXUSRCLK} / 2$

Figure 1.3: TXUSRCLK2 Frequency Relationship to TXUSRCLK

2 GTx Receiver

The GTx Rx block recieve serial data and convert it to parallel data through SIPO block. Figure 2-1 shows the blocks of the RX. High-speed serial data flows from traces on the board into the PMA of the RX, into the PCS, and finally into the FPGA logic.

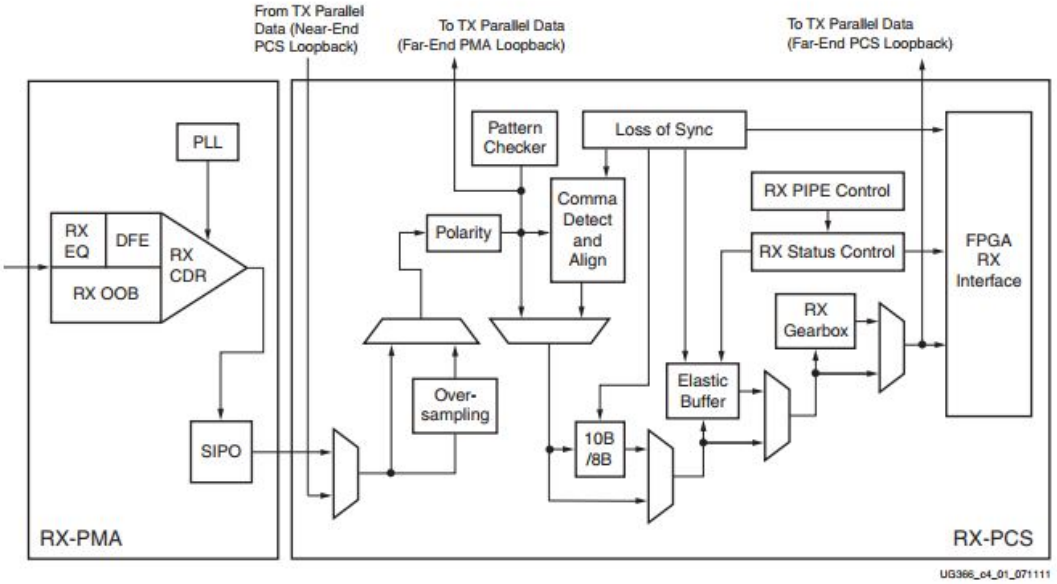

Figure 2.1: GTx Transciever Rx Block Diagram

Equation 2.1 shows how to determine the line rate (Gb/s).D is the PLL output divider that resides in the clock divider block.

$$f_{LineRate} = \frac{f_{PLLClkout \times 2}}{D} \tag{2.1}$$

For the simualtion in xilinx ISE with IP core generator following parameters are set as shown in the Table 2-1.

Table 2.1: Parameters for simulation(Single vertex 6 GTx LoopBack)

Vertex6 FPGA	XC6VSX315T-3FFG1156C
Line Rate	1 Gbps
Data Path Width	8 bits
Encoding	8b/10b
PLL Clock	2 GHz
PLL output divider (D)	4
Reference clock	500 MHz

64-bit frequency word will be send by GTx by 4 lines at a rate of 100MHz.

3 SIMULATION USING IP CORE (SINGLE VERTEX 6FPGA LOOP BACK)

Figure 2-2 and 2-3 the simulations results. The simualtion design use Block RAM based frame generators to provide test data to the GTX for transmission. By default the frame generator are loaded with incrementing data sequence that includes commas alignments.

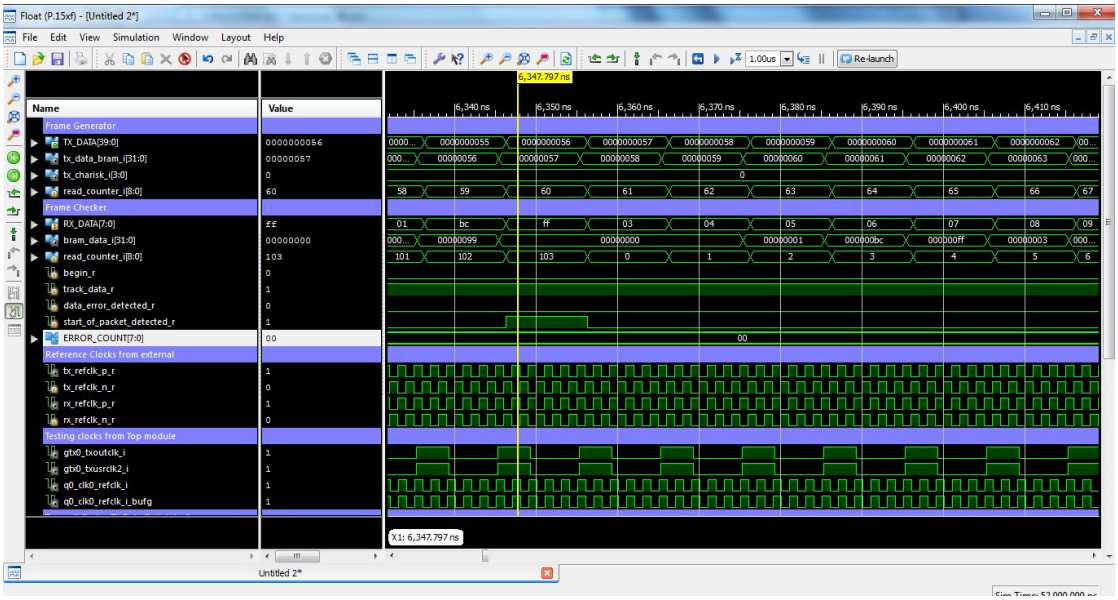

Figure 3.1: Simulation1 of GTx in xilinx

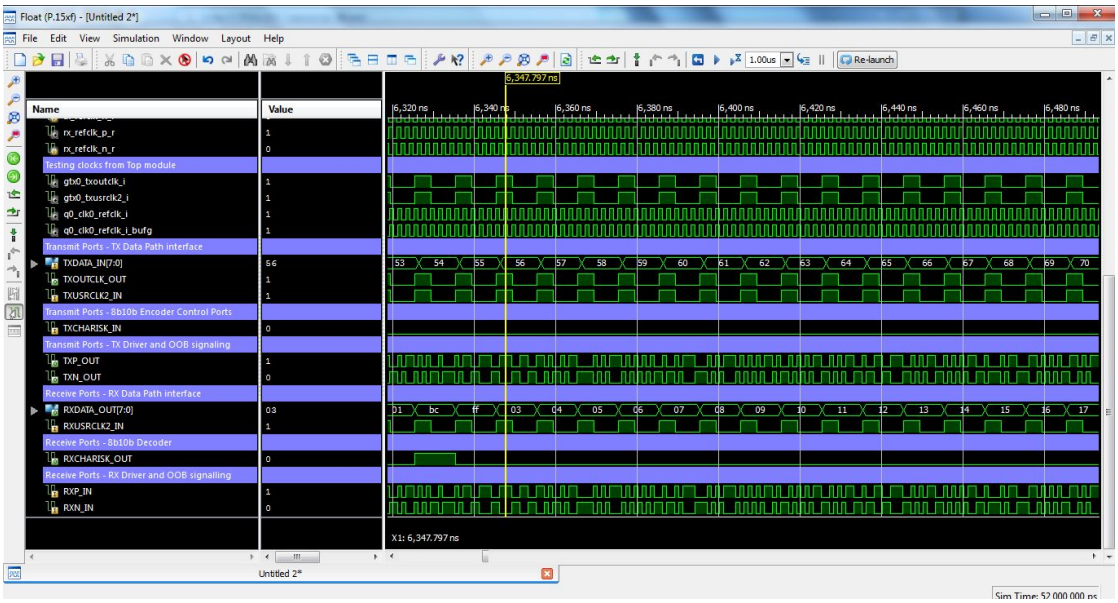

Figure 3.2: Simulation2 of GTx in xilinx

4 VERTEX 6 TO VERTEX 6 SERIAL COMMUNICATION VIA GTX

For the simualtion of GTx of vertex6 in xilinx ISE with IP core generator following parameters are set as shown in the Table.

Both transmitter and reciever should be configured with same setting as depicted in the table below.

Table 4.1: Parameters for simulation of vertex 6

Vertex6 FPGA	XC6VSX315T-3FFG1156C
Line Rate	1 Gbps
Data Path Width	16 bits
Encoding	8b/10b
PLL Clock	2 GHz
PLL output divider (D)	4
Reference clock	500 MHz
Tx and Rx buffers	enabled

5 FILES AND FOLDER

For vertex-6 to vertex-6, we have two separate folder i.e vertex6 gtx tx and vertex6 gtx rx. All testing file, wave-ism, scripts are placed in vertex6-gtx-tx folder.