CELLULAR

SARA-N2 series

Power-optimized NB-IoT (LTE Cat NB1) modules

System Integration Manual

Abstract

This document describes the features and the system integration of the SARA-N2 series NB-IoT modules.
These modules are a complete and cost efficient solution offering single-band and dual-band data transmission for the Internet of Things technology in the compact SARA form factor.

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This document applies to the following products:

Product name	Type number	Firmware version	PCN reference	Product Status
SARA-N200	SARA-N200-02B-00	V100R100C10B656	UBX-17016302	Prototypes
SARA-N201	SARA-N201-02B-00	V100R100C10B656	UBX-17015830	Prototypes
SARA-N210	SARA-N210-02B-00	V100R100C10B656	UBX-17016302	Prototypes
SARA-N211	SARA-N211-02B-00	V100R100C10B656	UBX-17016302	Prototypes
SARA-N280	SARA-N280-02B-00	V100R100C10B656	UBX-17016302	Prototypes

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **AT Commands Manual:** This document provides the description of the AT commands supported by the u-blox cellular modules.
- **System Integration Manual:** This document provides the description of u-blox cellular modules' system from the hardware and the software point of view, it provides hardware design guidelines for the optimal integration of the cellular modules in the application device and it provides information on how to set up production and final product tests on application devices integrating the cellular modules.

Application Notes: These documents provide guidelines and information on specific hardware and/or software software topics on u-blox cellular modules. See

- Related documents for a list of application notes related to your cellular module.

How to use this Manual

The SARA-N2 series System Integration Manual provides the necessary information to successfully design in and configure these u-blox cellular modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:


An index finger points out key information pertaining to module integration and performance.


A warning symbol indicates actions that could negatively impact or damage the module.

Questions

If you have any questions about u-blox cellular Integration:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (http://www.u-blox.com) is a rich pool of information. Product information and technical documents can be accessed 24h a day.

By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the closest Technical Support office. To ensure that we process your request as soon as possible, use our service pool email addresses rather than personal staff email addresses. Contact details are at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support, have the following information ready:

- Module type (e.g. SARA-N280) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

SARA-N2 series modules are a Narrow Band Internet of Things (NB-IoT) solution coming in the miniature SARA LGA form factor (26.0 x 16.0 mm, 96-pin). The modules offer IoT data communication over an extended operating temperature range of –40 to +85 °C, with extremely low power consumption.

The SARA-N2 series includes five variants supporting single-band communication over the LTE bands 5, 8, 20 and 28, plus a dual-band variant designed to operate in the frequency range of the LTE bands 8 and 20.

SARA-N2 series modules are ideally suited to battery-powered IoT applications characterized by occasional communications of small amounts of data.

SARA-N2 series modules are the optimal choice for IoT devices designed to operate in locations with a very limited coverage and requiring low energy consumption to permit a very long operating life of the primary batteries. Examples of applications include and are not limited to: smart grids, smart metering, telematics, street lighting, environmental monitoring and control, security and asset tracking.

Table 1 describes a summary of interfaces and features provided by SARA-N2 series modules.

Module	Region	Bands			Positioning			Interfaces					Features						Grade		
		3GPP Release Baseline	3GPP Category	NB-IoT bandss	GNSS via modem	AssistNow Software	CellLocate®	UART	USB 2.0	SPI	DDC (I²C)	GPIO	Antenna supervisor	eDRX	Power Save Mode	Embedded UDP stack	FW update over AT (FOAT)	FW update over the air (FOTA)	Standard	Professional	Automotive
SARA-N200	Europe APAC	13	NB1	8	□			2			□	□	●	●	●	●	●	●			
SARA-N201	APAC	13	NB1	5	□			2			□	□	●	●	●	●	●	●			
SARA-N210	Europe	13	NB1	20	□			2			□	□	●	●	●	●	●	●			
SARA-N211	Europe	13	NB1	8,20	□			2			□	□	●	●	●	●	●	●			
SARA-N280	S.America APAC	13	NB1	28	□			2			□	□	●	●	●	●	●	●			

● = supported by "02" product version onwards □ = supported by future product versions

Table 1: SARA-N2 series characteristics summary

Table 2 reports a summary of cellular radio access technologies characteristics of SARA-N2 series modules.

Item	SARA-N200	SARA-N201	SARA-N210	SARA-N211	SARA-N280
NB-IoT protocol stack	3GPP Release 13	3GPP Release 13	3GPP Release 13	3GPP Release 13	3GPP Release 13
Operating band	Band 8 (900 MHz)	Band 5 (850 MHz)	Band 20 (800 MHz)	Band 8 (900 MHz), Band 20 (800 MHz)	Band 28 (700 MHz)
Power Class	Class 3 (23 dBm)	Class 3 (23 dBm)	Class 3 (23 dBm)	Class 3 (23 dBm)	Class 3 (23 dBm)
Data rate	NB1 category: Up to 62.5 kb/s UL Up to 27.2 kb/s DL	NB1 category: Up to 62.5 kb/s UL Up to 27.2 kb/s DL	NB1 category: Up to 62.5 kb/s UL Up to 27.2 kb/s DL	NB1 category: Up to 62.5 kb/s UL Up to 27.2 kb/s DL	NB1 category: Up to 62.5 kb/s UL Up to 27.2 kb/s DL

Table 2: SARA-N2 series NB-IoT characteristics summary

1.2 Architecture

Figure 1 summarizes the architecture of SARA-N2 series modules, describing the internal blocks of the modules, consisting of the RF, Baseband and Power Management main sections, and the available interfaces.

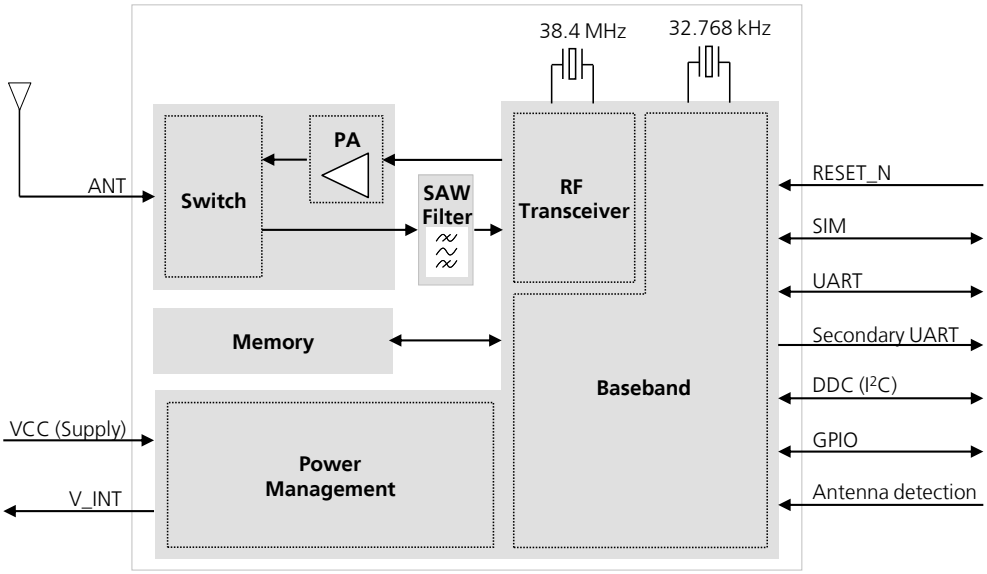

Figure 1: SARA-N2 series modules block diagram

The RF section is composed of the following main elements:

- LTE Power Amplifier, which amplifies the signals modulated by the RF transceiver
- RF switches, which connects the antenna input/output pin (**ANT**) of the module to the suitable RX/TX path
- RX low loss SAW filters
- 38.4 MHz crystal, connected to the digital controlled crystal oscillator to perform the clock reference in active-mode and connected-mode

The Baseband and Power Management section is composed of the following main elements:

- Baseband processor
- Flash memory
- Voltage regulators to derive all the system supply voltages from the module supply **VCC**
- Circuit for the RTC clock reference in low power deep-sleep

1.3 Pin-out

Table 3 lists the pin-out of the SARA-N2 series modules, with pins grouped by function.

Function	Pin Name	Pin No	I/O	Description	Remarks
Power	**VCC**	51, 52, 53	I	Module supply input	**VCC** pins are internally connected each other. **VCC** supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for description and requirements. See section 2.2.1 for external circuit design-in.
	GND	1, 3, 5, 14, 20-22, 30, 32, 43, 50, 54, 55, 57-61, 63-96	N/A	Ground	**GND** pins are internally connected each other. External ground connection affects the RF and thermal performance of the device.
	V_INT	4	O	Generic Digital Interfaces supply output	**V_INT** = 1.8 V (typical), generated by internal regulator when the module is switched on, out of deep-sleep state. Provide a test point on this pin for diagnostic purpose. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
System	**RESET_N**	18	I	External reset input	Internal 78 kΩ pull-up to **VCC**. Provide a test point on this pin for diagnostic purpose. See section 1.6.3 for functional description. See section 2.3.1 for external circuit design-in.
Antenna	**ANT**	56	I/O	RF input/output for antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for description and requirements. See section 2.4 for external circuit design-in.
	ANT_DET	62	I	Input for antenna detection	ADC input for antenna detection function. See section 1.7.2 for functional description.
SIM	**VSIM**	41	O	SIM supply output	**VSIM** = 1.80 V (typical). See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	39	I/O	SIM data	Internal 4.7 kΩ pull-up to **VSIM**. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	38	O	SIM clock	Clock for external SIM, operating at **VSIM** voltage level. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	40	O	SIM reset	Reset for external SIM, operating at **VSIM** voltage level. See section 1.8 for functional description. See section 2.5 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
UART	**RXD**	13	O	UART data output	Circuit 104 (RXD) in ITU-T V.24, for AT command and data, FOAT and FW upgrade via CodeLoader tool. It operates at **VCC** voltage level. Provide a test point on this pin for diagnostic purpose. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	TXD	12	I	UART data input	Circuit 103 (TXD) in ITU-T V.24, for AT command and data, FOAT and FW upgrade via CodeLoader tool. Internal active pull-up to **VCC**. Provide a test point on this pin for diagnostic purpose. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	11	O	UART clear to send output	Circuit 106 (CTS) in ITU-T V.24. It operates at **VCC** voltage level. Can be configured as the Ring Indicator output line. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	10	I	UART ready to send input	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to **VCC**. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
DDC	**SCL**	27	O	I^2C bus clock line	1.8 V open drain, for the communication with an external chip or u-blox positioning module / chip. External pull-up to **V_INT** required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	SDA	26	I/O	I^2C bus data line	1.8 V open drain, for the communication with an external chip or u-blox positioning module / chip. External pull-up to **V_INT** required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
GPIO	**GPIO1**	16	I/O	GPIO	1.8 V GPIO, operating at **V_INT** voltage level. Can be configured as secondary UART data output, used for diagnostic purpose. Provide a test point on this pin for diagnostic purpose. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO2	23	I/O	GPIO	1.8 V GPIO, operating at **V_INT** voltage level. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
Reserved	**RSVD**	33	N/A	RESERVED pin	This pin can be connected to GND. See sections 1.11 and 2.8.
	RSVD	2, 6-9, 15, 17,19, 23, 25, 28, 29, 31, 34-37, 42, 44-49	N/A	RESERVED pin	Leave unconnected. See sections 1.11 and 2.8.

Table 3: SARA-N2 series modules pin definition, grouped by function

1.4 Operating modes

SARA-N2 series modules have several operating modes. The operating modes defined in Table 4 and described in detail in Table 5 provide general guidelines for operation.

Figure 2 describes the transition between the different operating modes.

General Status	Operating Mode	Definition
Power-down	**Not-Powered Mode**	**VCC** supply not present or below operating range: module is switched off.
Normal operation	**Deep-sleep mode**	Module processor runs with internal 32 kHz reference; lowest current consumption
	Active-Mode	Module processor runs with internal 38.4 MHz reference.
	Connected-Mode	Module processor runs with internal 38.4 MHz reference; data transmission/reception or signaling activity with the network enabled.

Table 4: Module operating modes definition

Mode	Description	Transition between operating modes
Not-Powered	Module is switched off. Application interfaces are not accessible.	When **VCC** supply is removed, the module enters not-powered mode. When in not-powered mode, the modules can be switched on applying **VCC** supply (see section 2.2.1) so that the module switches from not-powered to active-mode.
Active	Module is switched on with application interfaces enabled or not suspended: the module is ready to communicate with an external device by means of the application interfaces.	The module enters active mode from not-powered mode by applying **VCC** supply (see section 2.2.1). Then, the module automatically switches from active to deep-sleep mode whenever possible or switches to connected mode in case there is any data to transmit or receive.
Deep-sleep	Only the internal 32 kHz reference is active; the RF section is completely disabled. This is the lowest currect consumption mode. The UART interface is still completely functional and the module can accept and respond to any AT command. All the other interfaces are disabled. If a trace is active on the secondary UART, it is automatically suspended when the module enters this mode. In this mode the module is not able to receive any down-link message or data from the network. To do so, the module must be in the active or connected mode. The module automatically enters deep-sleep mode whenever possible after a network dependent time of inactivity. It is possible to monitor when the module enters the deep-sleep mode checking the voltage level present on the **V_INT** pin: the voltage is set to a low level (0 V) in this mode.	The module automatically switches from active mode to deep-sleep mode whenever possible. The module wakes up from deep-sleep to active mode in the following events: • Automatic periodic monitoring of the paging channel for the paging block reception and periodic tracking area update (TAU) according to network conditions • A send-data request is issued to the module using the commands +NMGS or +NSOST (for more details, see u-blox SARA-N2 series AT Commands Manual [3])
Connected	The module is transmitting/receiving data to/from the network. Both internal references at 32 kHz and 38.4 MHz are active.	When a data connection is initiated, the module enters connected mode from active mode. Connected-mode is suspended if Tx/Rx data is not in progress. In such cases the module automatically switches from connected to active mode and then the module automatically switches to deep sleep mode whenever possible. Vice-versa, the module wakes up re-entering connected mode upon resume of RF Tx/Rx activity. When a data connection is terminated, the module returns to the active-mode and then the module automatically switches to deep sleep mode whenever possible.

Table 5: Module operating modes description

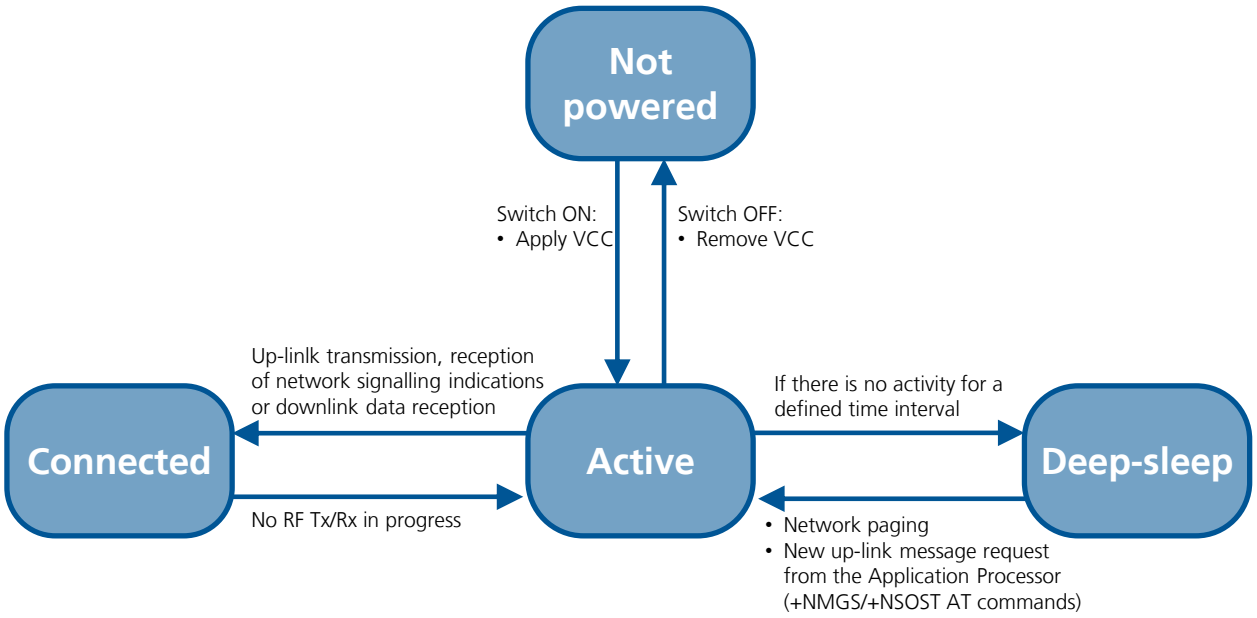

Figure 2: Operating modes transitions

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, including **V_INT** (digital interfaces supply) and **VSIM** (SIM card supply).

During operation, the current drawn by the SARA-N2 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the high peak of current consumption during data transmission at maximum power level in connected mode, to the low current consumption during deep-sleep mode (as described in section 1.5.1.2).

1.5.1.1 VCC supply requirements

Table 6 summarizes the requirements for the **VCC** module supply. See section 2.2.1 for all the suggestions to properly design a **VCC** supply circuit compliant to the requirements listed in Table 6.

VCC supply circuit desing may affect the RF compliance of the device integrating SARA-N2 series modules with applicable required certification schemes. Compliance is not guaranteed if the VCC requirements summarized in the Table 6 are not fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.1 V min. / 4.0 V max	The module cannot be switched on if **VCC** voltage value is below the normal operating range minimum limit. Ensure that the input voltage at **VCC** pins is above the minimum limit of the normal operating range for at least more than 3 s after the module switch-on.
VCC voltage during normal operation	Within **VCC** extended operating range: 2.5 V min. / 4.2 V max	The module may switch off when **VCC** voltage drops below the extended operating range minimum limit. Operation above extended operating range limit is not recommended and may affect device reliability. When operating below the normal operating range minimum limit, the internal PA may not be able to transmit at the network-required power level.
VCC average current	Support with margin the highest averaged **VCC** current consumption value in connected mode specified in SARA-N2 series Data Sheet [1].	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage.
VCC voltage ripple	Noise in the supply has to be minimized	High supply voltage ripple values during RF transmissions in connected-mode directly affect the RF compliance with applicable certification schemes.

Table 6: Summary of VCC supply requirements

1.5.1.2 VCC current consumption profile

Figure 3 shows an example of the module **VCC** current consumption profile starting from the switch-on event, followed by different phases and operating modes:

- Network registration and context activation procedure
- Transmission of an up-link datagram
- RRC connection release and related signaling operations
- Cyclic paging reception
- Deep sleep mode

Timings in the figure are purely indicative since these may significantly change depending on the network signaling activity. The current consumption peaks occur when the module is in the connected (transmitting) mode and the value of these peaks is strictly dependent on the transmitted power, which is regulated by the network. See the electrical specification section in the SARA-N2 series Data Sheet [1] for more details about the current consumption values in the different modes and the influence of the transmitting power level.

A proper power supply circuit for SARA-N2 series modules must be able to withstand the current values present during the data transmission at maximum power, even though NB-IoT systems should be designed to keep the module in deep-sleep mode for most of the time, with an extremely low current consumption in the range of few microamps.

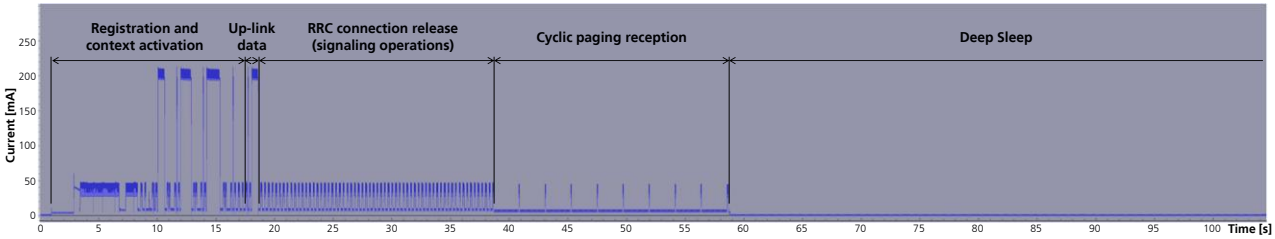

Figure 3: Example of module current consumption from the switch-on event up to deep-sleep mode

1.5.2 Generic digital interfaces supply output (V_INT)

The same 1.8 V voltage domain used internally to supply the generic digital interfaces (GDI) of SARA-N2 series modules is also available on the **V_INT** supply output pin, as described in Figure 4.

The internal regulator that generates the **V_INT** supply is a low drop out (LDO) converter that is directly supplied from **VCC**. The voltage regulator output is set to 1.8 V (typical) when the module is switched on and it is disabled when the module is switched off.

V_INT can also be used to monitor when the module enters the deep-sleep mode:

- In the deep-sleep mode the voltage level is kept "Low" (i.e. 0 V)
- In active and connected modes the voltage level is maintained "High" (i.e. 1.8 V)

☞ Provide a test point connected to the **V_INT** pin for diagnostic purpose.

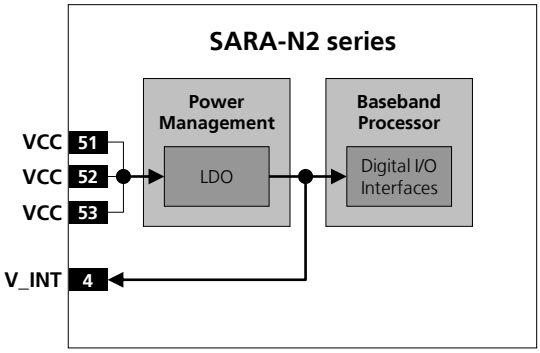

Figure 4: SARA-N2 series interfaces supply output (V_INT) simplified block diagram

1.6 System function interfaces

1.6.1 Module power-on

1.6.1.1 Switch-on events

When the SARA-N2 series modules are in the not-powered mode (i.e. switched off with the **VCC** module supply not applied), they can be switched on by:

- Rising edge on the **VCC** supply input to a valid voltage value for module supply (see SARA-N2 series Data Sheet [1])
- Alternately, the **RESET_N** pin can be held low during the **VCC** rising edge, so that the module switches on by releasing the **RESET_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal range.

1.6.1.2 Switch-on sequence from not-powered mode

Figure 5 shows the modules power-on sequence from the not-powered mode, describing the following phases:

- The external supply is applied to the **VCC** module supply inputs, representing the start-up event.
- The **RESET_N** line rises suddenly to high logic level due to internal pull-up to **VCC**.
- All the generic digital pins of the modules are tri-stated until the switch-on of their supply source (**V_INT**): any external signal connected to the generic digital pins must be tri-stated or set low at least until the activation of the **V_INT** supply output to avoid latch-up of circuits and allow a proper boot of the module.
- The **V_INT** generic digital interfaces supply output is enabled by the integrated power management unit. The **RXD** UART data output pin also rises to a high voltage level
- A greeting message is sent on the **RXD** pin (for more details see u-blox SARA-N2 series AT Commands Manual [3]). From now on the module is fully operational and the UART interface is functional

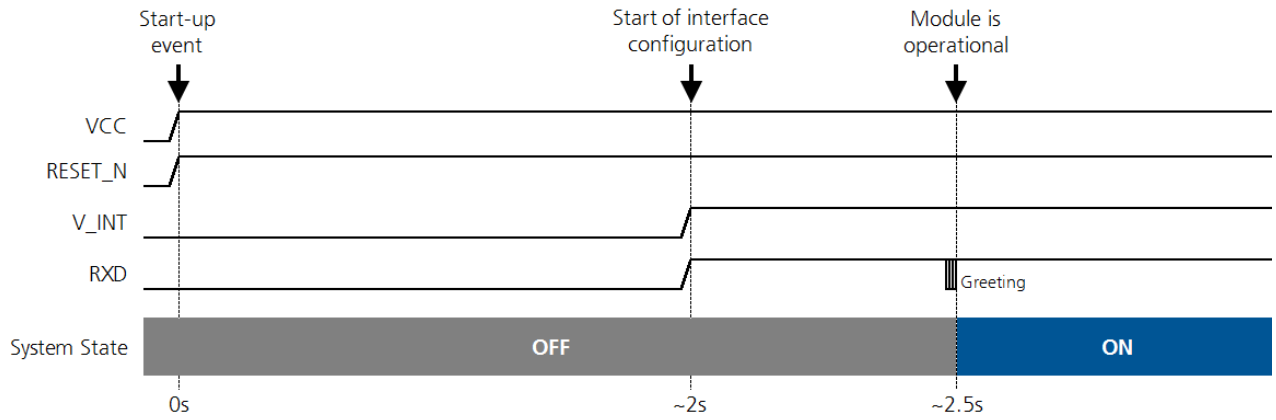

Figure 5: SARA-N2 series power-on sequence from not-powered mode

Before the switch-on of the generic digital interface supply source (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the modules.

1.6.2 Module power-off

The SARA-N2 series modules can be switched off by:

- Removal of the **VCC** supply supply; the voltage drops below the operating range minimum limit

1.6.3 Module reset

The **RESET_N** pin of SARA-N2 series modules is equipped with an internal pull-up to **VCC**.

SARA-N2 series modules can be properly reset (rebooted) by:

- AT+NRB command (see the u-blox SARA-N2 series AT Commands Manual [3] for more details).

This command causes an "internal" or "software" reset of the module, which is an asynchronous reset of the module baseband processor. The current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed: this is the proper way to reset the modules.

An abrupt hardware reset occurs on SARA-N2 series modules when a low level is applied on the **RESET_N** input pin for a specific time period. In this case, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

☞ It is highly recommended to avoid an abrupt hardware shutdown of the module by forcing a low level on the **RESET_N** input pin during module normal operation: the **RESET_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not reply to any specific AT command.

☞ Provide a test point connected to the **RESET_N** pin for diagnostic purpose.

1.7 Antenna interface

1.7.1 Antenna RF interface (ANT)

The **ANT** pin of SARA-N2 series modules represents the RF input/output for the cellular RF signals reception and transmission. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line for proper RF signals reception and transmission.

1.7.1.1 Antenna RF interface requirements

Table 7 summarizes the requirements for the antenna RF interface (**ANT**). See section 2.4.1 for suggestions to properly design an antenna circuit compliant to these requirements.

The antenna circuit affects the RF compliance of the device integrating SARA-N2 series module with applicable required certification schemes.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The nominal characteristic impedance of the antenna RF connection must match the **ANT** pin 50 Ω impedance.
Frequency range	See the SARA-N2 series Data Sheet [1]	The required frequency range of the antenna depends on the operating bands supported by the cellular module.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the RF antenna connection matches the 50 Ω impedance. The impedance of the antenna RF termination must match as much as possible the 50 Ω impedance of the **ANT** pin over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The efficiency needs to be enough high over the operating frequency range to comply with the Over-The-Air radiated performance requirements, as Total Radiated Power and Total Isotropic Sensitivity, specified by certification schemes
Input power	> 0.5 W peak	The antenna connected to **ANT** pin must support the maximum power transmitted by the modules.

Table 7: Summary of antenna RF interface (ANT) requirements

1.7.2 Antenna detection interface (ANT_DET)

The **ANT_DET** pin is an Analog to Digital Converter (ADC) input used to sense the antenna presence evaluating the resistance from the **ANT** pin to GND by means of an external antenna detection circuit implemented on the application board. This optional functionality can be manged by dedicated AT command (for more details see the u-blox SARA-N2 series AT Commands Manual [3]).

1.8 SIM interface

SARA-N2 series modules provide a high-speed SIM/ME interface working at 1.8 V, supporting SIM cards or SIM-on-chip.

The VSIM supply output provides internal short circuit protection to limit start-up current and protect the SIM to short circuits.

The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM card or chip.

1.9 Serial interfaces

SARA-N2 series modules provide the following serial communication interfaces:

- UART interface: 5-wire unbalanced 3.6 V asynchronous serial interface supporting (see 1.9.1)
  - AT command
  - FW upgrades by means of the FOAT feature
  - FW upgrades by means of the CodeLoader tool
- Auxiliary UART interface: 2-wire unbalanced 1.8 V asynchronous serial interface supporting (see 1.9.2)
  - Trace log capture (diagnostic purpose)
- DDC interface[1]: I²C-bus compatible 1.8 V interface supporting (see 1.9.3)
  - Communication with external chips and sensors

1.9.1 Asynchronous serial interface (UART)

1.9.1.1 UART features

The UART interface is a 5-wire unbalanced asynchronous serial interface available on all the SARA-N2 series modules, supporting:

- AT command
- FW upgrades by means of the FOAT feature
- FW upgrades by means of the CodeLoader tool

The main characteristics of the interface are the following:

- Serial port with RS-232 functionality working at the **VCC** voltage domain (0 V for low data bit or ON state and ~3.6 V, i.e. **VCC**, for high data bit or OFF state)
- Data lines (**RXD** as module data output, **TXD** as module data input)
- Hardware flow control lines (**CTS** as module output, **RTS** as module input)
- Default baud rate: 9600 b/s (4800, 57600 and 115200 b/s baud rates are also supported)
- Fixed frame format: 8N1 (8 data bits, No parity, 1 stop bit)

The **CTS** line can also be used as the RING indicator pin to signal an incoming message received by the module or an URC event (for more details see the u-blox SARA-N2 series AT Commands Manual [3]).

☞ Hardware flow control lines **CTS** and **RTS** are not supported by "02" product versions.

[1] Not supported on "02" product version

The UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation (more details available in ITU Recommendation [4]): SARA-N2 series modules are designed to operate as a cellular modem, which represents the Data Circuit-terminating Equipment (DCE) according to ITU-T V.24 Recommendation [4]. The application processor connected to the module through the UART interface represents the Data Terminal Equipment (DTE).

☞ The signal names of the SARA-N2 series modules' UART interface conform to the ITU-T V.24 Recommendation [4]: e.g. the **TXD** line represents the data transmitted by the DTE (application processor data line output) and received by the DCE (module data line input).

Figure 6 describes the 8N1 frame format, which is the default configuration with fixed baud rate.

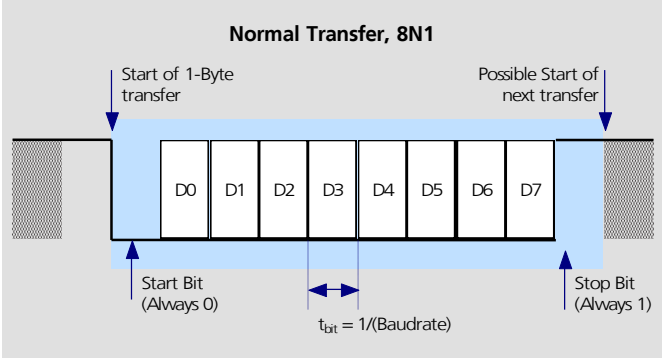

Figure 6: Description of UART default frame format (8N1) with fixed baud rate

1.9.1.2 UART signal behavior

At the module switch-on, before the UART interface initialization (as described in the power-on sequence reported in Figure 5), each pin is first tri-stated and then is set to its related internal reset state. At the end of the boot sequence, the UART interface is initialized and the UART interface is enabled as AT commands interface.

The configuration and the behavior of the UART signals after the boot sequence are described below. See section 1.4 for definition and description of module operating modes referred to in this section.

RXD signal behavior

The module data output line (**RXD**) is set by default to the OFF state (high level) at UART initialization. The greeting message is sent on the **RXD** line after the completion of the boot sequence to indicate the completion of the UART interface initialization.

The module holds **RXD** in the OFF state until the module does not transmit some data.

TXD signal behavior

The module data input line (**TXD**) is set by default to the OFF state (high level) at UART initialization. The **TXD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TXD** input.

CTS signal behavior

The module hardware flow control output line (**CTS**) can be set to signal incoming data received by the module or to signal an URC (for more details see the u-blox SARA-N2 series AT Commands Manual [3]).

1.9.1.3 UART and deep sleep mode

SARA-N2 series modules automatically enter deep-sleep mode whenever possible in case there is no data to transmit or receive to limit the current consumption. When in deep-sleep mode the UART interface is still completely functional and the module can accept and respond to any AT command. All the other interfaces are disabled.

At any time the DTE can request the module to send data using the commands +NMGS or +NSOST (for more details, see u-blox SARA-N2 series AT Commands Manual [3]); these commands automatically force the module to exit the deep-sleep mode.

1.9.2 Secondary asynchronous serial interface (Secondary UART)

The auxiliary UART interface is a 2-wire 1.8 V unbalanced asynchronous serial interface available over the **GPIO1** pins and upporting:

- Trace log capture (diagnostic purpose)

The interface can be used for diagnostic purpose to capture trace logs activated with the +DI AT command (see the u-blox SARA-N2 Series AT Commands Manual [3]).

The main characteristics of the auxiliary UART interface are:

- Serial port with RS-232 functionality working at the **V_INT** voltage domain (0 V for low data bit or ON state and 1.8 V, i.e. **V_INT**, for high data bit or OFF state)
- Data line (**GPIO1** as module data output)
- No flow control
- Fixed baud rate: 921600 b/s
- Fixed frame format: 8N1 (8 data bits, no parity, 1 stop bit)

☞ Provide a test point connected to the **GPIO1** pin for diagnostic purpose.

☞ The trace diagnostic log is temporarily stopped when the module is in deep-sleep mode.

1.9.3 DDC (I2C) interface

☞ DDC (I^2C) interface is not supported in the "02" version of the product.

1.10 General Purpose Input/Output (GPIO)

☞ GPIOs are not supported in the "02" version of the product, except for the **GPIO1** that can be used as the Secondary UART output line to collect trace logs: it is recommended to provide a direct access to the **GPIO1** pin by means of accessible testpoint for diagnostic purpose.

1.11 Reserved pins (RSVD)

SARA-N2 series modules have pins reserved for future use, marked as **RSVD**.

All the **RSVD** pins are to be left unconnected on the application board, except for the **RSVD** pin number **33** that can be externally connected to ground.

2 Design-in

2.1 Overview

For an optimal integration of SARA-N2 series modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the related interface, however a number of points require higher attention during the design of the application device.

The following list provides a ranking of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT** pin. Antenna circuit directly affects the RF compliance of the device integrating a SARA-N2 series module with the applicable certification schemes. Very carefully follow the suggestions provided in section 2.4 for schematic and layout design.
2. Module supply: **VCC** and **GND** pins. The supply circuit affects the RF compliance of the device integrating a SARA-N2 series module with applicable certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in section 2.2 for schematic and layout design.
3. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins. Accurate design is required to guarantee SIM card functionality and compliance with applicable conformance standards, reducing also the risk of RF coupling. Carefully follow the suggestions provided in section 2.5 for schematic and layout design.
4. System function: **RESET_N** pin. Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in section 2.3 for schematic and layout design.
5. Other digital interfaces: UART and secondary UART interfaces, DDC I^2C-compatible interface and GPIOs. Accurate design is required to guarantee proper functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6 and 2.7 for schematic and layout design.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins must be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected but connect all the available pins to a solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-N2 series modules must be supplied through the **VCC** pins by a proper DC power supply that should comply with the module **VCC** requirements summarized in Table 6.

The proper DC power supply can be selected according to the application requirements (see Figure 7) between the different possible supply sources types, which most common ones are the following:

- Primary (disposable) battery
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Switching regulator
- Low Drop-Out (LDO) linear regulator

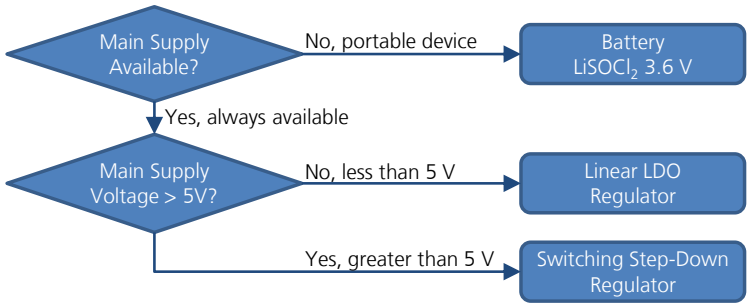

Figure 7: VCC supply concept selection

The NB-IoT technology is primarily intended for battery powered applications. A Lithium Thionyl Chloride ($LiSOCl_2$) battery directly connected to **VCC** pins is the usual choice for battery-powered devices. See sections 2.2.1.2, 2.2.1.3 and 2.2.1.6, 2.2.1.7, 2.2.1.8 for specific design-in.

The DC/DC switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the modules **VCC** operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See sections 2.2.1.2, 2.2.1.4 and 2.2.1.6, 2.2.1.7, 2.2.1.8 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See sections 2.2.1.2, 2.2.1.5 and 2.2.1.6, 2.2.1.7, 2.2.1.8 for specific design-in.

The use of rechargeable batteries is not the typical solution for NB-IoT applications, but it is feasible implementing a suitable external charger circuit. The charger circuit has to be designed to prevent over-voltage on **VCC** pins of the module, and it should be selected according to the application requirements: a DC/DC switching charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery

(e.g. 3.7 V Li-Pol) are available at the same time in the application as possible supply source, then a proper charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The usage of supercapacitors on the **VCC** supply line is generically not recommended since these components are highly temperature sensitive and may increase current leakages draining the battery faster.

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 6.

2.2.1.2 Guidelines to optimize power consumption

The NB-IoT technology is primarily intended for applications that require small amount of data exchange per day (i.e. few bytes in uplink and downlink per day) and these are typically battery powered. Depending on the application type, an operating life of 5 up to 15 years is usually required. For these reasons, the whole application board should be optimized in terms of current consumption and should carefully take into account the following aspects:

- Minimize current leakages on the power supply line
- Optimize the antenna matching since an un-matched antenna leads to higher current consumptions
- Use an application processor with digital interfaces working at the same level of the **VCC** supply input of the SARA-N2 module (for example, 3.3 V or 3.6 V. In this way it is possible to avoid voltage translators on the UART interface, which operates at the **VCC** voltage level
- Keep SARA-N2 module always powered on: the module will automatically enter the deep-sleep mode whenever possible to limit current consumption and avoid further network registration procedures each time there is an up-link message to be transmitted
- The application processor should go in standby (or lowest power consumption mode) as soon as SARA-N2 module enters the deep-sleep mode and there's no more data to be transmitted. The application processor (monitor the **V_INT** level)

2.2.1.3 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its output circuit must be capable of delivering to **VCC** pins the specified average current during a transmission at maximum power (see the SARA-N2 series Data Sheet [1] for more details). The antenna matching influences the current consumption; for this reason, the current consumption at maximum Tx power with the intended antenna (i.e. on the final application board) should be used to characterize the battery maximum pulse requirements.

  The maximum DC discharge current is not always reported in battery data sheets, but it is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable to limit as much as possible the DC resistance provided on the **VCC** supply line.

The LiSOCl2 (Lithium Thionyl Chloride Batteries) is currently the best technology available for NB-IoT applications since it provides:

- Very low self-discharge behavior and resulting ability to last longer
- Highest specific energy per unit weight and energy density per unit volume
- Wide operating temperature range

For the selection of the proper battery type, the following parameters should be taken into account:

- Capacity: > 3 Ah
- Current peak capability: ~400 mA (the consumption of whole application with the actual antenna should be considered)
- Continuous current capability: ~100 mA
- Temperature range: -20 °C to +85 °C
- Capacity vs temperature behavior: battery capacity is highly influenced by the temperature. This must be considered to properly estimate the battery life time
- Capacity vs discharge current performance
- Voltage vs temperature behavior: the battery voltage typically decreases at low temperatures values (for example, in the -10 °C / -20 °C range). In all the temperature conditions the battery voltage must always be above the SARA-N2 minimum extended operating voltage level
- Voltage vs pulse duration behavior: this information is typically not provided by battery manufacturers and many batteries reach too low voltage values during a long pulse. It is recommended to execute stress tests on battery samples to verify the voltage behavior as a function of the pulse duration and guarantee that the battery voltage is always above the minimum extended operating voltage level of SARA-N2 series
- Construction technology: spiral wound batteries are generically preferred over the bobbin construction
  - This technology typically supports high current pulses without the need for supercaps
  - A bobbin type battery usually does not support the current pulse

Figure 8 shows an example of connection of SARA-N2 module with a primary battery. Table 8 lists different batty pack part numbers that can be used.

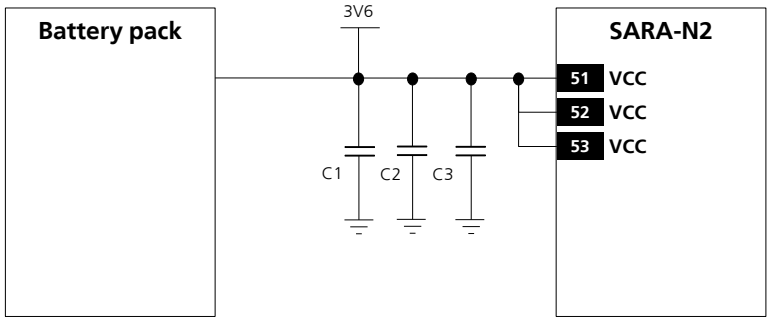

Figure 8: Suggested schematic design for the VCC voltage supply application circuit using a $LiSOCl_2$ primary battery

Reference	Description	Part Number - Manufacturer
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
Battery pack	Size FAT A LiSOCl battery, spiral wound, 3.2Ah	ER18505M - Titus Battery
	Size C LiSOCl battery, spiral wound, 6.5Ah	ER26500M - Titus Battery
	Size D LiSOCl battery, spiral wound, 13Ah	ER34615M - Titus Battery
	Size C LiSOCl battery, spiral wound, 5.8Ah	LSH14 – Saft
	Size D LiSOCl battery, spiral wound, 13Ah	LSH20 - Saft

Table 8: Suggested components for the VCC voltage supply application circuit using a $LiSOCl_2$ primary battery

An alternative battery design solution can be realized combining:

- Generic primary battery pack: not necessarily an optimized $LiSOCl_2$ spiral wound
- DC/DC buck-boost converter
- Load switch

There are switching regulators that integrate the load switch and the DC/DC converter logic with a so called bypass mode. See Figure 9 and Table 9 for an example of such an application circuit. In this case **V_INT** can be used to select between bypass and boost modes:

- V_INT = 0 V, deep-sleep, bypass mode
- V_INT = 1.8 V, out of deep-sleep, boost mode

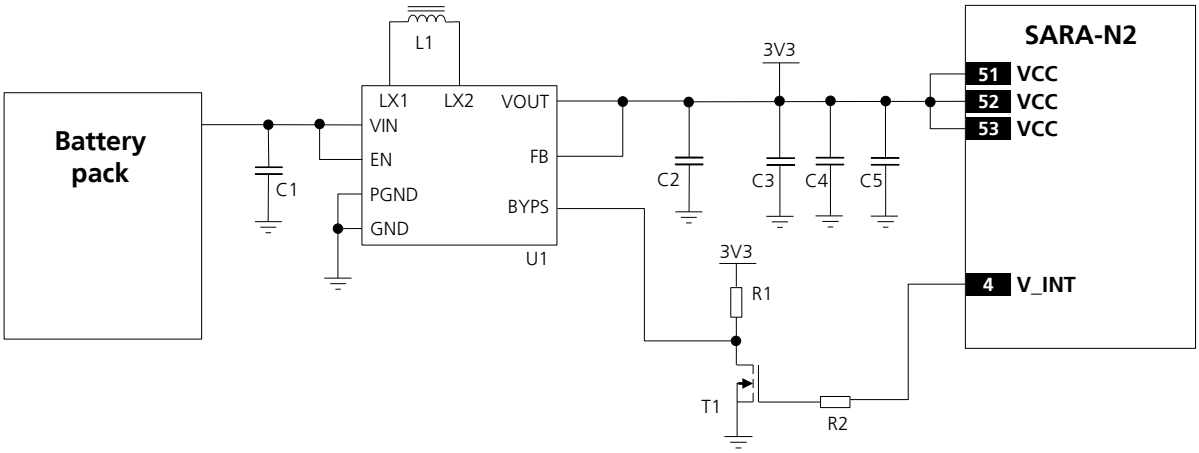

Figure 9: Alternative schematic design for the VCC voltage supply application circuit using a generic primary battery

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C2	22 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J226MEA0D - Murata
L1	1 µH Inductor 20% 3.1 A 60 mΩ	TFM201610GHM-1R0MTAA - TDK
C3, C6	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
R1	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
R2	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
T1	N-channel MOSFET	DMG1012T - Diodes Incorporated
U1	High Efficiency Low Power Buck-Boost Regulator with Bypass mode	ISL9120IRTNZ - Intersil

Table 9: Suggested components for an alternative VCC voltage supply application circuit using a generic primary battery

2.2.1.4 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.6 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins

the specified average current during a transmission at maximum power (see the SARA-N2 series Data Sheet [1]).

- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected-mode Pulse Frequency Modulation (PFM) mode and PFM/PWM mode, transitions must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators that are able to switch between low ripple PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition occurs when the module changes status from active-mode to connected-mode: it is suggest to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 10 mA).

Figure 10 and the components listed in Table 10 show an example of power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering to **VCC** pins the specified maximum current, with low output ripple and with fixed switching frequency in PWM.

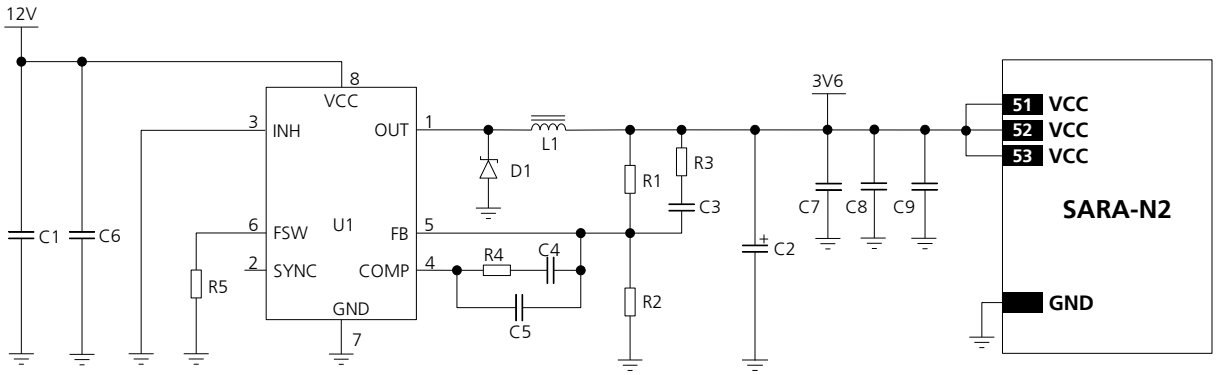

Figure 10: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2	100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 - Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 - Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 - Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H560JA01 - Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 - Murata
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C8	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C9	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
D1	Schottky Diode 25V 2 A	STPS2L25 - STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL - Coilcraft
R1	4.7 kΩ Resistor 0402 1% 0.063 W	RC0402FR-074K7L - Yageo
R2	1 kΩ Resistor 0402 1% 0.063 W	RC0402FR-071KL - Yageo
R3	82 Ω Resistor 0402 5% 0.063 W	RC0402JR-0782RL - Yageo
R4	8.2 kΩ Resistor 0402 5% 0.063 W	RC0402JR-078K2L - Yageo
R5	39 kΩ Resistor 0402 5% 0.063 W	RC0402JR-0739KL - Yageo
U1	Step-Down Regulator 8-VFQFPN 0.7 A 1 MHz	L5980TR - ST Microelectronics

Table 10: Suggested components for the VCC voltage supply application circuit using a step-down regulator

2.2.1.5 Guidelines for VCC supply circuit design using a Low Drop-Out (LDO) linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pins and of delivering to **VCC** pins the specified maximum average current during a transmission at maximum power (see the SARA-N2 series Data Sheet [1])
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator)

Figure 11 and the components listed in Table 11 show a power supply circuit example, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified current.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range. This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

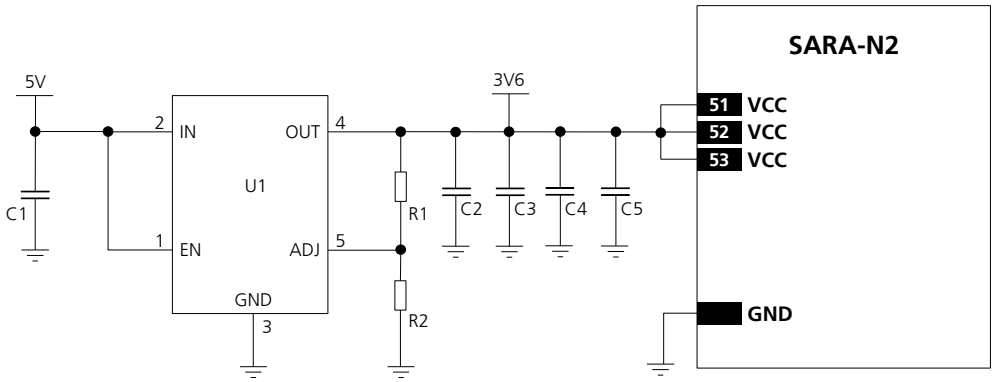

Figure 11: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	29.4 kΩ Resistor 0402 5% 0.1 W	RC0402FR-0729K4L - Yageo Phycomp
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 800 mA	LP38511TJ-ADJ/NOPB - Texas Instrument
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata

Table 11: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

2.2.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated for **VCC** supply. Another twenty pins are designated for **GND** connection. It is highly recommended to properly connect all the **VCC** pins and all the **GND** pins to supply the module, to minimize series resistance losses.

To reduce voltage noise, especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 10 µF capacitor (e.g Murata GRM188R60J106ME47) to stabilize the voltage profle at max power Tx
- 100 nF capacitor (e.g Murata GRM155R61C104K) to filter digital logic noise from clocks and data sources
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 56 pF capacitor with Self-Resonant Frequency in 700/800/900 MHz range (e.g. Murata GRM1555C1E560J) to filter transmission EMI in the NB-IoT bands 28 / 20 / 5 / 8

For devices integrating an internal antenna, it is recommended to provide space to allocate all the components shown in Figure 12 and listed in Table 12.

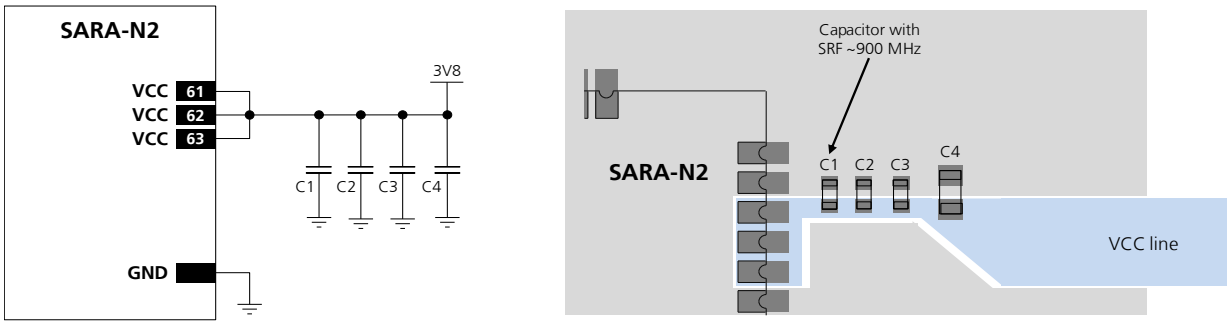

Figure 12: Suggested schematic and layout design for the VCC line, highly recommended when using an integrated antenna

Reference	Description	Part Number - Manufacturer
C1	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C4	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata

Table 12: Suggested components to reduce noise on VCC

☞ ESD sensitivity rating of the **VCC** supply pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to **VCC** pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

2.2.1.7 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing.
- The bypass capacitors in the pF range described in Figure 12 and Table 12 should be placed as close as possible to the **VCC** pins. This is highly recommended if the application device integrates an internal antenna.
- High frequency voltage ripples on the **VCC** line may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-N2 series modules in the worst case.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the cellular module, preferably closer to the DC source (otherwise protection functionality may be compromised).

2.2.1.8 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pin surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application board as ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pins also ensures thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating.

2.2.2 Interface supply (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

The **V_INT** digital interfaces 1.8 V supply output can be mainly used to:

- Indicate when the module is switched on and out of the deep-sleep mode (see section 1.6.1 for more details)
- Supply external devices in place of a discrete regulator

☞ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply, as this can cause malfunctions in internal circuitry supplies to the same domain. The SARA-N2 series Data Sheet [1] describes the detailed electrical characteristics.

☞ **V_INT** can only be used as an output; do not connect any external regulator on **V_INT**.

☞ **V_INT** supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

☞ If the **V_INT** supply output is not required by the customer application, the pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint directly for diagnostic purpose

2.2.2.2 Guidelines for V_INT layout design

There are no specific layout design recommendations for **V_INT** output.

2.3 System functions interfaces

2.3.1 Module reset (RESET_N)

2.3.1.1 Guidelines for RESET_N circuit design

As described in SARA-N2 series Data Sheet [1], the module has an internal pull-up resistor on the reset input line, so an external pull-up is not required on the application board.

Connecting the **RESET_N** input to a push button that shorts the **RESET_N** pin to ground, the pin will be externally accessible on the application device: according to EMC/ESD requirements of the application, provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point, as described in Figure 13 and Table 13.

ESD sensitivity rating of the **RESET_N** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **RESET_N** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

Connecting the **RESET_N** input to an external device (e.g. application processor), an open drain output can be directly connected without any external pull-up, as described in Figure 13 and Table 13: the internal pull-up resistor provided by the module pulls the line to the high logic level when the **RESET_N** pin is not forced low by the application processor. A compatible push-pull output of an application processor can be used too.

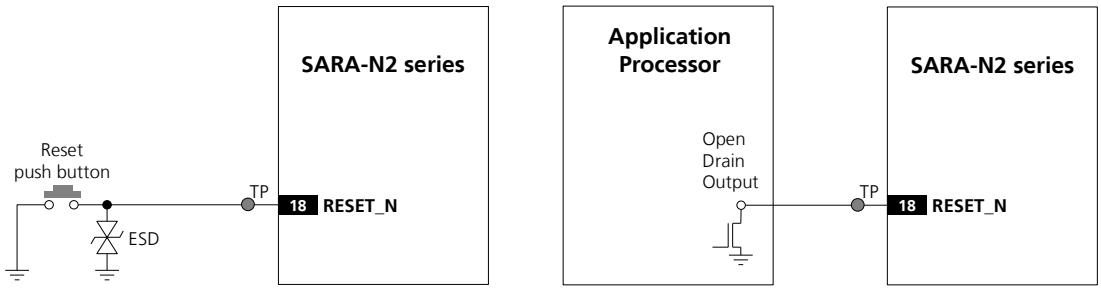

Figure 13: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 13: Example of ESD protection component for the RESET_N application circuit

If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint for diagnostic purpose.

2.3.1.2 Guidelines for RESET_N layout design

The reset circuit (**RESET_N**) requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** as short as possible.

2.4 Antenna interface

The **ANT** pin, provided by all the SARA-N2 series modules, represents the RF input/output used to transmit and receive the RF cellular signals: the antenna must be connected to this pin. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the operating bands.

2.4.1 Antenna RF interface (ANT)

2.4.1.1 General guidelines for antenna selection and design

The cellular antenna is the most critical component to be evaluated: care must be taken about it at the start of the design development, when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating a SARA-N2 series module with all the applicable required certification schemes depends from antenna radiating performance.

Cellular antennas are typically available as:

- External antenna (e.g. linear monopole):
  - External antenna usage basically does not imply physical restrictions on the design of the PCB where the SARA-N2 series module is mounted.
  - The radiation performance mainly depends on the antenna: select the antenna with optimal radiating performance in the operating bands.
  - If antenna detection functionality is required, select an antenna assembly provided with a proper built-in diagnostic circuit with a resistor connected to ground: see guidelines in section 2.4.2.
  - Select an RF cable with minimum insertion loss: additional insertion loss due to low quality or long cable reduces radiation performance.
  - Select a suitable 50 Ω connector providing proper PCB-to-RF-cable transition: it is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antenna (PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antenna implies physical restriction to the design of the PCB: the ground plane can be reduced down to a minimum size that must be similar to the quarter of the wavelength of the minimum frequency that has to be radiated. As numerical example:

    Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
  - The radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage: select the antenna with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
  - Select a complete custom antenna designed by an antenna manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide): the antenna design process should begin at the start of the whole product design process.
  - Select an integrated antenna solution provided by an antenna manufacturer if the required ground plane dimensions are large enough according to the related integrated antenna solution specifications: the antenna selection and the definition of its placement in the product layout should begin at the start of the product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
  - Further to the custom PCB and product restrictions, the antenna may require tuning to obtain the required performance for compliance with the applicable certification schemes. It is recommended to ask the antenna manufacturer for the design-in guidelines related to the custom application.

In both cases, selecting an external or an internal antenna, observe these recommendations:

- Select an antenna providing optimal return loss (or V.S.W.R.) figure over all the operating frequencies.
- Select an antenna providing optimal efficiency figure over all the operating frequencies.
- Select an antenna providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States).

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for ANT pin RF connection design

Proper transition between the **ANT** pin and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the pad designed for the **ANT** pin:

- On a multi layer board, the whole layer stack below the RF connection should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** pad, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 14
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 14

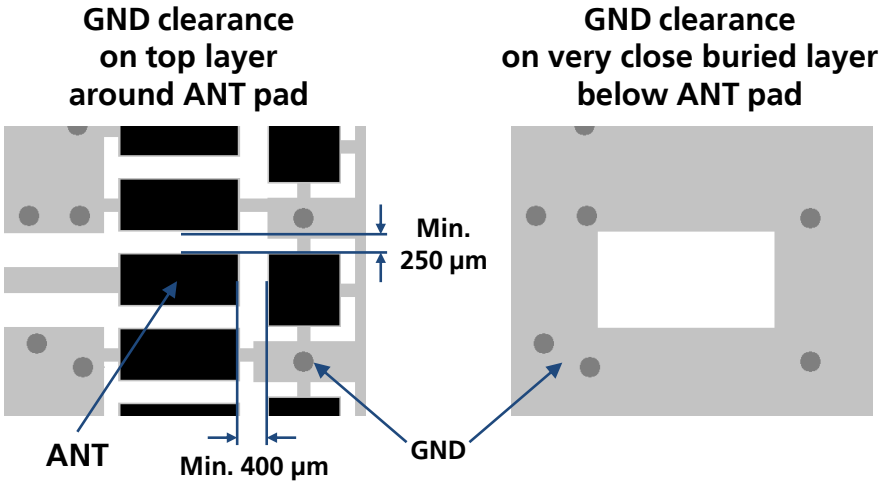

Figure 14: GND keep-out area on the top layer around ANT pad and on the very close buried layer below ANT pad

Guidelines for RF transmission line design

The transmission line from the **ANT** pad up to antenna connector or up to the internal antenna pad must be designed so that the characteristic impedance is as close as possible to 50 Ω.

The transmission line can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 15 and Figure 16 provide two examples of proper 50 Ω coplanar waveguide designs. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

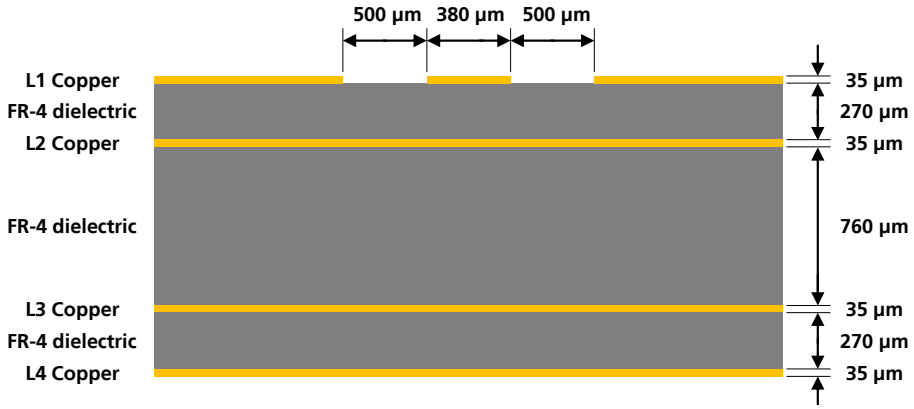

Figure 15: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

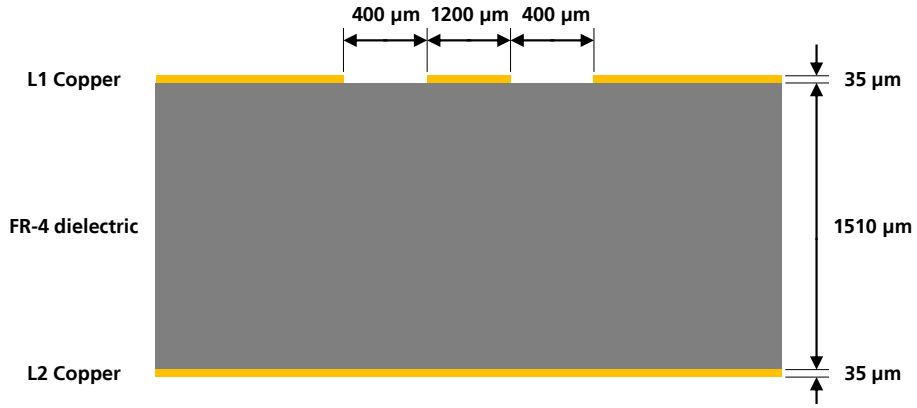

Figure 16: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB layup, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent (www.agilent.com) or TXLine from Applied Wave Research (www.mwoffice.com), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 15 and Figure 16)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 15, 1510 µm in Figure 16)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 15 and Figure 16)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 15, 400 µm in Figure 16)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for the transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission line width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND vias around transmission line, as described in Figure 17.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough on the adjacent metal layer, as described in Figure 17.
- Route RF transmission line far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as analog audio lines).
- Avoid stubs on the transmission line.
- Avoid signal routing in parallel to transmission line or crossing the transmission line on buried metal layer.
- Do not route microstrip line below discrete component or other mechanics placed on top layer.

Two examples of proper RF circuit design are reported in the Figure 17, where the antenna detection circuit is not implemented (if the antenna detection function is required by the application, follow the guidelines for circuit and layout implementation reported in section 2.4.2):

- In the first example described on the left, the **ANT** pin is directly connected to an SMA connector by means of a proper 50 Ω transmission line, designed with proper layout.
- In the second example described on the right, the **ANT** pin is connected to an SMA connector by means of a proper 50 Ω transmission line, designed with proper layout, with an additional high pass filter (consisting of a proper series capacitor and a proper shunt inductor) to improve the ESD immunity at the antenna port of SARA-N2 modules

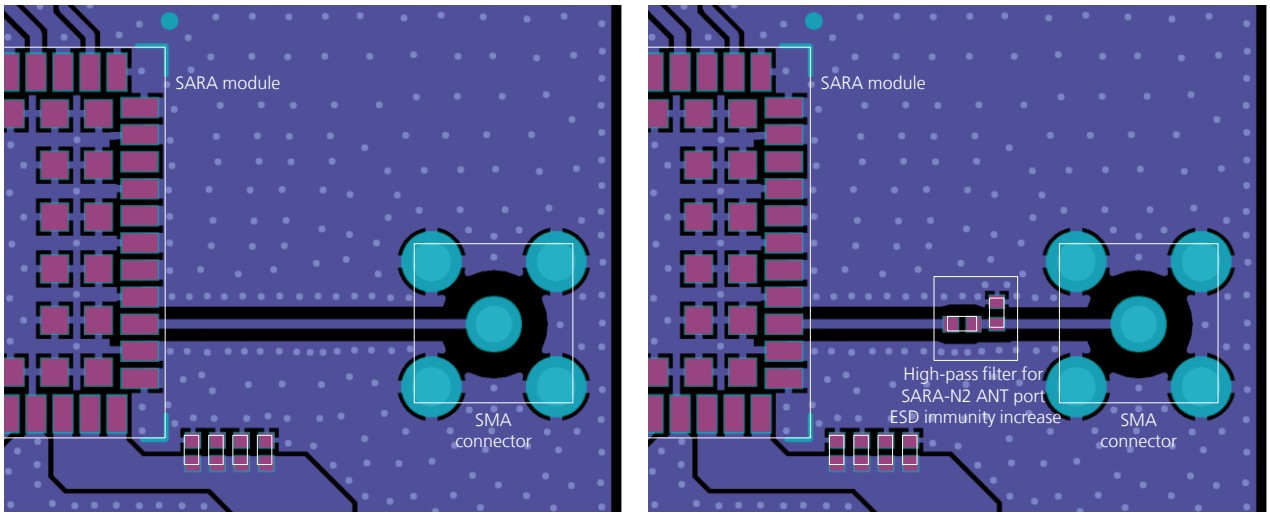

Figure 17: Suggested circuit and layout for antenna RF circuit on application board, if antenna detection is not required

Guidelines for RF termination design

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination itself, to match the characteristic impedance of the **ANT** pin of the module.

However, real antennas do not have perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antenna mismatch, the RF termination must provide optimal return loss (or V.S.W.R.) figure over all the operating frequencies, as summarized in Table 7.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing proper PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts, as shown in Figure 17.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under RF connectors and close to buried vias, to remove stray capacitance and thus keep the RF line 50 Ω: e.g. the active pad of U.FL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on first inner layer to reduce parasitic capacitance to ground

If an integrated antenna is used, the RF termination is represented by the integrated antenna itself:

- Use an antenna designed by an antenna manufacturer, providing the best possible return loss (or V.S.W.R.).
- Provide a ground plane large enough according to the related integrated antenna requirements: the ground plane of the application PCB can be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. As numerical example:

  Frequency = 824 MHz → Wavelength = 36.4 cm → Minimum GND plane size = 9.1 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna related to the custom application.

Additionally, these recommendations regarding the antenna system must be followed:

- Do not include antenna within closed metal case.
- Do not place the antenna in close vicinity to end users, since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues.
- Take care of interaction between co-located RF systems since the GSM / UMTS transmitted RF power may interact or disturb the performance of companion systems.
- The antenna shall provide optimal efficiency figure over all the operating frequencies.
- The antenna shall provide appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity does not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States).
- Consider including extra footprints for a "pi" network in between the cellular module and the antenna, for further improvement in the antenna matching circuit to reach optimal antenna performance.

Examples of antennas

Table 14 lists some examples of possible internal on-board surface-mount antennas

Manufacturer	Part Number	Product Name	Description
Taoglas	PA.25.A	Anam	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 36.0 x 6.0 x 5.0 mm
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PA.711.A	Warrior II	GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.06.A	Havok	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm
Antenova	A10340	Calvus	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 28.0 x 8.0 x 3.2 mm
Ethertronics	P522304	Prestta	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 35.0 x 9.0 x 3.2 mm
2J	2JE04		GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 24.0 x 5.5 x 4.4 mm
Yaego	ANT3505B000TWPENA		GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 35.0 x 5.0 x 6.0 mm

Table 14: Examples of internal surface-mount antennas

Table 15 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part Number	Product Name	Description
Taoglas	FXP14.A.07.0100A		GSM / WCDMA PCB Antenna with cable and U.FL connector 824..960 MHz, 1710..2170 MHz 70.4 x 20.4 mm
Taoglas	FXP14R.A.07.0100A		GSM / WCDMA PCB Antenna with cable and U.FL connector Integrated 10k shunt diagnostic resistor 824..960 MHz, 1710..2170 MHz 80.0 x 20.8 mm
Taoglas	PC29.09.0100A	TheStripe	GSM / WCDMA PCB Antenna with cable and MMCX(M)RA connector 824..960 MHz, 1710..2170 MHz 80.4 x 29.4 mm
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Ethertronics	P522310	Prestta	GSM / WCDMA PCB Antenna with cable and U.FL connector 824..960 MHz, 1710..2170 MHz 41.0 x 15.0 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm
Yaego	ANTX100P001BWPEN3		GSM / WCDMA PCB Antenna with cable and I-PEX connector 824..960 MHz, 1710..2170 MHz 50.0 x 20.0 mm

Table 15: Examples of internal antennas with cable and connector

Table 16 lists some examples of possible external antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE low-profile adhesive-mount Antenna with cable and SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm
Taoglas	GSA.8821.A.301721	I-Bar	GSM / WCDMA low-profile adhesive-mount Antenna with cable and Fakra (code-D) connector 824..960 MHz, 1710..2170 MHz 106.7 x 14.7 x 5.8 mm
Taoglas	TG.30.8112		GSM / WCDMA / LTE swivel dipole Antenna with SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm
Taoglas	OMB.8912.03F21		GSM / WCDMA pole-mount Antenna with N-type (F) connector 824..960 MHz, 1710..2170 MHz 527 x Ø 26 mm
Taoglas	FW.92.RNT.M		GSM / WCDMA whip monopole Antenna with RP-N-type(M) connector 824..960 MHz, 1710..2170 MHz 274 x Ø 20 mm
Nearson	T6150AM		GSM / WCDMA swivel monopole Antenna with SMA(M) connector 824..960 MHz, 1710..2170 MHz 179.3 x 22 x 6.5 mm
Laird Tech.	MAF94300	HEPTA-SM	GSM / WCDMA swivel monopole Antenna with SMA(M) connector 824..960 MHz, 1575.42 MHz,1710..2170 MHz, 2400..2500 MHz 161 x 9.3 mm
Laird Tech.	TRA806/171033P		GSM / WCDMA screw-mount Antenna with N-type(F) connector 824..960 MHz, 1710..2170 MHz 69.8 x Ø 38.1 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount Antenna with N-type(F) connector 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount Antenna with N-type(M) connector 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Abracon	APAMS-102		GSM / WCDMA low-profile adhesive-mount Antenna with cable and SMA(M) connector 824..960 MHz, 1710..2170 MHz 138 x 21 x 6 mm

Table 16: Examples of external antennas

2.4.2 Antenna detection interface (ANT_DET)

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 18 and Table 17 describe the recommended schematic and components for the antenna detection circuit to be provided on the application board for the diagnostic circuit that must be provided on the antenna assembly to achieve antenna detection functionality.

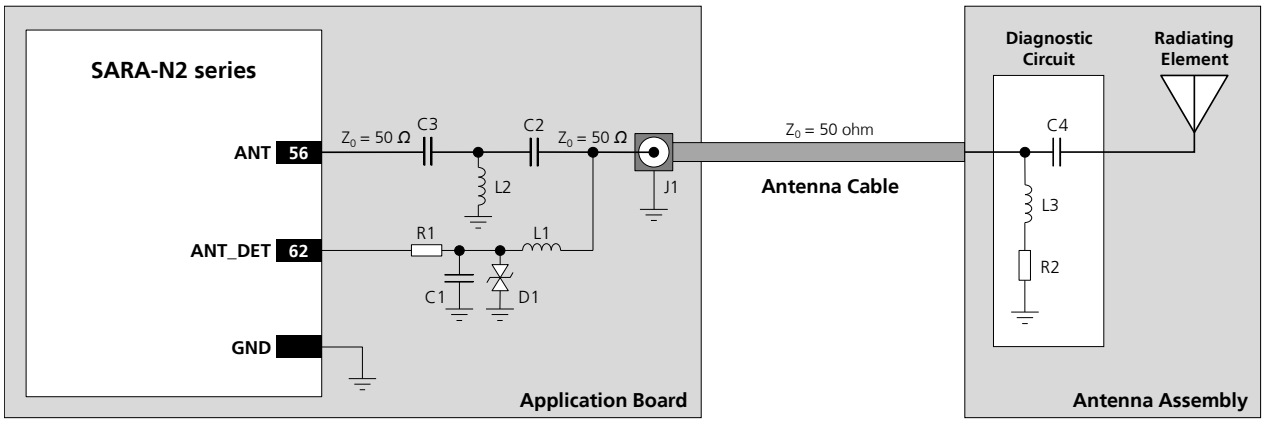

Figure 18: Suggested schematic for antenna detection circuit on application board and diagnostic circuit on antenna assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C3	SARA:U2: 15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150J - Murata
	SARA-G3: 0 Ω jumper 0402	Various Manufacturers
L2	SARA:U2: 39 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 - Murata
	SARA-G3: Do not install	
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 17: Suggested components for antenna detection circuit on application board and diagnostic circuit on antenna assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 18 and Table 17 are here explained:

- When antenna detection is forced by the dedicated AT command (see u-blox SARA-N2 series AT Commands Manual [3]), the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 18) are needed at the **ANT_DET** pin as ESD protection.
- Additional high pass filter (C3 and L2 in Figure 18) is provided at the **ANT** pin as ESD immunity improvement

- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 18, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the dedicated AT command (see u-blox SARA-N2 series AT Commands Manual [3]), the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit, or an open-circuit "over range" report, means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 17.

2.4.2.2 Guidelines for ANT_DET layout design

Figure 19 describes the recommended layout for the antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 18 and Table 17.

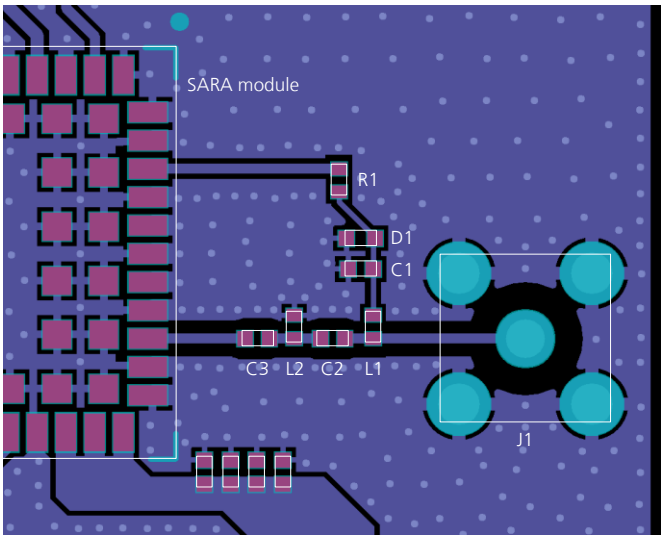

Figure 19: Suggested layout for antenna detection circuit on application board

The antenna detection circuit layout suggested in Figure 19 is here explained:

- The **ANT** pin is connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at the **ANT** pin (C2) is placed in series to the 50 Ω transmission line.
- The **ANT_DET** pin is connected to the 50 Ω transmission line by means of a sense line.
- Choke inductor in series at the **ANT_DET** pin (L1) is placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT_DET** line are placed as ESD protection.
- The additional high pass filter (C3 and L2) on the **ANT** line are placed as ESD immunity improvement.

2.5 SIM interface

2.5.1.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC) which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the cellular network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1 = VCC, C2 = RST, C3 = CLK, C5 = GND, C6 = VPP, C7 = I/O) or 8 contacts, providing also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses. Only 5 contacts are required and must be connected to the module SIM card interface as described above, since the modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Removable SIM card are suitable for applications where the SIM changing is required during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins related to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided.

Solderable UICC / SIM chip contacts mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as follows:

- Package Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Package Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Package Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Package Pin 5 = UICC Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Package Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to **GND**
- Package Pin 2 = UICC Contact C6 = VPP (Programming supply) → It can be left not connected
- Package Pin 3 = UICC Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Package Pin 4 = UICC Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can provide also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses, but only 5 contacts are required and must be connected to the module SIM card interface as described above, since the SARA-N2 series modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for SIM card connection

An application circuit for the connection to a removable SIM card placed in a SIM card holder is described in Figure 20.

Follow these guidelines connecting the module to a SIM connector:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector ESD sensitivity rating of the SIM interface pins is 1 kV (Human Body Model according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines).

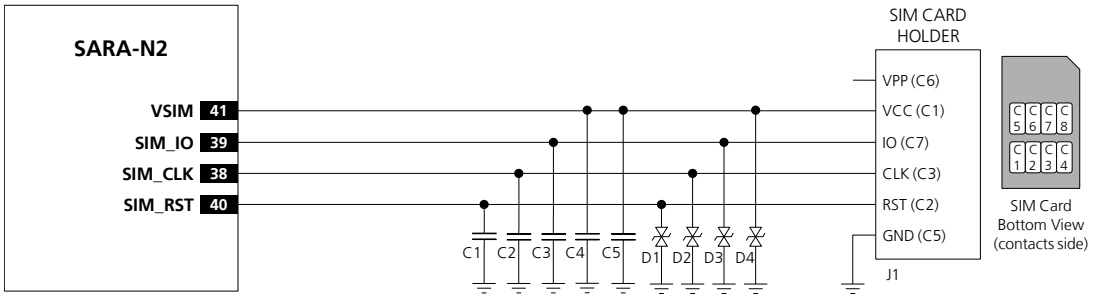

Figure 20: Application circuit for the connection to a single removable SIM card

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol

Table 18: Example of components for the connection to a removable SIM card

Guidelines for single SIM chip connection

Figure 21 describes an application circuit for the connection to a solderable SIM chip (M2M UICC Form Factor).

Follow these guidelines connecting the module to a solderable SIM chip:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**) close to the related pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface.

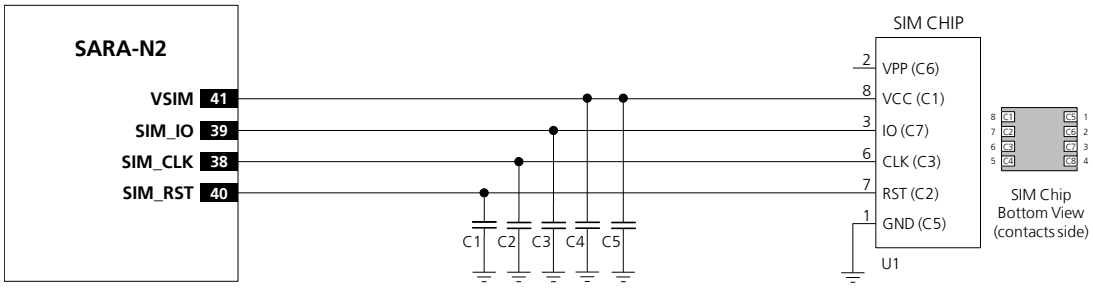

Figure 21: Application circuit for the connection to a single solderable SIM chip

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 19: Example of components for the connection to a solderable SIM chip

2.5.1.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the SARA-N2 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface: keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of the receiver channels whose carrier frequency is coincidental with harmonic frequencies: placing the RF bypass capacitors suggested in 2.5.1.1 near the SIM connector will mitigate the problem.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection as suggested in 2.5.1.1 to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications: the connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Serial interfaces

2.6.1 Asynchronous serial interface (UART)

2.6.1.1 Guidelines for UART circuit design without RING indication

If a 3.3 V Application Processor (DTE) is used, the UART interface of SARA-N2 module can be directly connected with the UART interface of the DTE as shown in Figure 22:

- Connect DTE TxD output line with the **TXD** input pin of SARA-N2
- Connect DTE RxD input line with the **RXD** output pin of SARA-N2
- Leave **RTS** and **CTS** lines of the module unconnected and floating.
- Use the same external supply rail (for example, at 3.3 V or 3.6 V) for both the SARA-N2 module and the Application Processor (DTE), so that the interface of both devices operates at the same level, considering that the UART interface of SARA-N2 module operates at the **VCC** voltage level

Hardware flow control lines **CTS** and **RTS** are not supported by "02" product versions.

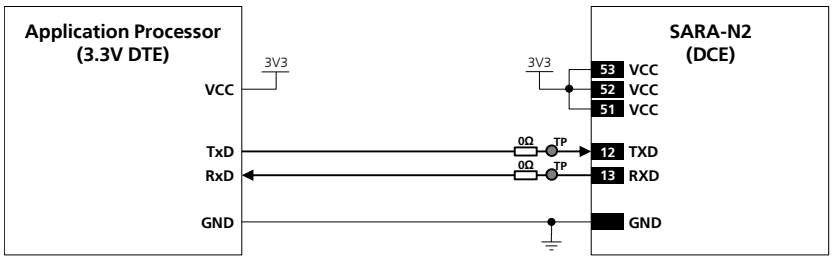

Figure 22: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (3.3 V DTE)

If a 1.8 V Application Processor (DTE) is used, then it is recommended to connect the UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **VCC** line as the supply for the voltage translators on the module side, as described in Figure 23.

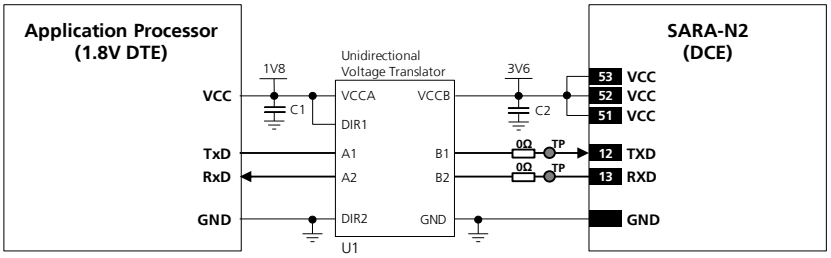

Figure 23: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (1.8 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74LVC2T45 - Texas Instruments

Table 20: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (1.8 V DTE)

It is not recommended to use **V_INT** pin as the control line of the external voltage translator

It is recommended to provide a direct access to the **TXD** and **RXD** lines by means of accessible testpoints for diagnostic purpose

2.6.1.2 Guidelines for UART circuit design with RING indication

If the application board requires a RING indication to get notifications when an URC or when new data is available, the **CTS** line can be used for such a functionality. In this case the circuit should be implemented as shown in Figure 24:

- Connect DTE TxD output line with the **TXD** input pin of SARA-N2
- Connect DTE RxD input line with the **RXD** output pin of SARA-N2
- Connect DTE RI input line with the **CTS** output pin of SARA-N2
- Leave **RTS** line of the module unconnected and floating.
- Use the same external supply rail (for example, at 3.3 V or 3.6 V) for both the SARA-N2 module and the Application Processor (DTE), so that the interface of both devices operates at the same level, considering that the UART interface of SARA-N2 module operates at the **VCC** voltage level

Hardware flow control lines **CTS** and **RTS** are not supported by "02" product versions.

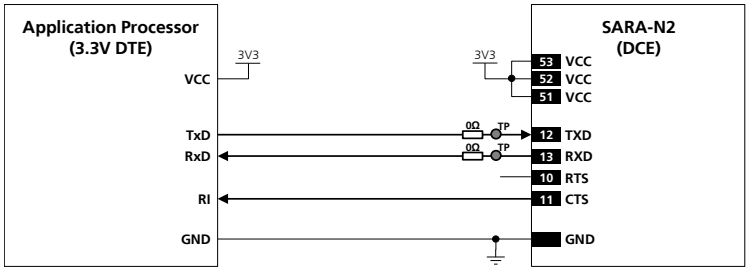

Figure 24: UART interface application circuit with partial V.24 link (3-wire) serial communication and RING indication (3.3 V DTE)

2.6.1.3 Additional considerations

If a 1.8 V Application Processor (DTE) is used, the voltage scaling from any UART output of the DCE, working at **VCC** voltage level (3.6 V nominal) to the apposite 1.8 V input of the DTE can be implemented, as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the Application Processor (DTE) for the correct selection of the voltage divider resistance values.

ESD sensitivity rating of UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.6.1.4 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 Secondary asynchronous serial interface (Secondary UART)

2.6.2.1 Guidelines for Secondary UART circuit design

The Secondary UART interface is provided on the **GPIO1** pin and can be used for diagnostic, to collect trace logs.

A suitable application circuit can be the one illustrated in Figure 25, where direct external access is provided for diagnostic purpose by means of Test-Points made available on the application board for **GPIO1** and **V_INT** lines.

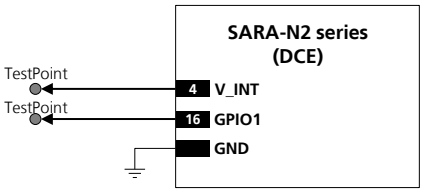

Figure 25: UART AUX interface application circuit providing direct external access for diagnostic purpose

The circuit with a 1.8 V application processor should be implemented as described in Figure 26.

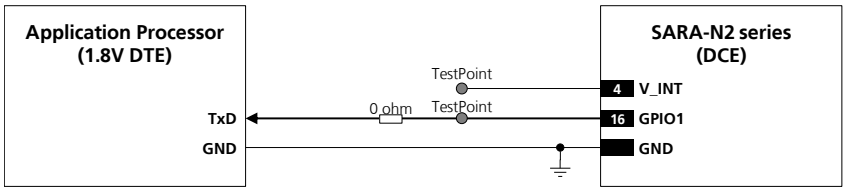

Figure 26: UART AUX interface application circuit connecting a 1.8 V application processor

If a 3.3 V application processor is used, then it is recommended to connect the 1.8 V auxiliary UART interface of the module by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 27.

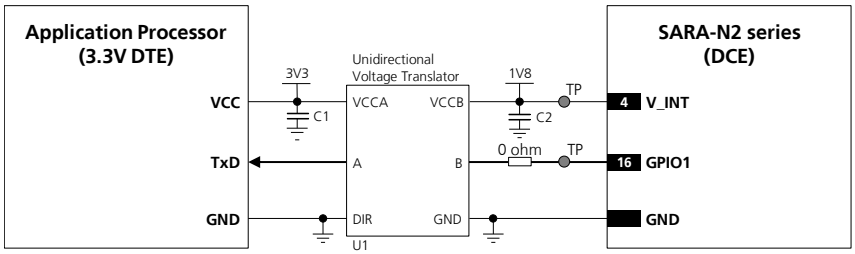

Figure 27: UART AUX interface application circuit connecting a 3.3 V application processor

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74LVC1T45 - Texas Instruments

Table 21: Component for UART AUX interface application circuit connecting a 3.3 V application processor

☞ It is recommended to provide a direct access to the **GPIO1** pin by means of accessible testpoints for diagnostic purpose

☞ ESD sensitivity rating of auxiliary UART pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.6.3 DDC (I^2C) interface

☞ DDC (I^2C) interface is not supported by the "02" version of the product.

2.7 General Purpose Input/Output (GPIO)

☞ GPIOs are not supported by the "02" version of the product.

As described in sections 1.9.2 and 2.6.2, the **GPIO1** can be used as the Secondary UART output line to collect trace logs: it is recommended to provide a direct access to the **GPIO1** pin by means of accessible testpoint for diagnostic purpose.

2.8 Reserved pins (RSVD)

SARA-N2 series modules have pins reserved for future use, marked as **RSVD**.

All the **RSVD** pins are to be left unconnected on the application board, except for the **RSVD** pin number **33** that can be externally connected to ground.

2.9 Module placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

Make sure that the module, RF and analog parts / circuits are clearly separated from any possible source of radiated energy, including digital circuits that can radiate some digital frequency harmonics, which can produce Electro-Magnetic Interference affecting module, RF and analog parts / circuits' performance or implement proper countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Make sure that the module, RF and analog parts / circuits, high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by Electro-Magnetic Interference or employ countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Provide enough clearance between the module and any external part.

2.10 Module footprint and paste mask

Figure 28 and Table 22 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, implementing the solder mask opening 50 µm larger per side than the corresponding copper pad.

The recommended solder paste thickness is 150 µm, according to application production process requirements.

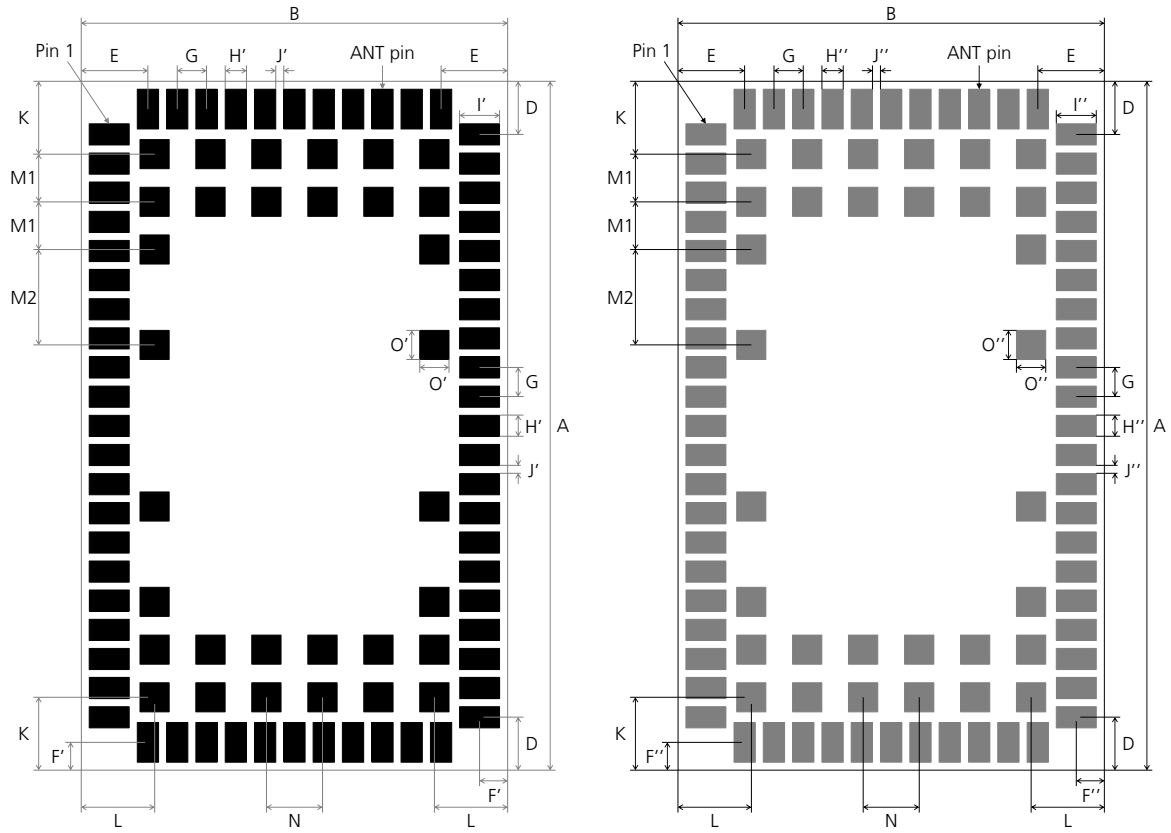

Figure 28: SARA-N2 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	G	1.10 mm	K	2.75 mm
B	16.0 mm	H'	0.80 mm	L	2.75 mm
C	3.00 mm	H''	0.75 mm	M1	1.80 mm
D	2.00 mm	I'	1.50 mm	M2	3.60 mm
E	2.50 mm	I''	1.55 mm	N	2.10 mm
F'	1.05 mm	J'	0.30 mm	O'	1.10 mm
F''	1.00 mm	J''	0.35 mm	O''	1.05 mm

Table 22: SARA-N2 series modules suggested footprint and paste mask dimensions

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.11 Schematic for SARA-N2 series module integration

Figure 29 is an example of a schematic diagram where a SARA-N2 series module "02" product version is integrated into an application board, using all the available interfaces and functions of the module.

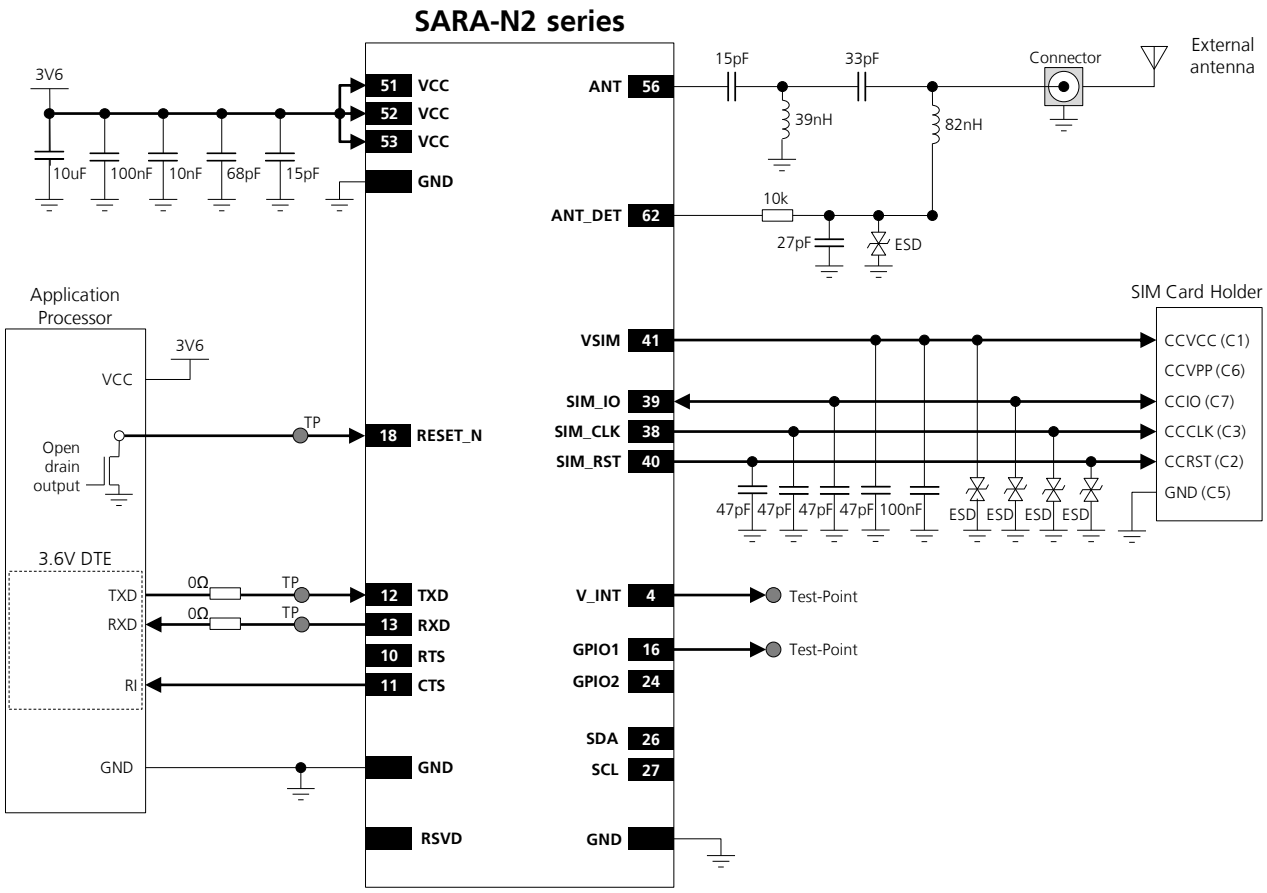

Figure 29: Example of schematic diagram to integrate a SARA-N2 module "02" product version using all available interfaces

2.12 Design-in checklist

This section provides a design-in checklist.

2.12.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin above the minimum operating range limit.
- ☑ DC supply must be capable of providing, at **VCC** pins, the specified average current during a transmission at maximum power with a voltage level above the minimum operating range limit.
- ☑ **VCC** supply should be clean, with very low ripple/noise.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, since the signal names follow the ITU-T V.24 Recommendation [4].
- ☑ Provide accessible testpoints directly connected to the following pins: **TXD**, **RXD**, **GPIO1**, **V_INT** and **RESET_N** for diagnostic purpose.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ Any external signal connected to any generic digital interface pin must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** output of the module), to avoid latch-up of circuits and let a proper boot of the module.
- ☑ All unused pins can be left unconnected.

2.12.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** pad (antenna RF input/output interface).
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (like SIM signals and high-speed digital lines).
- ☑ **VCC** line should be wide and short.
- ☑ Route **VCC** supply line away from sensitive analog signals.
- ☑ Ensure proper grounding.
- ☑ Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.

2.12.3 Antenna checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Follow the guidelines in section 2.4.2 to get proper antenna detection functionality, if required.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the SARA-N2 series Data Sheet [1] and the u-blox Package Information Guide [2].

3.2 Handling

The SARA-N2 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ **Ensure ESD precautions are implemented during handling of the module.**

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of SARA-N2 series modules (as Human Body Model according to JESD22-A114F) is specified in the SARA-N2 series Data Sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the SARA-N2 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,…).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.10

☞ The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Reflow profiles are to be selected according to the following recommendations.

⚠ **Failure to observe these recommendations can result in severe damage to the device!**

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 to 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 to 200 °C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of 217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217 °C liquidus temperature: 40 to 60 s
- Peak reflow temperature: 245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

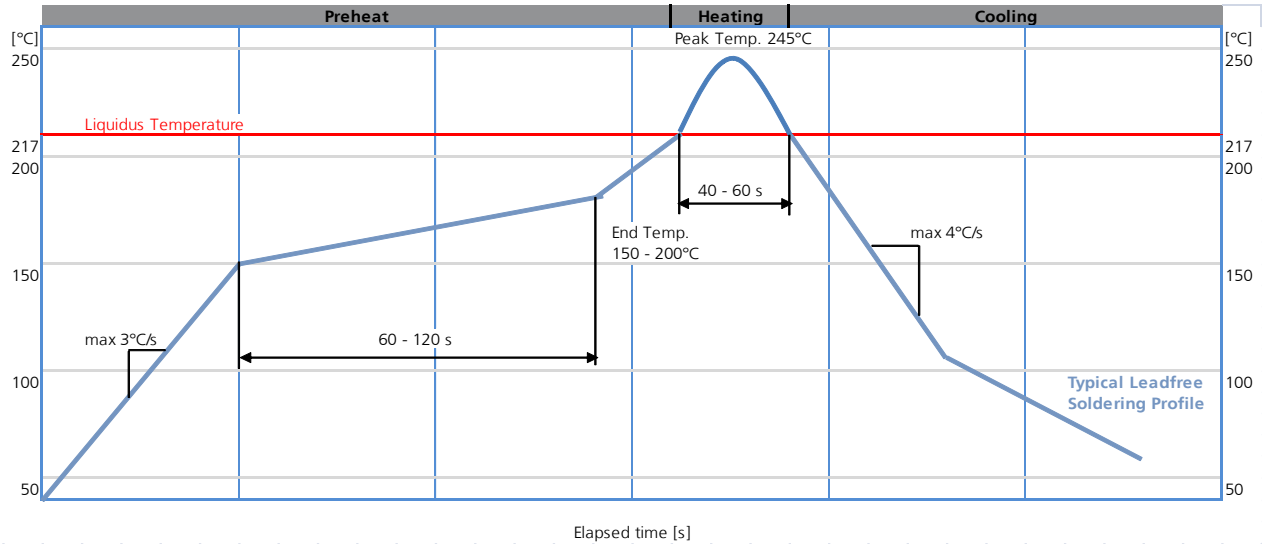

Figure 30: Recommended soldering profile

SARA-N2 series modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the SARA-N2 series modules, inspect the modules optically to verify that the module is properly aligned and centered.

3.3.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a SARA-N2 series module populated on it.

3.3.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with SARA-N2 series modules.

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the RF properties of the SARA-N2 series modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the SARA-N2 series modules before implementing this in the production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the SARA-N2 series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

SARA-N2 series modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the SARA-N2 series modules caused by any Ultrasonic Processes.

4 Approvals

4.1 Reliability tests

Tests for product family qualifications are according to ISO 16750 "Road vehicles - Environmental conditions and testing for electrical and electronic equipment", and appropriate standards.

4.2 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" RoHS).

SARA-N2 series modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

Table 23 lists the scheduled approvals for SARA-N2 series modules.

Certification Scheme	SARA-N200	SARA-N201	SARA-N210	SARA-N211	SARA-N280
CE (European Conformity)	•		•	•	
CCC (China Compulsory Certification)	•	•			
NCC (Taiwanese National Communications Commission)					•
Anatel (Agência Nacional de Telecomunicações Brazil)					•
RCM (Australia Regulatory Compliance Mark)					•

Table 23: SARA-N2 series series main certification approvals

☞ For all the certificates of compliancy and for the complete list of approvals (including countries' and network operators' approvals) of SARA-N2 series series modules, see our website (http://www.u-blox.com/) or please contact the u-blox office or sales representative nearest you.

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Functional tests (serial interface communication, real time clock)
- Digital tests (GPIOs, digital interfaces)
- Measurement and calibration of RF characteristics in all supported bands (Receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels)
- Verification of RF characteristics after calibration (modulation accuracy, power levels and spectrum performance are checked to be within tolerances when calibration parameters are applied)

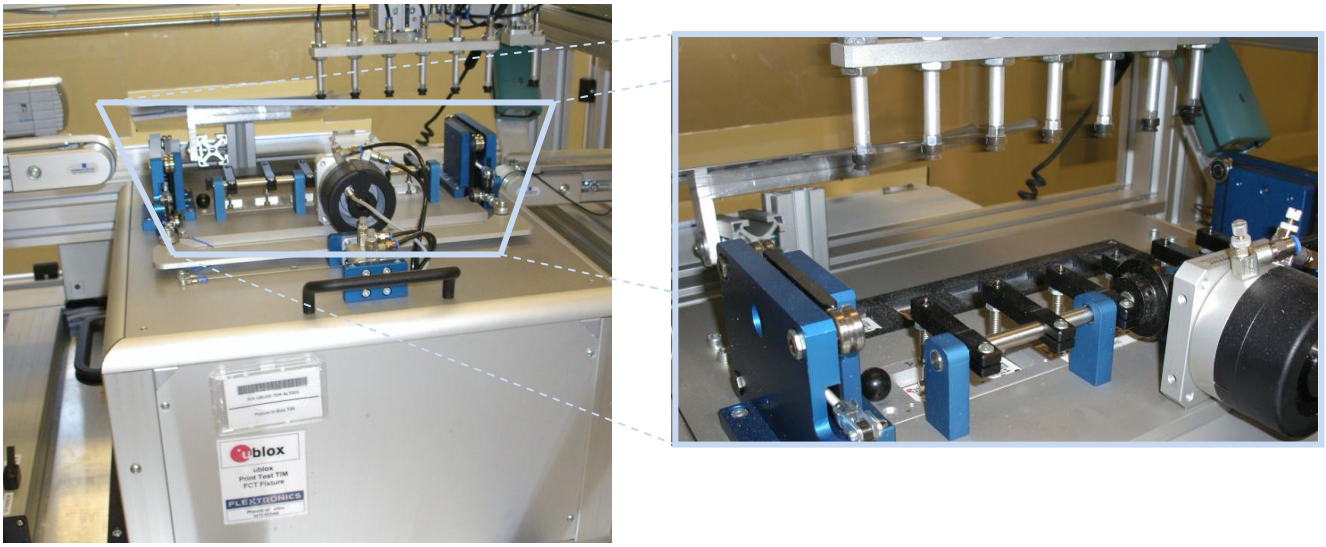

Figure 31: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damaged the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, AT commands can be used to perform functional tests and to perform RF performance tests.

Appendix

A Migration between SARA modules

A.1 Overview

SARA-G3 2G modules, SARA-U2 3G/2G modules, SARA-R4 LTE Cat M1 modules and SARA-N2 NB-IoT modules have exactly the same u-blox SARA form factor (26.0 x 16.0 mm, 96-pin LGA), with compatible pin assignment as described in Figure 32, so that the modules can be alternatively mounted on a single application board using exactly the same copper mask, solder mask and paste mask.

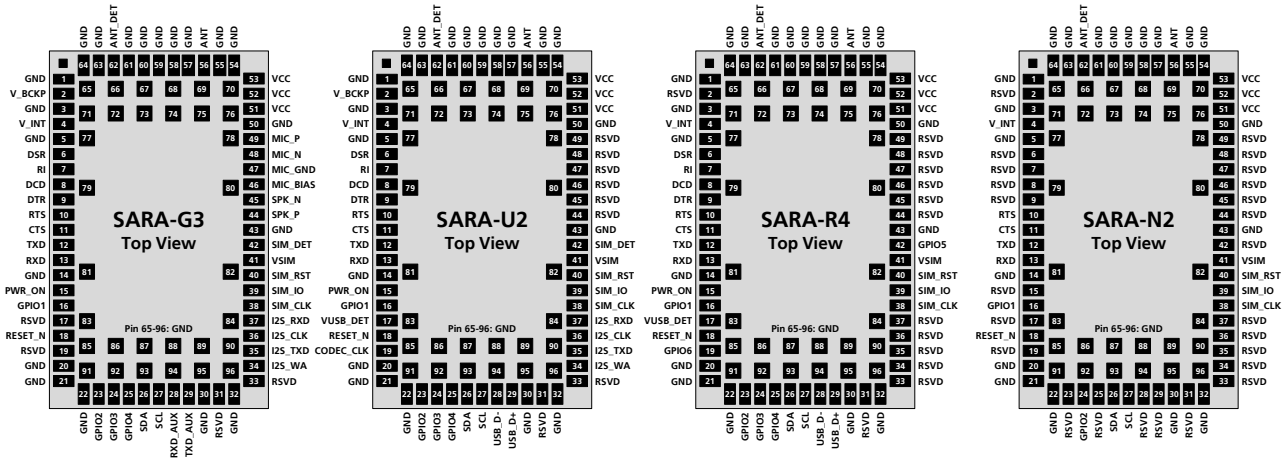

Figure 32: SARA-G3, SARA-U2, SARA-R4 and SARA-N2 series modules' layout and pin assignment

SARA modules are also form-factor compatible with the u-blox LISA, LARA and TOBY cellular module families: although each has a different form factor, the footprints for the TOBY, LISA, SARA and LARA modules have been developed to ensure layout compatibility.

With the u-blox "nested design" solution, any TOBY, LISA, SARA or LARA module can be alternatively mounted on the same space of a single "nested" application board as described in Figure 33. Guidelines in order to implement a nested application board, description of the u-blox reference nested design and comparison between TOBY, LISA, SARA and LARA modules are provided in the Nested Design Application Note [5].

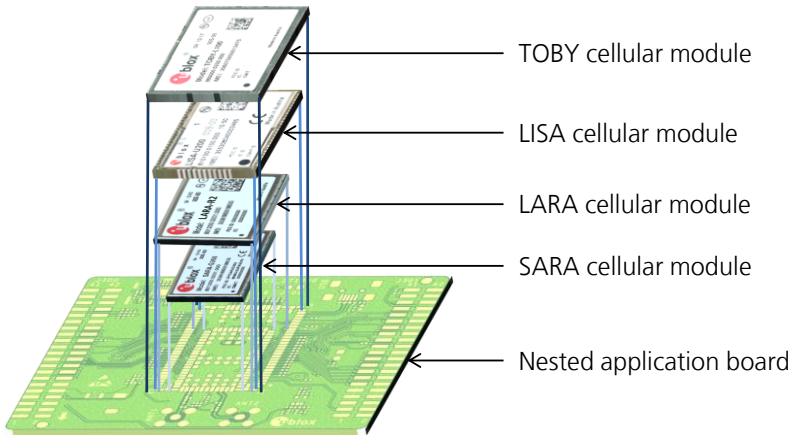

Figure 33: TOBY, LISA, SARA, LARA modules' layout compatibility: all modules are accommodated on the same nested footprint

Table 24 summarizes the interfaces provided by SARA-G3, SARA-U2, SARA-R4 and SARA-N2 series modules, while Figure 34 summarizes the frequency ranges of the modules' operating bands.

Modules	RAT	Power			System			SIM		Serial						Audio			Other			
		Module supply input	RTC supply I/O	1.8 V supply Output	Switch-on input	Switch-off input	Reset input	SIM interface	SIM detection	UART	UART AUX	SPI	USB	SDIO	DDC (I2C)	Analog audio	Digital audio	13/26 MHz output	GPIOs	Network indication	Antenna detection	GNSS via modem
SARA-G3	2G	●	●	●	●		●	●	●	●	●				●	●	●		●	●	●	●
SARA-U2	3G / 2G	●	●	●	●	●	●	●	●	●			●		●		●	●	●	●	●	●
SARA-R4	LTE Cat M1	●		●	●	●	●	●	●	●		□	●	□	□		□	□	●	●	●	□
SARA-N2	NB-IoT	●		●			●	●		●	●				□				□	●	●	□

● = supported by available product version □ = supported by future product versions

Table 24: Summary of SARA-G3, SARA-U2, SARA-R4 and SARA-N2 series modules interfaces

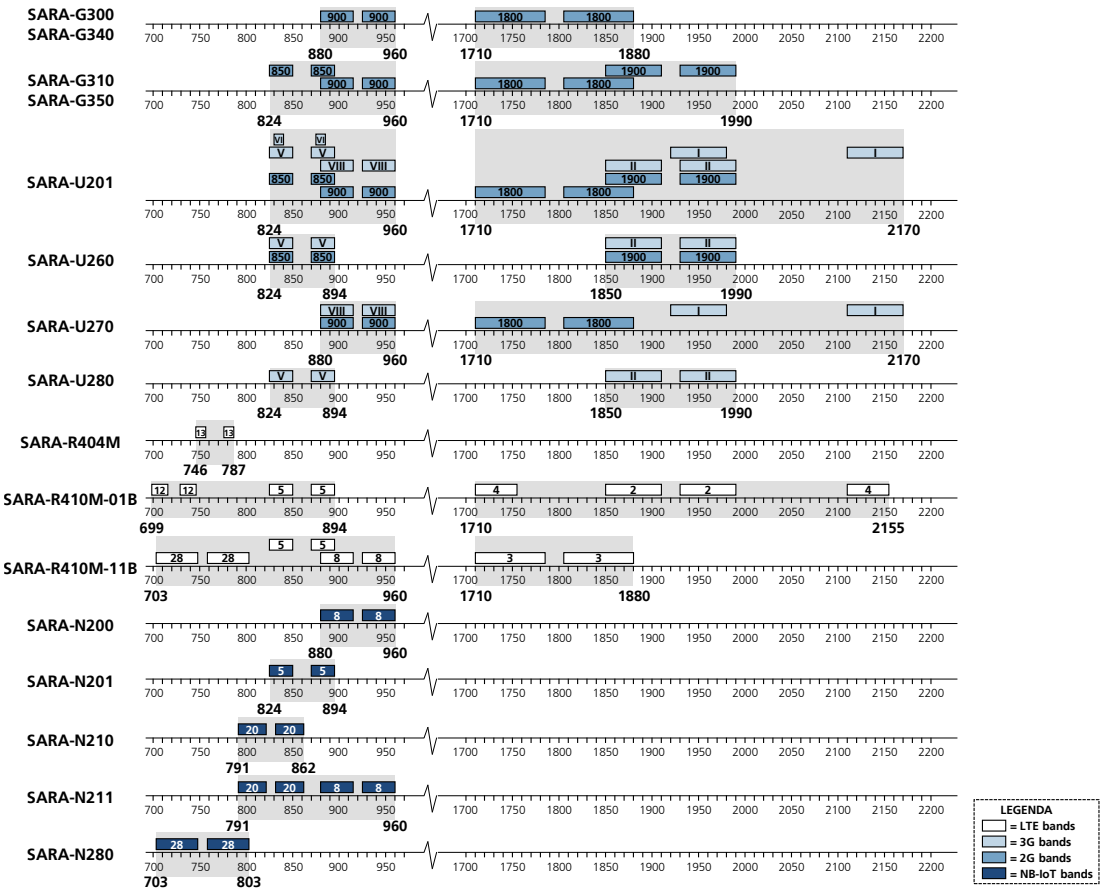

Figure 34: Summary of operating frequency bands supported by SARA-G3, SARA-U2, SARA-R4 and SARA-N2 series modules

A.2 Pin-out comparison between SARA-G3, SARA-U2, SARA-R4 and SARA-N2 modules

	SARA-G3		SARA-U2		SARA-R4		SARA-N2		
No	**Pin Name**	**Description**	**Pin Name**	**Description**	**Pin Name**	**Description**	**Pin Name**	**Description**	**Remarks for migration**
1	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
2	V_BCKP	RTC Supply I/O	V_BCKP	RTC Supply I/O	RSVD	Reserved	RSVD	Reserved	RTC supply vs Reserved
3	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
4	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 70 mA max	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 70 mA max	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 70 mA max Switched-off in deep-sleep	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 70 mA max Switched-off in deep-sleep	V_INT is switched off when R4 and N2 are in deep-sleep state TestPoint always recommended
5	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
6	DSR	UART DSR Output V_INT level (1.8 V) Driver strength: 6 mA	DSR	UART DSR Output V_INT level (1.8 V) Driver strength: 1 mA	DSR	UART DSR Output V_INT level (1.8 V) Driver strength: 2 mA	RSVD	Reserved	Not supported by SARA-N2 Diverse driver strength
7	RI	UART RI Output V_INT level (1.8 V) Driver strength: 6 mA	RI	UART RI Output V_INT level (1.8 V) Driver strength: 2 mA	RI	UART RI Output V_INT level (1.8 V) Driver strength: 2 mA	RSVD	Reserved	Not supported by SARA-N2 Diverse driver strength
8	DCD	UART DCD Output V_INT level (1.8 V) Driver strength: 6 mA	DCD	UART DCD Output V_INT level (1.8 V) Driver strength: 2 mA	DCD	UART DCD Output V_INT level (1.8 V) Driver strength: 2 mA	RSVD	Reserved	Not supported by SARA-N2 Diverse driver strength
9	DTR	UART DTR Input V_INT level (1.8 V) Internal pull-up: ~33 k	DTR	UART DTR Input V_INT level (1.8 V) Internal pull-up: ~14 k	DTR	UART DTR Input V_INT level (1.8 V) Internal pull-up: ~100 k	RSVD	Reserved	Not supported by SARA-N2 Diverse internal pull-up value
10	RTS	UART RTS Input V_INT level (1.8 V) Internal pull-up:~58 k	RTS	UART RTS Input V_INT level (1.8 V) Internal pull-up: ~8 k	RTS	UART RTS Input V_INT level (1.8 V) Internal pull-up: ~100 k	RTS	UART RTS Input[2] VCC level (3.6 V typ.) Internal pull-up: ~78 k	Diverse level (V_INT vs VCC) Diverse internal pull-up value
11	CTS	UART CTS Output V_INT level (1.8 V) Driver strength: 6 mA	CTS	UART CTS Output V_INT level (1.8 V) Driver strength: 6 mA	CTS	UART CTS Output V_INT level (1.8 V) Driver strength: 2 mA	CTS	UART CTS Output[2] VCC level (3.6 V typ.) Driver strength: 1 mA Configurable as RI output line	Diverse level (V_INT vs VCC) Diverse driver strength. Diverse functions supported.
12	TXD	UART Data Input V_INT level (1.8 V) Internal pull-up:~18 k	TXD	UART Data Input V_INT level (1.8 V) Internal pull-up: ~8 k	TXD	UART Data Input V_INT level (1.8 V) Internal pull-up: ~100 k	TXD	UART Data Input VCC level (3.6 V typ.) Internal pull-up: ~78 k	Diverse level (V_INT vs VCC) Diverse internal pull-up value TestPoint always recommended
13	RXD	UART Data Output V_INT level (1.8 V) Driver strength: 6 mA	RXD	UART Data Output V_INT level (1.8 V) Driver strength: 6 mA	RXD	UART Data Output V_INT level (1.8 V) Driver strength: 2 mA	RXD	UART Data Output VCC level (3.6 V typ.) Driver strength: 1 mA	Diverse level (V_INT vs VCC) Diverse driver strength TestPoint always recommended
14	GND	Ground	GND	Ground	GND	Ground	GND	Ground	

[2] Supported by future product version

No	SARA-G3 Pin Name	SARA-G3 Description	SARA-U2 Pin Name	SARA-U2 Description	SARA-R4 Pin Name	SARA-R4 Description	SARA-N2 Pin Name	SARA-N2 Description	Remarks for migration
15	PWR_ON	Power-on Input No internal pull-up L-level: -0.10 V ÷ 0.65 V H-level: 2.00 V ÷ 4.50 V ON L-level time: 5 ms min OFF L-level pulse time: Not Available	PWR_ON	Power-on Input No internal pull-up L-level: -0.30 V ÷ 0.65 V H-level: 1.50 V ÷ 4.40 V ON L-level pulse time: 50 µs min / 80 µs max OFF L-level pulse time: 1 s min	PWR_ON	Power-on Input 200 k internal pull-up L-level: -0.30 V ÷ 0.35 V H-level: 1.17 V ÷ 2.10 V ON L-level pulse time: 0.15 s min – 3.2 s max OFF L-level pulse time: 1.5 s min	RSVD	Reserved	Not supported by SARA-N2 Internal vs No internal pull-up Diverse voltage levels. Diverse timings. Diverse functions supported. TestPoint recommended for R4
16	GPIO1 / RSVD	GPIO (G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Default: Pin disabled Driver strength: 6 mA	GPIO1	GPIO V_INT level (1.8 V) Default: Pin disabled Driver strength: 6 mA	GPIO1	GPIO V_INT level (1.8 V) Default: Pin disabled Driver strength: 2 mA	GPIO1	GPIO V_INT level (1.8 V) Configurable as secondary UART data output: TestPoint recommended for diagnostic	Diverse driver strength TestPoint recommended for N2
17	RSVD	Reserved	VUSB_DET	5 V, USB Supply Detect Input	VUSB_DET	5 V, USB Supply Detect Input	RSVD	Reserved	USB detection vs Reserved TestPoint recommended for U2/R4
18	RESET_N	Reset input Internal diode & pull-up L-level: -0.30 V ÷ 0.30 V H-level: 2.00 V ÷ 4.70 V Reset L-level pulse time: 50 ms min (G340/G350) 3 s min (G300/G310)	RESET_N	Abrupt shutdown / reset input 10 kΩ internal pull-up L-level: -0.30 V ÷ 0.51 V H-level: 1.32 V ÷ 2.01 V Reset L-level pulse time: 50 ms min	RESET_N	Abrupt shutdown input 37 k internal pull-up L-level: -0.30 V ÷ 0.35 V H-level: 1.17 V ÷ 2.10 V OFF L-level pulse time: 10 s min	RESET_N	Reset input 78 k internal pull-up L-level: -0.30 V ÷ 0.36*VCC H-level: 0.52*VCC ÷ VCC Reset L-level pulse time: 100 ms min	Diverse internal pull-up Diverse voltage levels. Diverse timings. Diverse functions supported. TestPoint always recommended
19	RSVD	Reserved	CODEC_CLK	13 or 26 MHz Output V_INT level (1.8 V) Default: Pin disabled Driver strength: 4 mA	GPIO6	GPIO V_INT level (1.8 V) Default: Pin disabled Driver strength: 2 mA	RSVD	Reserved	Clock / GPIO vs Reserved
20-22	GND	Ground	GND	Ground	GND	Ground	GND	Ground	

No	SARA-G3 Pin Name	SARA-G3 Description	SARA-U2 Pin Name	SARA-U2 Description	SARA-R4 Pin Name	SARA-R4 Description	SARA-N2 Pin Name	SARA-N2 Description	Remarks for migration
23	GPIO2 / RSVD	GPIO (G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Default: GNSS supply enable Driver strength: 6 mA	GPIO2	GPIO V_INT level (1.8 V) Default: GNSS supply enable Driver strength: 1 mA	GPIO2	GPIO V_INT level (1.8 V) Default: Pin disabled Driver strength: 2 mA	RSVD	Reserved	GPIO vs Reserved
24	GPIO3 / 32K_OUT	GPIO (G340/G350) 32 kHz Output (G300/G310) V_INT level (1.8 V) Default: GNSS data ready Driver strength: 5 mA	GPIO3	GPIO V_INT level (1.8 V) Default: GNSS data ready Driver strength: 6 mA	GPIO3	GPIO V_INT level (1.8 V) Default: Pin disabled Driver strength: 2 mA	GPIO2	GPIO[3] V_INT level (1.8 V) Default: Pin disabled Driver strength: 1 mA	Diverse driver strength
25	GPIO4 / RSVD	GPIO (G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Default: GNSS RTC sharing Driver strength: 6 mA	GPIO4	GPIO V_INT level (1.8 V) Default: GNSS RTC sharing Driver strength: 6 mA	GPIO4	GPIO V_INT level (1.8 V) Default: Output/Low Driver strength: 2 mA	RSVD	Reserved	GPIO vs Reserved
26	SDA / RSVD	I²C Data I/O (G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Open drain No internal pull-up	SDA	I²C Data I/O V_INT level (1.8 V) Open drain No internal pull-up	SDA	I²C Data I/O[3] V_INT level (1.8 V) Open drain Internal 2.2 k pull-up	SDA	I²C Data I/O[3] V_INT level (1.8 V) Open drain No internal pull-up	Internal vs No internal pull-up
27	SCL / RSVD	I²C Clock Output (G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Open drain No internal pull-up	SCL	I²C Clock Output V_INT level (1.8 V) Open drain No internal pull-up	SCL	I²C Clock Output[3] V_INT level (1.8 V) Open drain Internal 2.2 k pull-up	SCL	I²C Clock Output[3] V_INT level (1.8 V) Open drain No internal pull-up	Internal vs No internal pull-up
28	RXD_AUX	Aux UART Data Out V_INT level (1.8 V)	USB_D-	USB Data I/O (D-) High-Speed USB 2.0	USB_D-	USB Data I/O (D-) High-Speed USB 2.0	RSVD	Reserved	USB / AUX UART vs Reserved TestPoint recommended for SARA-G3/U2/R4 modules
29	TXD_AUX	Aux UART Data In V_INT level (1.8 V)	USB_D+	USB Data I/O (D+) High-Speed USB 2.0	USB_D+	USB Data I/O (D+) High-Speed USB 2.0	RSVD	Reserved	USB / AUX UART vs Reserved TestPoint recommended for SARA-G3/U2/R4 modules
30	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
31	RSVD / EXT32K	Reserved (G340/G350) 32 kHz Input (G300/G310)	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	32 kHz Input vs Reserved
32	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
33	RSVD	It must be connected to GND	RSVD	It must be connected to GND	RSVD	It can be connected to GND	RSVD	It can be connected to GND	

[3] Supported by future product version

No	SARA-G3 Pin Name	SARA-G3 Description	SARA-U2 Pin Name	SARA-U2 Description	SARA-R4 Pin Name	SARA-R4 Description	SARA-N2 Pin Name	SARA-N2 Description	Remarks for migration
34	I2S_WA / RSVD	I²S Word Align.(G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Driver strength: 6 mA	I2S_WA	I²S Word Alignment V_INT level (1.8 V) Driver strength: 2 mA	RSVD	Reserved	RSVD	Reserved	I2S vs Reserved
35	I2S_TXD / RSVD	I²S Data Output (G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Driver strength: 5 mA	I2S_TXD	I²S Data Output V_INT level (1.8 V) Driver strength: 2 mA	RSVD	Reserved	RSVD	Reserved	I2S vs Reserved
36	I2S_CLK / RSVD	I²S Clock (G340/G350) Reserved (G300/G310) V_INT level (1.8 V) Driver strength: 5 mA	I2S_CLK	I²S Clock V_INT level (1.8 V) Driver strength: 2 mA	RSVD	Reserved	RSVD	Reserved	I2S vs Reserved
37	I2S_RXD / RSVD	I²S Data Input (G340/G350) Reserved (G300/G310) V_INT level (1.8 V)	I2S_RXD	I²S Data Input V_INT level (1.8 V)	RSVD	Reserved	RSVD	Reserved	I2S vs Reserved
38	SIM_CLK	1.8V/3V SIM Clock Output	SIM_CLK	1.8V/3V SIM Clock Output	SIM_CLK	1.8V/3V SIM Clock Output	SIM_CLK	1.8V SIM Clock Output	
39	SIM_IO	1.8V/3V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8V/3V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8V/3V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8V SIM Data I/O Internal 4.7 k pull-up	
40	SIM_RST	1.8V/3V SIM Reset Output	SIM_RST	1.8V/3V SIM Reset Output	SIM_RST	1.8V/3V SIM Reset Output	SIM_RST	1.8V SIM Reset Output	
41	VSIM	1.8V/3V SIM Supply Output	VSIM	1.8V/3V SIM Supply Output	VSIM	1.8V/3V SIM Supply Output	VSIM	1.8V SIM Supply Output	
42	SIM_DET	SIM Detection Input V_INT level (1.8 V)	SIM_DET	SIM Detection Input V_INT level (1.8 V)	GPIO5	SIM Detection Input V_INT level (1.8 V)	RSVD	Reserved	SIM Detection vs Reserved
43	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
44	SPK_P / RSVD	Analog Audio Out (+) / Reserved	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	Analog Audio vs Reserved
45	SPK_N / RSVD	Analog Audio Out (-) / Reserved	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	Analog Audio vs Reserved
46	MIC_BIAS / RSVD	Microphone Supply Out / Reserved	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	Analog Audio vs Reserved
47	MIC_GND / RSVD	Microphone Ground / Reserved	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	Analog Audio vs Reserved
48	MIC_N / RSVD	Analog Audio In (-) / Reserved	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	Analog Audio vs Reserved
49	MIC_P / RSVD	Analog Audio In (+) / Reserved	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	Analog Audio vs Reserved
50	GND	Ground	GND	Ground	GND	Ground	GND	Ground	

	SARA-G3		SARA-U2		SARA-R4		SARA-N2		
No	**Pin Name**	**Description**	**Pin Name**	**Description**	**Pin Name**	**Description**	**Pin Name**	**Description**	**Remarks for migration**
51-53	VCC	Module Supply Input Normal op. range: 3.35 V – 4.5 V Extended op. range: 3.00 V – 4.5 V Current consumption: ~2.0A pulse current in 2G (recommended >100uF cap.) Switch-on by applying VCC	VCC	Module Supply Input Normal op. range: 3.3 V – 4.4 V Extended op. range: 3.1 V – 4.5 V Current consumption: ~2.0A pulse current in 2G (recommended >100uF cap.) Ferrite bead for GHz noise recommended for U201 Switch-on by applying VCC	VCC	Module Supply Input Normal op. range: 3.2 V – 4.2 V Extended op. range: 3.0 V – 4.3 V Current consumption: ~0.5A pulse current in LTE M1 (recommended 10uF cap.) No switch-on by applying VCC	VCC	Module Supply Input Normal op. range: 3.1 V – 4.0 V Extended op. range: 2.5 V – 4.2 V Current consumption: ~0.22A pulse current in NB-IoT (recommended 10uF cap.) Switch-on by applying VCC	Diverse voltage levels. Diverse current consumption. Diverse recommended external capacitors and other parts. Regular pF / nF recommended Diverse functions supported.
54-55	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
56	ANT	RF Antenna I/O	ANT	RF Antenna I/O	ANT	RF Antenna I/O	ANT	RF Antenna I/O	Diverse bands supported (summarized in Figure 34)
57-61	GND	Ground	GND	Ground	GND	Ground	GND	Ground	
62	ANT_DET / RSVD	Antenna Detection Input / Reserved	ANT_DET	Antenna Detection Input	ANT_DET	Antenna Detection Input	ANT_DET	Antenna Detection Input	Antenna Detection vs Reserved
63-96	GND	Ground	GND	Ground	GND	Ground	GND	Ground	

Table 25: SARA-G3, SARA-U2, SARA-R4 and SARA-N2 series modules pin assignment with remarks for migration

For further details regarding the characteristics, capabilities, usage or settings applicable for each interface of the SARA-G3, SARA-U2, SARA-R4 and SARA-N2 series cellular modules, see the related Data Sheet [6], [7], [10], [1], the related System Integration Manual [8], [11], the related AT Commands Manual [9], [12], [3] and the Nested Design Application Note [5].

B Glossary

3GPP	3rd Generation Partnership Project
AP	Application Processor
AT	AT Command Interpreter Software Subsystem, or attention
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
eDRX	Extended Discontinuous Reception
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
ESR	Equivalent Series Resistance
FEM	Front End Module
FOAT	Firmware Over AT commands
FW	Firmware
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
HF	Hands-free
HW	Hardware
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit interface
IP	Internet Protocol
LDO	Low-Dropout
LGA	Land Grid Array
LNA	Low Noise Amplifier
M2M	Machine-to-Machine
N/A	Not Applicable
N.A.	Not Available
NB-IoT	Narrow Band – Internet of Things
PA	Power Amplifier
PCM	Pulse Code Modulation
PCN	Sample Delivery Note / Information Note / Product Change Notification
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PWM	Pulse Width Modulation
RF	Radio Frequency
RI	Ring Indicator

RRC	Radio Resource Control
RTC	Real Time Clock
RTS	Request To Send
SAW	Surface Acoustic Wave
SIM	Subscriber Identification Module
TBD	To Be Defined
TP	Test-Point
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-link (Transmission)
VSWR	Voltage Standing Wave Ratio

Related documents

[1] u-blox SARA-N2 series Data Sheet, Docu No UBX-15025564
[2] u-blox Package Information Guide, Docu No UBX-14001652
[3] u-blox SARA-N2 series AT Commands Manual, Docu No UBX-16014887
[4] ITU-T Recommendation V.24 - 02-2000 - List of definitions for interchange circuits between the Data Terminal Equipment (DTE) and the Data Circuit-terminating Equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en
[5] u-blox Nested Design Application Note, Docu No UBX-16007243
[6] u-blox SARA-G3 series Data Sheet, Docu No UBX-13000993
[7] u-blox SARA-U2 series Data Sheet, Docu No UBX-13005287
[8] u-blox SARA-G3 / SARA-U2 series System Integration Manual Docu No UBX-13000995
[9] u-blox AT Commands Manual, Docu No UBX-13002752
[10] u-blox SARA-R4 series Data Sheet, u-blox Document UBX-16024152
[11] u-blox SARA-R4 series System Integration Manual, Docu No UBX-16029218
[12] u-blox SARA-R4 series AT Commands Manual, Docu No UBX-17003787

Some of the above documents can be downloaded from u-blox web-site (http://www.u-blox.com).

Revision history

Revision	Date	Name	Status / Comments
R01	06-Jun-2017	sfal / sses	Initial release

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