OV9665 Color CMOS SXGA CAMERACHIP™ Sensor Implementation Guide

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Revision Number	Date	Revision
1.0	10/11/07	Initial Release
1.1	05/02/08	Replaced Figure 9-4 on page 59.

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1 Introduction

This general application note is provided as a brief overview of the settings required for programming the OV9665 CAMERACHIP™ sensor. The Implementation Guide supplies the design engineer with quick-start tips for successful design solutions.

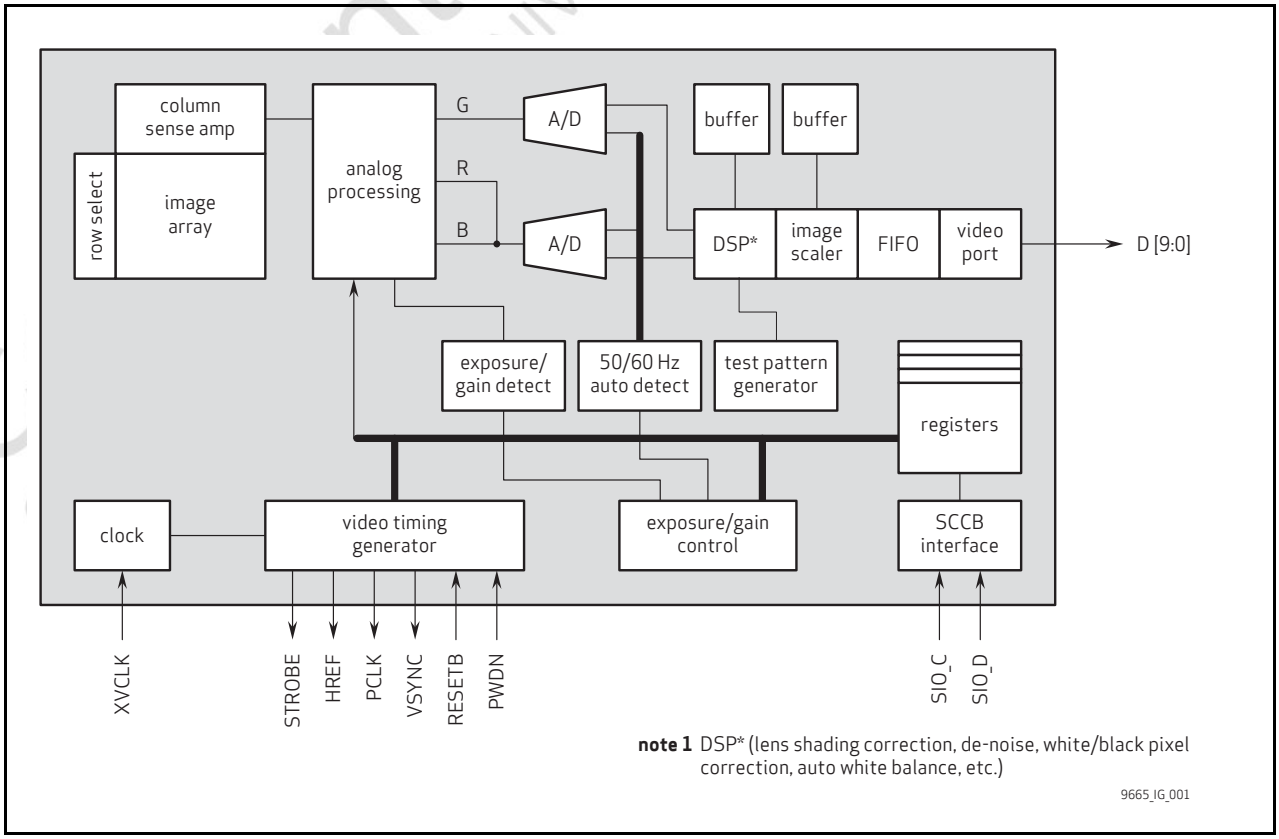
The *OV9665 Datasheet* provides complete information on the features, pin descriptions, and registers of the OV9665. The Implementation Guide is intended to complement the *OV9665 Datasheet* with considerations for PCB layout, register configurations, and timing parameters for rapid product design and deployment.

1.1 Function Description

Figure 1-1 shows the functional block diagram of the OV9665 image sensor. The OV9665 includes:

- Image Sensor Array (1304 x 1036 resolution)
- Analog Processing Block
- A/D Converters
- Digital Signal Processing
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 1-1 OV9665 Functional Block Diagram



2 Image Sensor Array

The OV9665 CAMERACHIP sensor has an active image array size of 1304 columns by 1036 rows (1,350,944 pixels).

The pixel cells themselves are identical but have RGB color filters arranged in a line-alternating BG/GR Bayer Pattern. The final YUV/YCbCr image uses this filter pattern to interpolate each pixel's BG or GR color from the light striking the cell directly, as well as from the light striking the surrounding cells. The 'Raw RGB' image does not have any image processing. RGB555/565/444 formats are converted from YUV/YCbCr.

Table 2-1 lists all OV9665 output formats.

Table 2-1. OV9665 Output Formats

Format	Output	Register	Address	Value
YUV/YCbCr	8 bits, 4:2:2 (Interpolated color)	REG63[5], REG85[4], REGD7[1:0], REGD8[1:0]	0x63, 0x85, 0xD7, 0xD8	0'b0, 0'b0, 0'b00, 0'bxx
RGB565	5-bit R, 6-bit G, 5-bit B	REG63[5], REG85[4], REGD7[1:0], REGD8[1:0]	0x63, 0x85, 0xD7, 0xD8	0'b0, 0'b0, 0'b01, 0'b01
RGB555	5-bit R, 5-bit G, 5-bit B	REG63[5], REG85[4], REGD7[1:0], REGD8[1:0]	0x63, 0x85, 0xD7, 0xD8	0'b0, 0'b0, 0'b01, 0'b10
RGB444	4-bit R, 4-bit G, 4-bit B	REG63[5], REG85[4], REGD7[1:0], REGD8[1:0]	0x63, 0x85, 0xD7, 0xD8	0'b0, 0'b0, 0'b01, 0'b11
Raw RGB	10/8 bits (Bayer filter color)	REG63[5], REG85[4], REGD7[1:0], REGD8[1:0]	0x63, 0x85, 0xD7, 0xD8	0'b1, 0'b0, 0'b11, 0'bxx
ISP Raw RGB	10/8 bits (after AWB and Gamma)	REG63[5], REG85[4], REGD7[1:0], REGD8[1:0]	0x63, 0x85, 0xD7, 0xD8	0'b1, 0'b1, 0'b10, 0'bxx

2.1 Resolution Formats

The OV9665 CAMERACHIP sensor supports SXGA (1280x1024), VGA (640x480), and any size scaled down.

Note: Contact your local OmniVision field applications engineer (FAE) for OV9665 Reference SCCB settings. Sensor power-on default values are not the best settings for image quality.

Table 2-2. Resolution Register Settings

Resolution	Register	Address	Value	Description (24 MHz Input Clock)
SXGA	CLKRC	0x11	0x80	15 fps SXGA YUV mode
	COM7	0x12	0x00	
	HREFST	0x17	0x0C[a]	
	HREFEND	0x18	0x5C[b]	
	VSTRT	0x19	0x01	
	VEND	0x1A	0x82	
	REG32	0x32	0x34	
VGA30	CLKRC	0x11	0x80	30 fps VGA YUV mode
	COM7	0x12	0x40	
	HREFST	0x17	0x0C[a]	
	HREFEND	0x18	0x5C[b]	
	VSTRT	0x19	0x02	
	VEND	0x1A	0x3F	
	REG32	0x32	0xB4	

a. 0x0D when register VER (0x0B) = 0x62 or 0x61

b. 0x5D when register VER (0x0B) = 0x62 or 0x61

For other sizes, refer to Section 6, Image Scaling on page 45 for more details.

3 Timing Generator

In general, the timing generator controls the following functions:

- Array Control and Frame Generation
- SXGA and VGA output
- Internal timing signal generation and distribution
- Frame Rate Timing
- Exposure Control
- External timing outputs (VSYNC, HREF, and PCLK)

3.1 Array Control and Frame Generation

3.1.1 Frame Generation (SXGA and VGA)

SXGA frame generation uses progressive scanning of the array in which rows are sequentially read and transferred out to the Analog Processing Block (APB). The 'Raw RGB' output preserves the Bayer Filter pattern so odd rows follow the BG pattern and even rows follow the GR pattern (GR). Simple sub-sampling mode just skips every other two rows and every other two columns for VGA mode. The OV9665 has built-in VarioPixel® technology to improve sub-sampled image resolution and reduce noise level.

3.2 Sync Signal Selection

The OV9665 CAMERACHIP sensor supplies two output sync signals: VSYNC and HREF. The vertical sync (VSYNC) signal is output on pin E5. The horizontal reference signal (HREF) is output on pin F5.

The HREF signal is valid only when there is output data. If there is no output data, the HREF signal will remain at either high or low, depending on the polarity selection. The VSYNC/HREF/PCLK polarity selection is controlled by register COM10[1] (0x15), REGD8[5] (0xD8), COM10[4] (0x15), respectively. Usually, an application uses the rising edge of PCLK to capture data when HREF is high.

The OV9665 can encode horizontal and vertical sync information into data. Set register REGD8[3] (0xD8) high to enable the CCIR656 format.

Refer to the *OV9665 Datasheet* for detailed signal timing information.

3.3 Frame Rate Timing

The OV9665 offers three methods of frame rate adjustment:

- Clock Prescalar
- Dummy Pixel Adjustment (Output Formatter)
- Dummy Line Adjustment

3.3.1 Clock Prescalar

The OV9665 uses an internal PLL to multiply the input clock (XVCLK) first and then uses a divider to get the required internal clock. The PLL control registers are register REG3D (0x3D) and CLKRC (0x11).

Register CLKRC (0x11) is the internal clock scalar. By programming register CLKRC[5:0], the frame rate and pixel rate can be divided by 2, 3, 4, ..., 64.

PCLK output clock is calculated as follows:

$$PCLK = \frac{XCLK \times (64 - REG3D[5:0])}{2 \times (CLKRC[5:0] + 1)} \quad \text{(SXGA YUV mode)}$$

$$PCLK = \frac{XCLK \times (64 - REG3D[5:0])}{4 \times (CLKRC[5:0] + 1)} \quad \text{(VGA YUV mode)}$$

If no image scaling is involved (output size is the same as the sensor array output), the output pixel clock (PCLK) will be divided by 2 for sensor raw mode. If image scaling is involved, the output pixel clock can be lower. For more details of PCLK calculation, refer to Section 6, Image Scaling on page 45.

Table 3-1 shows the maximum frame rate and pixel clock (PCLK) for the given input clock rate (XVCLK). The RGB raw pixel clock rate is half of YUV mode for the same frame rate and resolution.

Table 3-1. Frame Rate, Pixel Clock Rate, and Input Clock Rate

Resolution/Mode	Max Frame Rate (fps)	XVCLK (MHz)	Register CLKRC (0x11)	PLL (0x3D)	PCLK Output (MHz)
SXGA/YUV	15	24	0x80	0x3C	48
SXGA/YUV	7.6	24	0x81	0x3C	24
VGA30/YUV	30.4	24	0x80	0x3C	24
VGA30/YUV	10.1	24	0x82	0x3C	8
NOTE: Lower resolutions using Image Scaling do not support RGB raw mode					

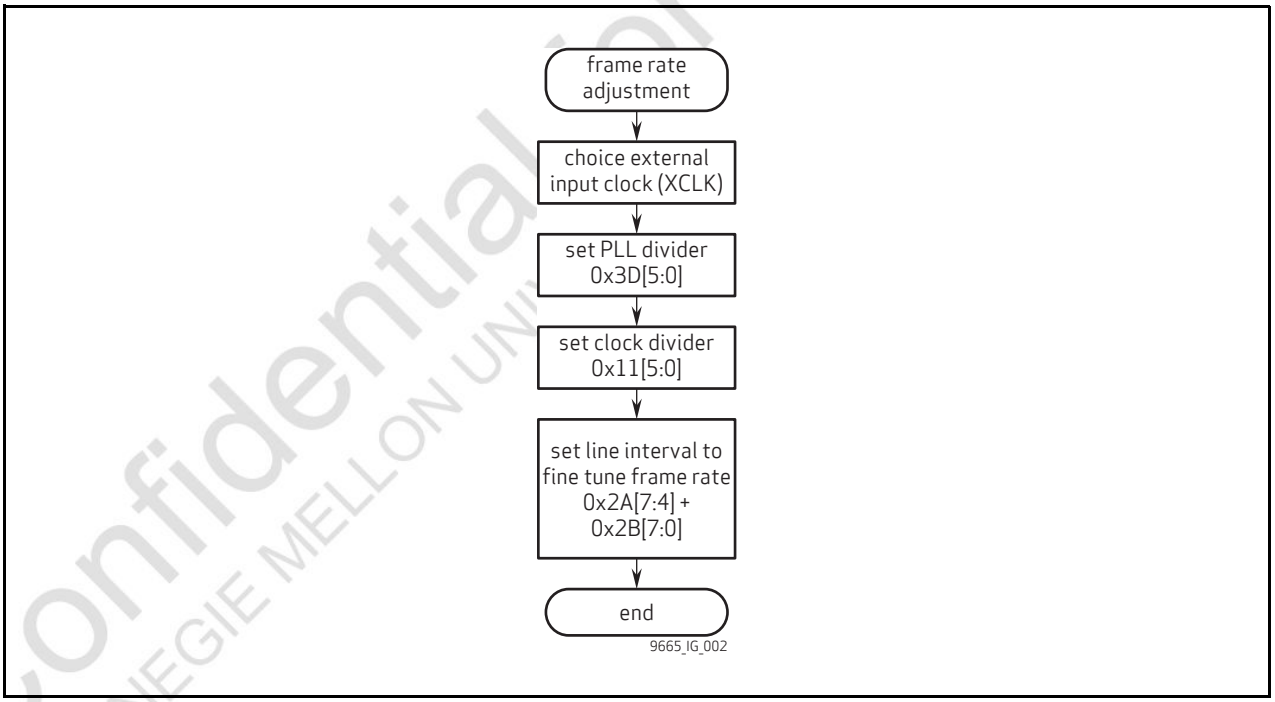
3.3.2 Dummy Line Adjustment

By inserting dummy lines in each row's output, the frame rate can be changed while leaving the pixel rate unchanged. The user can set registers ADDVSL (0x2D) and ADDVSH (0x2E) to adjust the VSYNC pulse signal in order to change the frame rate. The frame rate is calculated as follows:

$$\text{FPS (SXGA YUV)} = \frac{(\text{XCLK}) \times (64 - \text{REG3D}[5:0])}{1052 \times 4 \times (\text{CLKRC}[5:0] + 1) \times (1520 + \text{REG2A}[7:4] \times 256 + \text{REG2B}[7:0])}$$

$$\text{FPS (VGA YUV)} = \frac{(\text{XCLK}) \times (64 - \text{REG3D}[5:0])}{526 \times 4 \times (\text{CLKRC}[5:0] + 1) \times (1520 + \text{REG2A}[7:4] \times 256 + \text{REG2B}[7:0])}$$

Figure 3-1 Frame Rate Adjustment Flow



3.3.2.1 SXGA Example

External input clock = 24 MHz
REG3D[5:0] = PLL divider = 0x3C = 60
CLKRC[5:0] = Clock divider = 0x02 = 2
REG2A[7:0] = Line interval adjustment MSB = 0x01 = 1
REG2B[7:0] = Line interval adjustment LSB = 0x7D = 125
FPS ~= 4

3.3.2.2 VGA Example

External input clock = 24 MHz
REG3D[5:0] = PLL divider = 0x3C = 60
CLKRC[5:0] = Clock divider = 0x02 = 2
ADDVSH[7:0] = Line interval adjustment MSB = 0x04 = 4
ADDVSL[7:0] = Line interval adjustment LSB = 0x75 = 117
FPS ~= 4

3.3.3 Dummy Pixel Adjustment (Output Formatter)

By inserting dummy pixels in each frame output, the frame rate can be changed while leaving the pixel rate unchanged (see Section 7.2.2, Frame Rate Adjust).

3.4 Exposure Control

The OV9665 CAMERACHIP sensor supports both automatic and manual exposure control modes. The exposure time is defined as the interval from the cell precharge to the end of the photo-induced current measurement and can be controlled manually or by using the AEC function. This exposure control uses a 'rolling' shutter as exposure time is set on a row-by-row basis rather than on a frame-by-frame basis.

Exposure Time interval is defined as follows:

$t_{EXPOSURE} = 1520 \times (t_{INT\ CLK} \times 2) \times AEC[15:0]$ for 15fps SXGA in YUV/RGB mode

$t_{EXPOSURE} = 1520 \times (t_{INT\ CLK}) \times AEC[15:0]$ for 15fps SXGA in RAW mode

where AEC[15:0] is defined as:

AEC[15:0] = {MSB, LSB} = {REG45[5:0], AEC[7:0], REG04[1:0]}

Each bit in AEC[15:0] = $t_{ROW\ INTERVAL} = 2 \times (1520 \times t_{INT\ CLK})$ for YUV/RGB mode

Note that both the AEC and AGC functions are interactive, so registers and functions may be common to both. Also, in general, the AEC is the primary control and will be adjusted before the AGC (the AGC acts to adjust and center the AEC).

The OV9665 supports two types of automatic exposure algorithms, Histogram-based AEC and Average-based AEC. The algorithm used for Histogram-based AEC is based on image histogram distribution and probability. The algorithm used for Average-based AEC is based on luminance of the full image with weighting in night regions. The exposure is optimized for a "normal" scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the AEC white/black ratio may be adjusted to suit the needs of the application.

3.4.1 Manual Exposure Control Mode

The manual exposure control mode allows for the companion backend processor to control the OV9665 image exposure. The companion backend processor may write exposure values to CAMERACHIP sensor registers REG45[5:0] (0x45) (MSB), AEC[7:0] (0x10), and REG04[1:0] (0x04) (LSB) according to its corresponding Auto-Exposure Control (AEC) algorithm.

The minimum allowable exposure value is 1 line. Exposure modes of less than 1 line may be used in special cases. The LSB signifies the 1 line exposure time. The exposure value data is 16 bits in length.

3.4.2 Automatic Exposure Control Mode (AEC)

The AEC function allows for the CAMERACHIP sensor to adjust the exposure without external command or control. Registers REG45[5:0] (0x45), AEC[7:0] (0x10), and REG04[1:0] (0x04) are adjusted by the CAMERACHIP sensor's internal controls and cannot be overwritten by an external device in Automatic Exposure Control mode.

Also, the OV9665 provides two different AEC algorithms, Histogram-based and Average-based.

3.4.2.1 Auto-Exposure Control Enable Bit

The Automatic Exposure Control enable bit is in register COM8[0] (0x13) as shown in Table 3-2.

Table 3-2. AEC Enable Register

Function	Register	Address	Description
Automatic Exposure Control Enable	COM8[0]	0x13	0: Disable 1: Enable

3.4.2.2 AEC Algorithm Selection

The OV9665 has two different built-in AEC algorithms, Histogram-based and Average-based. The user can select either algorithm based on their particular application.

Table 3-3. AEC Enable Register

Function	Register	Address	Value
Average-based AEC/GC selection	REG7C[7]	0x7C	0'b0
Histogram-based AEC/GC selection	REG7C[7]	0x7C	0'b1

3.4.2.3 Average-based AEC

The Average-based AEC controls image luminance using registers AEW (0x24) and AEB (0x25). The value of register AEW (0x24) indicates the high threshold value and the value of register AEB (0x25) indicates the low threshold value. When the target image luminance average value (YAVG) is within the range specified by registers AEW (0x24) and AEB (0x25), the AEC keeps the image exposure. When YAVG is greater than the value in register AEW (0x24), the AEC will decrease the image exposure. When YAVG is less than the value in register AEB (0x25), the AEC will increase the image exposure. Accordingly, the value in register AEW (0x24) should be greater than the value in register AEB (0x25). The gap between the values of registers AEW (0x24) and AEB (0x25) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers AEW (0x24) and AEB (0x25). AEC set to normal mode will allow for single-step increase or decrease in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increase or decrease in the image exposure to maintain the specified range. A value of "0" in register COM8[7] (0x13) will result in normal speed operation and a "1" will result in fast speed operation.

Register VV (0x26) controls the fast AEC range. If the target image YAVG is greater than VV[7:4] × 16, AEC will decrease by 2. If YAVG is less than VV[3:0] × 16, AEC will increase by 2.

Table 3-4 lists the registers used for setting AEC convergence limits when the average-based AEC is used.

Table 3-4. AEC Convergence Limits for Average-based AEC

Function	Register	Address
Control Zone – Upper Limit high nibble	VV[7:4]	0x26
Control Zone – Lower Limit high nibble	VV[3:0]	0x26
Stable Operating Region – Upper Limit	AEW[7:0]	0x24
Stable Operating Region – Lower Limit	AEB[7:0]	0x25

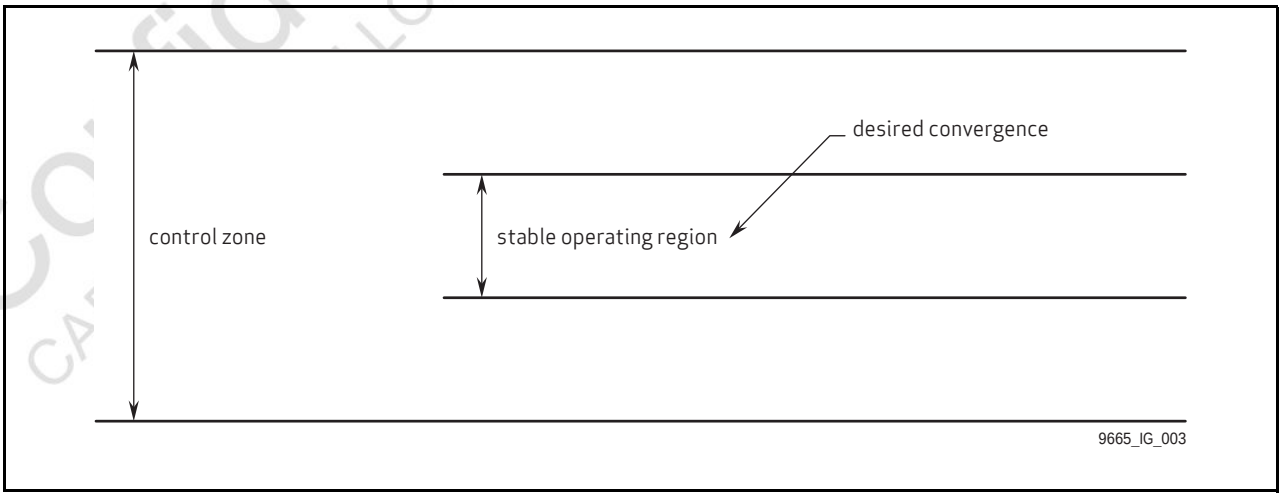
As shown in Figure 3-2, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size change as follows:

- Outside Control Zone
  Step Size: 2 × (AEC[9:0])
  t_{STEP}: t_{ROW} x (2 x AEC[9:0])
- Inside Control Zone
  Step Size: 2 x (AEC[9:0]) ÷ 16)
  t_{STEP}: t_{ROW} x (2 x AEC[9:0] ÷ 16)

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

The Step Limit register acts to create a "middle ground" by limiting the maximum step size to 32 rows (delay time = t_{ROW} x 32).

Figure 3-2 Desired Convergence



Control Zone Upper Limit: {VV[7:4] (0x26), 4'b0000}
Control Zone Lower Limit: {VV[3:0] (0x26), 4'b0000}
Stable Operating Region Upper Limit: AEW[7:0] (0x24)
Stable Operating Region Lower Limit: AEB[7:0] (0x25)

For average-based AEC/AGC algorithm only, the whole image is divided by nine (3x3) zones (see Figure 3-3). Each zone (or block) is 1/9th of the image and has a 2-bit weight in calculating the average luminance (YAVG). The 2-bit weight could be 0(0), 1(1/4), 2(1/2), or 3(1). The final YAVG is the weighted average of the nine zones (see registers REG5D[7:0] (0x5D), REG5E[7:0] (0x5E), and REG5F[1:0] (0x5F)).

Figure 3-3 9-Zone Based Reference Area

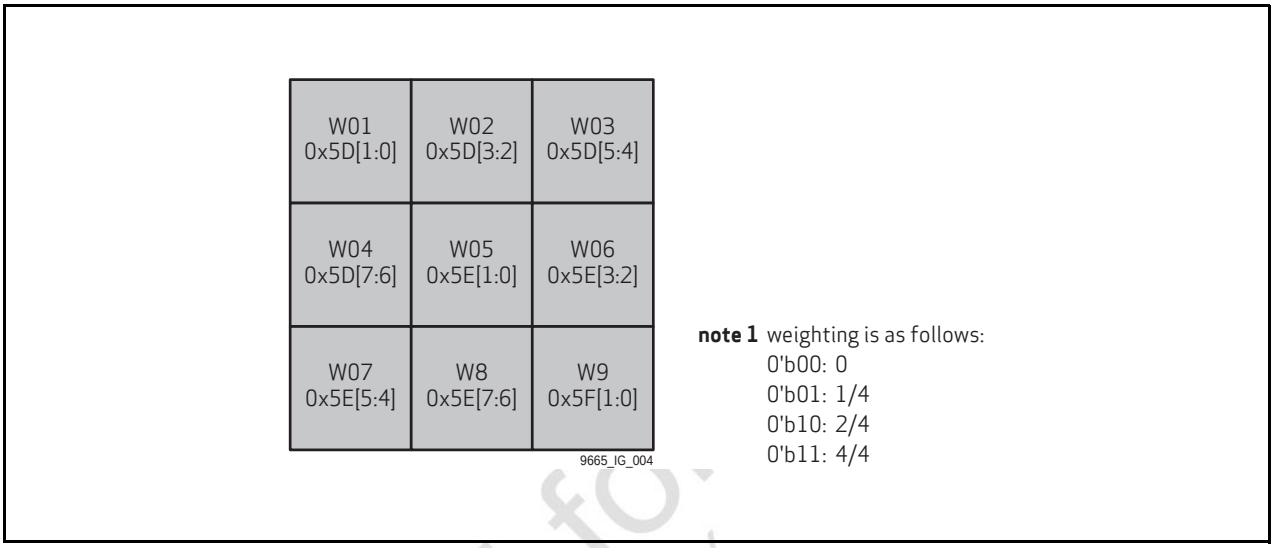


Table 3-5. 9-Zone AEC/AGC Windowing Registers

Function	Register	Address	Description
AEC Windowing Option	REG5C[7]	0x5C	0: 9-zone weighting 1: Full frame
Window01 9-Zone Weighting Option	REG5D[1:0]	0x5D	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4
Window02 9-Zone Weighting Option	REG5D[3:2]	0x5D	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4
Window03 9-Zone Weighting Option	REG5D[5:4]	0x5D	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4
Window04 9-Zone Weighting Option	REG5D[7:6]	0x5D	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4

Table 3-5. 9-Zone AEC/AGC Windowing Registers (Continued)

Function	Register	Address	Description
Window05 9-Zone Weighting Option	REG5E[1:0]	0x5E	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4
Window06 9-Zone Weighting Option	REG5E[3:2]	0x5E	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4
Window07 9-Zone Weighting Option	REG5E[5:4]	0x5E	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4
Window08 9-Zone Weighting Option	REG5E[7:6]	0x5E	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4
Window09 9-Zone Weighting Option	REG5F[1:0]	0x5F	00: Weighting = 0 01: Weighting = 1/4 10: Weighting = 2/4 11: Weighting = 4/4

3.4.2.4 Histogram-based AEC

The OV9665 histogram-based AEC controls exposure levels based on image histogram distribution and probability.

Table 3-6 lists the registers used for histogram-based AEC.

Table 3-6. Histogram-based AEC Registers

Function	Register	Address
LRL – Low Reference Luminance	HISTO_LOW[7:0]	0x61
HRL – High Reference Luminance	HISTO_HIGH[7:0]	0x62
LPH – Lower Limit of Probability for HRL, after exposure/gain stabilizes	REG75[7:0]	0x75
UPL – Upper Limit of Probability for LRL, after exposure/gain stabilizes	REG76[7:0]	0x76
TPL – Probability Threshold for LRL to control AEC/AGC speed	REG77[7:0]	0x77
TPH – Probability Threshold for HRL to control AEC/AGC speed	REG78[7:0]	0x78
TLH – High nibble of Luminance Threshold for AEC/AGC speed control	REG79[7:4]	0x79
TLL – Low nibble of Luminance Threshold for AEC/AGC speed control	REG79[3:0]	0x79

Refer to Figure 3-4 for each control illumination based on cumulative density function.

Figure 3-4 Histogram-Based AEC Control

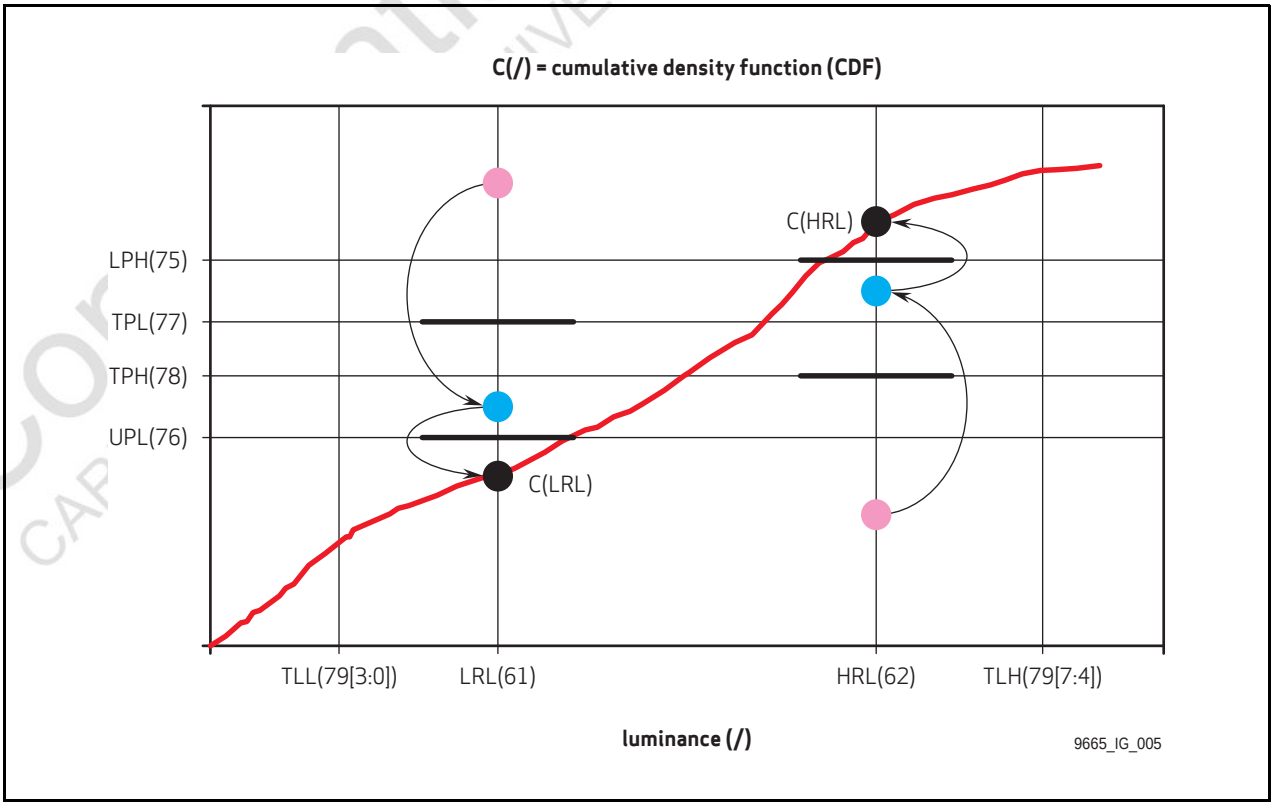


Table 3-7 lists all the registers that control the Histogram-based AEC adjustments.

Table 3-7. Histogram-based AEC Algorithm Adjustment Controls

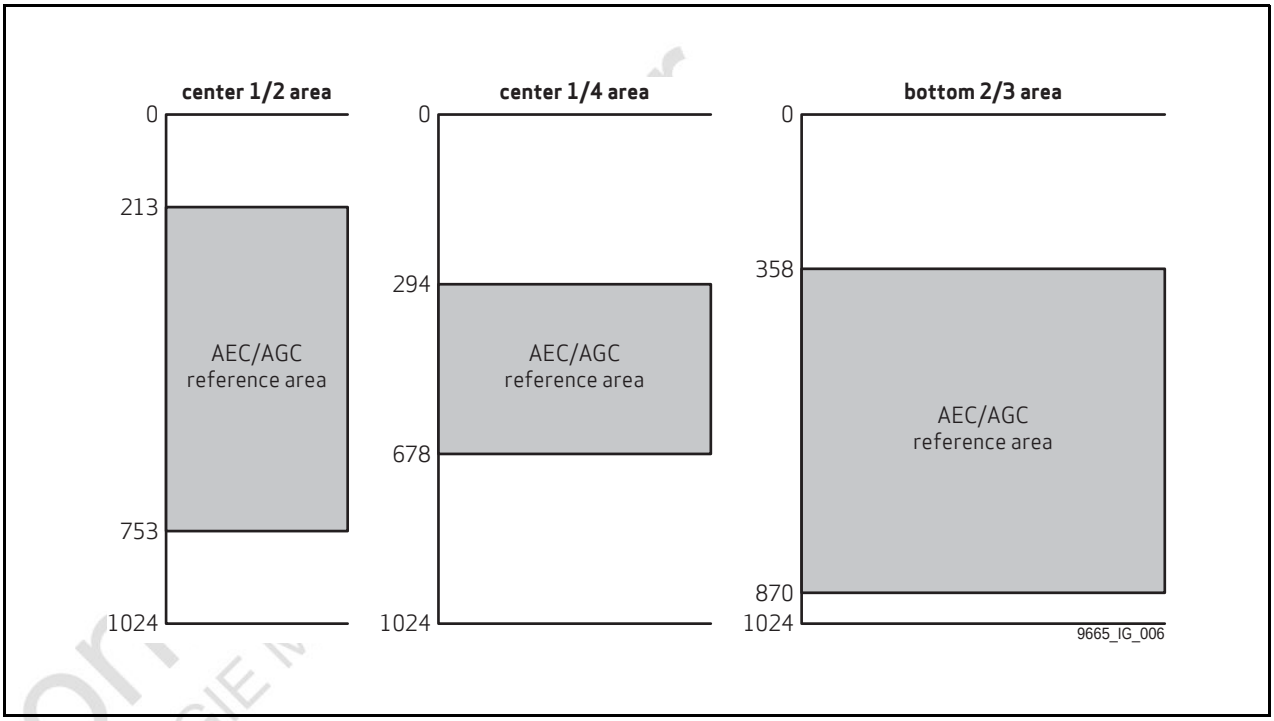
Control	Selection	Registers
Luminance Saturation Control	More saturated	Decrease both LPH (0x75) and UPL (0x76) values
	Less saturated	Increase both LPH (0x75) and UPL (0x76) values
Image Brightness Control	Brighter image	Increase both LRL (0x61) and HRL (0x62) values
	Darker image	Decrease both LRL (0x61) and HRL (0x62) values
AEC Speed Controlled by TLH and TLL	Higher speed	Decrease TLH (0x79[7:4]) but not less than target image luminance and increase TLL (0x79[3:0]) but not larger than target luminance. TLH (0x79[7:4]) should be larger than 1.2 × target image luminance and TLL (0x79[3:0]) should be less than 0.8 × target image luminance.
	Lower speed	Increase TLH (0x79[7:4]) and decrease TLL (0x79[3:0])
AEC Speed Controlled by TPL and TPH	Higher speed	Decrease TPL (0x77) but not less than UPL (0x76) and increase TPH (0x78) but not bigger than LPH (0x75)
	Lower speed	Increase REG77 (0x77) and decrease REG78 (0x78)
AEC Flickering versus LRL and HRL	HRL (0x62) should be larger than LRL (0x61) In order to prevent flickering, the recommended relationship between these two values should be: HRL ≥ 1.07 x LRL	
AEC Flickering versus LPH and UPL	LPH should be larger than UPL If the difference (LPH – UPL) is large, AEC flickering can occur. The recommended relationship between these two values is shown below: LPH ≤ 1.07 x UPL	

The user can choose the area of the image that will be used by the AEC/AGC algorithm. Table 3-8 lists the options.

Table 3-8. AEC/AGC Reference Area Option

Function	Register	Address	Description
AEC Windowing Option	REG5C[7]	0x5C	0: 9-zone weighting 1: Full frame
Full Image Area	REG5B[1:0]	0x5B	0'b00
Center 1/2 Area	REG5B[1:0]	0x5B	0'b01
Center 1/4 Area	REG5B[1:0]	0x5B	0'b10
Bottom 2/3 Area	REG5B[1:0]	0x5B	0'b11

Figure 3-5 AEC/AGC Reference Areas



3.5 Banding Filter

The OV9665 supports a rolling shutter exposure mode and requires special exposure values when used in 50/60 Hz lighting conditions to eliminate rolling horizontal banding (flicker). The minimum exposure value is 1/120 second for 60 Hz and 1/100 second for 50 Hz lighting conditions. It supports both manual adjust exposure mode and auto adjust exposure mode. Register COM8[5] (0x13) is the control bit where 0 is for manual mode and 1 is for auto mode.

3.5.1 Rolling Horizontal Band Elimination in Manual Mode

The following steps outline how to calculate the proper exposure value under 50/60 Hz lighting conditions:

1. Calculate the CAMERACHIP Minimum Exposure Line (MEL):
   Line period is $T_{line} = K \times T_{pclk} = K/f_{pclk}$, while K is PCLK number in one line, T_{pclk} is PCLK period (sec) and f_{pclk} is PCLK frequency (Hz). $T_{pclk} = 1/f_{pclk}$. For example, for default 1280 x 1024 at 7.5 fps, K is 1520 x 2 in YUV mode and 1520 in RGB Raw Data mode. But YUV PCLK frequency is double that of RGB Raw Data mode with same T_{line}.
   For 60 Hz lighting: $MEL = (1/120)/T_{line} = 1/(120 \times K \times T_{pclk}) = f_{pclk}/(120 \times K)$
   For 50 Hz lighting: $MEL = (1/100)/T_{line} = 1/(100 \times K \times T_{pclk}) = f_{pclk}/(100 \times K)$
2. Set the CAMERACHIP Available Exposure Line (AEL):
   Suppose N is an integer, N = 1,2,3…
   Available exposure lines are: AEL = N × MEL where AEL should be equal to or less than the maximum exposure line limitation based on different resolutions.
3. Convert AEL to binary, and then send 2 LSBs hex number to register REG04[1:0] (0x04) and 8-bit hex number to register AEC[7:0] (0x10) and 6 MSBs to register REG45[5:0] (0x45).

3.5.1.1 Maximum Exposure Line Limitation

OV9665 maximum exposure line values are:

- SXGA - 1051 lines
  Register setting: {REG45[5:0] (0xA1) = 0x01, AEC[7:0] (0x10) = 0x06, REG04[1:0] (0x04) = 0x03}
- VGA - 525 lines
  Register setting: {REG45[5:0] (0xA1) = 0x00, AEC[7:0] (0x10) = 0x83, REG04[1:0] (0x04) = 0x01}

3.5.1.2 Rolling Horizontal Band Elimination in Auto Mode

The OV9665 also provides a rolling horizontal band eliminate function in auto exposure mode. A banding filter is employed to filter out banding caused by 50/60 Hz lighting. To enable this function, set register COM8[5] (0x13) to 1.

When the banding filter is enabled, the AEC will set the exposure time to a set of discrete values, among which the minimum value is called the Banding Filter Value. OV9665 has two options to set the Banding Filter Value. The first option is the manual banding filter mode, which is enabled by setting register COM3[1] (0x0C) to 0. In manual banding filter mode, the Banding Filter Value is specified by register COM3[2] (0x0C). If this bit is 1, the sensor will use the register BD50[7:0] (0x4F) value as the Banding Filter value and if COM3[2] (0x0C) is 0, the sensor will use the register BD60[7:0] (0x50) value as the Banding Filter value. The companion backend processor can set

register BD50[7:0] (0x4F) and register BD60[7:0] (0x50) for 50 and 60 Hz, respectively, and then toggle register COM3[2] (0x0C) to switch between 50 Hz and 60 Hz lighting frequency.

The second option is the auto banding mode, which is enabled by setting register COM3[1] (0x0C) to 1. In auto banding mode, the sensor automatically detects 50/60hz light conditions and automatically changes the minimum banding exposure time, which is defined in registers BD50 (0x4F) and BD60 (0x50).

If the light is too strong, the minimum exposure time (Banding Filter Value) to eliminate banding may result in an over-exposed image. To avoid over-exposure, the OV9665 has an option to allow the real exposure time to be less than the Banding Filter Value. Setting register COM9[3] (0x14) enables this option.

Table 3-9 lists all banding filter related registers.

Table 3-9. Banding Filter Registers

Function	Register	Address	Description
Banding Filter Enable	COM8[5]	0x13	0: Disable 1: Enable
Banding Filter Value Selection	COM3[2]	0x0C	0: Use register BD60 (0x50) value as minimum banding exposure time 1: Use register BD50 (0x4F) value as minimum banding exposure time
50 Hz Banding Maximum AEC Step	REG5A[7:4]	0x5A	Maximum AEC banding step for 50 Hz
60 Hz Banding Maximum AEC Step	REG5A[3:0]	0x5A	Maximum AEC banding step for 60 Hz
Auto Banding Filter Value (50 Hz)	COM25[7:6], BD50[7:0]	0x4E, 0x4F	Minimum banding exposure time for 50 Hz light in automatic 50/60 Hz detection mode or manual/external 50/60 Hz selection by register COM3[2] (0x0C)
Auto Banding Filter Value (60 Hz)	COM25[5:4], BD60[7:0]	0x4E, 0x50	Minimum banding exposure time for 60 Hz light in automatic 50/60 Hz detection mode or manual/external 50/60 Hz selection by register COM3[0] (0x0C)
Minimum Exposure Limitation Option	COM9[3]	0x14	In the case of very strong lighting conditions: 0: Exposure time will not be less than Banding Filter Value 1: Exposure time can be less than Banding Filter Value
Auto Banding Filter Enable	COM3[1]	0x0C	0: Disable 1: Enable Sensor automatically detects 50/60hz light condition. Select minimum banding exposure time (0x4F and 0x50) automatically.

3.5.1.3 Banding Filter Value Calculation

The Banding Filter Value depends on the lighting frequency, frame rate, and maximum exposure. The equations are shown below. Frame rate can be derived from Table 3-1. Refer to section "Maximum Exposure Line Limitation" on page 22 for the maximum exposure.

$$\text{Banding Filter Value} = \frac{\text{Frame Rate x Maximum Exposure Line}}{120} \quad \text{for 60 Hz}$$

$$\text{Banding Filter Value} = \frac{\text{Frame Rate x Maximum Exposure Line}}{100} \quad \text{for 50 Hz}$$

Note:

1. If the frame rate is adjusted by inserting dummy lines, the Maximum Exposure Line is equal to the original value plus the number of dummy lines. Consequently, the Banding Filter Value does not change with the number of dummy lines.
2. If the frame rate is adjusted by inserting dummy pixels, the Maximum Exposure Line does not change. Consequently, the Banding Filter Value will change with the number of dummy pixels. In the case where the OV9665 works at a system clock frequency other than 24 MHz or 48 MHz, it is very convenient to adjust the frame rate by adding some dummy pixels (setting register REG2A (0x2A) and REG2B (0x2B)) while keeping the Banding Filter Value the same with that using a 24 MHz or 48MHz system clock.

Table 3-10 shows the Banding Filter Values for 50 Hz and 60 Hz light frequency conditions. Contact your local OmniVision FAE to get the appropriate settings for your application.

Table 3-10. Banding Filter Value (Input Clock Frequency = 24 MHz and 4x PLL)

Resolution	Clock Pre-Scalar (CLKRC (0x11))	Format	Frame Rate (fps)	Banding Filter Value	
				50 Hz (BD50 (0x4F))	60 Hz (BD60 (0x50))
SXGA	0x00	YUV/RAW	15	0x9D	0x83
VGA and lower resolutions	0x00	YUV/RAW	15	0x4B	0x3E

3.5.2 Automatic 50/60 Hz Banding Detection

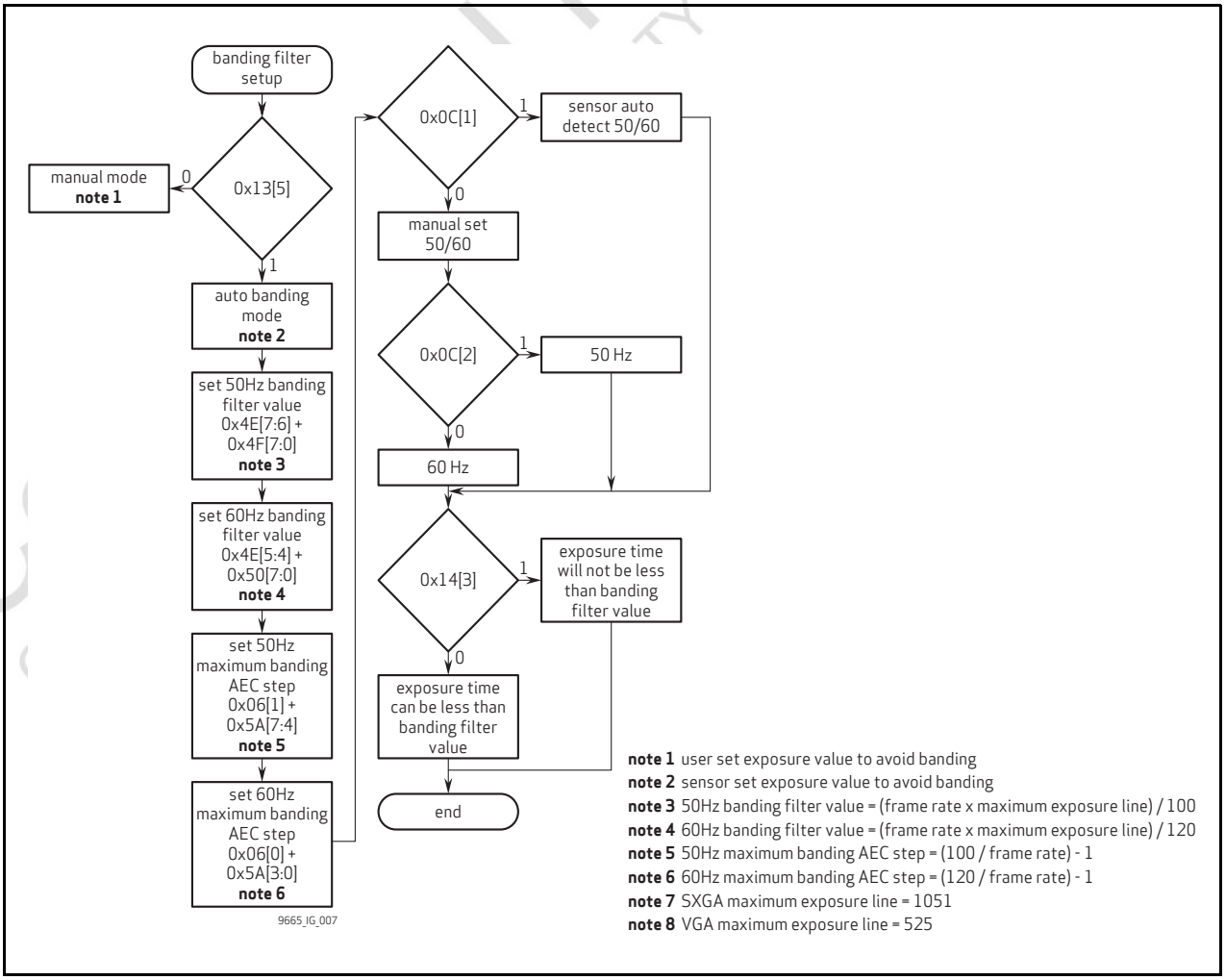
The OV9665 CAMERACHIP sensor supports the automatic 50/60 Hz banding detection function. The OV9665 detects the light frequency from the input image and automatically adjusts the minimum banding exposure time.

Table 3-11. Automatic 50/60 Hz Banding Detection Registers

Function	Register	Address	Description
Banding Filter Enable	COM8[5]	0x13	0: Disable 1: Enable
Auto Banding Filter Enable	COM3[1]	0x0C	0: Disable 1: Enable
Auto Banding Filter Value (50 Hz)	BD50[7:0]	0x4F	Minimum banding exposure time for 50 Hz light in automatic 50/60 Hz detection mode
Auto Banding Filter Value (60 Hz)	BD60[7:0]	0x50	Minimum banding exposure time for 60 Hz light in automatic 50/60 Hz detection mode

Contact your local OmniVision FAE for automatic 50/60 Hz banding detection settings.

Figure 3-6 Automatic Banding Detection



3.6 Strobe Flash Control

To achieve the best image quality possible in low light conditions, the use of a strobe flash is recommended. The OV9665 provides a programmable strobe signal function.

3.6.1 Sensor Controlled

The OV9665 can generate a programmable strobe signal from the Strobe pin (pin D4). Table 3-12 lists the strobe pulse control registers.

Table 3-12. Strobe Pulse Control Registers

Function	Register	Address	Description
Strobe Function Enable	COM22[7]	0x4B	1: Start strobe enable
Strobe Output Pulse Polarity Control	COM22[6]	0x4B	0: Positive pulse 1: Negative pulse
Xenon Mode Strobe Pulse Width	COM22[3:2]	0x4B	00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines
Strobe Mode	COM22[1:0]	0x4B	00: Xenon mode 01: LED 1&2 mode 10: LED 1&2 mode 11: LED 3 mode
Strobe Pad Output Selection (pin D0 output control)	COM2[3]	0x09	0: D0 1: Strobe

3.6.1.1 Strobe Pulse

The strobe signal is programmable. It supports both LED and Xenon mode. The polarity of the pulse can be changed. The strobe signal is enabled (turned high / low depending on the pulse's polarity) by requesting the signal via the SCCB. Flash modules are typically triggered to the rising edge (falling edge, if signal polarity is changed). It supports the flashlight modes shown in Table 3-13.

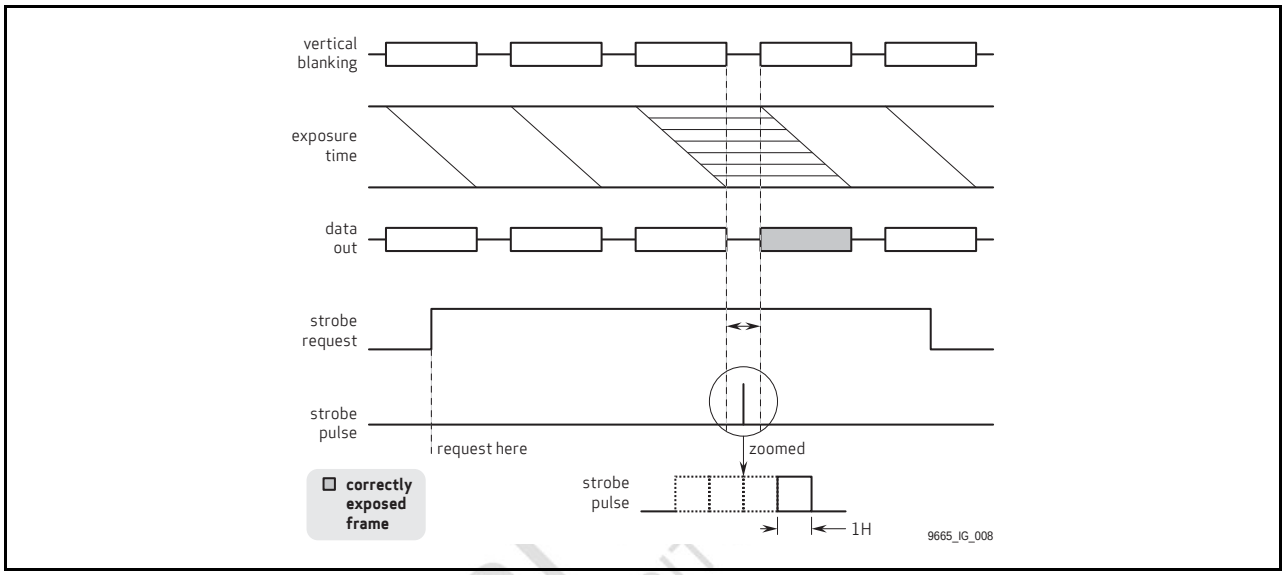
Table 3-13. Flashlight Modes

Mode	Output	AEC/AGC	AWB
Xenon	One pulse	No	No
LED 1	Pulse	No	No
LED 2	Pulse	No	Yes
LED 3	Continuous	Yes	Yes

3.6.1.2 Xenon Flash Control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see Figure 3-7). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, where H is one horizontal period ([1 / fps] x [1 / number of total lines] sec).

Figure 3-7 Xenon Flash Mode



3.6.1.3 LED 1&2 Mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see Figure 3-8). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see Figure 3-9). The number of skipped frames is programmable.

Figure 3-8 LED 1&2 Mode – One Pulse Output

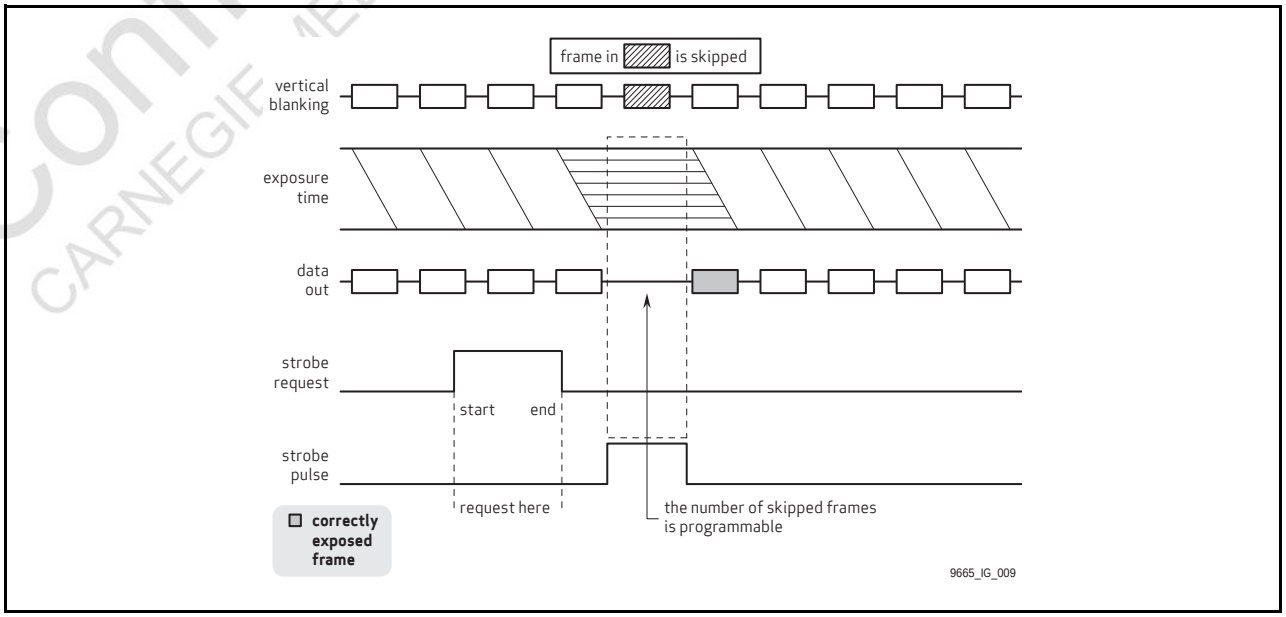
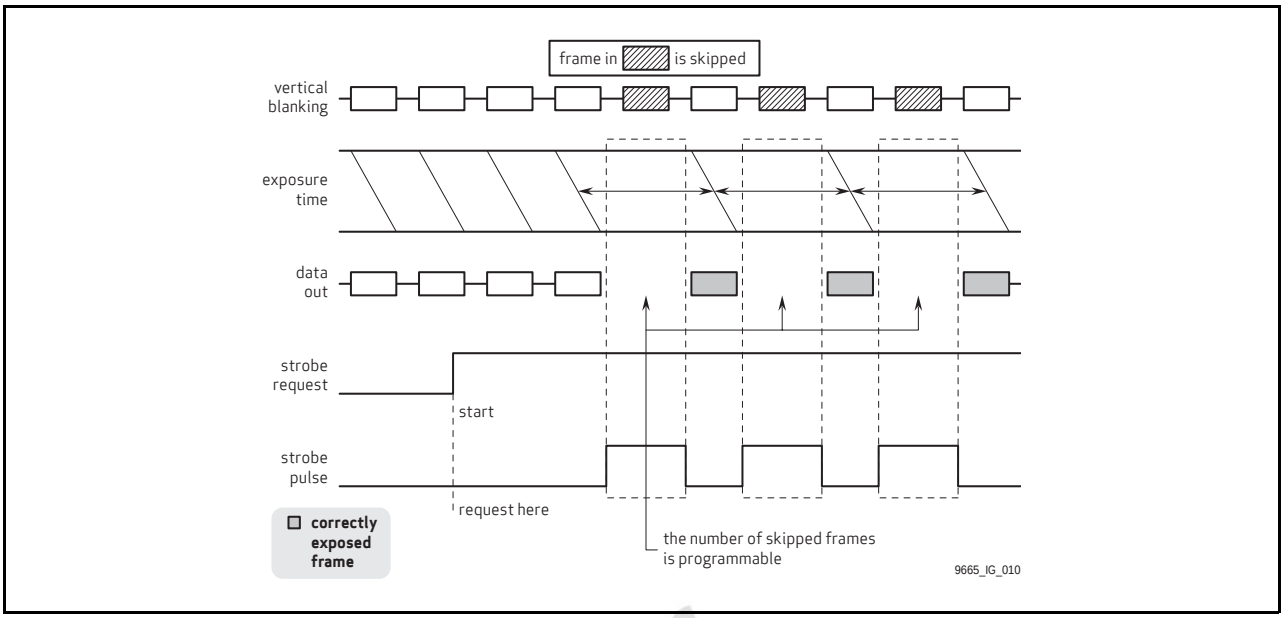


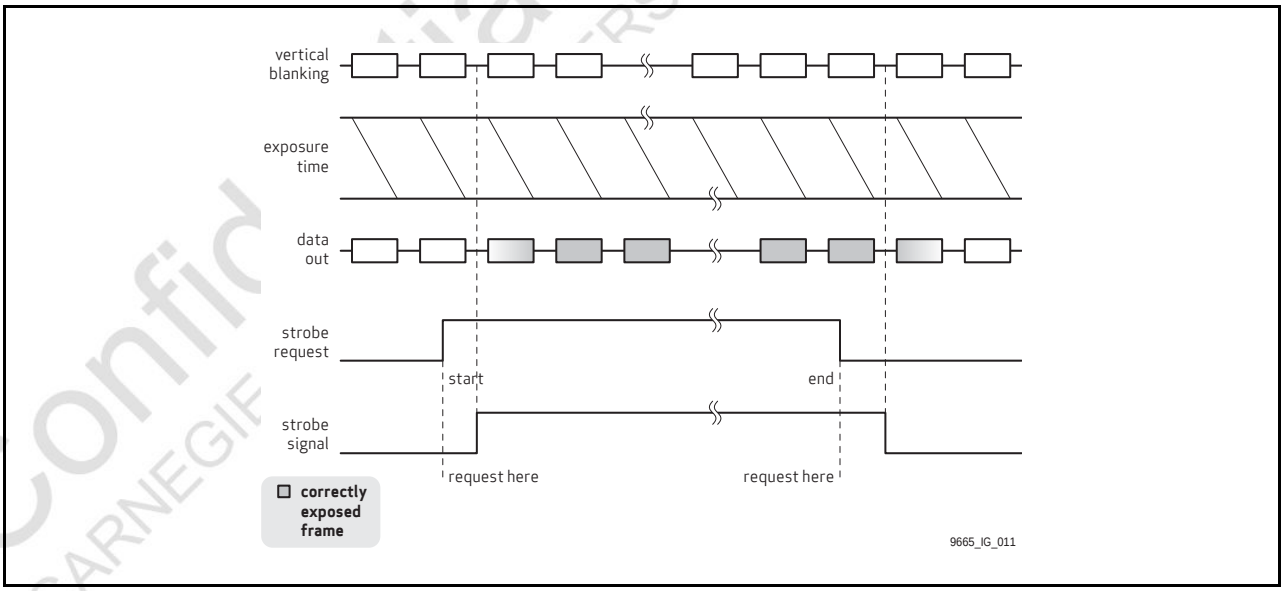
Figure 3-9 LED 1&2 Mode – Multiple Pulse Output



3.6.1.4 LED 3 Mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see Figure 3-9).

Figure 3-10 LED 3 Mode



3.6.2 External Processor Controlled

In the case where Strobe Flash is controlled by an external processor to avoid the need for a mechanical shutter, the OV9665 should be set to rolling shutter mode. When rolling shutter mode is enabled and the image requires strobe flash illumination, the strobe timing must be limited. Timing diagrams for strobe flash timing are shown in Figure 3-11 and Figure 3-12.

Figure 3-11 SXGA Strobe Flash Timing Diagram

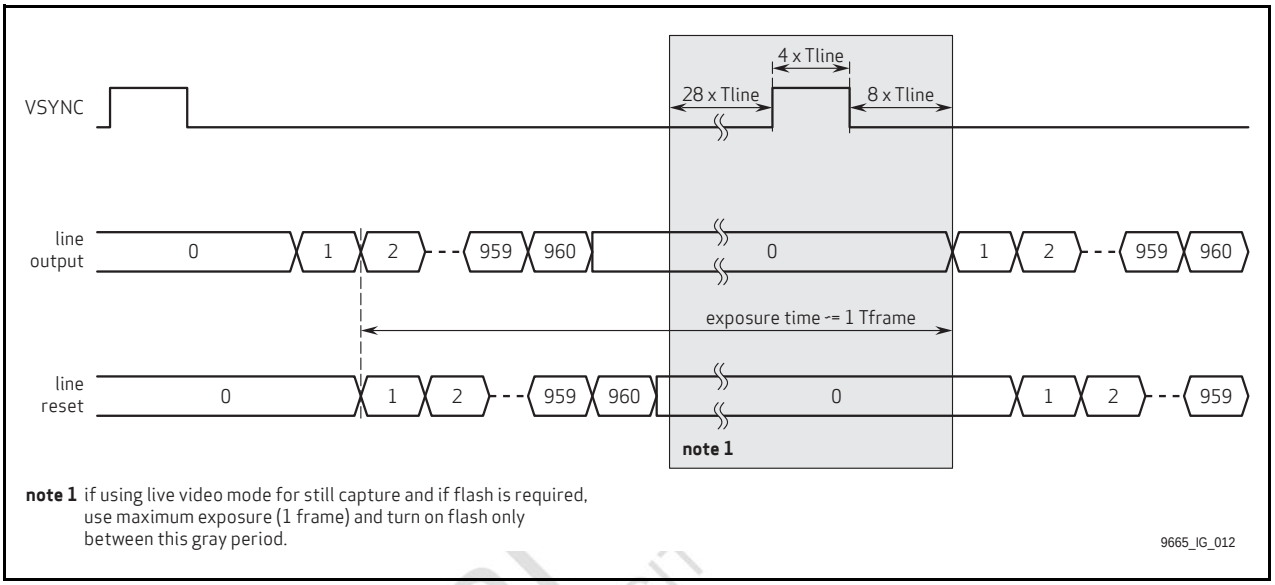
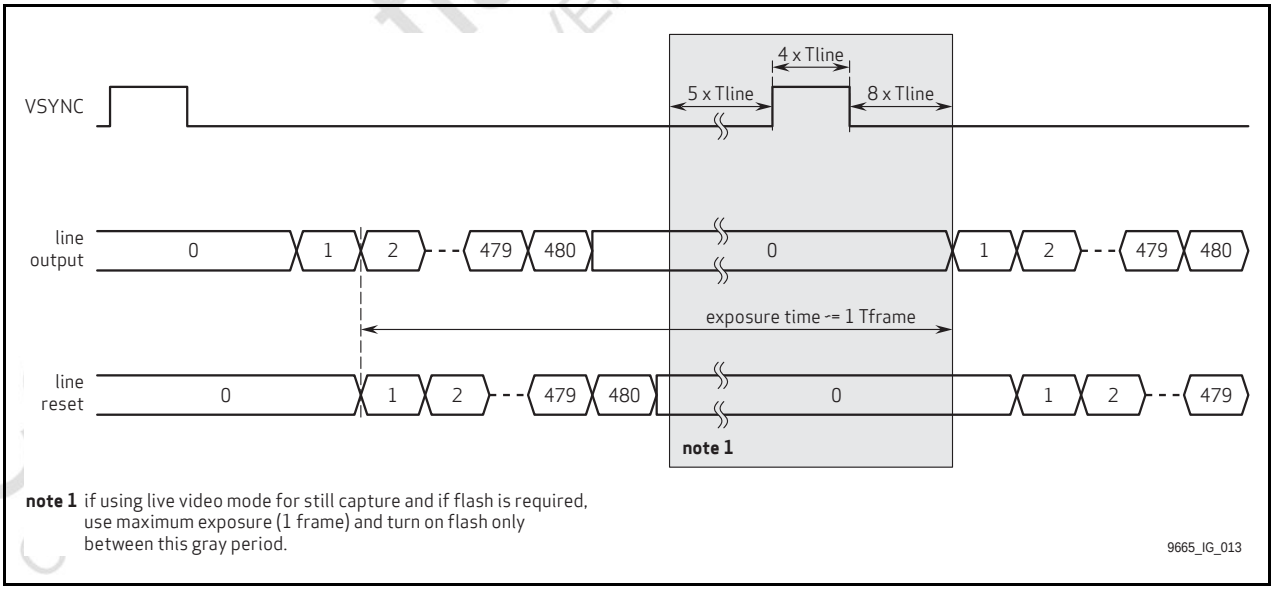


Figure 3-12 VGA Strobe Flash Timing Diagram



4 Analog Processing Block

This block performs all analog image functions including Automatic Gain Control (AGC) and other image manipulation functions.

4.1 Gain Control

The OV9665 CAMERACHIP sensor provides support for both AGC and manual gain control modes.

4.1.1 Manual Gain Control

The manual gain control mode allows for the companion backend processor to control the OV9665 gain value. The companion backend processor may write gain control values to the CAMERACHIP sensor's RGB raw data register GAIN[7:0] (0x00) according to its corresponding AGC algorithm. The gain value is shown in Table 4-1.

Table 4-1. Total Gain to Control Bit Correlation

Registers GAIN[7:0] (0x00)	Gain	dB
0000 0000	1	0
0000 0001	1 + 1/16	.375
0000 0010	1 + 2/16	.75
0000 0011	1 + 3/16	1.125
0000 0100	1 + 4/16	1.5
0000 0101	1 + 5/16	1.875
0000 0110	1 + 6/16	2.25
0000 0111	1 + 7/16	2.625
0000 1000	1 + 8/16	3
0000 1001	1 + 9/16	3.375
0000 1010	1 + 10/16	3.75
0000 1011	1 + 11/16	4.125
0000 1100	1 + 12/16	4.5
0000 1101	1 + 13/16	4.875
0000 1110	1 + 14/16	5.25
0000 1111	1 + 15/16	5.625
0001 0000	2 × (1 + 0/16)	6
0011 0000	4 × (1 + 0/16)	12
0111 0000	8 × (1 + 0/16)	18
1111 0000	16 × (1 + 0/16)	24

Note: To achieve the best image quality, using "maximum" exposure and "minimum" gain for the highest S/N ratio is recommended. When operating in low-light condition, use the strobe flash.

4.1.2 Automatic Gain Control (AGC)

The AGC function allows the CAMERACHIP sensor to adjust image luminance and target level gain without external command or control. Register setting COM8[2] (0x13) enables AGC.

As with the AEC, the AGC can also be controlled by either of two different algorithms, Histogram-based or Average-based. Refer to Section 3.4.2 for additional details.

The target level control registers are registers AEW (0x24) and AEB (0x25). Refer to Section 3.4.2 for additional details regarding the target level controls. When operating in fast AEC/AGC mode, use register VV[7:0] (0x26) to set the conditions for fast AGC. Table 4-2 shows the general controls for the AGC.

Table 4-2. AGC General Controls

Function	Register	Address	Description
AGC Enable	COM8[2]	0x13	0: Disable AGC function, gain control function is still active 1: Enable AGC function
Gain Setting	GAIN[7:0]	0x00	Gain setting. Read-only when AGC is enabled. When AGC is disabled, these registers can be programmed manually.
Gain Ceiling Select	COM9[7:5]	0x14	000: 2x 001: 4x 010: 8x 011: 16x 100: 32x

The analog pixel data first arrives at the AGC amplifier which can be automatically controlled by the AGC circuit or manually programmed by the user (see Table 4-3). In both cases, the gain control is active but when AGC is disabled, the gain setting is generated by the user and not updated by the AGC circuit.

Table 4-3. AGC Enable Bit

COM8[2] (0x13)	AGC Status	GAIN[7:0] (0x00)
1	Enabled	Controlled by AGC
0	Disabled	Controlled by user

The AGC operation is identical to the AEC (see Section 3.4.2). Table 4-4 lists the registers used to set the histogram-based AGC function.

Table 4-4. Histogram-based AEC Registers

Function	Register	Address
LRL – Low Reference Luminance	HISTO_LOW[7:0]	0x61
HRL – High Reference Luminance	HISTO_HIGH[7:0]	0x62
LPH – Lower Limit of Probability for HRL, after exposure/gain stabilizes	REG75[7:0]	0x75
UPL – Upper Limit of Probability for LRL, after exposure/gain stabilizes	REG76[7:0]	0x76
TPL – Probability Threshold for LRL to control AEC/AGC speed	REG77[7:0]	0x77
TPH – Probability Threshold for HRL to control AEC/AGC speed	REG78[7:0]	0x78
TLL – Low nibble of Luminance Threshold for AEC/AGC speed control	REG79[3:0]	0x79
TLH – High nibble of Luminance Threshold for AEC/AGC speed control	REG79[7:4]	0x79

Table 4-5 lists the registers used to set the AGC convergence limits of the average-based AGC function.

Table 4-5. Average-based AGC Convergence Limits

Function	Register	Address
Control Zone – Upper Limit high nibble	VV[7:4]	0x26
Control Zone – Lower Limit high nibble	VV[3:0]	0x26
Stable Operating Region – Upper Limit	AEW[7:0]	0x24
Stable Operating Region – Lower Limit	AEB[7:0]	0x25

5 Digital Signal Processing

The following subsections describe the controls for white balance, gamma, color matrix, sharpness, and other functions controlled by the DSP.

5.1 White Balance Control

The OV9665 CAMERACHIP sensor supports auto/manual white balance control. After the initial pixel level adjustment, the Red and Blue channel gains are optimized to the Green channel to set the white balance. This white balance is either automatically controlled by the AWB circuit or manually controlled by the user. The following describes these AWB modes:

- Full user control – RED/BLUE channels are set manually
- Normal AWB control – RED/BLUE channels are under AWB control based on R/G/B average values
- Advanced AWB control – RED/BLUE channels are under AWB control based on color temperature

Register COM8[1] (0x13) enables the AWB function. If this bit is set low, the user can manually control red and blue gain. If this bit is set to high, both red and blue gain are controlled by the sensor's internal AWB algorithm.

5.1.1 Automatic White Balance Control

In general, the white balance is done in two steps, by adjusting the Red/Blue gain to match the Green channel and by controlling the AWB response time.

Table 5-1. AWB Red/Blue Balance Control

Function	Register	Address
Green Channel Gain Setting	GREEN[7:0]	0x16
Red Channel Gain Setting	RED[7:0]	0x02
Blue Channel Gain Setting	BLUE[7:0]	0x01

Contact your local OmniVision field applications engineer (FAE) for AWB settings.

5.1.2 Manual White Balance

In manual mode, the companion backend processor can control OV9665 internal Red and Blue register values to achieve white balance. These registers, BLUE (0x01), RED (0x02), and GREEN (0x16), are defined as follows:

- Blue Gain: (BLUE[7:0] (0x01)) = BLUE[7:0] / 64 when REG86[2] (0x86) = 1;
  BLUE[7:0] / 128 when REG86[2] (0x86) = 0
- Red Gain: (RED[7:0] (0x02)) = RED[7:0] / 64 when REG86[2] (0x86) = 1;
  RED[7:0] / 128 when REG86[2] (0x86) = 0
- Green Gain: (GREEN[7:0] (0x16)) = GREEN[7:0] / 64 when REG86[2] (0x86) = 1;
  GREEN[7:0] / 128 when REG86[2] (0x86) = 0

5.2 Gamma Control

The OV9665 gamma curve is composed of approximately 16 linear lines as shown in Figure 5-1 and Table 5-2.

Figure 5-1 Gamma Curve

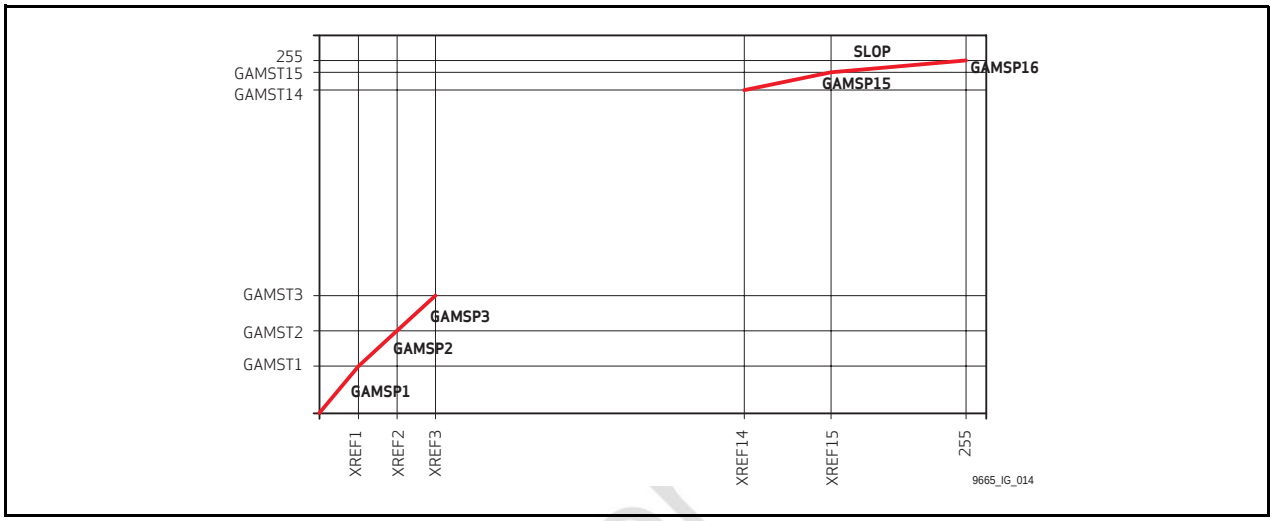


Table 5-2. Gamma Related Registers and Parameters

Gamma Segments Start Point		Gamma Segments Horizontal Reference	
Name	**Register**	**Name**	**Value**
SLOP	0xAA		
GAM1	0x9B	XREF1	4
GAM2	0x9C	XREF2	8
GAM3	0x9D	XREF3	16
GAM4	0x9E	XREF4	32
GAM5	0x9F	XREF5	40
GAM6	0xA0	XREF6	48
GAM7	0xA1	XREF7	56
GAM8	0xA2	XREF8	64
GAM9	0xA3	XREF9	72
GAM10	0xA4	XREF10	80
GAM11	0xA5	XREF11	96
GAM12	0xA6	XREF12	112
GAM13	0xA7	XREF13	144
GAM14	0xA8	XREF14	176
GAM15	0xA9	XREF15	208

5.2.1 Highest Segment Gamma Slope Calculation

The highest segment slope (register SLOP (0xAA) is calculated by the following equation:

$$SLOP[7:0] = (255 - GAM15[7:0] + 1) \times 40/30$$

5.3 Color Matrix

The color matrix is used to eliminate the crosstalk induced by the micro-lens and color filter process. It also compensates for lighting and temperature effects. It can be implemented for hue, color saturation, and color space conversion from RGB to YUV or RGB to YCbCr.

5.3.1 Color Matrix Control

The OV9665 has a built-in 3x3 color matrix circuit. This color matrix performs color correction and RGB to YUV conversion. Also, because of the Matrix linear algebra characteristic, it can also do color gain and hue control as shown below:

[YUV] = [RGB to YUV Matrix] × [Color correction] × [RGB]

[YUV] = [Combined Matrix] [RGB]

Table 5-3. Color Matrix Related Registers and Parameters

Name	Register	Address	Description
CMX1	CMX1	0xBD	
CMX2	CMX2	0xBE	
CMX3	CMX3	0xBF	
CMX4	CMX4	0xC0	
CMX5	CMX5	0xC1	
CMX6	CMX6	0xC2	
CMX7	CMX7	0xC3	
CMX8	CMX8	0xC4	
CMX9	CMX9	0xC5	
Sign Bit	CMX10[7:0]	0xC6	For CMX8 through CMX1, respectively
	CMX11[7]	0xC7	For CMX9

The OV9665 has an internal 3x3 matrix that can be described as follows:

M1 M2 M3
M4 M5 M6
M7 M8 M9

where:

M1 M2 M3 <= Y = (CMX1 × R + CMX2 × G + CMX3 × B) / 32
M4 M5 M6 <= U = (CMX4 × R + CMX5 × G + CMX6 × B) / 32
M7 M8 M9 <= V = (CMX7 × R + CMX8 × G + CMX9 × B) / 32

and the sign is assigned as shown below:

CMX10[0]	(0xC6)	sign bit of CMX1
CMX10[1]	(0xC6)	sign bit of CMX2
CMX10[2]	(0xC6)	sign bit of CMX3
CMX10[3]	(0xC6)	sign bit of CMX4
CMX10[4]	(0xC6)	sign bit of CMX5
CMX10[5]	(0xC6)	sign bit of CMX6
CMX10[6]	(0xC6)	sign bit of CMX7
CMX10[7]	(0xC6)	sign bit of CMX8
CMX11[7]	(0xC7)	sign bit of CMX9

5.3.1.1 Color Correction Matrix

Below is OmniVision's recommended OV9665 color correction matrix:

2.221	-1.119	0.062
-0.669	2.2173	-0.474
-0.193	-1.544	2.942

5.3.1.2 RGB to YUV Conversion Matrix

Below is the OV9665 RGB to YUV conversion matrix.

10/32	19/32	3/32
-5/32	-11/32	16/32
16/32	-13/32	-3/32

5.3.1.3 Final Matrix

[YUV] = [RGB to YUV Matrix] × [Color correction] × [R G B]

[YUV] = [Combined Matrix] [R G B]

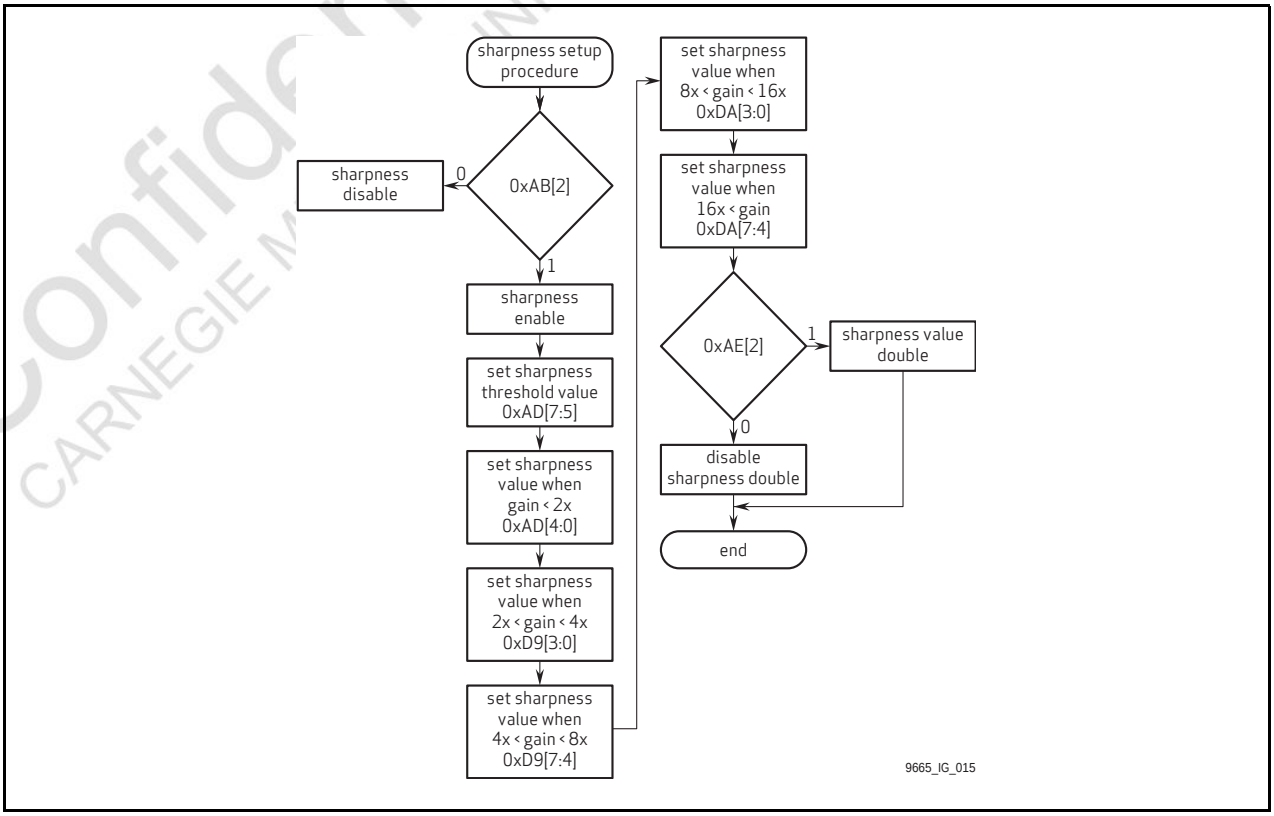
5.4 Sharpness Control

The OV9665 features digital sharpness enhancement. It detects the edge first and then only amplifies the edge difference. Also, the OV9665 has an auto sharpness adjust mode which detects the light condition and noise level of the image and automatically adjusts the sharpness level. Table 5-4 lists the related registers and parameters.

Table 5-4. Sharpness Registers and Parameters

Function	Register	Address	Description
Sharpness Mode Selection	REGAB[2]	0xAB	0: Sharpness disable 1: Sharpness enable
Sharpness Level	REGAD[4:0]	0xAD	Sharpness value when GAIN < 2x
Sharpness Level	REGD9[3:0]	0xD9	Sharpness value when 2x < GAIN < 4x
Sharpness Level	REGD9[7:4]	0xD9	Sharpness value when 4x < GAIN < 8x
Sharpness Level	REGDA[3:0]	0xDA	Sharpness value when 8x < GAIN < 16x
Sharpness Level	REGDA[7:4]	0xDA	Sharpness value when 16x < GAIN
Sharpness Threshold	REGAD[7:5]	0xAD	Sharpness value threshold
Sharpness Double	REGAE[2]	0xAE	Sharpness double

Figure 5-2 Sharpness Setup Function



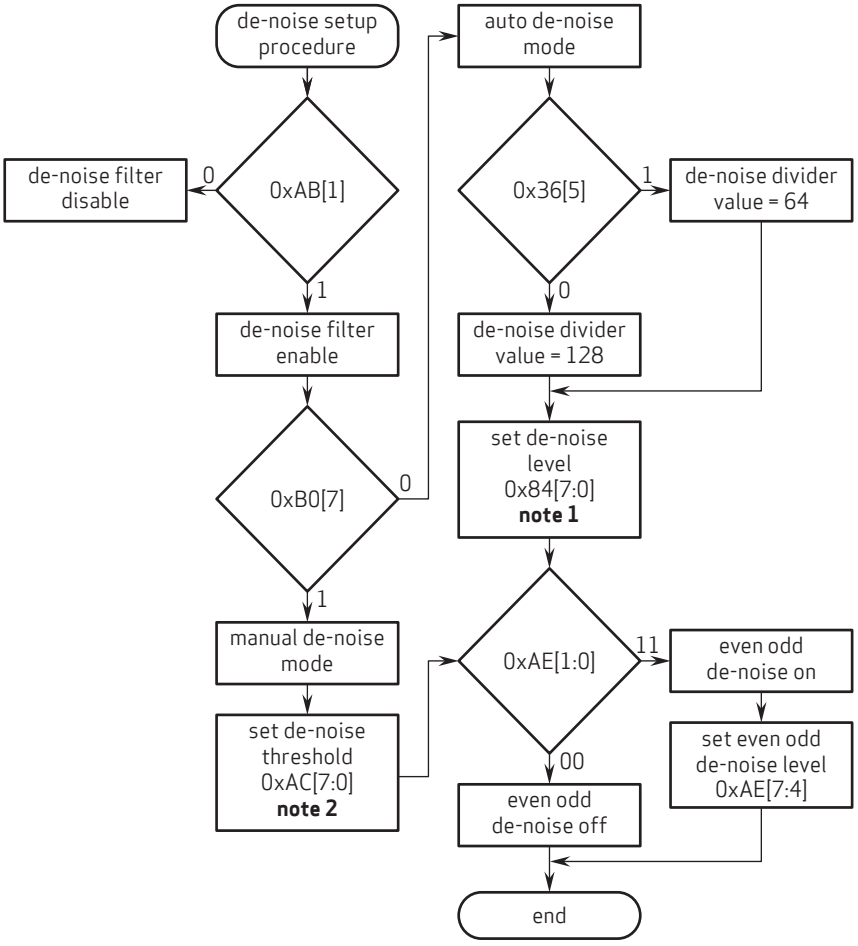
5.5 De-Noise

The OV9665 has a built-in de-noise circuit to reduce noise. Also, the OV9665 supports an auto and manual de-noise adjust mode. In the case of OV9665 auto de-noise mode, the OV9665 detects the light condition and noise level of the image and automatically adjusts the de-noise level. Table 5-5 lists the related registers and parameters.

Table 5-5. De-Noise Registers and Parameters

Function	Register	Address	Description
De-noise Enable	REGAB[1]	0xAB	0: Disable de-noise function 1: Enable de-noise function
De-noise Mode Selection	REGB0[7]	0xB0	0: Auto de-noise mode - de-noise level automatically changes with gain value 1: Manual de-noise mode - de-noise threshold value is set by register REGAC[7:0] (0xAC)
De-noise Level in Auto De-noise Mode	REG84[7:0]	0x84	De-noise threshold level adjustment De-Noise threshold level = gain value × REG84[7:0] / (de-noise divider value) If value < 1, then use 1. Gain value = 1 when register GAIN (0x00) = 0 and gain value = 31 when GAIN (0x00) = FF
De-noise divider value in Auto De-noise Mode	REG36[5]	0x36	0: De-noise divider value = 128 1: De-noise divider value = 64
De-noise Level in Manual De-noise Mode	REGAC[7:0]	0xAC	De-noise level value in manual de-noise mode.
Even-Odd De-noise Function Switch	REGAE[1:0]	0xAE	00: Disable even-odd de-noise function 11: Enable even-odd de-noise function
Even-Odd De-noise Threshold	REGAE[7:4]	0xAE	Even-Odd de-noise threshold value

Figure 5-3 De-Noise Function



note 1 de-noise threshold level = gain value × 0x84[7:0] / (de-noise divider value), if value < 1 then use 1. gain value = 1 when 0x00 = 0 and gain value = 31 when 0x00 = FF.

note 2 gain value has no effect on manual de-noise mode.

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5.6 Defect Pixel Correction

The OV9665 has a built-in defect pixel correction circuit. Table 5-6 lists the related registers and parameters.

Table 5-6. Defect Pixel Correction Registers and Parameters

Function	Register	Address	Description
White Pixel Correction	REG1E[7]	0x1E	0: Disable 1: Enable
Black Pixel Correction	REG1E[6]	0x1E	0: Disable 1: Enable

5.7 Brightness and Contrast Control

The OV9665 has built-in gamma and exposure-independent brightness control. Table 5-7 lists the the related registers and parameters.

$Y' = (Y + Y_{offset}) \times Y_{gain} + Brightness$

Table 5-7. Brightness Control Registers and Parameters

Function	Register	Address	Description
SDE Enable	CMX11[4]	0xC7	0: Special digital effect ON 1: Special digital effect OFF
Contrast Enable	REGC8[2]	0xC8	0: Contrast effect ON 1: Contrast effect OFF
Y_{offset}	REGCF[7:0]	0xCF	Luminance offset to adjust contrast value
Y_{gain}	REGD0[7:0]	0xD0	Luminance gain to adjust contrast value
Brightness Control Sign Bit	REGD1[7]	0xD1	0: Positive 1: Negative
Brightness Control Level	REGD1[6:0]	0xD1	Brightness level control

5.8 Lens Shading Correction

Because of the non-uniform light transparence, the outer areas of the image appears darker than the center area. The lens correction function amplifies the outer areas of the image to obtain a uniform image.

Figure 5-4 Lens Shading Correction

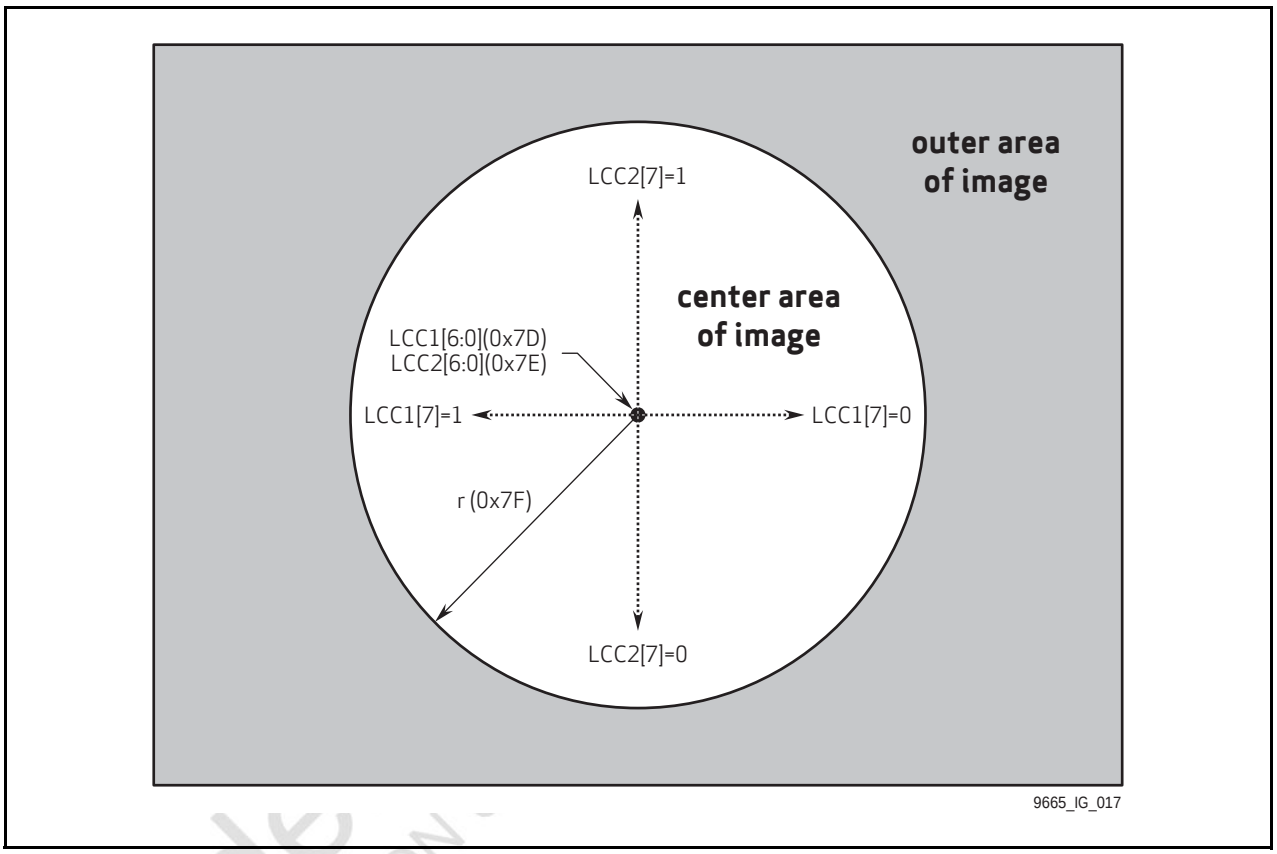


Table 5-8. Lens Shading Correction Registers and Parameters

Function	Register	Address	Note
Lens Correction Center Coordinates X Default LC_XY = (X,Y) = (0,0)	REG7D[6:0] REG7D[7] 0: Offset REG7D[6:0] to +X direction 1: Offset REG7D[6:0] to -X direction	0x7D	Lens Correction Center Coordinates X, one bit equals one pixel in full resolution.
Lens Correction Center Coordinates Y Default LC_XY = (X,Y) = (0,0)	REG7E[6:0] REG7E[7] 0: Offset REG7E[6:0] to +Y direction 1: Offset REG7E[6:0] to -Y direction	0x7E	Lens Correction Center Coordinates Y, one bit equals one line in full resolution.
Radius of the circular section where lens correction is not needed	REG7F	0x7F	
Green Gain Parameter/3-channel (R, G and B) Gain Parameter	REG82	0x82	Green gain parameter if LC7[2] = 1; Gain parameter for R,G,B channels if LC7[2] = 0
Multi-Gain Control	LC7[2] 0: Use register REG82 for gain parameter for R, G, and B channels 1: Use register REG82 for Green Gain parameter, REG80 for Blue Gain parameter, and REG81 for Red Gain parameter LC7[0] 0: Disable lens correction 1: Enable lens correction	0x83	
Blue Gain Parameter	REG80	0x80	Not used if LC7[2] = 0
Red Gain Parameter	REG81	0x81	Not used if LC7[2] = 0

5.9 UV Adjust Function

For optimized color performance in low light conditions, the OV9665 provides a UV adjust function by detecting light conditions.

This function provides optimized color performance in low light conditions and best color performance in normal light conditions.

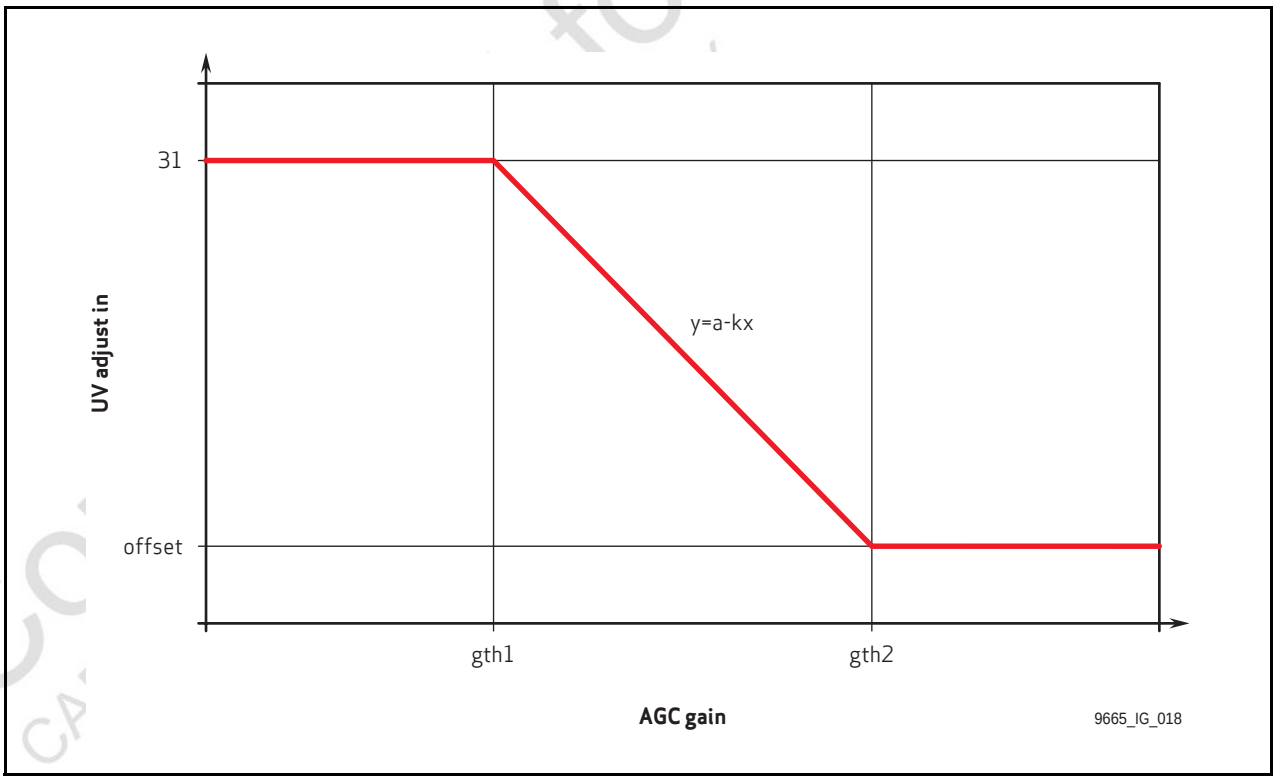
5.9.1 Manual Mode

By setting uvadj_gth2 (register REG65 (0x65) and register REG66 (0x66)) to 0, the UV adjust function is controlled only by register REGD2[4:0] (0xD2) at all gain settings.

5.9.2 Auto Mode

If the UV adjust function is set to auto mode, then the UV adjust curve parameters should be entered into the corresponding registers:

Figure 5-5 Auto UV Adjust



Calculating the UV adjust parameters as follows:

The values, gth1, gth2, a and k, should be entered into the registers to set the curve. To get these values, first set the values of gth1, gth2 and offset. Then, calculate the values of a and k as follows:

k = (31 – offset) / (gth2 – gth1)
a = 31 + k × gth1

Registers to be changed:

k[7:0]: {COM1[5:4] (0x03), REG05[2:0] (0x05), REG60[2:0] (0x60)}
a[5:0]: {REG41[7:5] (0x41), REG5B[4:2] (0x5B)}
gth1[3:0]: REG7C[6:3] (0x7C)
gth2[4:0]: {REG65[1:0] (0x65), REG66[7:5] (0x66)}
offset[4:0]: REGD2[4:0] (0xD2)

It is not necessary to enter the value of the offset. The values of a, k and gth2 are enough to determine the offset.

Note that when entering k into the registers, we have 4 bits for the integer and 4 bits for the fraction part. Use the exact k value for calculations. For example, if k = (31 – 8) / (31 – 15) = 1.4375, the value to be entered for k is <<4 = 23.

Table 5-9 lists auto UV adjust control registers.

Table 5-9. Automatic UV Adjustment Registers

Function	Register	Address	Description
Auto UV Adjust Enable	REGD2[7]	0xD2	0: Disable 1: Enable
k[7:0]	{COM1[5:4], REG05[2:0], REG60[2:0]}	{0x03, 0x05, 0x60}	UV adjust slope between gain threshold 1 and gain threshold 2
a[5:0]	{REG41[7:5], REG5B[4:2]}	{0x41, 0x5B}	UV adjust offset value between gain threshold 1 and gain threshold 2
gth1[3:0]	REG7C[6:3]	0x7C	Gain threshold 1
gth2[4:0]	{REG65[1:0], REG66[7:5]}	{0x65, 0x66}	Gain threshold 2
offset[4:0]	REGD2[4:0]	0xD2	Offset value

6 Image Scaling

The OV9665 Image Scaling circuit allows for image output starting from 352x288. Because the OV9665 CAMERACHIP sensor has SXGA (1280x1024) and VGA (640x480) array resolution output, image scaling can be from SXGA (1280x1024) resolution or VGA (640x480).

6.1 Image Output Size

The OV9665 allows the user to select an output size other than SXGA or VGA. The user can define any horizontal output size and vertical output size that is less than 1280x1024 in SXGA mode (or 640x480 in VGA mode). The output image will crop the original image to match the output size.

Table 6-1. Image Output Control Registers

Function	Register	Address	Description
Output Size H (11 bits)	{REGBB[7:0], REGB7[7:6]}	{0xBB, 0xB7}	Output image, horizontal size
Output Size V (11 bits)	{REGBC[7:0], REGB8[7:6], REGB7[7]}	{0xBC, 0xB8, 0xB7}	Output image, vertical size

6.2 Image Scaling

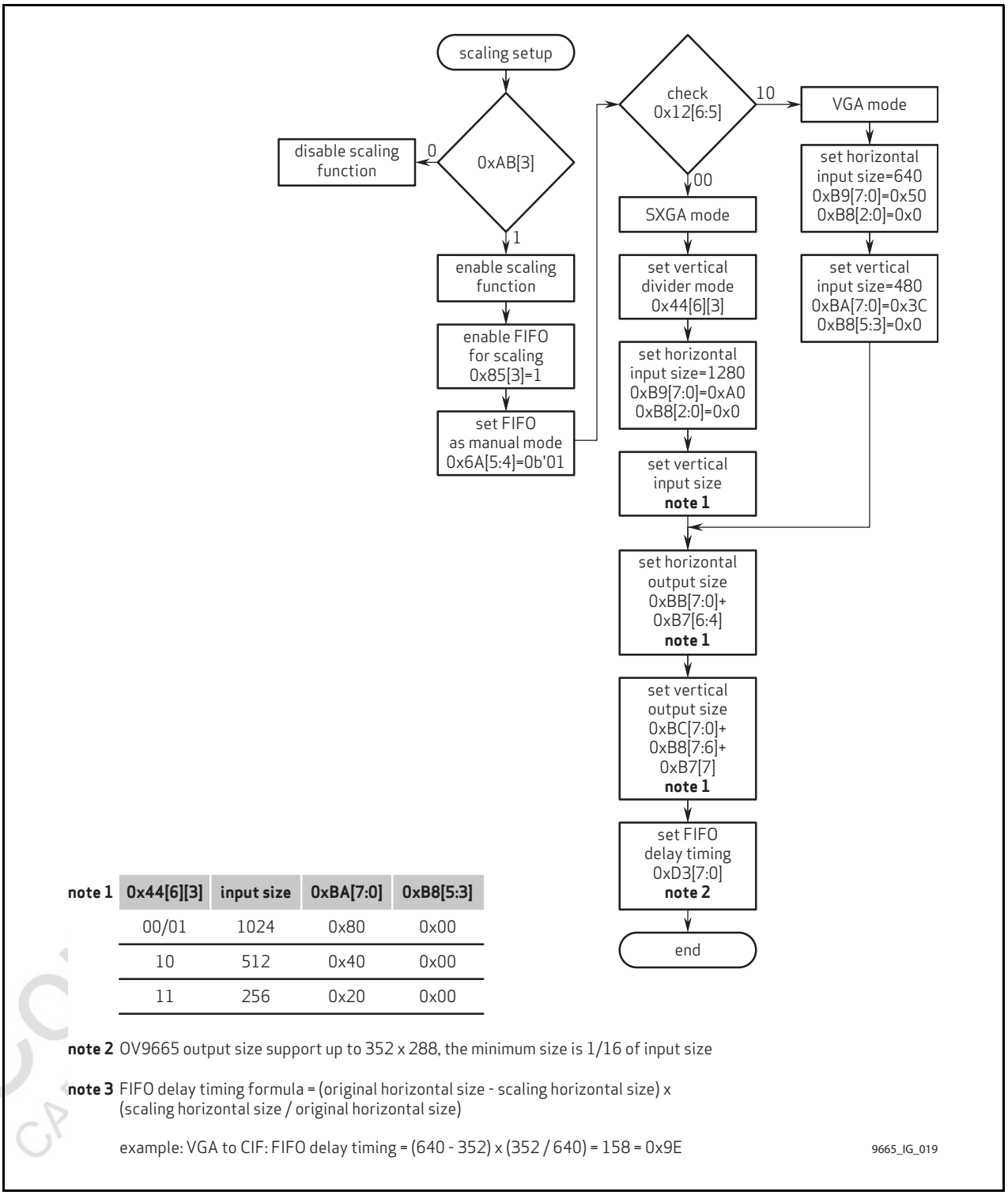
The OV9665 provides the image scaling function when the output size is less than CIF (352x288). The output image will scale down in proportion to the output size.

Table 6-2. Image Scaling Control Registers

Function	Register	Address	Description
Digital Scaling Enable	REGAB[3]	0xAB	0: Disable 1: Enable
Vertical Line Divider[a]	REG44[6]	0x44	0: No divider 1: Divider
Vertical Line Divider Number	REG44[3]	0x44	0: Divide vertical line by 2 1: Divide vertical line by 4
Input Size H	{REGB9[7:0], REGB8[2:0]}	{0xB9, 0xB8}	Original image, horizontal size
Input Size V	{REGBA[7:0], REGB8[5:3]}	{0xBA, 0xB8}	When register REG44[6],[3] (0x44) = 0x, set to original image, vertical size When register REG44[6],[3] (0x44) = 10, set to original image, vertical size /2 When register REG44[6],[3] (0x44) = 11, set to original image, vertical size /4
FIFO Manual Option	REG6A[4]	0x6A	0: Auto mode 1: Manual mode (recommended)
FIFO Enable	REG85[3]	0x85	0: Disable FIFO 1: Enable FIFO
FIFO Delay Timing	REGD3	0xD3	FIFO delay configuration

a. User can set the vertical divider mode when scale factor is larger than 4x to avoid lost bit phenomenon.

Figure 6-1 Image Scaling Function



note 1

0x44[6][3]	input size	0xBA[7:0]	0xB8[5:3]
00/01	1024	0x80	0x00
10	512	0x40	0x00
11	256	0x20	0x00

note 2 OV9665 output size support up to 352 x 288, the minimum size is 1/16 of input size

note 3 FIFO delay timing formula = (original horizontal size - scaling horizontal size) x (scaling horizontal size / original horizontal size)

example: VGA to CIF: FIFO delay timing = (640 - 352) x (352 / 640) = 158 = 0x9E

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6.2.1 Examples of Zoom/Scaling

Table 6-3. Scaling from SXGA Mode (15 fps maximum)

Register	Address	SXGA (1280x1024)	VGA (640x480)	QVGA (320x240)	CIF (352x288)
REGAB[3]	0xAB	0	0	1	1
REGB7[7:4]	0xB7	0	0	0	0
REGB8	0xB8	0x0	0x0	0x0	0x0
REGB9	0xB9	0xA0	0xA0	0xA0	0xA0
REGBA	0xBA	0x80	0x80	0x80	0x80
REGBB	0xBB	0xA0	0x50	0x28	0x2C
REGBC	0xBC	0x80	0x3C	0x1E	0x24
REG6A	0x6A	0x14	0x14	0x14	0x14
REG85	0x85	0xE7	0xE7	0xE7	0xE7
REGD3	0xD3	0x00	0x00	0x00	0x00
REG44	0x44	0x00	0x00	0x00	0x00

Table 6-4. Scaling from VGA Mode (30 fps maximum)

Register	Address	VGA (640x480)	QVGA (320x240)	QQVGA (160x120)	CIF (352x288)	QCIF (176x144)
REGAB[3]	0xAB	0	1	1	1	1
REGB7[7:4]	0xB7	0	0	0	0	0
REGB8	0xB8	0x0	0x0	0x0	0x0	0x0
REGB9	0xB9	0x50	0x50	0x50	0x50	0x50
REGBA	0xBA	0x3C	0x3C	0x3C	0x3C	0x3C
REGBB	0xBB	0x50	0x28	0x14	0x2C	0x16
REGBC	0xBC	0x3C	0x1E	0x0F	0x24	0x12
REG6A	0x6A	0x14	0x14	0x14	0x14	0x14
REG85	0x85	0xE7	0xEF	0xEF	0xEF	0xEF
REGD3	0xD3	0x00	0xA0	0x78	0x9E	0x7F

7 Output Formatter

This block controls all output and data formatting required prior to sending the image out on D[7:0]. Table 7-1 lists the control registers for the Output Formatting functions.

Table 7-1. Output Formatting General Controls

Function		Register	Address	Value
Mirror Image Enable		REG33[3]	0x33	0'b1
		REG04[7]	0x04	0'b1
Vertical Flip Enable		REG04[6]	0x04	0'b1
YUV/YCbCr Mode		REGD7[1:0]	0xD7	0'b00
RGB Mode	RGB RAW	REGD7[1:0]	0xD7	0'b10
	RGB565	REGD7[1:0], REGD8[1:0]	0xD7, 0xD8	0'b01, 0'b01
	RGB555	REGD7[1:0], REGD8[1:0]	0xD7, 0xD8	0'b01, 0'b10
	RGB444	REGD7[1:0], REGD8[1:0]	0xD7, 0xD8	0'b01, 0'b11

RGB565, RGB555 and RGB444 are alternate output formats where each color is represented by different D[7:0] bit widths.

This format uses an odd/even byte pair to express the color for each pixel:

- RGB565

Bytes	D9	D8	D7	D6	D5	D4	D3	D2
First Byte	R7	R6	R5	R4	R3	G7	G6	G5
Second Byte	G4	G3	G2	B7	B6	B5	B4	B3

- RGB555

Bytes	D9	D8	D7	D6	D5	D4	D3	D2
First Byte	00	R7	R6	R5	R4	R3	G7	G6
Second Byte	G5	G4	G3	B7	B6	B5	B4	B3

- RGB444

Bytes	D9	D8	D7	D6	D5	D4	D3	D2
First Byte	00	00	00	00	R7	R6	R5	R4
Second Byte	G7	G6	G5	G4	B7	B6	B5	B4

7.1 Windowing

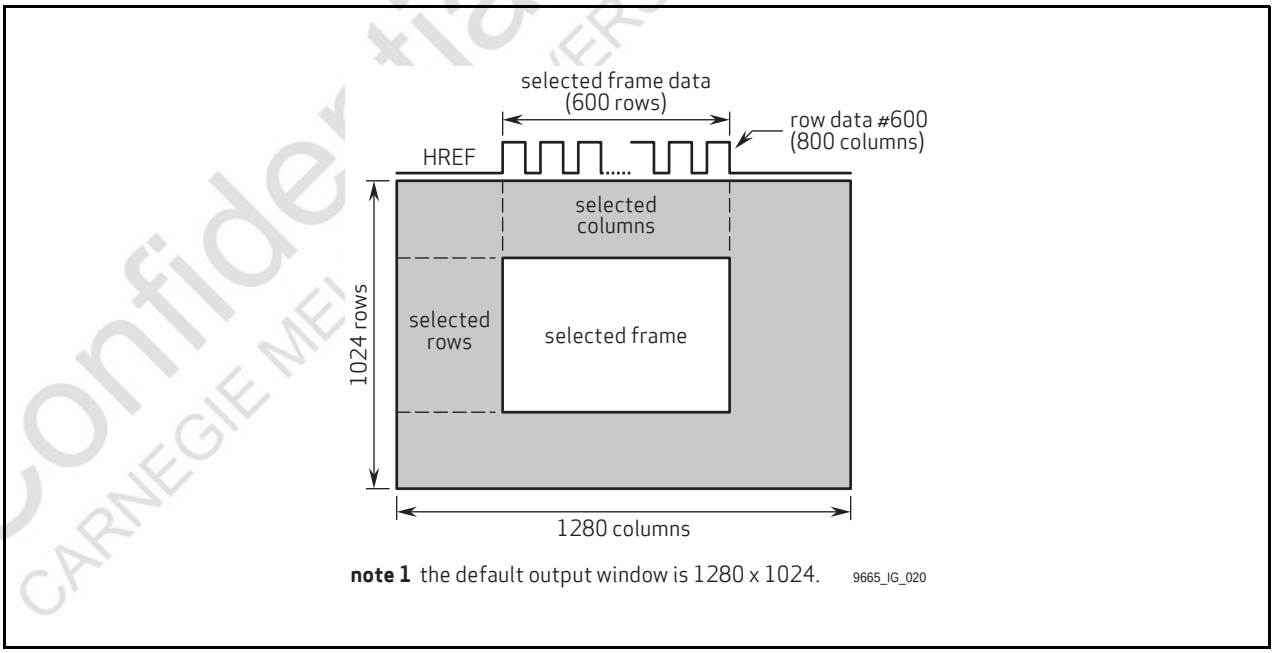
The OV9665 CAMERACHIP sensor windowing feature allows the user to define the active pixels used in the final image (frame) as required for low-resolution applications. Selecting the Start/Stop Row/Column addresses (modifying window size and/or position) does not change the frame or data rate. When windowing is enabled, the HREF signal is asserted to be consistent with the programmed 'active' horizontal and vertical region. Table 7-2 lists the control registers

Table 7-2. Windowing Control Registers

Function	Register	Address
Horizontal Frame (HREF Column) Start	HREFST[7:0] REG32[2:0]	0x17 0x32
Horizontal Frame (HREF Column) Stop	HREFEND[7:0] REG32[5:3]	0x18 0x32
Vertical Frame (Row) Start	VSTRT[7:0] COM1[2:0]	0x19 0x03
Vertical Frame (Row) Stop	VEND[7:0] COM1[5:3]	0x1A 0x03

Figure 7-1 shows an example of a windowed frame.

Figure 7-1 Example of Windowing



The OV9665 windowing function can be implemented with the sub-sampling mode for the camera zoom function. For example, if the preview image size is 160 x 120 (QQVGA), the camera can be set to output QQVGA sub-sampling mode, then set to output QVGA mode (320 x 240) and use the windowing function to capture center-quarter area (160 x 120) to implement the 2x zoom-in function. Then, the camera can be set to VGA mode (640 x 480) or SXGA (1280 x 1028) mode, to implement 4x and 8x zoom-in function.

7.2 Data Formatting

Table 7-3 lists the registers used for Data Formatting.

Table 7-3. Data Formatting

Function	Register	Address	Note	
VSYNC Polarity	COM10[1]	0x15	High: Negative	
HREF/HSYNC Polarity	REGD8[5]	0xD8	High: Negative	
YUV Formatting	REGD7[1:0]	0xD7	00: YUV 01: Raw RGB interpolation 10: ISP RAW 11: Sensor RAW	
YU Sequence Exchange	REGD7[4]	0xD7	0: UY 1: YU	
UV Sequence Exchange	REGD2[5]	0xD2	0: UV 1: VU	
Output Data MSB/LSB Swap Enable	REGD7[3]	0xD7	0: D9 = MSB; D0 = LSB 1: D9 = LSB; D0 = MSB	
D[9:0] - PCLK Reference Edge	COM10[4]	0x15	0: Data update at falling edge 1: Data update at rising edge	
ITU-656 Format Enable	REGD8[3]	0xD8	1: Enable	
Frame Rate Adjust Setting (by inserting dummy pixels)	REG2A[7:4] (MSB) REG2B[7:0] (LSB)	0x2A 0x2B	SXGA	LSB: 1/1520 Line Period increase
			VGA	LSB: 1/760 Line Period increase
Frame Rate Adjust Setting (by inserting dummy lines)	ADDVSH[7:0] (MSB) ADDVSL[7:0] (LSB)	0x2E 0x2D	SXGA	LSB: 1/1052 Frame Period increase
			VGA	LSB: 1/526 Frame Period increase
Auto Frame Rate Adjust Enable (by inserting dummy lines in VSYNC period)	COM6[3]	0x0F	0: Disable - set registers ADDVSH (0x2E) and ADDVSL (0x2D) to 0 1: Enable - registers ADDVSH (0x2E) and ADDVSL (0x2D) are automatically updated	
Auto Frame Rate Adjust Range	COM1[7:6]	0x03	00: Frame rate does not change 01: Minimum 1/2 frame rate 10: Minimum 1/4 frame rate 11: Minimum 1/8 frame rate	
Output HSYNC on HREF Pin Enable	REGD7[2]	0xD7	0: HREF 1: HSYNC	
PCLK Output Gated by HREF Enable	COM10[5]	0x15	0: Free running PCLK 1: PCLK gated by HREF	
HSYNC Rising Edge Delay	REG2A[1:0] (MSB) HSDY[7:0] (LSB)	0x2A 0x30		
HSYNC Falling Edge Delay	REG2A[3:2] (MSB) HEDY[7:0] (LSB)	0x2A 0x31		
VSYNC and HREF/DATA drop	COM9[2:1]	0x14	Drop over-exposure image	

7.2.1 ITU-656 Format Enable

Instead of using HREF to define each row, the ITU-656 standard inserts a 4-byte header before and after the row data.

Header Footer: [FF] [00] [00] [Sync Byte]

In vertical black period

HREF start [FF][00][00][EC]

HREF end [FF][00][00][F1]

In valid data period

HREF start [FF][00][00][C7]

HREF end [FF][00][00][DA]

7.2.2 Frame Rate Adjust

The OV9665 offers three methods of frame rate adjustment using the clock prescaler (see Section 3.3.1), by inserting 'dummy' pixels in each row's output, and by inserting dummy lines in each frame output. By inserting these dummy pixels (using REG2A[6:4] (0x2A) and REG2B[7:0] (0x2B)), the frame rate can be changed while leaving the pixel unchanged.

Dummy Pixel Number = REG2A[7:4] (0x2A) × 256 + REG2B[7:0] (0x2B)

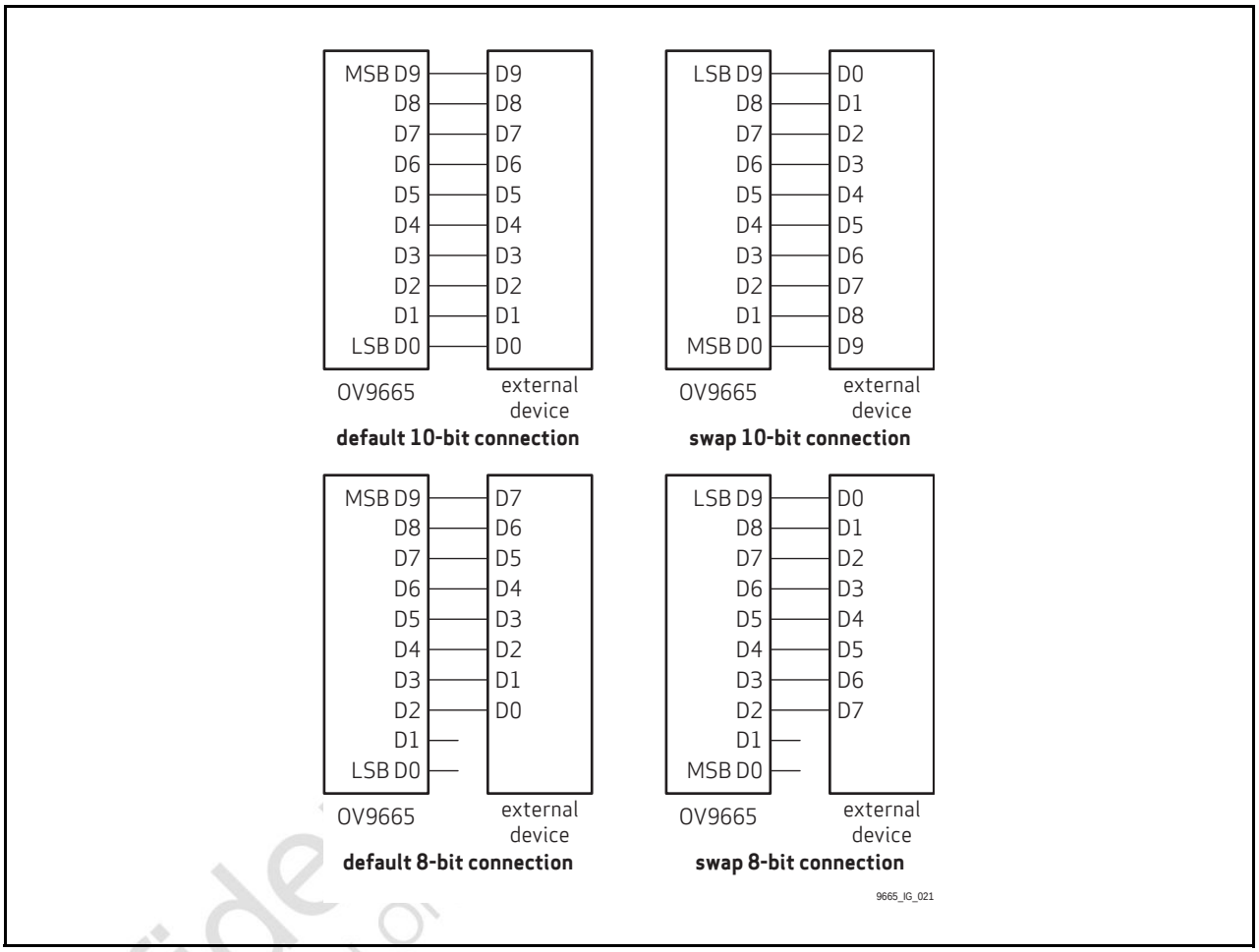
By inserting dummy lines at frame output, the user can get the same data rate and the same data readout time at one frame.

Also, in low light (night mode) conditions, the user can turn on auto frame adjust to decrease the random noise and increase the sensitivity (get more exposure time). In this mode, COM6[3] (0x0F) is high. COM1[7:6] (0x03) is used to control the frame adjust range. See Table 7-3 for details.

7.2.3 Output Data MSB/LSB Swap Enable

See Figure 7-2 for details when MSB/LSB output data swap is enabled.

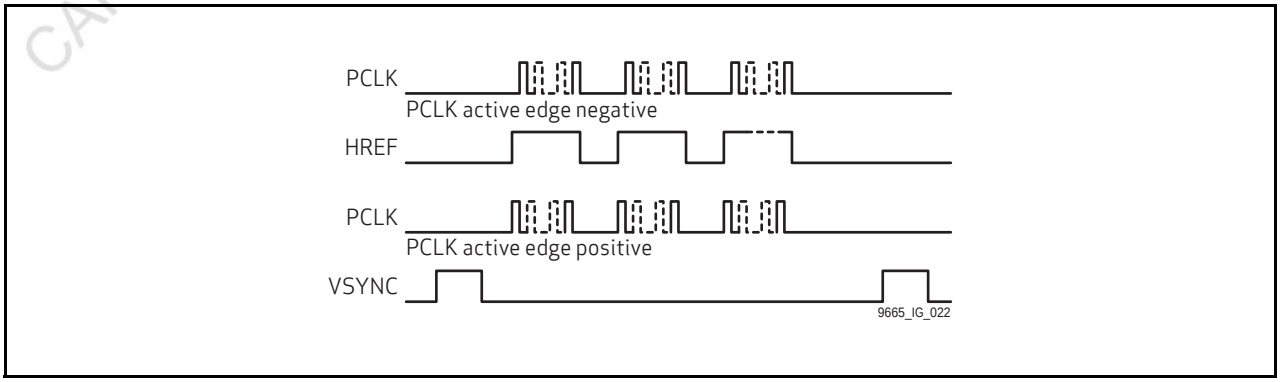
Figure 7-2 MSB/LSB Output Data Swap



7.2.4 D[9:0] - PCLK Reference Edge

To conserve the user's memory space, the PCLK output can be gated by HREF, which defines the active video period.

Figure 7-3 PCLK Output Only at Valid Pixels



8 Digital Video Port

The two bits shown in Table 8-1 are used to increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's D[9:0], HREF, VSYNC, and PCLK loading.

Table 8-1. Output Drive Current

Function	Register	Address	Value
1x I_{OL}/I_{OH} Enable	COM2[1:0]	0x09	2'b00
2x I_{OL}/I_{OH} Enable	COM2[1:0]	0x09	2'b01 or 2'b10
4x I_{OL}/I_{OH} Enable	COM2[1:0]	0x09	2'b11

9 SCCB Interface

The *OmniVision Serial Camera Control Bus (SCCB) Functional Specification* is available at http://www.ovt.com. The Functional Specification provides complete information for using the SCCB to control the features of an OmniVision CAMERACHIP sensor.

The OV9665 CAMERACHIP sensor uses the SCCB protocol to control the features noted in this document via the companion backend system ASIC. The device slave addresses of the OV9665 CAMERACHIP sensor are: 0x60 for write (7-bit address and 1-bit write) and 0x61 for read (7-bit address and 1-bit read). The first command in the SCCB transmission must be a register reset, as most registers will rely on the default value setting.

9.1 Control Functions

Table 9-1 lists the SCCB control functions.

Table 9-1. SCCB Control Functions

Function	Register	Address
Register Reset	COM7[7]	0x12
Standby Mode Enable	COM2[4]	0x09
Tri-state Enable for Output Clock during Standby Mode	REGD6[3]	0xD6
Tri-state Enable for Output Data during Standby Mode	REGD5[7:0], REGD6[1:0]	0xD5, 0xD6

9.1.1 Register Reset

All registers can be reset to their default values by using the RESET pin (RESET to VDD_IO) or by using the SCCB interface (see register COM7[7] (0x12)). OmniVision suggests putting the reset register setting (set register COM7 (0x12) to 0x80) at the beginning of the sensor initialization. After software reset, wait 1 ms for the next register access (there is no limitation for other register settings).

9.1.2 Tri-state Enable

The output clock and data pin mode is optional during Standby Mode. If Tri-state mode is enabled, the output clock and data pin will be Tri-stated during Standby Mode and if Tri-state mode is disabled, the output pin will keep the last status before sensor goes to standby.

Table 9-2 lists related control registers.

Table 9-2. Tri-State Enable Registers

Function	Register	Address	Description
Tri-state Enable for Output Clock During Standby Mode	REGD6[3]	0xD6	0: Disable 1: Enable
Tri-state Enable for Output Data During Standby Mode	REGD5[7:0], REGD6[1:0]	0xD5, 0xD6	For each bit: 0: Disable 1: Enable

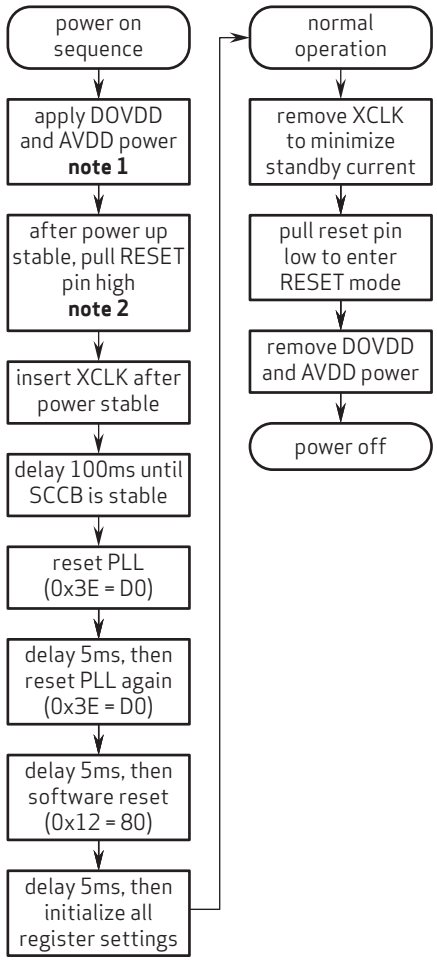
9.2 Power Management

The OV9665 supports two kinds of suspend modes, sleep mode and power down mode, to save power consumption when the sensor is not being used.

9.2.1 Power ON/OFF Sequence

Proper power ON and power OFF sequence is important in order for the OV9665 to work in the correct state. Figure 9-3 shows OmniVision's recommended sequence.

Figure 9-1 Sleep Mode Setup and Wake Up Procedure



note 1 if AVDD and DOVDD are applied separately, the power ON sequence should be DOVDD first and AVDD last. the delay between AVDD and DOVDD should be less than 10ms.

note 2 delay between when power becomes stable and when the RESET signal is inserted should be more than 1ms.

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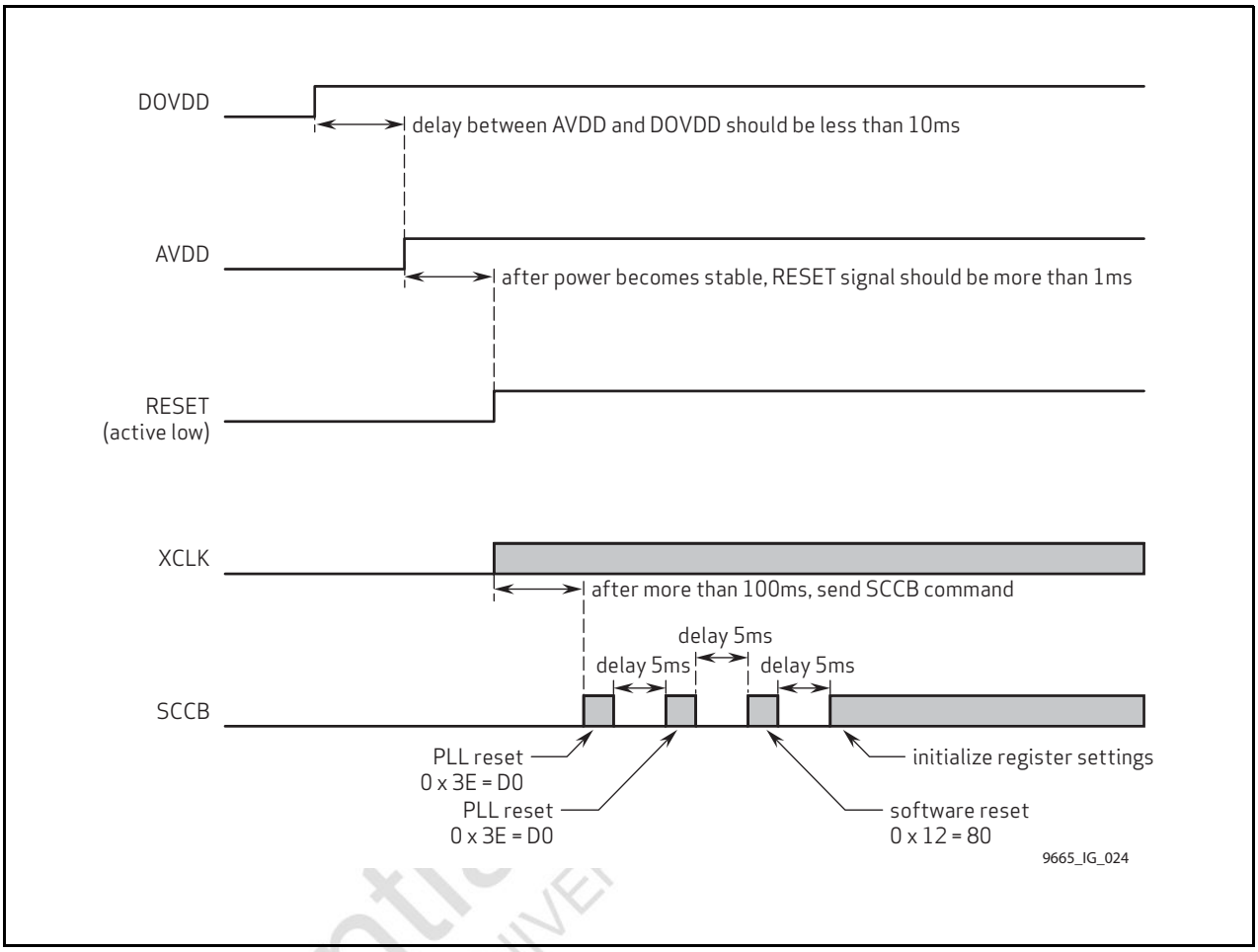
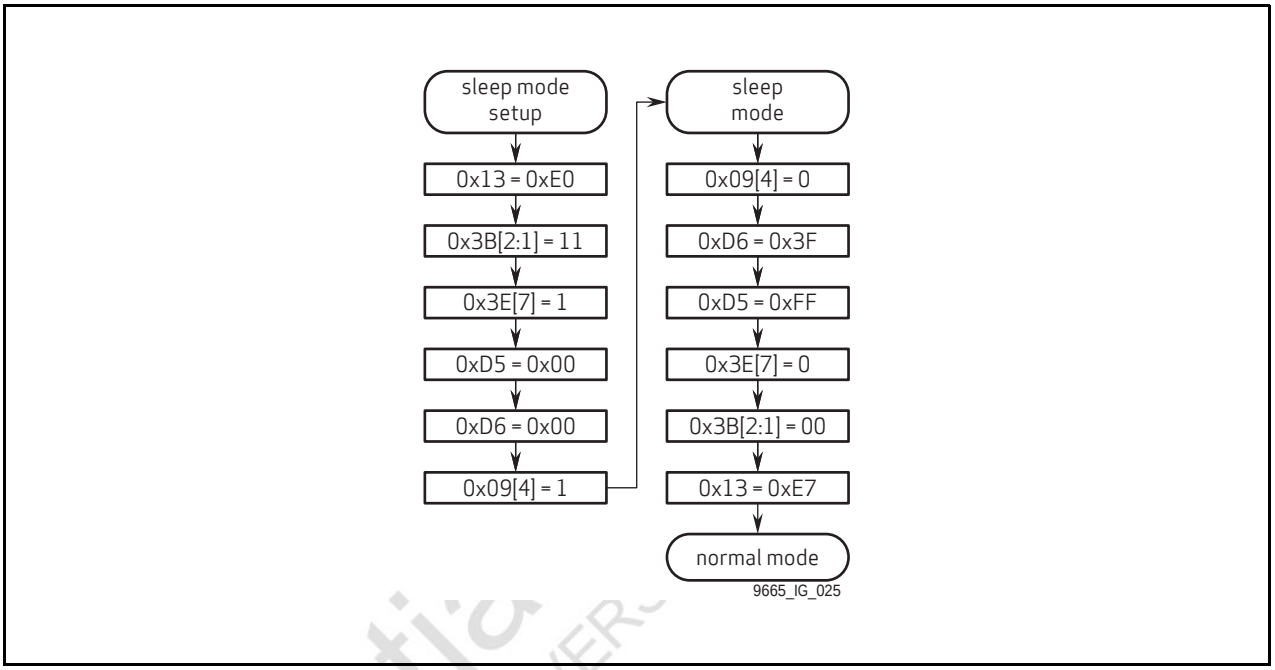
Figure 9-2 Power ON/OFF Timing



9.2.2 Sleep Mode

The OV9665 supports a sleep mode that turns off most of its function blocks yet keeps the SCCB block working. The standby current in this condition will typically be less than 1 mA. The user can wake up the OV9665 by sending a value to a particular register. Figure 9-3 shows the sleep mode setup and wake up procedure.

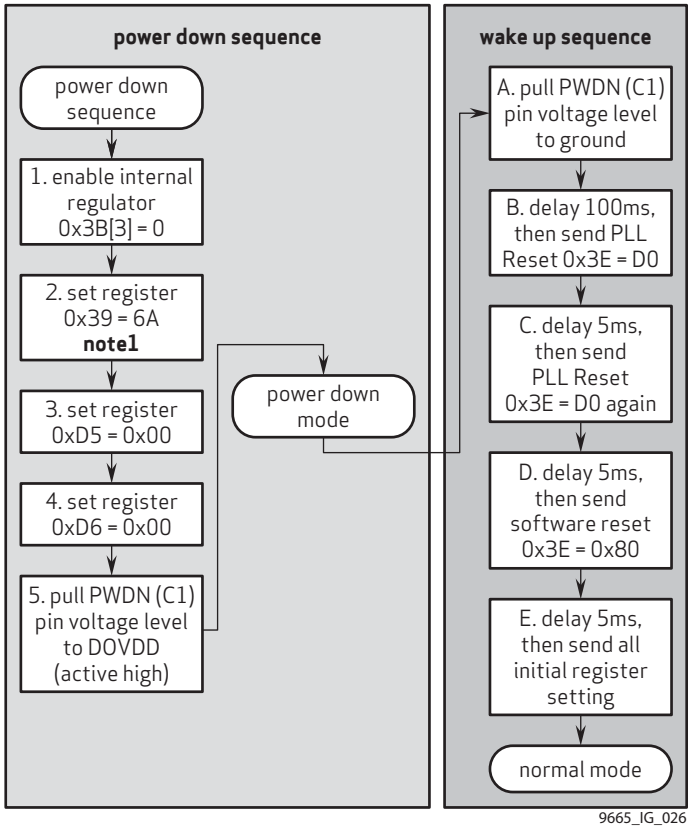
Figure 9-3 Sleep Mode Setup and Wake Up Procedure



9.2.3 Power Down Mode

The OV9665 supports a power down mode that turns off most function blocks including the timing circuit. The standby current for this condition is typically less than 20 µA. The user must pull up the power down pin (C1) voltage level to VDD-IO in order to enter power down mode and pull down this pin to ground level in order to exit power down mode. It is highly recommend that the user pull down all sensor output pins (D0~D9, VSYNC, HREF, PCLK) to ground level during power down mode. This may avoid unnecessary floating power loss during power down mode. Figure 9-4 shows the power down mode init and wake up procedure.

Figure 9-4 Power Down Mode Initialization and Wake Up Procedure



note 1 if DOVDD>2.5V, set 0x39=6A. if DOVDD<2.5V, set 0x39=42.

9.3 Register Set

Table 9-3 provides a list and description of the Device Control registers contained in the OV9665. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses for the OV9665 are 0x60 for write and 0x61 for read.

For factory-recommended settings, contact your local OmniVision FAE.

Note: All registers shown as reserved have no function or are very sensitive analog circuit references. Use OmniVision reference values (not default values).

Table 9-3. Device Control Register List (Sheet 1 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7:0]: Gain setting • Range: 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0])/16) ***NOTE**: Set COM8[2] = 0 to disable AGC.*
01	BLUE	40	RW	Blue Gain Control
02	RED	40	RW	Blue Gain Control
03	COM1	03	RW	Common Control 1 Bit[7:6]: Dummy frame control - effective when register bit COM6[3] = 1 (0x0F) (night mode enable) 00: Not used 01: Allow 1 dummy frame 10: Allow 3 dummy frames 11: Allow 7 dummy frames Bit[5:4]: Reserved Bit[3:2]: Vertical window end line control 2 LSBs (see register VEND for 8 MSBs) Bit[1:0]: Vertical window start line control 2 LSBs (see register VSTRT for 8 MSBs)
04	REG04	28	RW	Register 04 Bit[7]: Horizontal mirror (effective when register bit REG33[3] = 1 (0x33) Bit[6]: Vertical flip Bit[5:2]: Reserved Bit[1:0]: AEC low 2 LSBs – AEC[1:0] (see register AEC for AEC[9:2] and register REG45[5:0] for AEC[15:10])
05	REG05	00	RW	Register 05 Bit[7:3]: Reserved Bit[2:0]: UV adjust slope[5:3] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG60[2:0] (0x60).

Table 9-3. Device Control Register List (Sheet 2 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
06	REG06	10	RW	Register 06 Bit[7:6]: Dummy line insertion beginning gain 00: 2x 01: 4x 10: 8x 11: 8x Bit[5:0]: Reserved
07	REG07	A4	RW	Register 07 Bit[7]: Reserved Bit[6:4]: VS start point Bit[3]: Reserved Bit[2:0]: VS width
08	RSVD	XX	–	Reserved
09	COM2	00	RW	Common Control 2 Bit[7:5]: Always precharge Bit[4]: Sleep mode enable (SCCB standby enable) 0: Normal mode 1: Sleep mode Bit[3]: Pin D0 output control 0: D0 1: STROBE Bit[2]: Reserved Bit[1:0]: Output drive current select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PID	96	R	Product ID Number MSB (Read only)
0B	VER	63	R	Product ID Number LSB (Read only)
0C	COM3	38	RW	Common Control 3 Bit[7:3]: Reserved Bit[2]: Manually set banding 0: 60 Hz 1: 50 Hz Bit[1]: Auto set banding Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D	REG0D	80	RW	Register 0D Bit[7:5]: Reserved Bit[4]: DSP clock selection 0: For SXGA mode 1: For VGA 30 mode Bit[3:0]: Reserved

Table 9-3. Device Control Register List (Sheet 3 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0E	RSVD	XX	–	Reserved
0F	COM6	46	RW	Common Control 6 Bit[7:4]: Reserved Bit[3]: Night mode enable 0: Disable 1: Enable Bit[2:0]: Reserved
10	AEC	00	RW	Automatic Exposure Control - AEC[9:2] (see register REG45[5:0] for AEC[15:10] and register REG04 for AEC[1:0]) AEC[15:0]: Exposure time TEX = tLINE x AEC[15:0] ***NOTE**: The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period*
11	CLKRC	80	RW	Clock Rate Control Bit[7:6]: Reserved Bit[5:0]: Clock divider for frame rate adjustment CLK = XVCLK / (decimal value of CLKRC[5:0] + 1)
12	COM7	00	RW	Common Control 7 Bit[7]: SRST 1: Initiates soft reset. All registers are set to factory default values after which the chip resumes normal operation Bit[6:5]: Resolution selection 00: SXGA (full size) mode 01: Not used 10: VGA mode 11: Not used Bit[4:3]: Reserved Bit[2]: Zoom mode Bit[1:0]: Reserved

Table 9-3. Device Control Register List (Sheet 4 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COM8	E7	RW	Common Control 8 Bit[7]: Reserved Bit[6]: AEC step size limit Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure to 1/120s or 1/100s Bit[4:3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14	COM9	40	RW	Common Control 9 Bit[7:5]: AGC gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: Not used 110: Not used 111: Not used Bit[4]: Reserved Bit[3]: Exposure time can be less than limitation of banding filter (1/120s or 1/100s) when light is too strong Bit[2]: Data output format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than the exposure gap Bit[0]: Reserved
15	COM10	00	RW	Common Control 10 Bit[7:6]: Reserved Bit[5]: PCLK output selection (works on row data output) 0: PCLK always output 1: PCLK output qualified by HREF Bit[4:2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: Reserved
16	GREEN	40	RW	Green Gain Control

Table 9-3. Device Control Register List (Sheet 5 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
17	HREFST	0D	RW	Horizontal Window Start 8 MSBs (3 LSBs in register REG32[2:0]) Bit[10:0]: Select beginning of horizontal window, each LSB represents two pixels
18	HREFEND	5D	RW	Horizontal Window End 8 MSBs (3 LSBs in register REG32[5:3]) Bit[10:0]: Select end of horizontal window, each LSB represents two pixels
19	VSTRT	01	RW	Vertical Window Line Start 8 MSBs (2 LSBs are in register COM1[1:0]) Bit[9:0]: Select start of vertical window, each LSB represents two scan lines
1A	VEND	82	RW	Vertical Window Line End 8 MSBs (2 LSBs are in register COM1[3:2]) Bit[9:0]: Select end of vertical window, each LSB represents two scan lines
1B	RSVD	XX	–	Reserved
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	REG1E	F9	RW	Register 1E Bit[7]: White defect pixel correction 0: Disable 1: Enable Bit[6]: Black defect pixel correction 0: Disable 1: Enable Bit[5:0]: Reserved
1F-23	RSVD	XX	–	Reserved
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC Operation AEC/AGC value decreases in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC Operation AEC/AGC value increases in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Thresholds (effective only in AEC/AGC fast mode) Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]
27-29	RSVD	XX	–	Reserved

Table 9-3. Device Control Register List (Sheet 6 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2A	REG2A	00	RW	Common Control 2A Bit[7:4]: Line interval adjustment value 4 MSBs (see register REG2B[7:0] for 8 MSBs) Bit[3:2]: HSYNC timing end point adjustment 2 MSBs (see register HEDY for 8 LSBs) Bit[1:0]: HSYNC timing start point adjustment 2 MSBs (see register HSDY for 8 LSBs)
2B	REG2B	00	RW	Common Control 2B Bit[7:0]: Line interval adjustment value 8 LSBs (see register REG2A[7:4] for 4 MSBs) The frame rate will be adjusted by changing the line interval. Each LSB will add 1/1520 Tframe in SXGA and 1/760 Tframe in VGA mode to the frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width 8 LSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x tline. Each LSB count will add 1 x tline to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse Width 8 MSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x tline. Each MSB count will add 256 x tline to the VSYNC active period.
2F	YAVG	00	R	Luminance Average (this register will auto update)
30	HSDY	08	RW	HSYNC Position and Width Start 8 LSBs This register and register REG2A[1:0] define the HSYNC start position. Each LSB will shift the HSYNC starting point by a 2 pixel period.
31	HEDY	20	RW	HSYNC Position and Width End 8 LSBs This register and register REG2A[3:2] define the HSYNC end position. Each LSB will shift the HSYNC starting point by a 2 pixel period.
32	REG32	24	RW	Common Control 32 Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position 3 LSBs (8 LSBs in register HREFEND) Bit[2:0]: Horizontal window start position 3 LSBs (8 LSBs in register HREFST)
33	REG33	C0	RW	Register 33 Bit[7:4]: Reserved Bit[3]: Mirror function (used with register bit REG04[7] (0x04)) Bit[2:0]: Reserved

Table 9-3. Device Control Register List (Sheet 7 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
34-35	RSVD	XX	–	Reserved
36	REG36	94	RW	Register 36 Bit[7:6]: Reserved Bit[5]: Auto de-noise divider value 0: 128 1: 64 Bit[4:0]: Reserved
37-3A	RSVD	XX	–	Reserved
3B	REG3B	00	RW	Power Control 3B Bit[7:4]: Reserved Bit[3]: Bypass internal regulator 0: Use internal regulator to generate V_{DD-D} power 1: Bypass internal regulator (V_{DD-D} power needs to be provided by an external source) Bit[2:0]: Reserved
3C	RSVD	XX	–	Reserved
3D	REG3D	3C	RW	Common Control 3D Bit[7:6]: Reserved Bit[5:0]: PLL divider f_{CLK} = XCLK × (0x40 – REG3D[5:0]) / 8 / (CLKRC[5:0] + 1)
3E	REG3E	50	RW	Register 3E Bit[7]: PLL bypass option 0: Enable PLL 1: Bypass PLL Bit[6:0]: Reserved
3F-40	RSVD	XX	–	Reserved
41	REG41	00	RW	Register 41 Bit[7:5]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG5B[4:2] (0x5B). Bit[4:0]: Reserved
42	RSVD	XX	–	Reserved
43	REG43	00	RW	Register 43 Bit[7]: 9-zone average AEC option 0: Full size and VGA30 1: Other size Bit[6:0]: Reserved

Table 9-3. Device Control Register List (Sheet 8 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
44	REG44	00	RW	Register 44 Bit[7]: Reserved Bit[6]: Vertical line divider - works in scaling mode 0: No divider 1: Divider Bit[5:4]: Reserved Bit[3]: Vertical line divider number - works in scaling mode 0: Divide vertical line by 2 1: Divide vertical line by 4 Bit[2:0]: Reserved
45	REG45	00	RW	Register 45 Bit[7:6]: AGC[9:8], AGC highest gain control Bit[5:0]: AEC[15:10], AEC 6 MSBs (see register AEC for AEC[9:2] and register REG04 for AEC[1:0]).
46	FLL	00	RW	Frame Length Adjustment 8 LSBs Each bit will add 1 horizontal line timing in frame
47	FLH	00	RW	Frame Length Adjustment 8 MSBs Each bit will add 256 horizontal lines timing in frame
48-4A	RSVD	XX	–	Reserved
4B	COM22	00	RW	Common Control 22 Bit[7:0]: Flash light control
4C-4D	RSVD	XX	–	Reserved
4E	COM25	05	RW	Common Control 25 Bit[7:6]: 50 Hz banding AEC 2 MSBs Bit[5:4]: 60 Hz banding AEC 2 MSBs Bit[3:0]: Reserved
4F	BD50	9E	RW	50 Hz Banding AEC 8 LSBs (see register COM25[7:6] for 2 MSBs)
50	BD60	84	RW	60 Hz Banding AEC 8 LSBs (see register COM25[5:4] for 2 MSBs)
51-59	RSVD	XX	–	Reserved
5A	REG5A	57	RW	Register 5A Bit[7:4]: 50 Hz banding maximum AEC step Bit[3:0]: 60 Hz banding maximum AEC step
5B	REG5B	20	RW	Register 5B Bit[7:5]: Reserved Bit[4:2]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG41[7:5] (0x41). Bit[1:0]: Reserved

Table 9-3. Device Control Register List (Sheet 9 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
5C	REG5C	00	RW	Register 5C Bit[7]: Average AEC option 0: 9-zone average AEC 1: Full average AEC Bit[6:0]: Reserved
5D	REG5D	55	RW	9-zone Average Weight Option - AVGsel[7:0]
5E	REG5E	55	RW	9-zone Average Weight Option - AVGsel[15:8]
5F	REG5F	21	RW	Register 5F Bit[7:2]: Reserved Bit[1:0]: 9-zone average weight option - AVGsel[17:16]
60	REG60	80	RW	Register 60 Bit[7:3]: Reserved Bit[2:0]: UV adjust slope[2:0] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG05[2:0] (0x05).
61	HISTO_LOW	80	RW	Histogram Algorithm Low Level Bit[7:0]: Histogram algorithm low level
62	HISTO_HIGH	90	RW	Histogram Algorithm High Level Bit[7:0]: Histogram algorithm high level
63	REG63	01	RW	Register 63 Bit[7:6]: Reserved Bit[5]: Raw data output format (valid when register REG07[1:0] is 2'b11) 0: DSP function (AWB and Gamma) works on Raw output data 1: DSP functions do not work on Raw output data Bit[4:0]: Reserved
64	REG64	20	RW	Register 64 Bit[7]: BLC line select 0: SXGA 1: Other resolution Bit[6:0]: Reserved
65	REG65	10	RW	Register 65 Bit[7:2]: Reserved Bit[1:0]: UV adjustment gain threshold 2 value[4:3]
66	REG66	00	RW	Register 66 Bit[7:5]: UV adjustment gain threshold 2 value[2:0] Bit[4:0]: Reserved
67-69	RSVD	XX	–	Reserved

Table 9-3. Device Control Register List (Sheet 10 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
6A	REG6A	24	RW	Register 6A Bit[7:5]: Reserved Bit[4]: FIFO manual option (works with scaling function) 0: Auto mode 1: Manual mode Bit[3:0]: Reserved
6B-74	RSVD	XX	–	Reserved
75	REG75	D0	RW	Histogram-based AEC Lower Limit of Probability - LPH
76	REG76	D0	RW	Histogram-based AEC Upper Limit of Probability - UPL
77	REG77	F0	RW	Histogram-based AEC Probability Threshold for LRL - TPL
78	REG78	90	RW	Histogram-based AEC Probability Threshold for HRL - TPH
79	REG79	E5	RW	Register 79 Bit[7:2]: High nibble of luminance thrreshold for AEC/AGC speed control Bit[3:0]: Low nibble of luminance threshold for AEC/AGC speed control
7A-7B	RSVD	XX	–	Reserved
7C	REG7C	05	RW	Register 7C Bit[7]: AEC option 0: Average-based AEC 1: Histogram-based AEC Bit[6:0]: Reserved
7D	REG7D	00	RW	Lens Correction Center Coordinates X Bit[7]: Sign bit Bit[6:0]: X-coordinate for lens correction center
7E	REG7E	00	RW	Lens Correction Center Coordinates Y Bit[7]: Sign bit Bit[6:0]: Y-coordinate for lens correction center
7F	REG7F	18	RW	Radius of the Circular Section Where Lens Correction Is Not Needed
80	REG80	04	RW	Lens Correction Blue Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
81	REG81	04	RW	Lens Correction Red Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
82	REG82	04	RW	Lens Correction Green Gain Parameter

Table 9-3. Device Control Register List (Sheet 11 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
83	LC7	06	RW	Bit[7:3]: Reserved Bit[2]: Lens correction control select 0: Use register REG82 (0x82) for gain parameter for R, G, and B channels 1: Use register REG82 (0x82) for green gain parameter, register REG80 (0x80) for blue gain parameter, and register REG81 (0x81) for red gain parameter Bit[1]: Reserved Bit[0]: Lens correction enable switch 0: Disable 1: Enable
84	REG84	86	RW	De-noise Level
85	REG85	E7	RW	Register 85 Bit[7:5]: Reserved Bit[4]: RAW/YUV (only works when register bits REGD7[1:0] (0xD7) = 0'b10) Bit[3]: FIFO enable (works with scaling function) Bit[2]: Gamma enable option 0: Disable 1: Enable Bit[1]: AWB gain Bit[0]: AWB
86	REG86	86	RW	Register 86 Bit[7:6]: Reserved Bit[5]: Maximum AWB gain select 0: 2x maximum AWB gain 1: 4x maximum AWB gain Bit[4:0]: Reserved
87	RSVD	XX	–	Reserved
88	REG88	A2	RW	Register 88 Bit[7:5]: AWB option 0: Advanced AWB 1: Simple AWB Bit[6:0]: Reserved
89-9A	RSVD	XX	–	Reserved
9B	GAM1	04	RW	Gamma Curve Segment 1 End Point
9C	GAM2	07	RW	Gamma Curve Segment 2 End Point
9D	GAM3	10	RW	Gamma Curve Segment 3 End Point
9E	GAM4	28	RW	Gamma Curve Segment 4 End Point
9F	GAM5	36	RW	Gamma Curve Segment 5 End Point
A0	GAM6	44	RW	Gamma Curve Segment 6 End Point

Table 9-3. Device Control Register List (Sheet 12 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
A1	GAM7	52	RW	Gamma Curve Segment 7 End Point
A2	GAM8	60	RW	Gamma Curve Segment 8 End Point
A3	GAM9	6C	RW	Gamma Curve Segment 9 End Point
A4	GAM10	78	RW	Gamma Curve Segment 10 End Point
A5	GAM11	8C	RW	Gamma Curve Segment 11 End Point
A6	GAM12	9E	RW	Gamma Curve Segment 12 End Point
A7	GAM13	BB	RW	Gamma Curve Segment 13 End Point
A8	GAM14	D2	RW	Gamma Curve Segment 14 End Point
A9	GAM15	E5	RW	Gamma Curve Segment 15 End Point
AA	SLOP	24	RW	Gamma Curve Segment 15 Slope
AB	REGAB	E7	RW	Register AB Bit[7:4]: Reserved Bit[3]: Scaling enable option 0: Disable 1: Enable Bit[2]: Sharpness enable option 0: Disable 1: Enable Bit[1]: De-noise enable option 0: Disable 1: Enable Bit[0]: Reserved
AC	REGAC	02	RW	De-noise Offset Limit in Auto De-noise Mode
AD	REGAD	25	RW	Register AD Bit[7:5]: Reserved Bit[4:0]: Sharpness value when GAIN < 2x
AE	REGAE	20	RW	Register AE Bit[7:3]: Reserved Bit[2]: Sharpness threshold double Bit[1:0]: Reserved
AF	RSVD	XX	–	Reserved
B0	REGB0	43	RW	Register B0 Bit[7]: Manual de-noise mode enable 0: Auto de-noise mode 1: Manual de-noise Bit[6:0]: Reserved
B1-B6	RSVD	XX	–	Reserved

Table 9-3. Device Control Register List (Sheet 13 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
B7	REGB7	00	RW	Register B7 Bit[7]: Scaling mode vertical output size bit[0] (11 bits total). For others, refer to registers REGB8[7:6] and REGBC Bit[6:4]: Scaling mode horizontal output size bit[2:1] (11 bits total). For others, refer to register REGBB Bit[3:0]: Reserved
B8	REGB8	00	RW	Register B8 Bit[7:6]: Scaling mode vertical output size bit[2:1] (11 bits total). For others, refer to registers REGB7[7] and REGBC Bit[5:3]: Scaling mode vertical input size bit[2:0] (11 bits total). For others, refer to register REGBA Bit[2:0]: Scaling mode horizontal input size bit[2:0] (11 bits total). For others, refer to register REGB9
B9	REGB9	A0	RW	Scaling Mode Horizontal Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[2:0]
BA	REGBA	80	RW	Scaling Mode Vertical Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[5:3]
BB	REGBB	A0	RW	Scaling Mode Horizontal Output Size[10:3] (11 bits total). For others, refer to registers REGB8[7:6] and REGB7[6:4]
BC	REGBC	80	RW	Scaling Mode Vertical Output Size[10:3] (11 bits total). For others refer to registers REGB7[7] and REGB8[7:6]
BD	CMX1	05	RW	Color Matrix Parameter 1
BE	CMX2	16	RW	Color Matrix Parameter 2
BF	CMX3	05	RW	Color Matrix Parameter 3
				Y = (CMX1 × R + CMX2 × G + CMX3 × B) / 32
C0	CMX4	07	RW	Color Matrix Parameter 4
C1	CMX5	18	RW	Color Matrix Parameter 5
C2	CMX6	1F	RW	Color Matrix Parameter 6
				U = (CMX4 × R + CMX5 × G + CMX6 × B) / 32
C3	CMX7	2B	RW	Color Matrix Parameter 7
C4	CMX8	2B	RW	Color Matrix Parameter 8
C5	CMX9	00	RW	Color Matrix Parameter 9
				V = (CMX7 × R + CMX8 × G + CMX9 × B) / 32
C6	CMX10	98	RW	Color Matrix Control 1 Bit[7]: Sign bit of CMX8 Bit[6]: Sign bit of CMX7 Bit[5]: Sign bit of CMX6 Bit[4]: Sign bit of CMX5 Bit[3]: Sign bit of CMX4 Bit[2]: Sign bit of CMX3 Bit[1]: Sign bit of CMX2 Bit[0]: Sign bit of CMX1

Table 9-3. Device Control Register List (Sheet 14 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
C7	CMX11	10	RW	Color Matrix Control 2 Bit[7]: Sign bit of CMX9 Bit[6]: Reserved Bit[5]: Auto UV adjustment enable 0: Disable 1: Enable Bit[4]: Special Digital Effects (SDE) enable 0: Disable 1: Enable Bit[3:0]: Reserved
C8	REGC8	02	RW	Register C8 Bit[7]: Fixed Y output value 0: Disable 1: Enable Bit[6]: Negative output 0: Disable 1: Enable Bit[5]: Gray scale output 0: Disable 1: Enable Bit[4]: Fixed V output value 0: Disable 1: Enable Bit[3]: Fixed U output value 0: Disable 1: Enable Bit[2]: Contrast function enable 0: Disable 1: Enable Bit[1]: Color saturation function enable 0: Disable 1: Enable Bit[0]: Hue adjustment enable 0: Disable 1: Enable
C9	REGC9	80	RW	Hue Adjustment Cosine Parameter
CA	REGCA	00	RW	Hue Adjustment Sine Parameter
CB	REGCB	40	RW	Saturation U Gain Value
CC	REGCC	40	RW	Saturation V Gain Value
CD	REGCD	80	RW	Fixed U Output Value
CE	REGCE	80	RW	Fixed V Output Value

Table 9-3. Device Control Register List (Sheet 15 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
CF	REGCF	00	RW	Y Offset Value Y' = [(Y + Yoffset) × Ygain] + Ybrightness when enabling contrast function
D0	REGD0	20	RW	Y Gain Value
D1	REGD1	00	RW	Y Brightness Value
D2	REGD2	00	RW	Register D2 Bit[7]: Auto UV adjustment enable Bit[6:5]: Reserved Bit[4:0]: UV adjust offset value after gain threshold 2
D3	REGD3	00	RW	FIFO Delay Timing Configuration (works with scaling function)
D4	RSVD	XX	–	Reserved
D5	REGD5	00	RW	IO Pad Direction Control Bit[7]: D7 direction control 0: Input 1: Output Bit[6]: D6 direction control 0: Input 1: Output Bit[5]: D5 direction control 0: Input 1: Output Bit[4]: D4 direction control 0: Input 1: Output Bit[3]: D3 direction control 0: Input 1: Output Bit[2]: D2 direction control 0: Input 1: Output Bit[1]: D1 direction control 0: Input 1: Output Bit[0]: D0 direction control 0: Input 1: Output
D6	REGD6	00	RW	Register D6 Bit[7:2]: Reserved Bit[1]: D9 direction control 0: Input 1: Output Bit[0]: D8 direction control 0: Input 1: Output

Table 9-3. Device Control Register List (Sheet 16 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
D7	REGD7	10	RW	Register D7 Bit[7:5]: Reserved Bit[4]: YU swap function 0: U Y V Y 1: Y U Y V Bit[3]: Data pins swap function (changes MSB to D0 and LSB to D9) - works in YUV mode 0: Disable 1: Enable Bit[2]: HREF to HSYNC 0: Output HREF signal 1: Output HSYNC signal Bit[1:0]: Data output format selection 00: YUV output 01: RGB output 10: ISP RAW output 11: RAW output
D8	REGD8	C4	RW	Register D8 Bit[7:6]: Reserved Bit[5]: HREF/HSYNC negative output 0: Positive output 1: Negative output Bit[4]: Reserved Bit[3]: CCIR656 output selection 0: Disable 1: Enable Bit[2]: Reserved Bit[1:0]: RGB data output format selection (effective when register bits REGD7[1:0] = 01) 00: Not used 01: RGB565 10: RGB555 11: RGB444
D9	REGD9	64	RW	Register D9 Bit[7:4]: Sharpness value when 4x < GAIN < 8x Bit[3:0]: Sharpness value when 2x < GAIN < 4x
DA	REGDA	86	RW	Register DA Bit[7:4]: Sharpness value when 16x < GAIN Bit[3:0]: Sharpness value when 8x < GAIN < 16x
DB-DE	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Contact OmniVision Technologies for reference register settings.				

10 Prototyping and Evaluation Modules

OmniVision Technologies Inc. supplies prototyping and evaluation modules to demonstrate operation of the associated CAMERACHIP products, as well as to demonstrate associated companion backend processor, where required.

10.1 OV9665EAA Prototyping Module

The OV9665EAA prototyping module is used for general design-in and evaluation purposes. The module provides a simple 32-pin header-connector interface to the relevant I/O and control registers in the OV9665 CAMERACHIP sensor. The module includes the necessary sensor, lens/holder, a few capacitors, and resistors.

The OV9665EAA prototyping module can be directly connected to any companion backend processor solution or system interface. The header-connector interface allows for access to the 10-bit digital output data, PCLK, vertical sync, horizontal sync and SCCB signals. The backend interface can use the Serial Camera Control Bus (SCCB) interface software to adjust the control register values.

10.2 OV9665ECX USB 2.0 Evaluation Module

The OV9665ECX USB2.0 evaluation module is provided so that potential customers may evaluate both the live video function of the CAMERACHIP sensor as well as the SCCB control interface software. The OV9665 CAMERACHIP sensor output is a RGB raw data or YUV stream connected to a USB 2.0 controller operating at a high-speed bus data rate (480 Mbps).

Using a high performance computer system with a USB 2.0 host (cannot guarantee for every system), the OV9665 USB module will stream video in SXGA format (1280x1028 at 15 fps) or VGA format (640x480 at 30 fps). This configuration requires a Windows® 2000 or XP operating system. Additionally, the SCCB software allows the evaluator to adjust the image characteristics in real-time.

11 Lens selection

The OV9665 is a 1/5.5-inch format CAMERACHIP sensor that is compatible with numerous lenses in the market. The key considerations in lens selection are lens quality and resultant cost. OmniVision Technologies, Inc. has qualified several lens suppliers for the various formats, sizes, and quality of lenses available. OmniVision has developed a Lens Supplier Partner List to complement our CAMERACHIP products. This listing is available at http://www.ovt.com on the Partners page. Contact your local OmniVision field applications engineer (FAE) for recommended OV9665 lenses.

12 OV9665 Bug List

None as of this revision.

Appendix A Reference SCCB Settings

Contact your local OmniVision FAE for updated reference register settings.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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