

DEPARTAMENTO DE ENGENHARIA ELECTROTÉCNICA -FCT/UNL CONVERSORES DE SINAL –NYQUIST RATE ADCS (Nuno Paulino, DEEC, 2025)

Analysis of an ADC using a high-level model

The objective of this project is to develop a high-level model for a *nbit* SAR ADC. This model should accurately describe the behaviour of the ADC described in the paper,

"A 6.94-fJ/Conversion-Step 12-bit 100-MS/s Asynchronous SAR ADC Exploiting Split-CDAC in 65-nm CMOS," in IEEE Access, vol. 9, pp. 77545-77554, 2021 Using this high-level model, it should be possible to obtain the digital output code of the ADC for any given input voltage. The model should include capacitor mismatch errors, parasitic capacitance errors and comparator offset errors.

- a) Carefully read the paper to understand the operation of the ADC (Fig. 1). If necessary, obtain and read papers cited by this paper.
- b) Analyze the capacitor array circuits (shown in Fig. 1 in the paper) to obtain the expression of the capacitor array voltages (V_{xp} and V_{xn}) as a function of Δv_{in} , the control bits and the capacitors values. Use the charge conservation principle in your analysis. Suggestion: first analyze the MSB sub-array separately.
- c) Using the previous expression, write a Matlab/Octave model of the behavior of this SAR ADC, including the offset error of the comparator. Note that the SAR ADC uses two capacitor arrays (split into LSB and MSB arrays) and fully differential signals. Include random errors into the capacitors' values and into the comparator's offset voltage.
- d) Use the previous model to calculate the transfer function of the ADC $(d_{out}(v_{in}))$ and compute the transition voltages of the ADC for a given set of errors.
- e) Use the model to measure the linearity of the ADC using INL, DNL and FFT.
- f) Run Monte Carlo analysis of the ADC model to determine the sensitivity of the ADC to mismatch errors between the different components.
- g) Compare your results with the results reported in the paper.
- h) (optional) Estimate the minimum area and power dissipation of the DAC required for the ADC to have an expected linearity of 10.5 bits. Use the mismatch error estimation provided in Fig. 4 of the paper.