

Received March 19, 2021, accepted May 6, 2021, date of publication May 12, 2021, date of current version June 2, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3079406

A 6.94-fJ/Conversion-Step 12-bit 100-MS/s Asynchronous SAR ADC Exploiting Split-CDAC in 65-nm CMOS

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This work was supported in part by NSFC under Grant 62074038 and Grant 61934008, and in part by Fudan University under Grant JIH1233034.

ABSTRACT This paper presents a 12-bit 100-MS/s asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) for low-power wireless and imaging systems. A split-capacitor digital-to-analog converter (CDAC) structure is adopted for reducing the core area and improving the sampling speed. The linearity of the CDAC is calibrated by programming the least-significant-bits (LSBs) dummy capacitor. The unit capacitor in the CDAC array is customized for higher symmetry and reducing their mismatch. Our SAR ADC is based on asynchronous logic, and its timing is controlled by a delaying block in the critical path. The prototype is fabricated in a 65-nm CMOS process with a 1.2 V supply and occupies an active area of 0.029 mm². With a 100-MS/s sampling rate, the measured ENOB scores 10.17 bits for 1.5 MHz input with a figure-of-merit (FoM) of 6.94 fJ/conversion-step. It can achieve 8.83 bits for Nyquist input signal.

INDEX TERMS Successive approximation register (SAR) analog-to-digital converter (ADC), CMOS, split-CDAC, customized unit capacitor, asynchronous logic, figure-of-merit (FoM).

I. INTRODUCTION

Wireless system featuring ultra-low power consumption and wide bandwidth for IoT has recently attracted more attention. The limited battery capability and long-time working force the above system to urgently need the analog-to-digital converters (ADC) as the key building blocks with small core area and low power. Successive approximation register (SAR) ADC is considered as an appropriate candidate for its better power efficiency [1]–[6]. However, it is challenging to achieve high speed while maintaining high resolution. Many efforts have been made to improve the performance of the SAR ADC. Time-interleaving SAR ADCs [7], [8] can enhance the sampling rate (F_S) by increasing the number of the parallel channel, but the mismatch between each channel cannot be ignored. Coarse-fine ADCs [9], [10] relieve reference constraints and speed up the conversion rate by using

The associate editor coordinating the review of this manuscript and approving it for publication was Xi Zhu¹.

a fast-coarse SAR, but it is hard to overcome the mismatch between coarse and fine SAR.

Differently, asynchronous SAR ADC employs the clock-generating logic circuit to raise the conversion speed so that the high-speed synchronous clock can be removed [11]. The redundant technique [12] adds extra redundant bits to reduce the settling requirement and compensate for decision-error during bit-cycling. On the other hand, decreasing the capacitance can reduce the settling time with the given minimum unit capacitor and thus enhance the sampling speed [13]. Using the split-CDAC with the bridge capacitor instead of the binary CDAC can greatly reduce the total number of capacitors, but some compensation techniques must be applied to improve the linearity of the split-CDAC [14].

This paper presents a 12-bit 100-MS/s asynchronous SAR ADC with split-CDAC topology to address the above issues with the enhanced linearity. The linearity of the split-CDAC is sensitive to the parasitic capacitance, especially that induced by the bridge capacitor, we theoretically analyze the linearity

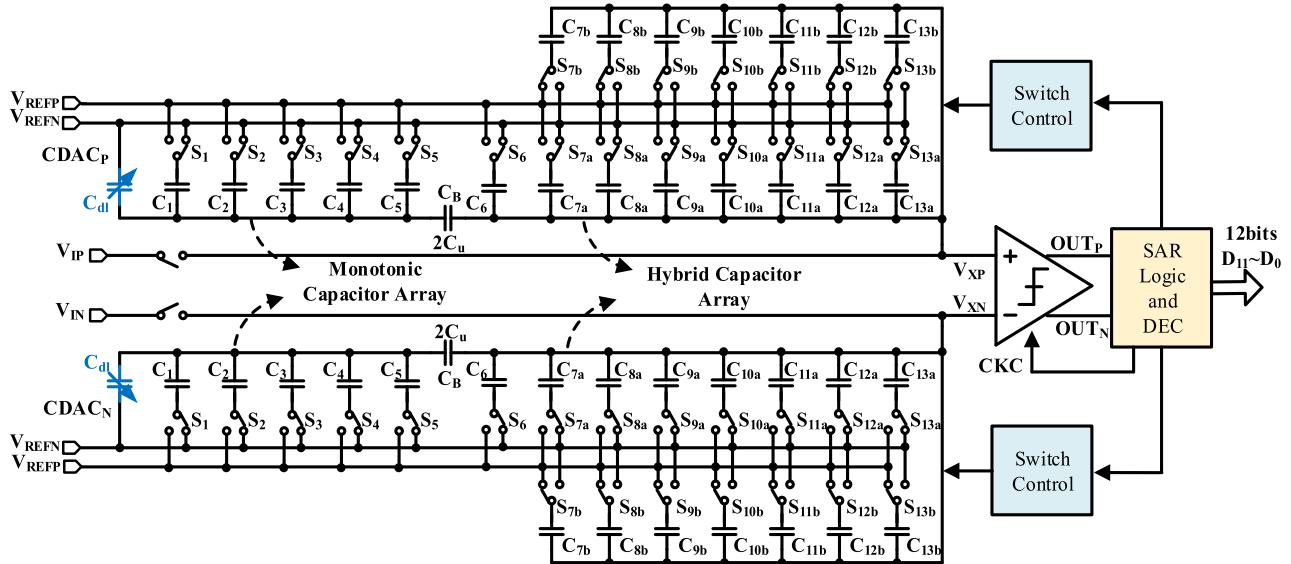


FIGURE 1. The top architecture of the proposed asynchronous SAR ADC.

of the split-CDAC, and then propose a programmable-dummy-capacitor method to improve its linearity. Furthermore, because the Metal-Oxide-Metal (MOM) capacitors provided by the 65- nm CMOS process are not symmetrical and large parasitic capacitance is induced during the layout routing. Thus, we design a customized symmetrical unit capacitor by virtue of the parasitic capacitance between M4-M7 layers. To implement the robust SAR control logic, a tunable delay block is merged to the critical signal path to properly adjust the time delay.

This paper is organized as follows. Section II introduces the top architecture of the proposed asynchronous SAR ADC and describes its working principle. Section III details the circuit implementation consideration, involving the linearity analysis and mismatch analysis of the split-CDAC, and also gives the realization of the SAR control logic. Section IV discusses the key blocks, including the sampling switch, dynamic comparator and digital error correction (DEC) circuit. The measurement results and the comparison with prior works are in Section V. Section VI summarizes the conclusion.

II. ADC TOP ARCHITECTURE

Fig. 1 illustrates the top architecture of our asynchronous SAR ADC, incorporating the bootstrapped switches, capacitor array, dynamic comparator, and asynchronous SAR control logic. Both the supply voltage and positive reference voltage of our SAR ADC are 1.2 V, while the negative reference voltage is GND. The input full swing signal is $2V_{pp,diff}$.

The operating principle of our asynchronous SAR ADC is divided into sampling and conversion. The sampling period is a quarter of one clock period, and the remaining time is for the conversion. It incorporates the top-plate sampling topology in which the sampling front-end is connected to the comparator input, thus the comparator starts to perform the first-bit

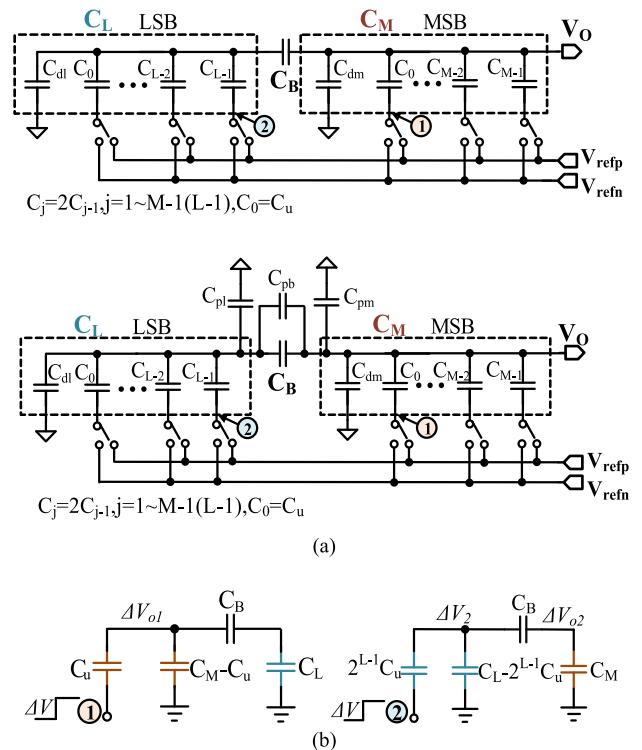


FIGURE 2. (a) Two-stage bridge capacitor array without and with the parasitic capacitor. (b) Applying a voltage change of ΔV to nodes 1 and 2.

decision step after the sampling phase is finished. Therefore, an $(N-1)$ bits CDAC can meet the quantization requirements for an N bits SAR ADC, which can save half of the capacitors [15]. During the data conversion phase, the comparison result of the comparator is used to control the flip direction of the bottom plate of the capacitor array. Our SAR ADC adopts the asynchronous logic control and the clock of the

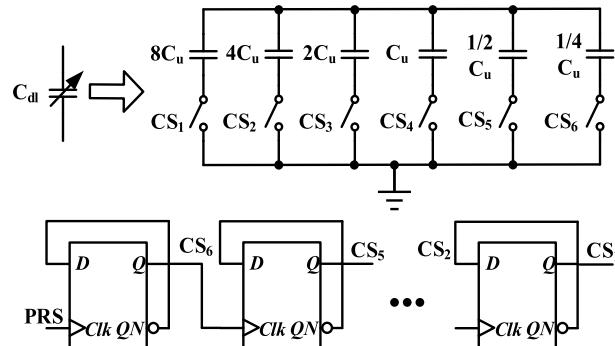
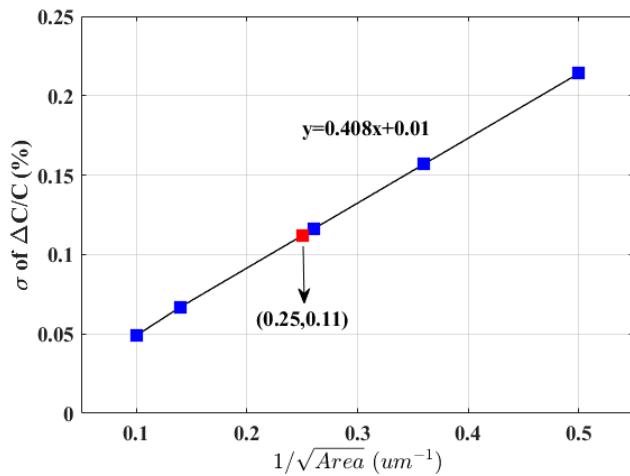
FIGURE 3. Adjustable C_{dl} and its control logic.

FIGURE 4. The relationship between area and mismatch of the MOM capacitor.

comparator is generated by the comparison-done signal from the previous bit-cycle. To save the core area and increase the sampling speed, the capacitor array is based on a bridge structure: 4 bits are allocated to the least-significant-bits (LSB) array with the monotonic structure [16] and 7 bits are allocated to the most-significant-bits (MSB) array with the hybrid structure [17]. Here, one redundant bit is added to MSB and LSB array, respectively, to form a 14-bit ($D_{13}\text{-}D_0$) digital output code. Eventually, 12-bit output code can be obtained from 14-bit digital code through the DEC circuit.

III. IMPLEMENTATION OF CDAC AND ITS CONTROL CIRCUIT

A. CDAC ARRAY AND ITS LINEARITY ANALYSIS

This work is designed with the top-plate sampling in which the sampling circuit is connected to the input of the comparator. Thus, $(N-1)$ bits capacitor array can shorten the CDAC setup time during the conversion and improve the sampling speed. The split-CDAC can effectively reduce the total capacitance with the same unit capacitor. Further, we use the bridge CDAC structure with a smaller capacitor and faster speed. The bridge capacitor (C_B) divides the capacitor array into high M bits and low L bits. The total number of capacitors is reduced from $2^{(N-1)}$ to $2^L + 2^M$. In order to free

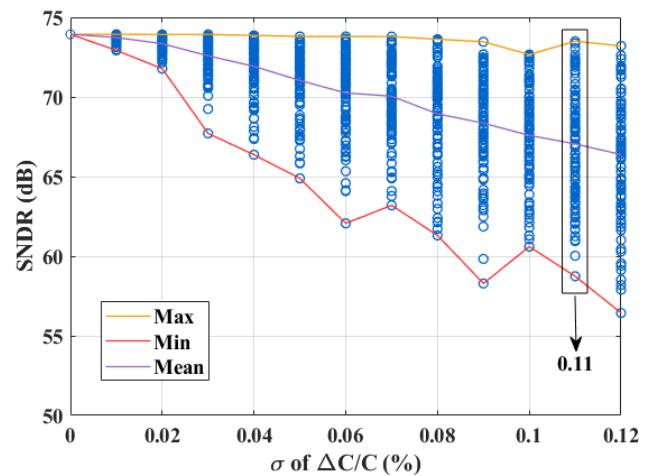


FIGURE 5. The simulated SNDR of the proposed 12-bit split CDAC versus the standard deviation of the relative deviation of the unit capacitance.

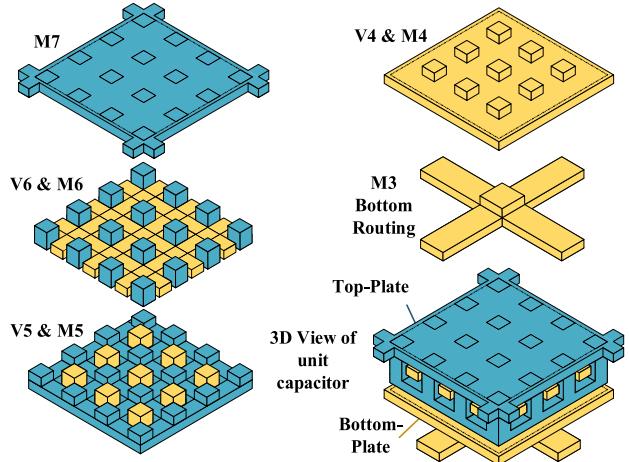


FIGURE 6. The 3D views of the MOM capacitor.

the split-CDAC from the gain error, the bridge capacitance should be written as the below equation (1) if the capacitance value of the dummy capacitor of the LSB array is equal to that of the unit capacitor.

$$C_B = \frac{2^L}{2^L - 1} C_u \quad (1)$$

where C_u is the unit capacitance. If the split-CDAC is further required to have no linear distortion, meaning that, the voltage change at the CDAC output (V_o) induced by the voltage change of ΔV applied at node 1 is twice that of node 2 (Fig. 2).

$$\Delta V_{o1} = \frac{C_u}{C_M + \frac{C_B \cdot C_L}{C_B + C_L}} \Delta V = \frac{C_u \cdot (C_B + C_L)}{C_M (C_B + C_L) + C_B C_L} \Delta V \quad (2)$$

$$\begin{aligned} \Delta V_{o2} &= \Delta V_2 \cdot \frac{C_B}{C_B + C_M} = \frac{2^{L-1} C_u}{C_L + \frac{C_B \cdot C_M}{C_B + C_M}} \cdot \frac{C_B}{C_B + C_M} \Delta V \\ &= \frac{2^{L-1} C_u C_B}{C_L (C_B + C_M) + C_B C_M} \Delta V \end{aligned} \quad (3)$$

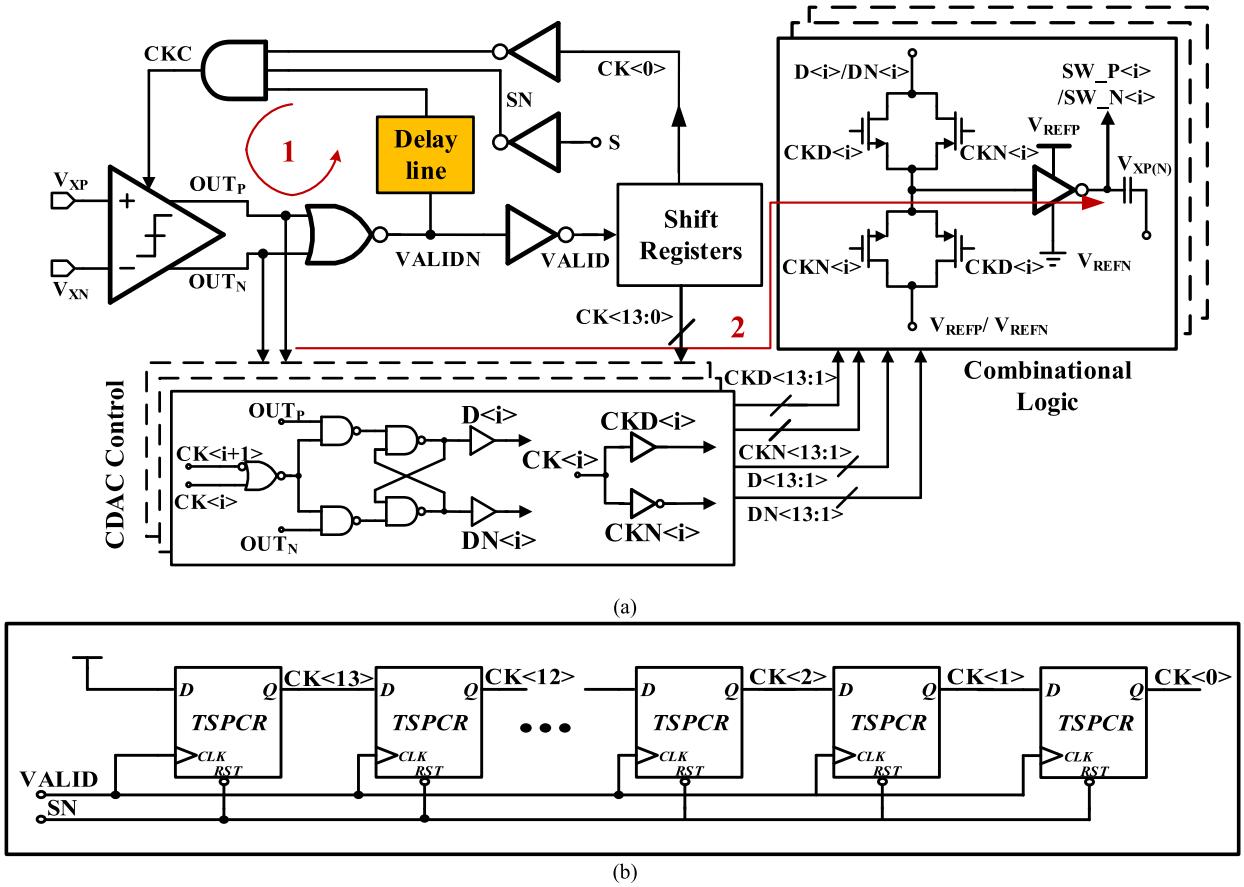


FIGURE 7. (a) The asynchronous control logic. (b) Shift registers.

where C_M and C_L are the total capacitance of the MSB array and LSB array, respectively. C_{dm} and C_{dl} are the dummy capacitors of the MSB array and LSB array, respectively.

$$\begin{aligned} C_M &= (2^M - 1) C_u + C_{dm} \\ C_L &= (2^L - 1) C_u + C_{dl} \end{aligned} \quad (4)$$

Then, we can get

$$\Delta V_{o1} = 2\Delta V_{o2} \Rightarrow C_{dl} = (2^L - 1) (C_B - C_u) \quad (5)$$

when setting $C_{dl} = C_u$, we write $C_B = 2^L/(2^L - 1)C_u$, which is the same as (1). Yet, it is hard to realize the fractional times of the unit capacitance, thus in order to meet the linearity requirement, C_B is usually selected as C_u or $2C_u$, since that a larger bridge capacitance is area wasting. Then, we theoretically analyze the parasitic capacitance to improve its linearity. As illustrated in Fig. 2(a), where C_{pm} is the parasitic capacitance between the top-plate of the MSB array and the ground, and C_{pl} is the parasitic capacitance between the top-plate of the LSB array and the ground, and C_{pb} is the parasitic capacitance between the two plates of the bridge capacitor (C_B). Similar to the above derivation process, we can get the output-node voltage change caused by the voltage change ΔV

of node 1 and node 2 [Fig. 2(b)] as

$$\begin{aligned} \Delta V_{O1p} &= \frac{C_u \cdot (C_B + C_{pb} + C_L + C_{pl})}{(C_M + C_{pm})(C_B + C_{pb} + C_L + C_{pl})(C_B + C_{pb})(C_L + C_{pl})} \Delta V \\ &= \frac{2^{L-1} C_u \cdot (C_B + C_{pb})}{(C_M + C_{pm})(C_B + C_{pb} + C_L + C_{pl})(C_B + C_{pb})(C_L + C_{pl})} \Delta V \end{aligned} \quad (6)$$

$$\begin{aligned} \Delta V_{O2p} &= \frac{2^{L-1} C_u \cdot (C_B + C_{pb})}{(C_M + C_{pm})(C_B + C_{pb} + C_L + C_{pl})(C_B + C_{pb})(C_L + C_{pl})} \Delta V \\ &= 2\Delta V_{O1p} \Rightarrow C_{dl} = (2^L - 1) (C_B + C_{pb} - C_u) - C_{pl} \end{aligned} \quad (7)$$

After considering the parasitic capacitance, the linearity of the CDAC can be held only when C_{dl} , C_B , C_{pb} , and C_{pl} satisfy the relationship of the above equation (8), but C_B , C_{pb} and C_{pl} have been determined once they are made, and we can only adjust the value of C_{dl} to make both sides of (8) as close as possible. In our design, the value of L and M are 4 and 7, C_B is $2C_u$, and the programmable range of C_{dl} is from 0 to $15\frac{3}{4}C_u$ is controlled by codes CS₁~CS₆, as shown in Fig. 3. Among them, $1/2C_u$ is obtained by connecting two-unit capacitors

TABLE 1. The arrangement of capacitor groups.

Comparison Period	Capacitor Ratios (C_u)	Bit Weighting	Redundancy Range (LSBs)
1	56 (28+28)	1792	512
2	32 (16+16)	1024	256
3	16 (8+8)	512	256
4	10 (5+5)	320	128
5	6 (3+3)	192	64
6	4 (2+2)	128	0
7	2 (1+1)	64	0
8	1	32	0
9	7	14	4
10	4	8	2
11	2	4	2
12	1	2	2
13	1	2	0
14	15	1	0

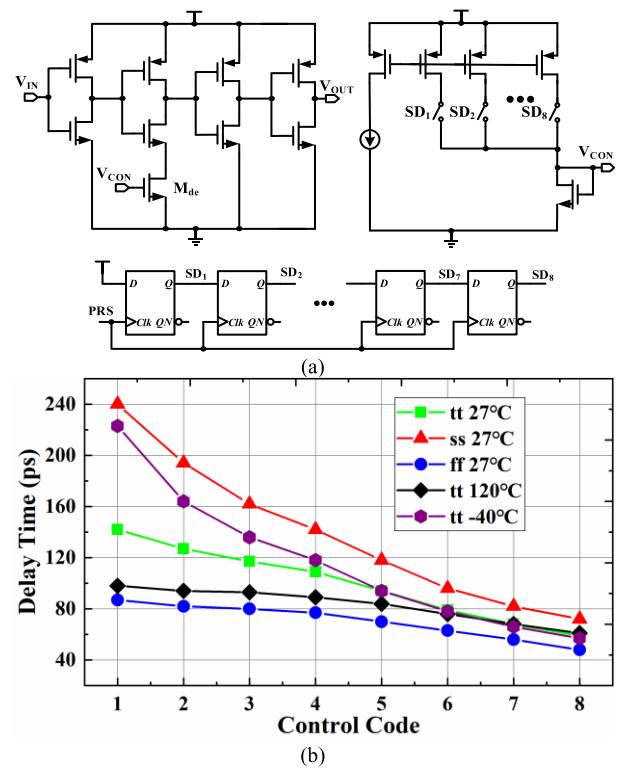
in series, and $1/4C_u$ is obtained by connecting four-unit capacitors in series.

The capacitor array in our design does not need a common-mode voltage (V_{cm}), which fully avoids the complicated three-way driving switches. The MSB-array capacitors use the hybrid arrangement. Each capacitor is equally separated into two sub-capacitors C_{ia} and C_{ib} , as shown in Fig. 1. During the sampling phase, the bottom plates of the sub-capacitors (such as C_{ia}) are connected to V_{REFP} while that of others (such as C_{ib}) connect to V_{REFN} . During the conversion phase, the bottom plates of the sub-capacitors C_{ia} on the higher voltage sides are discharged from V_{REFP} to V_{REFN} , and the bottom plates of the sub-capacitor C_{ib} on the lower voltage side are charged from V_{REFN} to V_{REFP} . The advantage of this structure is that the input common-mode voltage of the comparator remaining unchanged during the conversion phase. The LSB-array capacitors do not employ the hybrid arrangement. During the conversion phase, only the bottom plates of the capacitors on the higher voltage side are switched from V_{REFP} to V_{REFN} , while the bottom plates of the capacitors on the other side remain unchanged. Although this structure will change the input common-mode voltage of the comparator during the conversion phase, this variation can be tolerable for the comparator since the weight of the LSB-array capacitors is relatively small.

Redundancy is effective for high-speed ADC to tolerate non-ideal component errors that may incur wrong decisions [14]. In order to speed up the voltage establishment of the top plate of the MSB array, our design introduces a redundant bit in both the MSB and LSB array with the binary-scaled recombination weighting method [4], and finally the high 8 bits and the low 5 bits split-CDAC is realized. Table 1 shows the capacitors ratio, bit weighting, and redundancy range of all capacitors.

B. UNIT CAPACITOR DESIGN AND MISMATCH ANALYSIS

There are two types of capacitors commonly provided in CMOS: Metal-Insulator-Metal (MIM) and MOM capacitors [18]–[21]. The MIM capacitor has two layers of the

**FIGURE 8.** (a) The delay module. (b) Simulated delay time versus control code.

metal as the top and bottom plates, and the capacitance is proportional to the area, thus the standard deviation of the relative deviation of the capacitance is inversely proportional to the half-power of the capacitor area [18], as described in the equation (9), where σ_0 is the standard deviation of the relative deviation of the unit capacitance C_u . The MOM capacitor is a three-dimensional (3D) structure with finger strips. Note that the capacitance is closely related to the width and spacing of the metal strips. After Monte Carlo simulation of the MOM capacitance under the 65-nm technology, we can observe that when the size of the MOM capacitor is smaller ($<10 \times 10 \mu\text{m}^2$) and the number of fingers is small, the capacitance of the MOM capacitor basically meets the law of the below equation (9). Fig. 4 shows the relationship between the standard deviation of the relative deviation of the MOM capacitance and the size of the capacitor by Monte Carlo simulation. Furthermore, for a 12-bit split-CDAC according to the weights in Table 1, if the relationship between mismatch and area of each capacitor meets the law shown in Fig. 4, we can obtain the variation of the simulated SNDR caused by the mismatch of the CDAC with the standard deviation of the relative deviation of the unit capacitance. This behavior simulation result is plotted in Fig. 5.

$$\frac{\Delta C}{C} \in N \left(0, \frac{\sigma_0}{\sqrt{C}} \right) \quad (9)$$

Consider that the capacitance is determined by the matching properties [2], in order to improve the matching and reduce the routing parasitic capacitor, we design

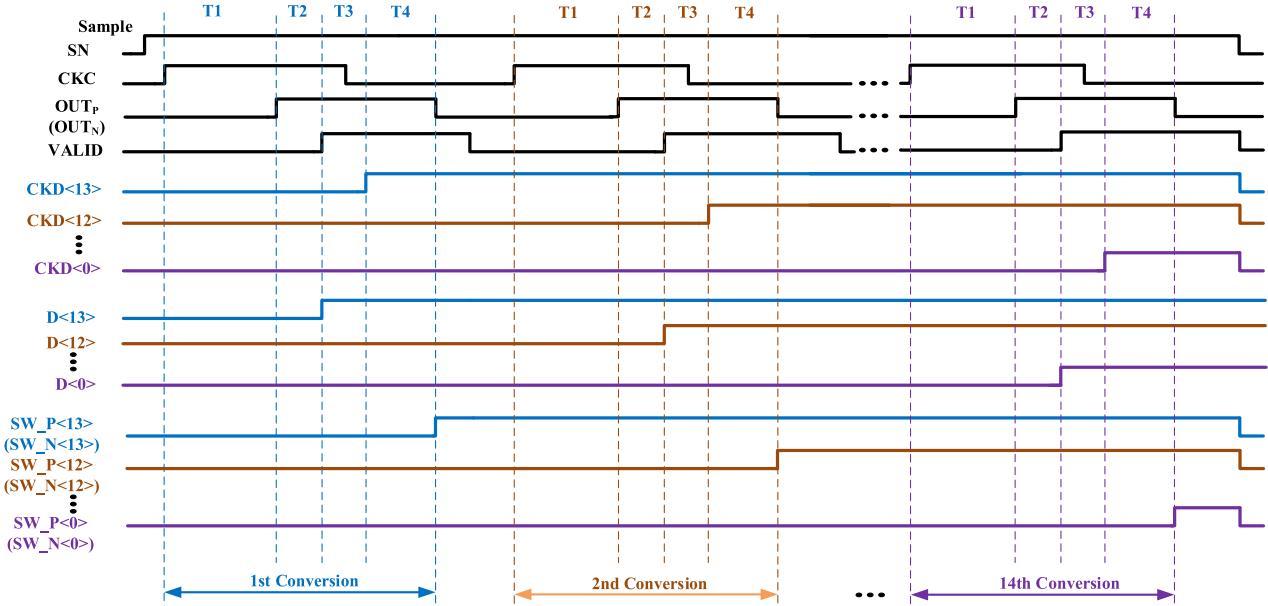


FIGURE 9. The timing diagram of the proposed asynchronous SAR ADC.

the unit capacitor in the split-CDAC by exploiting the custom-designed MOM capacitor denoted as the crossed-stripe capacitor (Fig. 6). We set one house to function the 3D capacitance. The metal block one M4 connected with stripes on M6 by VIA4 and VIA5 serves as the bottom plate, and the metal block on M7 connected with stripes on M5 by VIA5 and VIA6 serves as the top plate. The M3 layer is utilized as the routing layer for minimizing the detrimental capacitance between the routing paths and plates, and thus low mismatch can be achieved. This unit capacitor makes use of the parasitic capacitance between M4-M7 layers and has the unit capacitance of about 6.5 fF by post-simulation results and thus the total capacitance of a single-ended CDAC array is about 840 fF. The active area of this unit capacitor is $4\mu\text{m} \times 4\mu\text{m}$. The typical value of the simulated SNDR due to the mismatch introduced by the CDAC array is approximately between 58 dB and 73 dB which can be obtained from Fig. 4 and 5.

C. SAR CONTROL LOGIC

In order to avoid the usage of an external high-frequency clock and increase the conversion speed simultaneously, our design uses an asynchronous control logic. Fig. 7(a) shows the diagram of the logic control circuit of our SAR ADC. CKC is the internal clock signal of the dynamic comparator. When the comparator activates the right result, the VALID signal will jump to a high level, as the clock signal to manage the 14-bit shift registers, as shown in Fig. 7(b). S is the sampling clock signal, and SN is its inverse sampling signal. The output of the shift register chain is cleared upon setting a high-level S, while the data conversion is performed when S is enabled at a low level. The 14-bit true single-phase clocked

registers (TSPCR) are cascaded to construct a shift register. The shift register will shift in the right direction to generate a bit of $\text{CK}_{<i>}$ every time, enabling the comparator, and the resultant $\text{CK}_{<13:0>}$ is the signal that controls the flip of the capacitor, which changes to a high level in turn under the trigger of VALID. $\text{CKD}_{<13:0>}$ and $\text{CKN}_{<13:0>}$ are the control signals for the switch of the bottom plate of the positive and negative capacitor array, which are the delayed and inverted signals provided by $\text{CK}_{<13:0>}$.

There are two critical signal paths in the circuit. One is the path from the output of the comparator to the next time CKC goes high, which is path 1, as shown in Fig. 7(a). The second path is from the output of the comparator to the flipping of the bottom plate of the CDAC, which is path 2, as shown in Fig. 7(a). Before entering into the succeeding comparison period, the signal of the top plate of the CDAC should be established to the required precision. This requires that the delay time of path 1 is greater than that of path 2, thus a delay block is inserted into path 1. This block consists of the four cascaded inverters, and the delay time of the second stage can be controlled by the gate voltage (V_{CON}) of the transistor (M_{de}), as depicts in Fig. 8(a). V_{CON} is generated by a diode-connected NMOS transistor with a bias current controlled by a thermometer code SD_i , where the bias current is carefully designed so that the delay is nominally proportional to SD_i . Fig. 8(b) plots the simulated delay time versus V_{CON} over different process and temperature variations. Differently, using the CDAC control logic circuit [Fig. 7(a)] can make the output of the comparator reach the combinational logic circuit earlier than the rising edge of the signal $\text{CK}_{<i>}$, thereby reducing the delay of the path 2. Moreover, since the low to high transition delay of the TSPCR is much shorter than that of the typical data flip-flops (DFF), the combinational logic

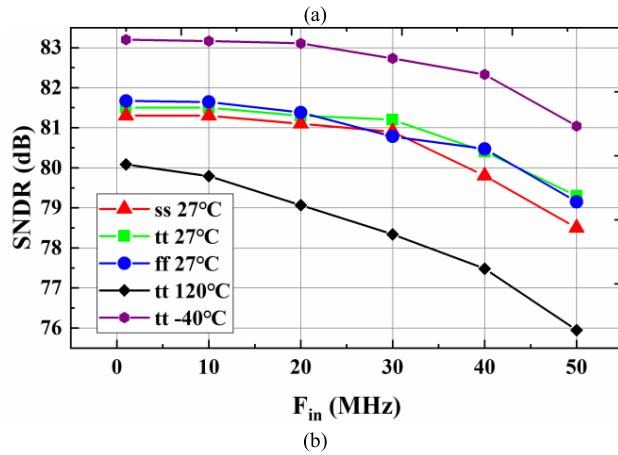
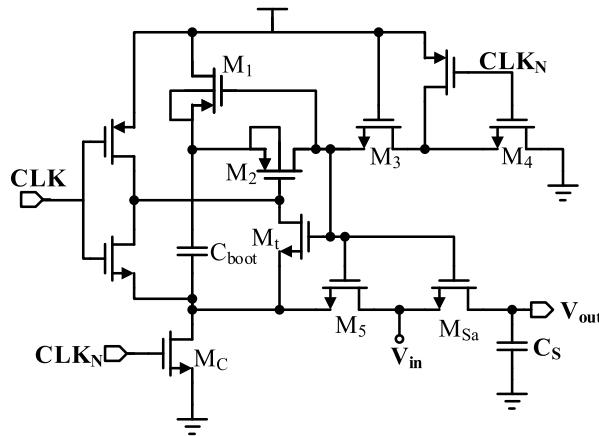


FIGURE 10. (a) The schematic of the bootstrapped switch. (b) Its simulated SNDR versus F_{in} .

circuit can generate the signal SW_P<i>/SW_N_i earlier than that in a typical asynchronous logic.

Fig. 9 details the timing diagrams of the first bit-cycle conversion in our design. Herein, T1 is the delay of the comparator, which changes with the input signal and can only be decreased by optimizing the design of the comparator. T2 is the delay between the NOR gate and the NOT gate. T3 is the transition delay of the TSPCR from low to high level. T4 is the delay of the combinational logic circuit, as shown in Fig. 7(a).

IV. KEY BUILDING BLOCKS

A. BOOTSTRAPPED SWITCH

The sampling switch is shown in Fig. 10 (a). The body of the transistors (M₁ and M₂) is connected to their source to avoid the latch-up effect. In addition, the transistor (M_t) is added to ensure that the source-gate voltage of M₂ is not too large to damage the transistor. In order to reduce the coupling of the parasitic capacitance to the signal, a dummy transistor can be introduced in parallel with M_{Sa} [4]. Fig. 10 (b) depicts the simulation results of the SNDR varying with the input frequency at 100 MS/s over the different process and temperature variations.

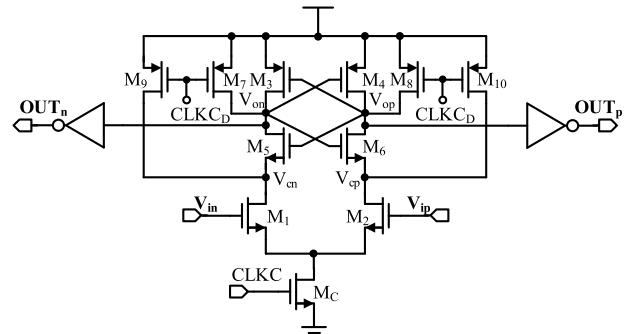


FIGURE 11. The schematic of the dynamic comparator.

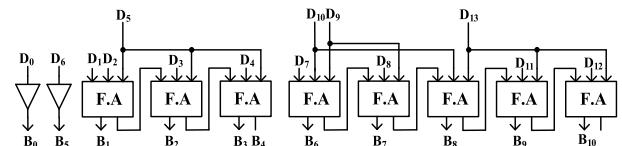


FIGURE 12. The schematic of the DEC circuit.

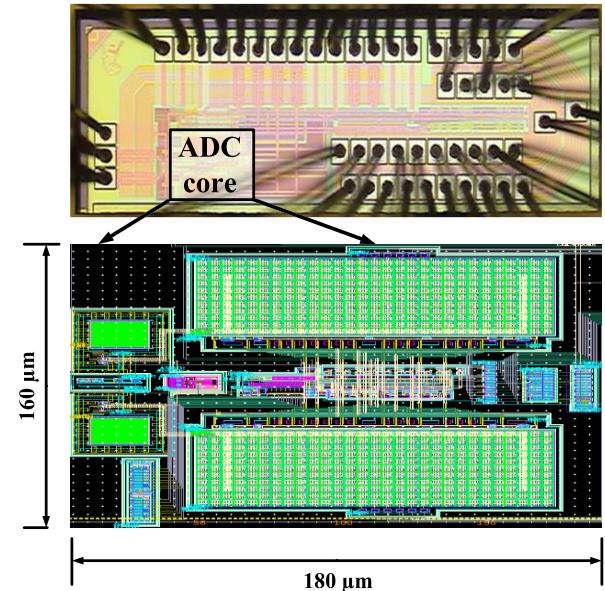


FIGURE 13. The chip photograph and detailed layout of the active core.

B. DYNAMIC COMPARATOR

Fig. 11 shows the schematic of the single-stage dynamic comparator [22]–[24]. When the clock signal (CLKC) is low, the tail current transistor (M_c) is turned off, and V_{cp,n} and V_{op,n} are charged up to VDD, and the comparator outputs are reset to GND. When CLKC is a high level, M_c will be turned on, and the input transconductance stage consisting of the transistors (M₁ and M₂) discharges the nodes (V_{cp,n}) with different currents according to the amplitude of the input signal. The latch (M₃–M₆) amplifies this difference by the positive feedback, and finally, one side is pulled up to VDD, and the other side is discharged to GND. Table 2 lists the size of each transistor in this dynamic comparator. The size of the

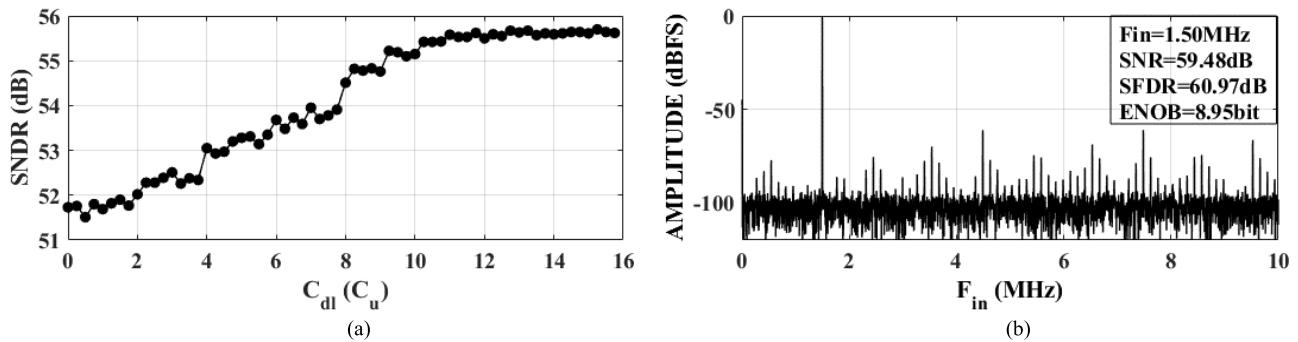


FIGURE 14. (a) The measured SNDR at $F_{in} = 1.5\text{MHz}$ by adjusting programmable C_{dl} with $F_S = 20\text{MS/s}$. (b) The measured spectra at $F_{in} = 1.5\text{MHz}$ with $F_S = 20\text{MS/s}$ when setting $C_{dl} = 15.75C_u$.

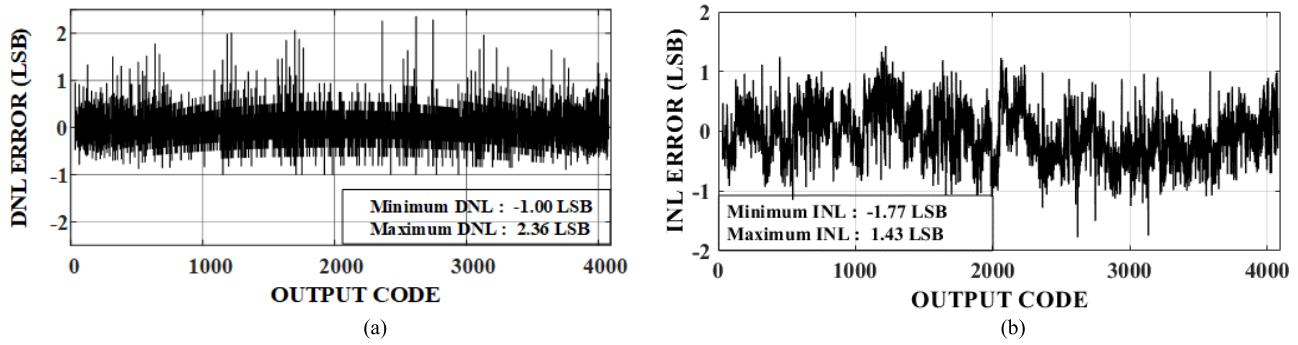


FIGURE 15. The measured (a) DNL and (b) INL.

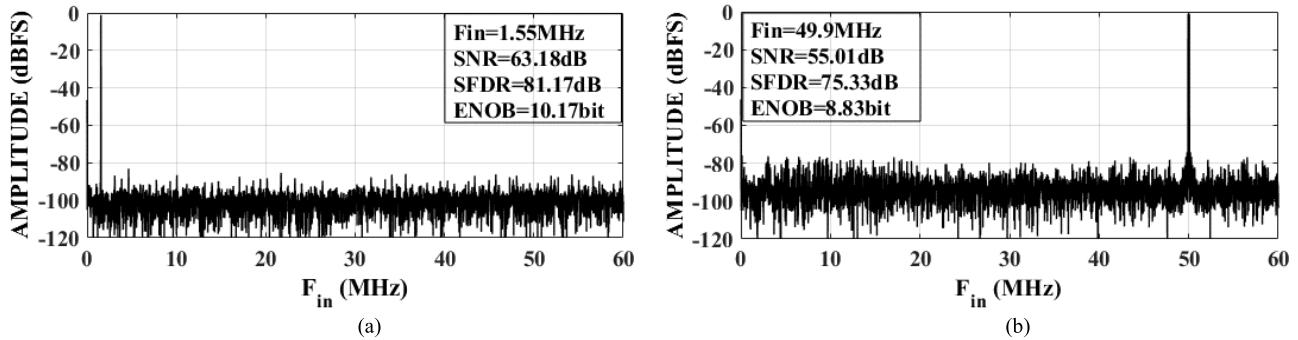


FIGURE 16. The measured spectra at $F_{in} = 1.5\text{MHz}$ (a) and 50MHz (b) with $F_S = 100\text{MS/s}$.

TABLE 2. Transistor size of comparator.

$M_{1,2}$	16 $\mu\text{m}/120\text{ nm}$	$M_{3,4}$	8 $\mu\text{m}/60\text{ nm}$
$M_{5,6}$	8 $\mu\text{m}/60\text{ nm}$	$M_{7,8}$	4 $\mu\text{m}/60\text{ nm}$
$M_{9,10}$	4 $\mu\text{m}/120\text{ nm}$	M_C	16 $\mu\text{m}/60\text{ nm}$

input transistors is carefully optimized to reduce DC offset and minimize the kick-back noise.

C. DIGITAL ERROR CORRECTION (DEC) LOGIC

Considering that our asynchronous SAR ADC is based on redundancy technology, where the target 12-bit binary code is represented by 14-bit redundant code. To obtain the target 12-bit binary code, we derive the mathematical

operations given in the below equation (10). According to Table 1 and (10), the 12-bit digital code can be achieved by the DEC circuit [25], as shown in Fig. 12.

$$\begin{aligned} D_{OUT} = & D_0 \times 1 + (D_1 + D_2 + D_5) \times 2 + (D_3 + D_5) \times 2^2 \\ & + (D_4 + D_5) \times 2^3 + D_6 \times 2^5 + (D_7 + D_8 + D_9) \\ & \times 2^6 + (D_8 + D_9) \times 2^7 + (D_{10} + D_{13}) \times 2^8 \\ & + (D_{11} + D_{13}) \times 2^9 + (D_{12} + D_{13}) \times 2^{10} \quad (10) \end{aligned}$$

V. MEASUREMENT RESULTS

The prototype of our asynchronous SAR ADC is fabricated in 65-nm CMOS technology with a 1.2-V supply voltage. Fig. 13 shows the chip photograph and its zoomed-in view of the core layout occupying an active area of $180 \times 160\mu\text{m}^2$.

TABLE 3. Performance summary and comparison.

	This work	[1]*	[2]	[26]	[27]	[28]	[29]
CMOS Technology	65 nm	28 nm	65 nm	90 nm	40 nm	40 nm	40 nm
Resolution (bits)	12	12	11	12	12	12	12
Supply Voltage (V)	1.2	1.1	1.2	1.2	1	0.9	0.9
Sampling Rate (MS/s)	100	104	100	120	120	100	150
Input Range (V _{pp,diff})	2	1.7	2	2	/	1.8	/
SNR (dB)	@LF 63.18	61.1	63.9	/	/	/	62.2
	@Nyquist 55.01	/	61.1	/	/	/	57.7
SFDR (dB)	@LF 81.17	76.2	74.7	72.9	82.12	/	74.4
	@Nyquist 75.33	51	68.7	72	82.09	74.61	63.5
ENOB (bits)	@LF 10.17	9.76	10.29	9.73	10.85	/	9.96
	@Nyquist 8.83	7.18	9.7	9.34	10.59	9.51	9.04
Power (mW)	0.8	0.88	1.6	3.2	1.9	2.6	1.5
Core Area (mm ²)	0.029	0.003	0.011	0.042	0.013	0.014	0.04
FoM	@LF 6.94	7.3	21.3	18.8	14.1	/	10.3
(fJ/conv.-step)	@Nyquist 17.6	58.4	32	24.26	14.6	21.9	18.9

*without both the reference buffer and input buffer.

Fig. 14(a) shows the SNDR of the output signal measured by adjusting different C_{dl} from 0 to $15.75C_u$ under a 1.5-MHz input frequency at 20 MS/s. Note that the value of C_{dl} is not accurate because the half unit capacitor and the quarter unit capacitor are implemented with the unit capacitor in the series connection, thus the value of these capacitors is influenced by the parasitic capacitance on the connection nodes. It can be observed that as C_{dl} increasing from 0 to $15.75C_u$, the SNDR increases by about 3 dB. The optimized value of C_{dl} is above $10 C_u$, referring to the curve tendency, although the exact value is not quite clear because the mismatch of this capacitor array, probably caused by the routing parasitic capacitor, limits the linearity benefit of the dummy optimization method.

The performance (Fig. 14) is based on the output digits with the original nominal weights. Then, the optimized weights are used to overcome the mismatch of the capacitor array. The measured spectra of 1.5-MHz F_{in} with $F_s = 20$ MS/s, while C_{dl} is equal to $15.75 C_u$, is depicted in Fig. 14(b).

Fig. 15 shows the measured static performance. The peak DNL error is $-1.00/2.36$ LSB and the peak INL error is $-1.77/1.43$ LSB. The most value of both DNL and INL is within $-1.00/1.00$ LSB, some relatively-large INL/DNL values are caused by the parasitic capacitance and the inability of the programmable compensation capacitor (C_{dl}) to eliminate the effects of the parasitic capacitor.

Fig. 16 plots the measured spectra at F_{in} of 1.5 MHz and 50 MHz with 100-MS/s F_s , respectively. At $F_{in} = 1.5$ MHz, the measured SNR and SFDR are 63.18 and 81.17 dB, respectively. As F_{in} increasing to the Nyquist frequency of 50 MHz, the measured SNR falls to 55.01 dB and SFDR is 75.33 dB due to the unexpected thermal noise and interference from the chip on board. Fig. 17 shows the measured SNR, SFDR and ENOB versus F_{in} when setting $F_s = 100$ MS/s. The power breakdown of our ADC prototype is shown in Fig. 18, where the ADC dissipates 0.8-mW power totally including

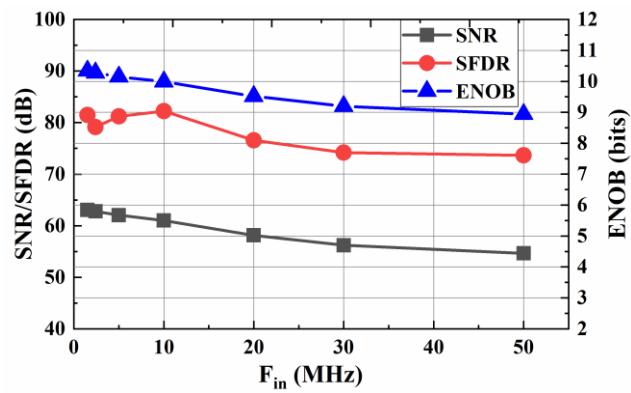


FIGURE 17. The measured SNR, SFDR and ENOB versus F_{in} at $F_s = 100$ MS/s.

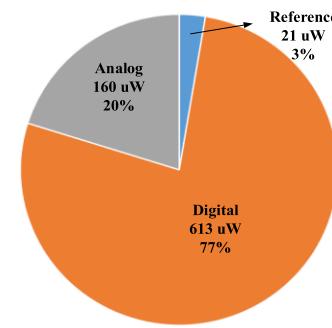


FIGURE 18. Power breakdown including the reference buffers.

analog, digital and reference circuits. The proportion of each part is also given in Fig. 18. Our SAR ADC achieves a figure-of-merit (FoM) of 6.94 and 17.6 fJ/conversion-step at low-frequency input and Nyquist input, respectively. Table 3 summarizes the performance and compares our work with recent arts, showing that our work achieves best FoM with similar sampling speed and resolution.

VI. CONCLUSION

This paper presents a 12-bit 100-MS/s asynchronous SAR ADC targeting for low-power wireless communication. The split-CDAC where the LSB array using the monotonic structure and MSB array based on the hybrid scheme is developed to reduce core area and enhance sampling speed. To improve its linearity and reduce the effects of the parasitic capacitance, we employ the programmable dummy capacitor and custom-designed unit capacitor. Adjustable delay module is embedded in the critical signal path for adjusting the asynchronous timing. Fabricated in a 65-nm CMOS, our prototype consumes 0.8-mW power. The measured ENOB score 10.17 and 8.83 bit under low frequency and Nyquist at 100 MS/s, respectively, corresponding to 6.94 and 17.6 fJ/conversion-step.

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