NOVA SCHOOL OF
SCIENCE & TECHNOLOGY

MEEC/MIEEC

Radio Frequency Electronics

Low Noise Amplifier - Part I

Authors:

Martim Duarte Agostinho (70392) md.agostinho@campus.fct.unl.pt
Francisco Simões Coelho Sá da Costa (70386) fsc.costa@campus.fct.unl.pt
Sofia Margarida Mafra Dias Inácio (58079) sm.inacio@campus.fct.unl.pt

2024/2025 – 2nd Semester, DEEC

Contents

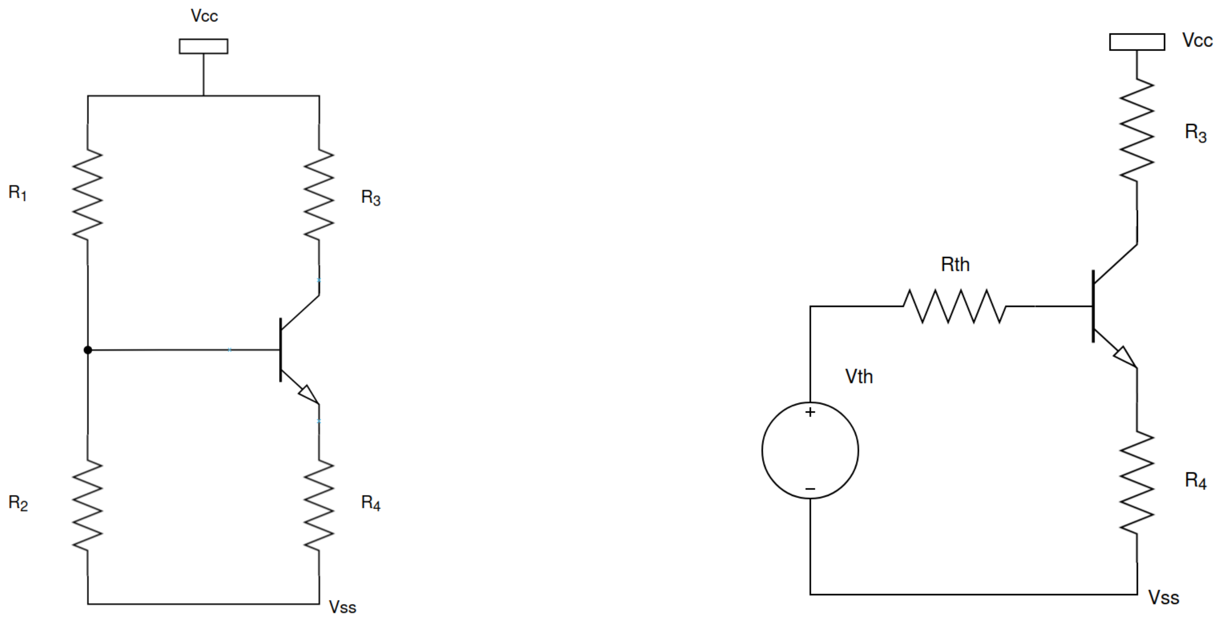
List of Figures

1 Introduction

2 Design of the LNA

2.1 Transistor Bias Network

The DC bias point of a transistor directly influences its small-signal S-parameters, and hence the gain, noise figure and stability of the LNA. This makes this step crucial. Figure ?? shows the biasing circuit and its Thévenin equivalent used to simplify analysis.



(a) Transistor DC biasing circuit

(b) Bias circuit equivalent circuit

As shown in Figure 1b the Thévenin equivalent is given by the equations 1, replacing the R_1, R_2 voltage divider.

$$\begin{aligned} R_{TH} &= R_1 // R_2 \\ V_{TH} &= V_{cc}\frac{R_2}{R_1 + R_2} \end{aligned} \tag{1}$$

Using Kirchhoff voltage law, the equations 2 are derived, the first starts at V_{TH} goes through R_{TH}, V_{BE} and R_4. The second goes from V_{CC} through R_3, V_{CE} and R_4.

$$\begin{cases} 0 = V_{TH} - I_b \cdot R_{TH} - V_{BE} - I_E \cdot R_4 \\ 0 = V_{CC} - R_3 \cdot I_C - V_{CE} - I_E \cdot R_4 \end{cases} \tag{2}$$

Solving the system of equations, assuming fixed values for R_2 and R_4, originates the equations 3.

$$
\begin{aligned}
R_1 &= \frac{R_2\left(-I_C R_4 \beta - I_C R_4 - V_{BE}\beta + V_{CC}\beta\right)}{I_C R_2 + I_C R_4 \beta + I_C R_4 + V_{BE}\beta} \\
R_3 &= \frac{-I_C R_4 \beta - I_C R_4 + V_{CC}\beta - V_{CE}\beta}{I_C \beta}
\end{aligned}
\tag{3}
$$

The Table 1, shows the provided values for the biasing circuit and the fixed values for R_2 and R_4.

Table 1: Transistor biasing parameters

Parameter	**Value**
R_2	$1\,\mathrm{k\Omega}$
R_4	$100\,\Omega$
β	72.534
I_C	$9\,\mathrm{mA}$
V_{CC}	$10\,\mathrm{V}$
V_{BE}	$1\,\mathrm{V}$
V_{CE}	$5\,\mathrm{V}$

Resulting in $R_1 = 4\,\mathrm{k\Omega}$ and $R_3 = 454\,\Omega$.
FALTA SIM E JUSTIFICAR A SIM

2.2 S-parameters with packaging effects

2.3 Transistor validation for the given bias point

2.4 Stability

2.5 Input and output matching networks

2.6 Gain and Noise Factor

3 Simulation

3.1 Validation of the LNA design

3.2 Input and output matching networks design optimization

4 Conclusion

References