

# MEEC/MIEEC

## RADIO FREQUENCY ELECTRONICS

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### Low Noise Amplifier - Part I

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#### Authors:

Martim Duarte Agostinho (70392)  
Francisco Simões Coelho Sá da Costa (70386)  
Sofia Margarida Mafra Dias Inácio (58079)

[md.agostinho@campus.fct.unl.pt](mailto:md.agostinho@campus.fct.unl.pt)  
[fsc.costa@campus.fct.unl.pt](mailto:fsc.costa@campus.fct.unl.pt)  
[sm.inacio@campus.fct.unl.pt](mailto:sm.inacio@campus.fct.unl.pt)

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# 1 Introduction

This report presents the design and analysis of a Low Noise Amplifier (LNA) designed to operate in the ISM (Industrial, Scientific and Medical) band. In modern telecom systems, LNAs play a crucial role in dealing with low amplitude signals at high frequencies with high data rates. During the development of this project, advanced RF design concepts were explored, including the use of adaptive loops for impedance, stability, gain and noise within the specified frequency range (3-6 GHz). The challenges faced, and the solutions adopted are detailed in this report.

The aim of this report is to comprehensively document the process of designing and analyzing a Low Noise Amplifier (LNA) for operation in the ISM band, with a focus on achieving critical performance specifications. The circuit will have to be designed following certain detailed specifications, starting by designing a suitable polarization network for the transistor, taking into account the effects of encapsulation.

## 1.1 Objectives

The main objectives of this report are as follows:

- Design a Low Noise Amplifier (LNA) for operation in a specified frequency in the 3-6 GHz range.
- Analyze the performance of the LNA in terms of gain, noise figure, and stability.
- Implement adaptive loops for impedance matching, stability, gain, and noise optimization.
- Document the design process, challenges faced, and solutions adopted.
- Provide a comprehensive analysis of the LNA's performance through simulation and measurement.
- Discuss the implications of the design choices made and their impact on the overall performance of the LNA.S
- Provide a Python script for the design and simulation of the LNA using the ‘scikit-rf’ library.

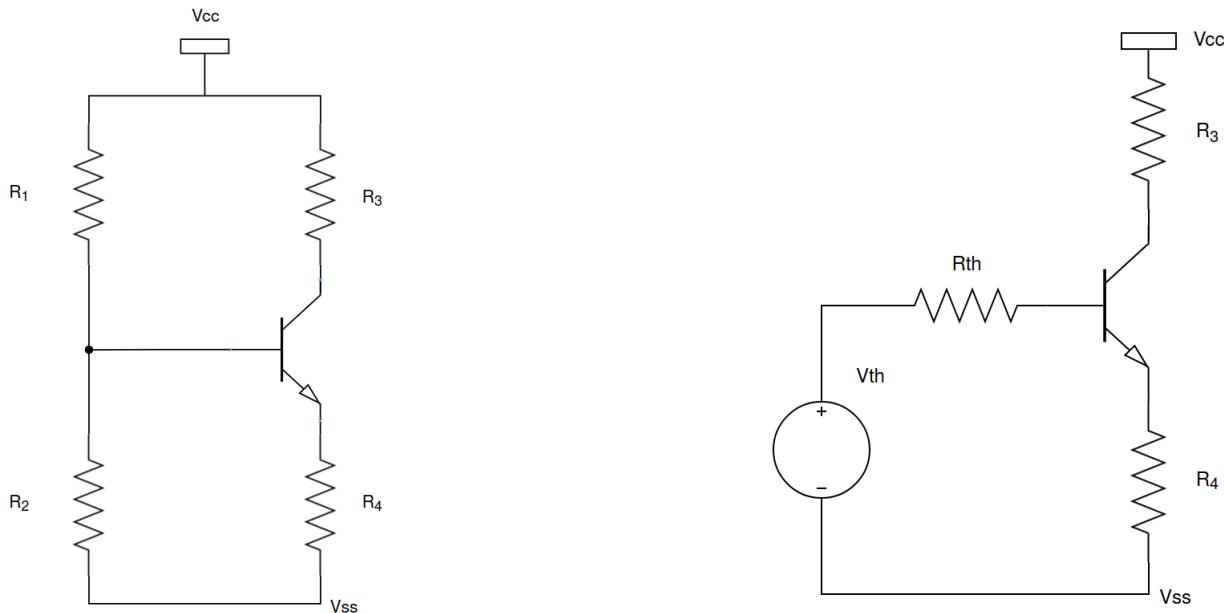
## 1.2 Motivation

The motivation behind this project stems from the increasing demand for high-performance RF components in modern communication systems. As wireless communication continues to evolve, the need for efficient and reliable amplifiers becomes paramount. The project aims to contribute to the field of RF design by providing a detailed analysis and design of an LNA that meets the statement requirements of modern communication systems. The project also serves as a practical application of theoretical concepts learned in the course, bridging the gap between theory and practice in RF design.

## 2 Design of the LNA

### 2.1 Transistor Bias Network

The DC bias point of a transistor directly influences its small-signal S-parameters, and hence the gain, noise figure and stability of the LNA. This makes this step crucial. Figure 1 shows the biasing circuit and its Thévenin equivalent used to simplify analysis.



(a) Transistor DC biasing circuit.

(b) Bias circuit equivalent circuit.

**Figure 1:** Transistor DC biasing circuit and its Thévenin equivalent.

As shown in Figure 1b the Thévenin equivalent is given by the equations 1, replacing the  $R_1$ ,  $R_2$  voltage divider.

$$\begin{aligned} R_{TH} &= R_1 // R_2 \\ V_{TH} &= V_{CC} \frac{R_2}{R_1 + R_2} \end{aligned} \quad (1)$$

Using Kirchhoff voltage law, the equations 2 are derived, the first starts at  $V_{TH}$  goes through  $R_{TH}$ ,  $V_{BE}$  and  $R_4$ . The second goes from  $V_{CC}$  through  $R_3$ ,  $V_{CE}$  and  $R_4$ .

$$\begin{cases} 0 = V_{TH} - I_b \cdot R_{TH} - V_{BE} - I_E \cdot R_4 \\ 0 = V_{CC} - R_3 \cdot I_C - V_{CE} - I_E \cdot R_4 \end{cases} \quad (2)$$

Solving the system of equations, assuming fixed values for  $R_2$  and  $R_4$ , originates the equations 3.

$$\begin{aligned} R_1 &= \frac{R_2(-I_C R_4 \beta - I_C R_4 - V_{BE} \beta + V_{CC} \beta)}{I_C R_2 + I_C R_4 \beta + I_C R_4 + V_{BE} \beta} \\ R_3 &= \frac{-I_C R_4 \beta - I_C R_4 + V_{CC} \beta - V_{CE} \beta}{I_C \beta} \end{aligned} \quad (3)$$

The Table 1, shows the provided values for the biasing circuit and the fixed values for  $R_2$  and  $R_4$ .

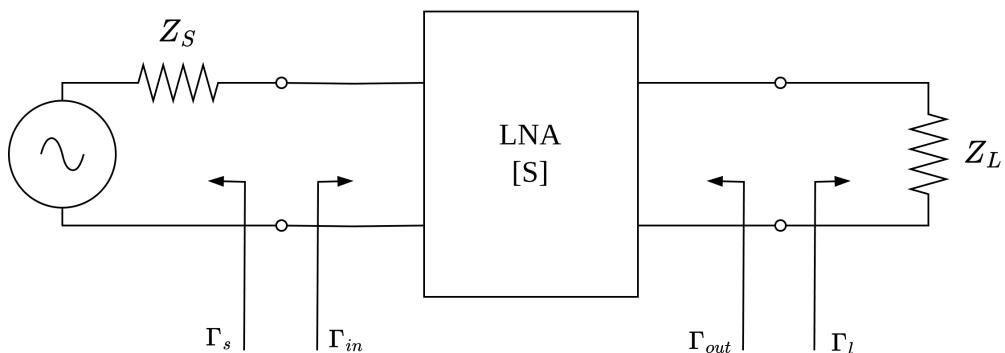
**Table 1:** Transistor biasing parameters

Parameter	Value
$R_2$	1 kΩ
$R_4$	100 Ω
$\beta$	72.534
$I_C$	9 mA
$V_{CC}$	10 V
$V_{BE}$	1 V
$V_{CE}$	5 V

Resulting in  $R_1 = 4 \text{ k}\Omega$  and  $R_3 = 454 \Omega$ .

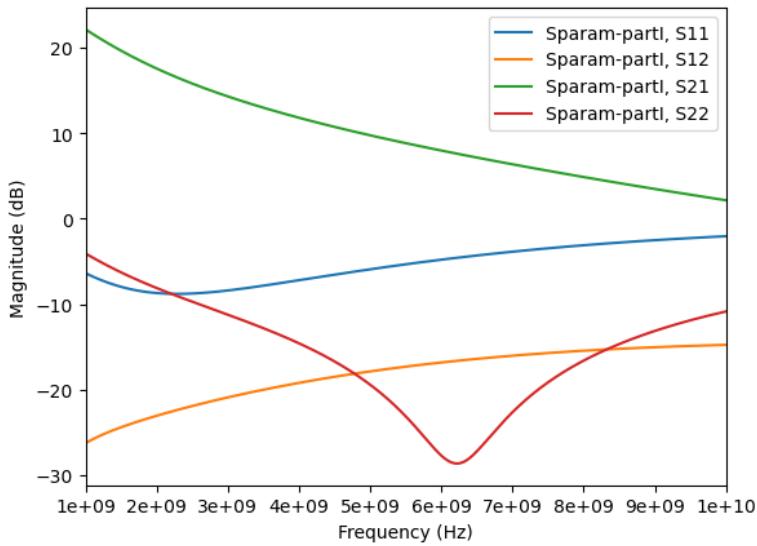
## 2.2 S-parameters with packaging effects

The diagram of the LNA is shown in Figure 2, where the LNA has arbitrary input and output impedances different from  $50 \Omega$  and reflection coefficients.



**Figure 2:** LNA diagram with reflection coefficients and no matching networks.

With the biasing circuit designed, the next step was to simulate the S-parameters of the transistor in LTSpice. The S-parameters were taken for a frequency range of 1 GHz to 10 GHz, Figure 3 shows the S-parameters of the transistor without any matching network.



**Figure 3:** S-parameters of the transistor, for the range of frequencies, without matching network.

## 2.3 Stability

Ensuring that the LNA remains stable is critical for reliable operation. The network is unconditionally stable for a frequency if for any source impedance value,  $|\rho_{in}| < 1$  and for the load impedance  $|\rho_{out}| < 1$ . Below, the stability analysis is performed using the S-parameters obtained in the previous step to calculate the stability factors, in this case, the  $K$  and  $\Delta$  factors and the  $\mu$  factor.

Defining  $\Delta$  as:

$$\Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \quad (4)$$

Where  $S_{11}$ ,  $S_{22}$ ,  $S_{12}$  and  $S_{21}$  are the S-parameters of the LNA.

And defining  $K$  as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} \cdot S_{21}|} \quad (5)$$

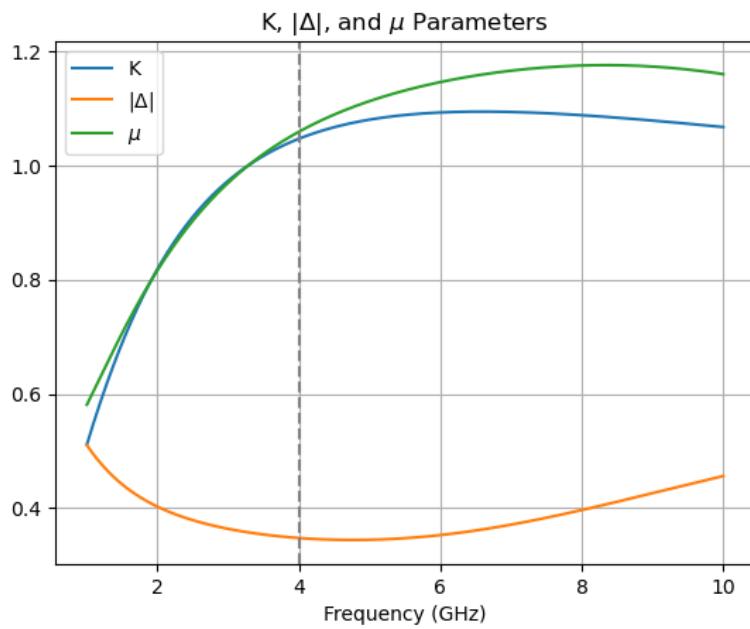
The stability conditions can be summarized as follows:

- $K > 1$  and  $|\Delta| < 1 \rightarrow$  unconditionally stable
- $K > 1$  and  $|\Delta| > 1$  or  $K < 1 \rightarrow$  potentially unstable or always unstable

Another criteria is the  $\mu$  factor, defining  $\mu$  as:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12} \cdot S_{21}|}$$

If  $\mu > 1 \rightarrow$  unconditionally stable In addition, it can be said that larger values of  $\mu$  imply greater stability.

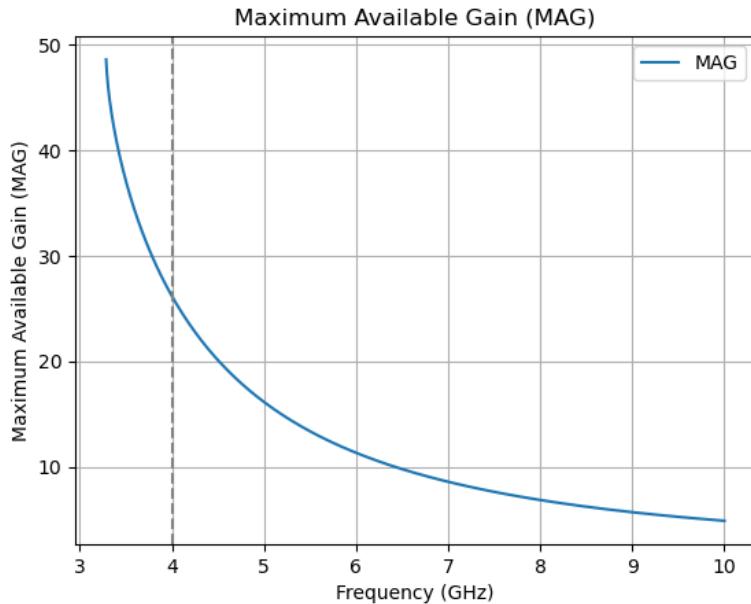


**Figure 4:** Stability factors  $K$ ,  $\Delta$  and  $\mu$  for the range of frequencies.

Figure 4, shows that the LNA is stable for frequencies above 3.1 GHz and above 10 GHz loses stability again.

At this stage another important figure is the Maximum Available Gain,  $MAG$ , which for the bilateral case can be expressed as the equation 6.

$$MAG = \left| \frac{S_{21}}{S_{12}} \right| \cdot [K - \sqrt{K^2 - 1}] \quad (6)$$



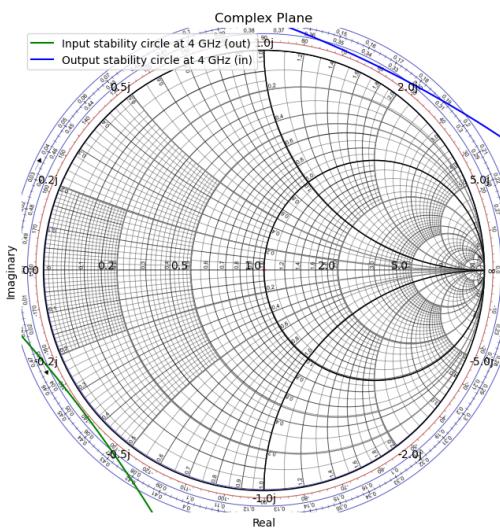
**Figure 5:** Maximum Available Gain for the range of frequencies.

Now having the full picture of the LNA characteristics, an operating frequency can be decided. The frequency chosen was the one that maximizes the gain while maintaining stability. In this case, the chosen was 4 GHz, where the  $MAG$  is 26, 13 and the stability factors are  $K = 1, 05$ ,  $\Delta = 0, 35$  and  $\mu = 1, 06$ , the summary of the stability parameters is shown in Table 2.

**Table 2:** Stability parameters for the chosen frequency.

Parameter	Value
Chosen Frequency	4 GHz
$ \Delta $	0, 35
$k$	1, 05
$\mu$	1, 06
$MAG$	26, 13

The stability circles in the Smith Chart for the input and output are shown in Figure 6, where is possible to see that at 4GHz the LNA is stable for all the source and load impedances.

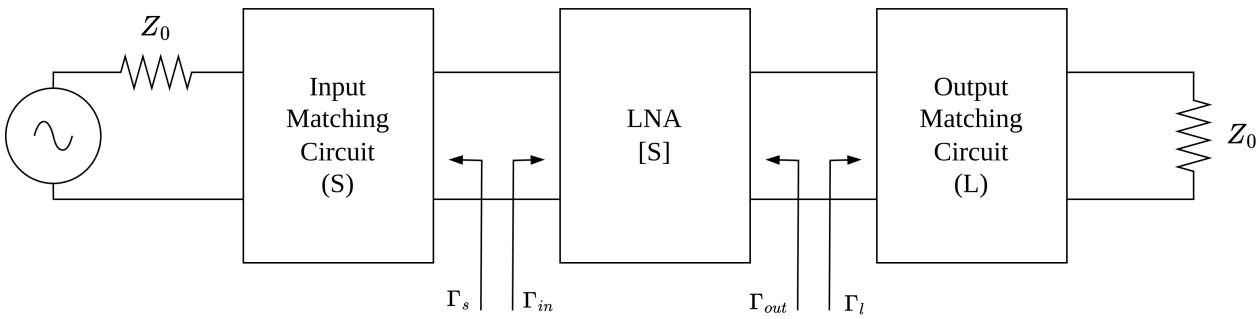


**Figure 6:** Stability circles for the input and output of the LNA.

## 2.4 Input and output matching networks for Maximum Gain

The adaptation for maximum gain is done using the line impedance transformation method. The input and output matching networks are designed to transform the input and output impedances of the transistor to the desired values, which are  $50\Omega$  in this case. In the Smith Chart, the matching is done with inductors and capacitors or lines and stubs.

In Figure 7 the diagram of the LNA is shown, where is possible to see the reflection coefficients, the input and output matching networks, the source and load impedances  $Z_0$ .



**Figure 7:** LNA diagram with matching networks and reflection coefficients.

Observing the diagram, the input and output matching networks are designed to transform the input and output impedances of the transistor to  $50\Omega$ , corresponding to the source and load impedances  $Z_0$ .

The maximum power transfer from the input matching network to the transistor will occur when:

$$\Gamma_{in} = \Gamma_s^* \quad (7)$$

And the maximum power transfer from the transistor to the output matching network will occur when:

$$\Gamma_{out} = \Gamma_l^* \quad (8)$$

where  $\Gamma_{in}$  and  $\Gamma_{out}$  are the reflection coefficients at the input and output of the transistor, respectively, and  $\Gamma_s$  and  $\Gamma_l$  are the reflection coefficients at the source and load impedances, respectively. Using the equations obtain in [1], the expressions that result in the reflection coefficients at the input and output of the transistor are:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (9)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (10)$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad (11)$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad (12)$$

Finally, the reflection coefficients at the source and load of the transistor are given by:

$$\Gamma_s = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (13)$$

$$\Gamma_l = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (14)$$

In Table 3 the reflection coefficients at the input and output of the transistor are shown, where the values are calculated using the S-parameters obtained in the previous step.

**Table 3:** Reflection coefficients at the input and output of the transistor.

Parameter	Value
$\Gamma_S$	$-0.61339711 - 0.4649262j$
$\Gamma_L$	$0.29177619 + 0.6148401j$
$B_1$	1.03559444
$B_2$	0.72244362
$C_1$	$-0.39891088 + 0.30235572j$
$C_2$	$0.144066 - 0.30358047j$
$S_{11}$	$-0.33990673 + 0.27537675j$
$S_{12}$	$0.06042986 - 0.17647029j$
$S_{21}$	$0.09296393 + 0.05839295j$
$S_{22}$	$2.52965222 + 2.95848991j$

With the values of the reflection coefficients at the source and load, the normalized impedances at the source and load can be calculated using the equations 15 and 16.

$$z_S = \frac{1 + \Gamma_S}{1 - \Gamma_S} \quad (15)$$

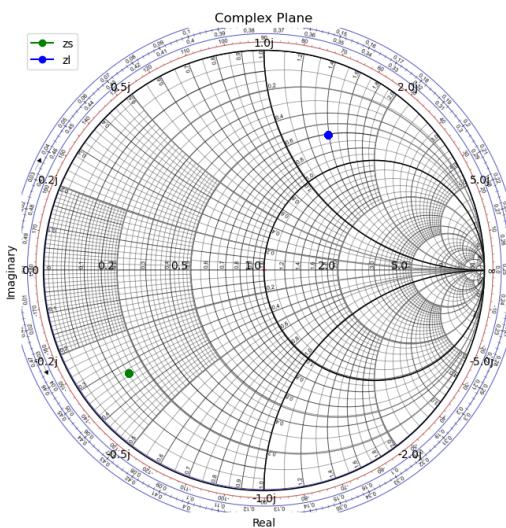
$$z_L = \frac{1 + \Gamma_L}{1 - \Gamma_L} \quad (16)$$

Where  $Z_0$  is the desired impedance, in this case  $50\Omega$ . The resulting normalized impedances at the source and load are shown in Table 4, where the values are calculated using the reflection coefficients obtained in the previous step.

**Table 4:** Impedances at the source and load of the transistor.

Parameter	Value
$z_S$	$0.14457529 - 0.32982769j$
$z_L$	$0.6103145 + 1.39798452j$

The Smith Chart representation of the normalized impedances at the source and load is shown in Figure 8, where the normalized impedances are represented as points.



**Figure 8:** Normalized impedances at the source and load of the transistor in the Smith Chart.

#### 2.4.1 Matching with lumped elements

The matching networks were first designed using the Smith chart, which allows for the visualization of the impedance transformation. A second analysis was done with an analytic approach using a Python script in order to have more accurate results. The input and output impedances of the LNA are transformed to  $50\Omega$  using a combination of inductors and capacitors. The values of the components are also calculated using the equations for impedance transformation.

#### Results with the Smith Chart:

The matching using the Smith Chart for the input and output are shown in Figures 9 and 11, where the input and output impedances of the transistor are transformed to  $50\Omega$  using a combination of inductors and capacitors, in this case an L-section matching network.

The adaptation mesh for the input was done with a shunt capacitor and a series inductor and the equivalent circuit is shown in Figure 10. The values of the components were also calculated using the equations for impedance transformation as a form of validation.

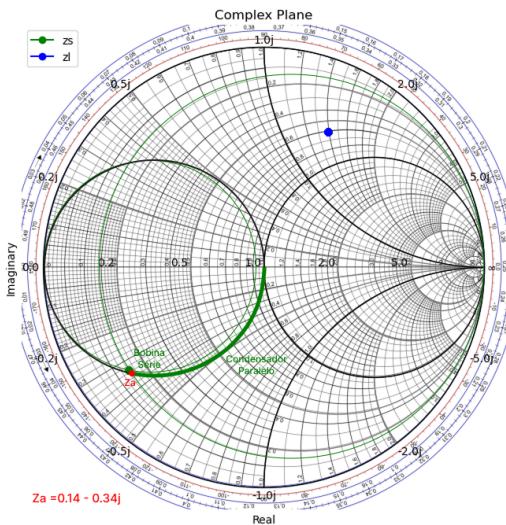
The adaptation mesh for the output is done with a series inductor and a shunt inductor and the equivalent circuit is shown in Figure 12. The values of the components were also calculated using the equations for impedance transformation as a form of validation.

After retrieving the values of the in-between impedances  $Z_a$  from the Smith Chart, it is possible to obtain the values of the components using the following equations [1]:

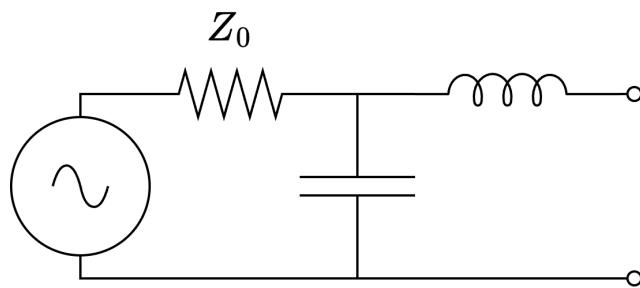
Series inductor:

$$z_L = z_2 - z_1 = jx \quad (x > 0) \quad (17)$$

$$L = \frac{xZ_0}{\omega}$$



**Figure 9:** Smith chart for input matching with lumped elements.



**Figure 10:** Matching circuit for input.

Shunt Inductor:

$$y_L = y_2 - y_1 = -jb \quad (b > 0) \quad (18)$$

$$L = \frac{Z_0}{b\omega}$$

Series Capacitor:

$$z_C = z_2 - z_1 = -jx \quad (x > 0) \quad (19)$$

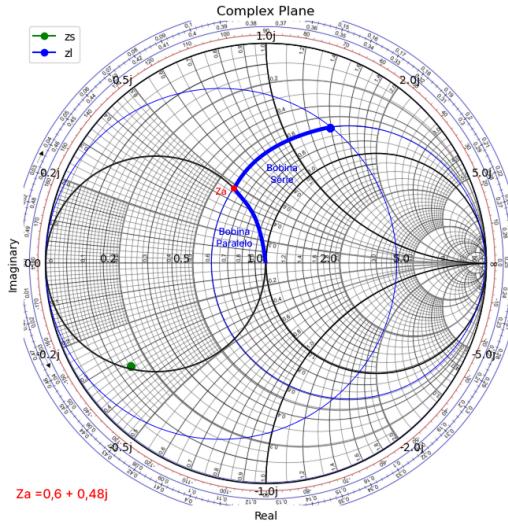
$$C = \frac{1}{xZ_0\omega}$$

Shunt Capacitor:

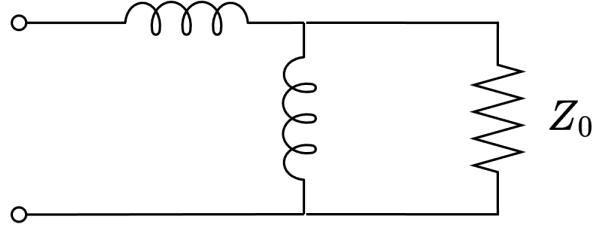
$$y_C = y_2 - y_1 = jb \quad (b > 0) \quad (20)$$

$$C = \frac{b}{Z_0\omega}$$

From input in-between impedance  $Z_a = 0.14 - 0.34j$  and the configuration chosen in the smith chart represented in Figure 10, the values of the components are calculated as follows:



**Figure 11:** Smith chart for output matching with lumped elements.



**Figure 12:** Matching circuit for output.

Shunt Capacitor:

$$y_C = y_a - y_0 = 1 + 2,5j - 1 = 2,5j \quad b = 2,5 \quad (21)$$

$$C_{in} = \frac{2,5}{2\pi 410^9 Z_0} = 1,989 \text{ pF}$$

Series Inductor:

$$z_L = z_s - z_a = 0,14 - 0,33j - 0,14 - 0,34j = 0,01j \quad x = 0,01 \quad (22)$$

$$L_{in} = \frac{0,01 \cdot Z_0}{2\pi 410^9} = 198,9 \text{ fH}$$

From output in-between impedance  $Z_a = 0,6 + 0,48j$  and the configuration chosen in the Smith Chart represented in Figure 12, the values of the components are calculated as follows:

Shunt Inductor:

$$y_L = y_a - y_0 = 1 - 0,81 - 1 = -0,81j \quad b = 0,81 \quad (23)$$

$$L_{1out} = \frac{Z_0}{0,81 \cdot 2\pi 4 \cdot 10^9} = 2,46 \text{ nH}$$

Series Inductor:

$$\begin{aligned} z_L = z_l - z_a &= 0,6 + 1,4j - 0,6 + 0,48 = 0,92j \\ x &= 0,92 \\ L_{2out} &= \frac{0,92 \cdot Z_0}{2\pi 4 \cdot 10^9} = 1,83 \text{ nH} \end{aligned} \quad (24)$$

### Results with analytic approach:

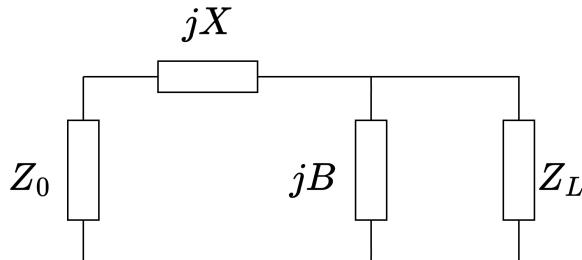
The matching using the analytic approach was done using a Python script (Appendix A) that calculates the values of the components based on the input and output impedances of the transistor. The equations used in the script are the following [1]:

Matching for  $z$  inside the  $1+jx$  circle:

$$B = \frac{x_l \pm \sqrt{rl/z_0} \sqrt{r_l^2 + x_l^2 - z_0 r_l}}{r_l^2 + x_l^2} \quad (25)$$

$$X = \frac{1}{B} + \frac{x_l z_0}{r_l} - \frac{z_0}{B r_l} \quad (26)$$

For this case the network is designed with a series reactance and a shunt susceptance, where  $B$  is the component susceptance and  $X$  the component reactance, as shown in Figure 13.



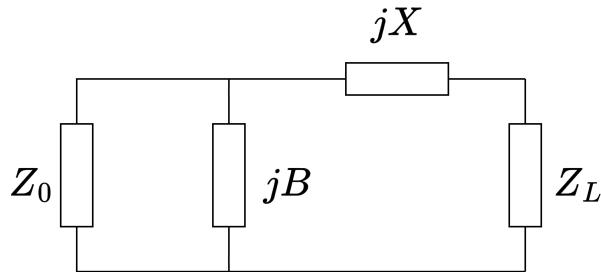
**Figure 13:** Matching circuit for  $z$  inside the  $1+jx$  circle.

Matching for  $z$  outside the  $1+jx$  circle:

$$X = \pm \sqrt{r_l(z_0 - r_l)} - x_l \quad (27)$$

$$B = \pm \frac{\sqrt{(z_0 - r_l)/r_l}}{z_0} \quad (28)$$

For this case the network is designed with a shunt susceptance and a series reactance, as shown in Figure 14.



**Figure 14:** Matching circuit for  $z$  outside the  $1 + jx$  circle.

With  $B$  being the component susceptance and  $X$  the component reactance,  $r_l$  the real part of the impedance  $z$  and  $x_l$  the imaginary part of the normalized impedance  $z$ .

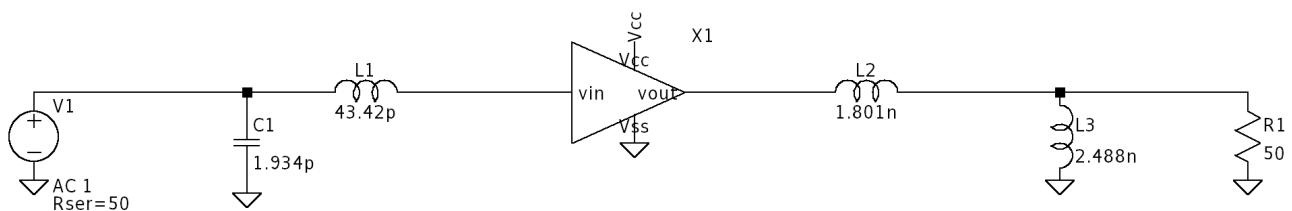
The results of the matching networks using the analytic approach are shown in Table 5, where the values of the components are calculated based on the input and output impedances of the transistor.

**Table 5:** Values of the components for the matching networks using the analytic approach.

Parameter	Value
$C_{in}$	1.93417775 pF
$L_{in}$	43.4243305 pH
$L_{1out}$	2.4877816 nH
$L_{2out}$	1.8095882 nH

Comparing the values obtained from the Smith Chart and the analytic approach, it is possible to see that the values are very similar, with a difference of less than 5% in all cases. This validates the results obtained from the Smith Chart.

The resulting circuit, with the final values, is shown in Figure 15.



**Figure 15:** Matching circuit for input and output with final values.

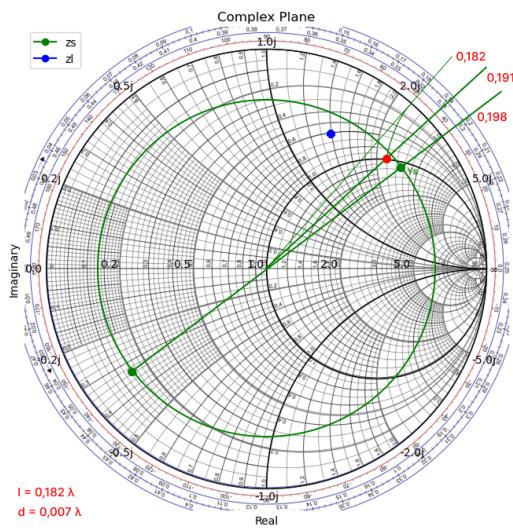
#### 2.4.2 Matching lines and stubs

The matching networks were also designed using transmission lines and stubs, this type of adaptation allows greater frequencies (more than 1 GHz) in real conditions. The input and output impedances of the transistor were transformed to  $50\Omega$  using a combination of transmission lines and stubs. The values were obtain with the Smith Chart and with an analytic

approach using a Python script (Appendix A) that calculates the values of the components based on the input and output impedances of the transistor.

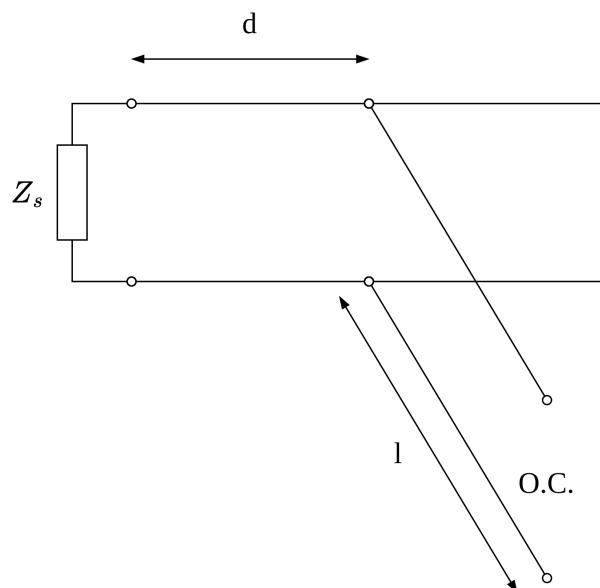
### Results with the Smith Chart:

The matching using the Smith Chart for the input and output are shown in Figures 16 and 18.



**Figure 16:** Smith chart for input matching with lines and stubs

The adaptation mesh for the input was done with an open circuit shunt stub and a series line, as shown in Figure 17.

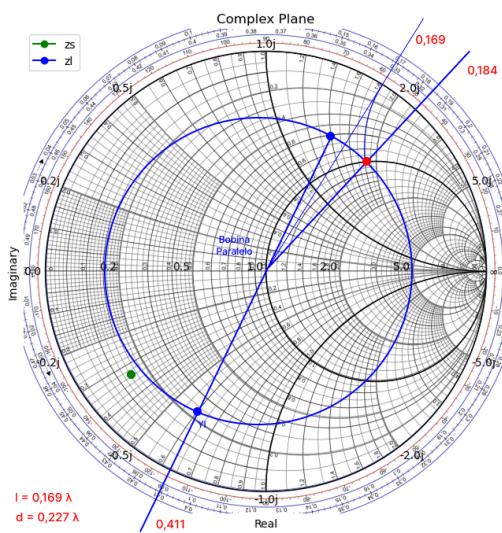


**Figure 17:** Matching circuit for input with lines and stubs

The values obtain from the Smith Chart for the input matching network are shown in Table 6.

**Table 6:** Values of the components for the matching networks using the Smith Chart with lines and stubs.

Parameter	Value
$l$	$0,182\lambda$
$d$	$0,007\lambda$



**Figure 18:** Matching circuit for input with lines and stubs

The adaptation mesh for the output is done with a series line and an open circuit shunt stub as shown in Figure 19.

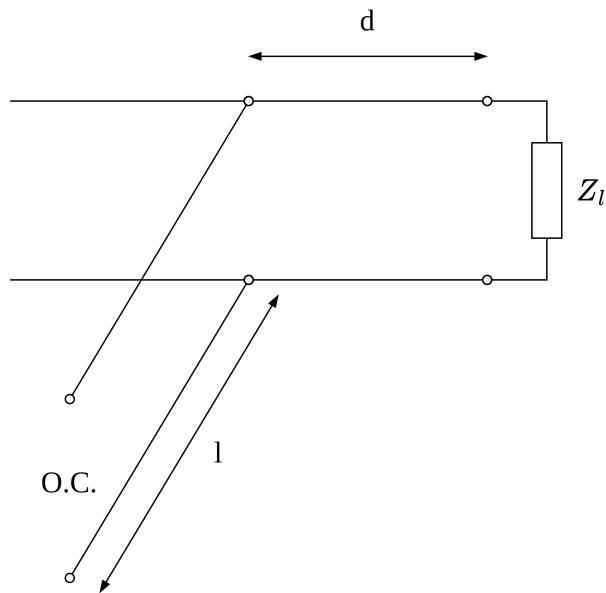
The values obtain from the Smith Chart for the output matching network are shown in Table 7.

**Table 7:** Values of the components for the matching networks using the Smith Chart with lines and stubs.

Parameter	Value
$l$	$0,169\lambda$
$d$	$0,227\lambda$

### Results with analytic approach:

The expressions used in the Python script to calculate the values of the components are the following [1]:



**Figure 19:** Matching circuit for output with lines and stubs

Considering an impedance  $Z$ :

$$Y = G + jB = \frac{1}{Z} \quad (29)$$

Where  $G$  is the conductance and  $B$  is the susceptance and can be calculated as:

$$G = \frac{R_l(1+t^2)}{R_L^2 + (X_L + Z_0 t)^2} \quad (30)$$

$$B = -\frac{R_l^2 t - (Z_0 - X_L t)(X_L + Z_0 t)}{Z_0 [R_L^2 + (X_L + Z_0 t)^2]} \quad (31)$$

Where  $R_l$  is the real part of the impedance,  $X_l$  is the imaginary part of the impedance,  $Z_0$  is the characteristic impedance of the line and  $t$  is the length of the line in wavelengths.

If  $R_L$  is different from  $Z_0$ , the equation for  $t$  can be expressed as:

$$t = \frac{X_L \pm \sqrt{R_L[(Z_0 - R_L)^2 + X_L^2]/Z_0}}{R_L - Z_0} \quad (32)$$

If  $R_L = Z_0$ , the equation for  $t$  can be expressed as:

$$t = \frac{-X_L}{2Z_0} \quad (33)$$

Thus, the solutions for the line lengths  $d$  normalized to the wavelength are:

$$\frac{d}{\lambda} = \begin{cases} \frac{1}{2\pi} \tan^{-1} t & \text{for } t \geq 0 \\ \frac{1}{2\pi} (\pi + \tan^{-1} t) & \text{for } t < 0 \end{cases} \quad (34)$$

Now to find the open-circuited stub length  $l$  normalized to the wavelength, the following equations are used:

$$\frac{l}{\lambda} = \frac{-1}{2\pi} \tan^{-1} \frac{B}{Y_0} \quad (35)$$

To calculate the wavelength  $\lambda$  in the line, the following equation is used:

$$\lambda = \frac{v}{f} \quad (36)$$

And the velocity  $v$  in the line is given by:

$$v = \frac{c}{\sqrt{\epsilon_{eff}}} \quad (37)$$

The effective permittivity  $\epsilon_{eff}$  is calculated as:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + \frac{12h}{w}\right)^{-0.5} \quad (38)$$

where  $w = 1,5\text{mm}$  and  $h = 800\mu\text{m}$  that correspond to the characteristics of the microstrip line used in the design.

The results obtain from the analytic approach are shown in Table 8. It is possible to observe that the values of the components are very similar to the ones obtained from the Smith Chart, with a difference of less than 5% in all cases. This validates the results obtained from the Smith Chart.

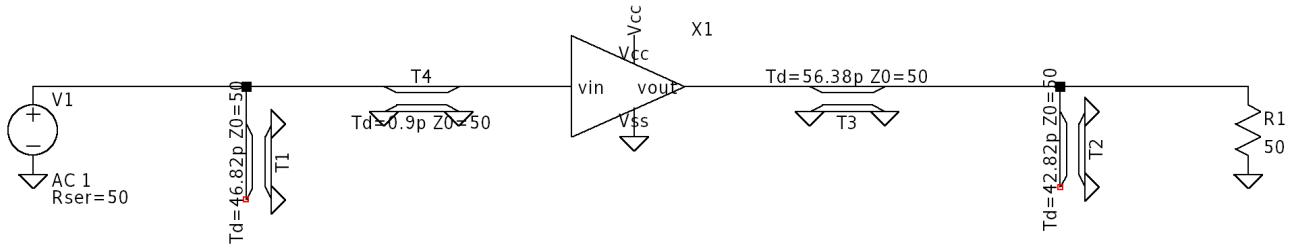
**Table 8:** Values of the components for the matching networks using the analytic approach with lines and stubs.

Parameter	Value
$v$	$171739780, 4465274 \text{ m s}^{-1}$
$\epsilon_{eff}$	$3,051410966570356$
$\lambda$	$42,90158139038047 \text{ mm}$
$l_{in}$	$8,0649 \text{ mm}$
$d_{in}$	$157,9 \mu\text{m}$
$l_{out}$	$7,3823 \text{ mm}$
$d_{out}$	$9,6999 \text{ mm}$

The final circuit is shown in Figure 20, where the input and output matching networks are designed using a combination of transmission lines and stubs.

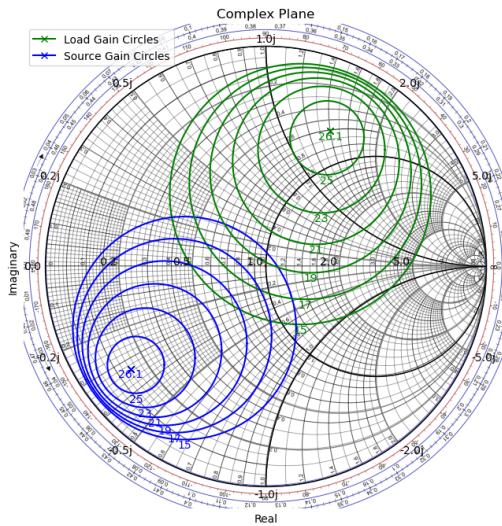
#### 2.4.3 Constant Gain circles

A Python script (Appendix A) was made, in line with [2], to calculate the constant gain circles for the input and output matching networks and plot it in the Smith Chart, which are shown in Figure 21. The constant gain circles are used to visualize the gain of the LNA for different source and load impedances. For maximum gain, the source and load impedances



**Figure 20:** Matching circuit for input and output with values.

should be located on the crosses that represent the maximum gain circles, in this case represent 26, 1 in linear scale or 14, 17dB.



**Figure 21:** Constant gain circles for the input matching network.

## 2.5 Input and output matching networks for Minimum Noise

After designing the LNA for maximum gain, the next step is to design the input and output matching networks for minimum noise. The goal is to minimize the noise figure ( $F$ ).

The noise figure is a measure of how much noise the LNA adds to the signal. The lower the noise figure, the better the LNA performs in terms of noise. And it can be defined as [2]:

$$F = \frac{P_{No}}{P_{Ni}G_A} \quad (39)$$

Where  $P_{No}$  is the output available noise power,  $P_{Ni}$  is the input available noise power due to  $R_n$  and  $G_A$  is the available gain of the LNA.

The available gain of the LNA is defined as:

$$G_A = \frac{P_{So}}{P_{Si}} \quad (40)$$

Where  $P_{So}$  is the output available signal power and  $P_{Si}$  is the input available signal power.

Thus, rewriting equation 39 in terms of the available gain, the noise figure can be expressed as:

$$F = \frac{P_{Si}/P_{Ni}}{P_{So}/P_{No}} = \frac{SNR_i}{SNR_o} \quad (41)$$

When working with scattering and noise parameters, the noise figure can be expressed as [2]:

$$F = F_{min} + \frac{r_n}{g_s} |y_s - y_{opt}|^2 \quad (42)$$

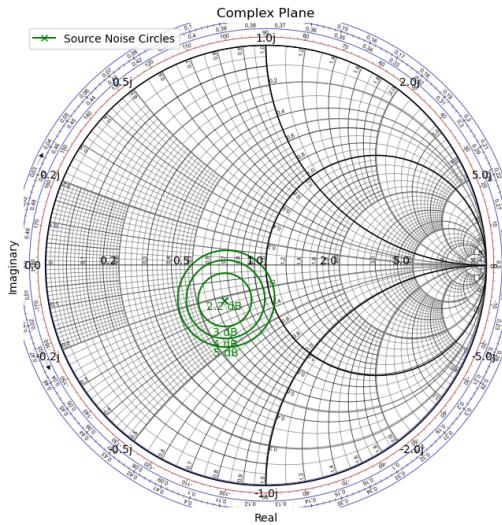
Where  $F_{min}$  is the minimum noise figure,  $r_n$  is the normalized noise resistance,  $g_s$  is the normalized source conductance and  $y_s$  is the normalized source admittance. The  $y_{opt}$  is the optimal source admittance that minimizes the noise figure to the value  $F_{min}$ .

The following noise parameters were obtained in cadence from the transistor model without any matching network, and compiled in Table 9.

**Table 9:** Noise parameters of the transistor.

Parameter	Value
$F_{min}$	2,171
$r_n$	9.505 Ω
$g_s$	1.11479037 S
$y_s$	$1.11479037 + 2.54323358j$ S
$y_{opt}$	$0.02750192 + 0.00928327j$ S
$\Gamma_s$	$-0.1889065597 - 0.1585114245j$

Once again a Python script (Appendix A) was made to calculate and plot the constant input noise figure circles in the Smith Chart, which are shown in Figure 22. The constant noise figure circles are used to visualize the noise figure of the LNA for different source and load impedances. For minimum noise, the source and load impedances should be located on the points that represent the minimum noise figure circles, in this case the crosses, that represent 2, 2dB corresponding to the minimum noise figure of the transistor.



**Figure 22:** Constant noise figure circles for the input matching network.

In order to do the impedance matching for minimum noise, the output reflection coefficient has to be calculated with the following equation [3]:

$$\Gamma_L = \left( \frac{s_{22} + (s_{12}s_{21}\Gamma_s)}{1 - s_{11}\Gamma_s} \right)^* \quad (43)$$

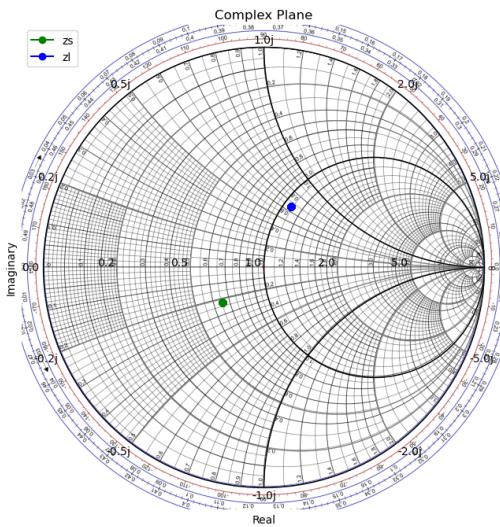
Now for the sake of simplicity, the reflection coefficients were transformed to the normalized impedances using Equations 15 and 16.

In table 10 the normalized impedances at the source and load for minimum noise are shown, where the values are calculated using the reflection coefficients obtained in the previous step.

**Table 10:** Normalized impedances at the source and load for minimum noise.

Parameter	Value
$z_S$	$0.652838 - 0.2203652j \Omega$
$z_L$	$1.07281071 + 0.65421904j\Omega$

In figure 23 the normalized impedances at the source and load for minimum noise are shown in the Smith Chart.



**Figure 23:** Normalized impedances at the source and load for minimum noise in the Smith Chart.

Since the Python script (Appendix A) for calculating the matching networks has already been verified in the previous section, in this section the matching networks were calculated using it, without the use of the Smith Chart. The equations used in the script are the same as in the previous section, but with the values of the normalized impedances at the source and load for minimum noise.

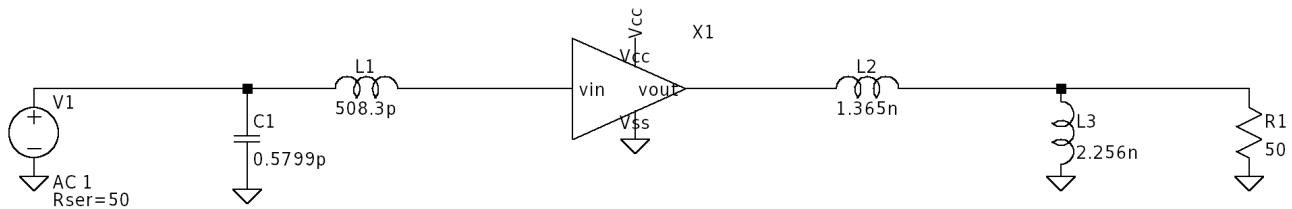
### 2.5.1 Matching with lumped elements for minimum noise

Using the same matching circuits as in the previous sections, depicted in Figures 10 and 12, the values of the components were calculated using the Equations 25 to 28. The results of the matching networks for minimum noise using the analytic approach are shown in Table 11, where the values of the components are calculated based on the input and output impedances of the transistor for minimum noise.

**Table 11:** Values of the components for the matching networks for minimum noise using the analytic approach.

Parameter	Value
$C_{in}$ (shunt)	0.5798506944259898 pF
$L_{in}$ (series)	0.5083089871809204 nH
$L_{1out}$ (shunt)	2.25632568 nH
$L_{2out}$ (series)	1.36538599 nH

In Figure 24 the final circuit with the values of the components for minimum noise is shown, where the input and output matching networks are designed using a combination of inductors and capacitors.



**Figure 24:** Matching circuit for input and output with final values for minimum noise.

### 2.5.2 Matching lines and stubs for minimum noise

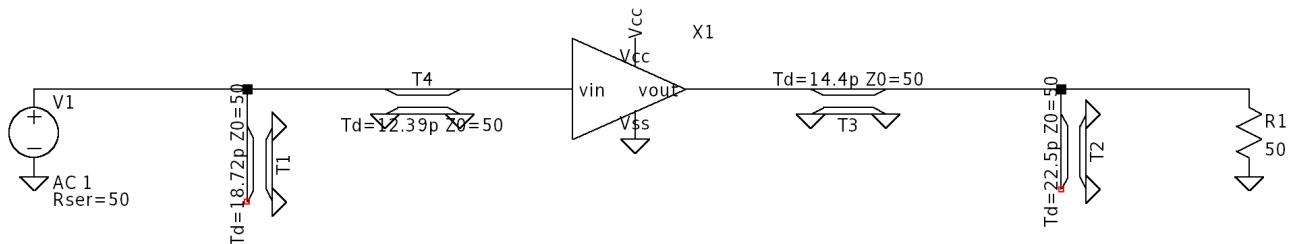
Using the same matching circuits as in the previous sections, depicted in Figures 17 and 19, the values of the components were calculated using the Equations 34 to 35 in the Python script (Appendix A).

The results of the matching networks for minimum noise using the analytic approach are shown in Table 12.

**Table 12:** Values of the components for the matching networks for minimum noise using the analytic approach with lines and stubs.

Parameter	Value
$l_{in}$	3, 21 mm
$d_{in}$	2, 13 mm
$l_{out}$	3, 87 mm
$d_{out}$	2, 47 mm

The final circuit with the values of the components for minimum noise is shown in Figure 25, where the input and output matching networks are designed using a combination of transmission lines and stubs.

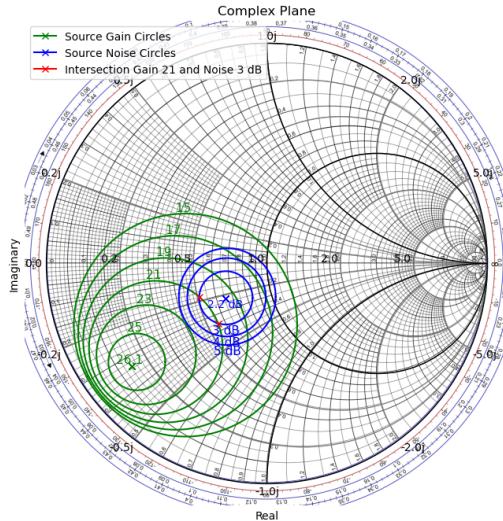


**Figure 25:** Matching circuit for input and output with values for minimum noise.

## 2.6 Gain-Noise Optimization

To optimize the LNA for both gain and noise, a trade-off between the two parameters is necessary. The goal is to find a balance between the maximum gain and the minimum noise

figure. To obtain this result the input gain circles and the input noise circles were plotted in the Smith Chart and analyzed, the plot is shown in Figure 26.



**Figure 26:** Gain and noise circles for the input matching network.

The intersection of the gain and noise circles represents the optimal point for the LNA, where the gain is maximized ( $G = 21$ ) while the noise figure is minimized ( $F = 3\text{dB}$ ).

In table 13 the values of the intersection points of the 21 gain circle and the 3 dB noise figure circle are shown, where the values were calculated using the Python script (Appendix A).

**Table 13:** Values of the intersection points of the gain and noise circles.

Parameter	Value
$\Gamma_{A1}$	$-0.30695536 - 0.15142555j \Omega$
$\Gamma_{A2}$	$-0.22141437 - 0.27183862j \Omega$
$z_{A1}$	$0.51000409 - 0.17495104j \Omega$
$z_{A2}$	$0.56016594 - 0.34723135j \Omega$

For the following calculations  $\Gamma_s = \Gamma_{A1}$  and  $z_{A1} = z_s$  will be used.

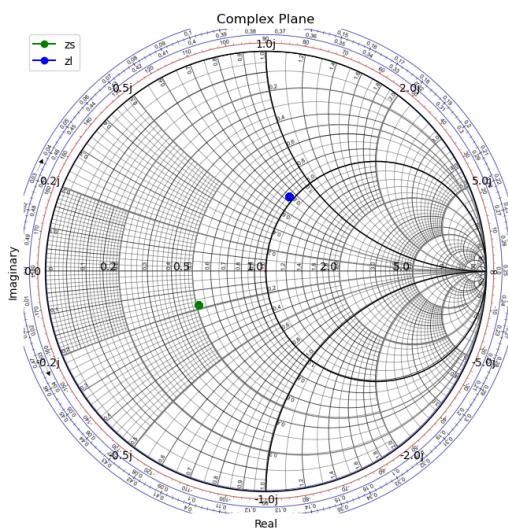
Once again in order to obtain a bilateral matching network, the output reflection coefficient has to be calculated with the equation 43. With the reflection coefficient value, it is possible to obtain the normalized impedance at the load using the equation 16.

In table 14 the normalized impedances at the source and load and the reflection coefficients for gain-noise optimization are shown.

**Table 14:** Normalized impedances at the source and load for gain-noise optimization.

Parameter	Value
$z_S$	$0.51000409 - 0.17495104j \Omega$
$z_L$	$0.95353092 + 0.74623035j\Omega$
$\Gamma_S$	$-0.30695536 - 0.15142555j$
$\Gamma_L$	$0.10657803 + 0.34127875j$

In Figure 27 the normalized impedances at the source and load for gain-noise optimization are shown in the Smith Chart.



**Figure 27:** Normalized impedances at the source and load for gain-noise optimization in the Smith Chart.

### 2.6.1 Matching with lumped elements for gain-noise optimization

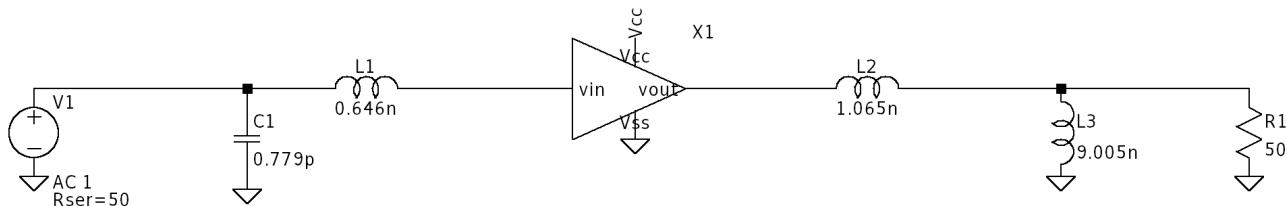
Using the same matching circuits as in the previous sections, depicted in Figures 10 and 12, the values of the components were calculated using the Equations 25 to 28 in the Python script (Appendix A).

The results of the matching networks for gain-noise optimization using the analytic approach are shown in Table 15.

**Table 15:** Values of the components for the matching networks for gain-noise optimization using the analytic approach.

Parameter	Value
$C_{in}$ (shunt)	0.779402735 pF
$L_{in}$ (series)	0.64596288 nH
$L_{1out}$ (shunt)	9.00487954 nH
$L_{2out}$ (series)	1.06497606 nH

In Figure 28 the final circuit with the values of the components for gain-noise optimization is shown.



**Figure 28:** Matching circuit for input and output with final values for gain-noise optimization.

### 2.6.2 Matching lines and stubs for gain-noise optimization

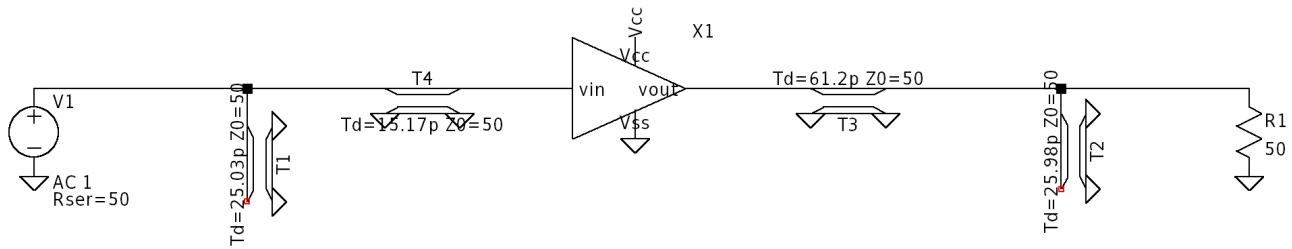
Once again were used the same matching circuits as in the previous sections, depicted in Figures 17 and 19, the values of the components were calculated using the Equations 34 to 35 in the Python script (Appendix A).

The results of the matching networks for gain-noise optimization using the analytic approach are shown in Table 16.

**Table 16:** Values of the components for the matching networks for gain-noise optimization using the analytic approach with lines and stubs.

Parameter	Value
$l_{in}$	4,299 mm
$d_{in}$	2,605 mm
$l_{out}$	4,462 mm
$d_{out}$	10,511 mm

The final circuit with the values of the components for gain-noise optimization is shown in Figure 29, where the input and output matching networks are designed using a combination of transmission lines and stubs.



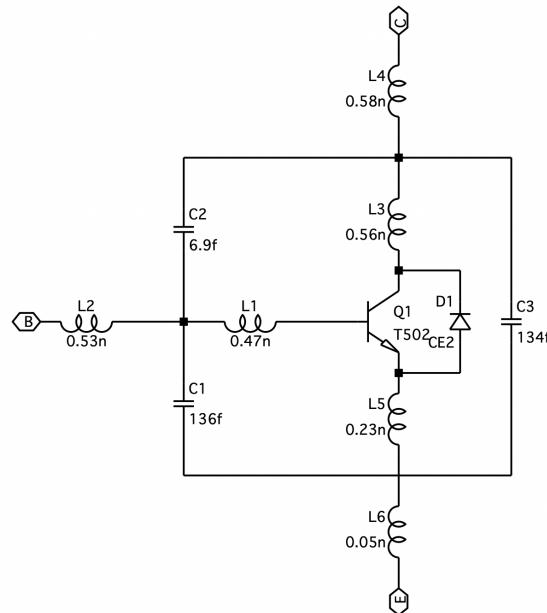
**Figure 29:** Matching circuit for input and output with values for gain-noise optimization.

### 3 Simulation and Results analysis

In order to simulate the LNA, the LTSpice and Cadence software were used to validate the results obtain in the previous section.

#### 3.1 Validation of the LNA design

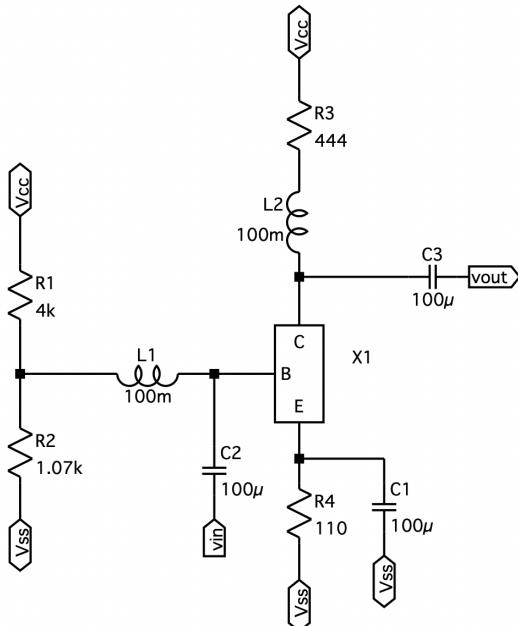
The first step was to create a transistor schematic using the T502 transistor, which is a transistor with a low noise figure and high gain, suitable for LNA applications. The schematic of the transistor can be seen in Figure 30. In this schematic the packaging effects were considered, which is important for high frequency applications like this one, since the parasitic capacitance and inductance affect the performance of the circuit.



**Figure 30:** Transistor with packaging effects.

In a transistor simulation that can be close to the real one, the biasing circuit is essential to ensure that the transistor operates in the correct region. The biasing circuit was designed

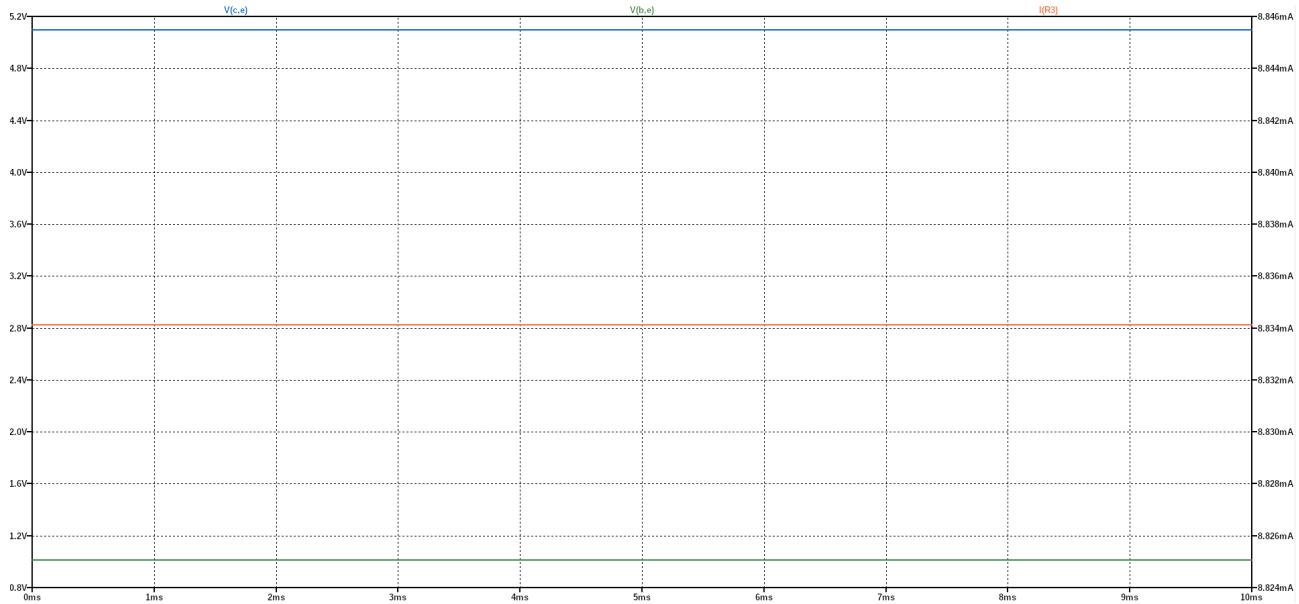
to provide the necessary DC voltage and current required in the initial parameters, so it can operate properly. The biasing circuit can be seen in Figure 31.



**Figure 31:** Biasing circuit simulated.

The operating point of the circuit was simulated using LTSpice, where the DC analysis was performed to obtain the biasing parameters. The goal is to ensure that the transistor operates in the active region, which is essential for amplification. The parameters to be obtained are the DC voltage at the collector ( $V_{CE}$ ), the DC voltage at the base ( $V_{BE}$ ), and the DC current at the collector ( $I_C$ ).

The results of the operation point simulation is shown in Figure 32.



**Figure 32:** Result of the operating point simulation.

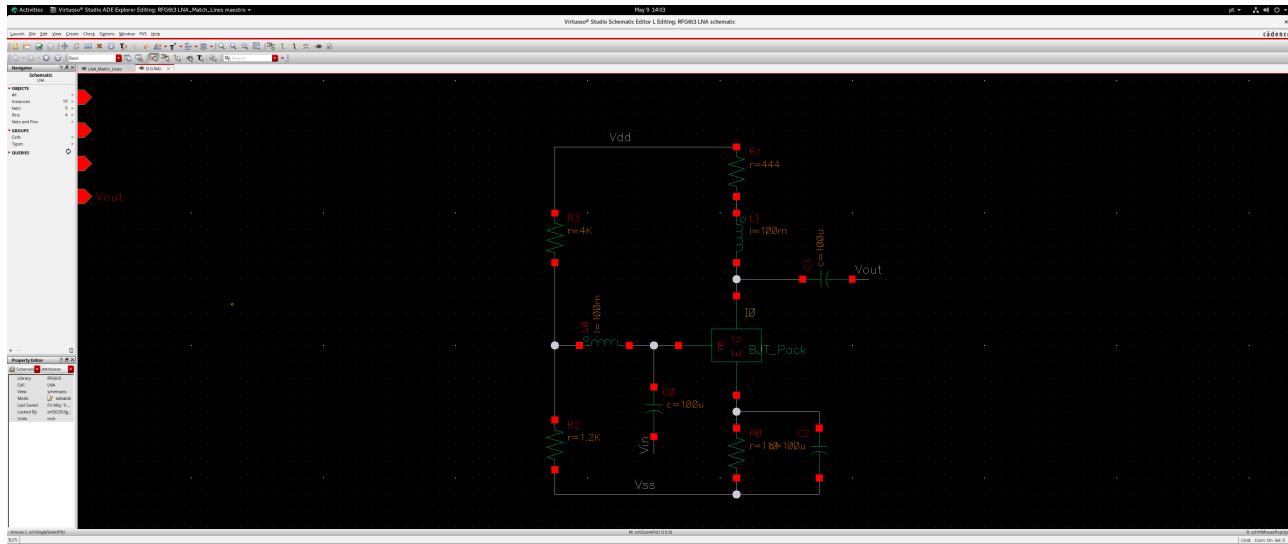
In table 17 the results of the biasing circuit are summarized.

**Table 17:** Biasing circuit parameters.

Parameter	Value
$V_{CE}$	5.094 V
$V_{BE}$	1.012 V
$I_C$	8.83 mA

The results obtain are within the required parameters for the biasing circuit designed in the previous section. With the transistor biasing validated was possible to proceed with the simulations for the matching networks.

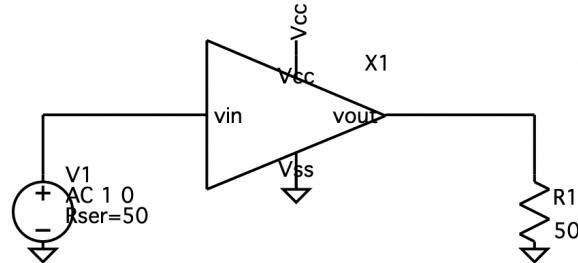
At the same time, the same circuit was implemented in Cadence, to ensure greater reliability of the results obtained. The schematic implementation in Cadence can be seen in Figure 33.



**Figure 33:** Biasing circuit simulated in Cadence

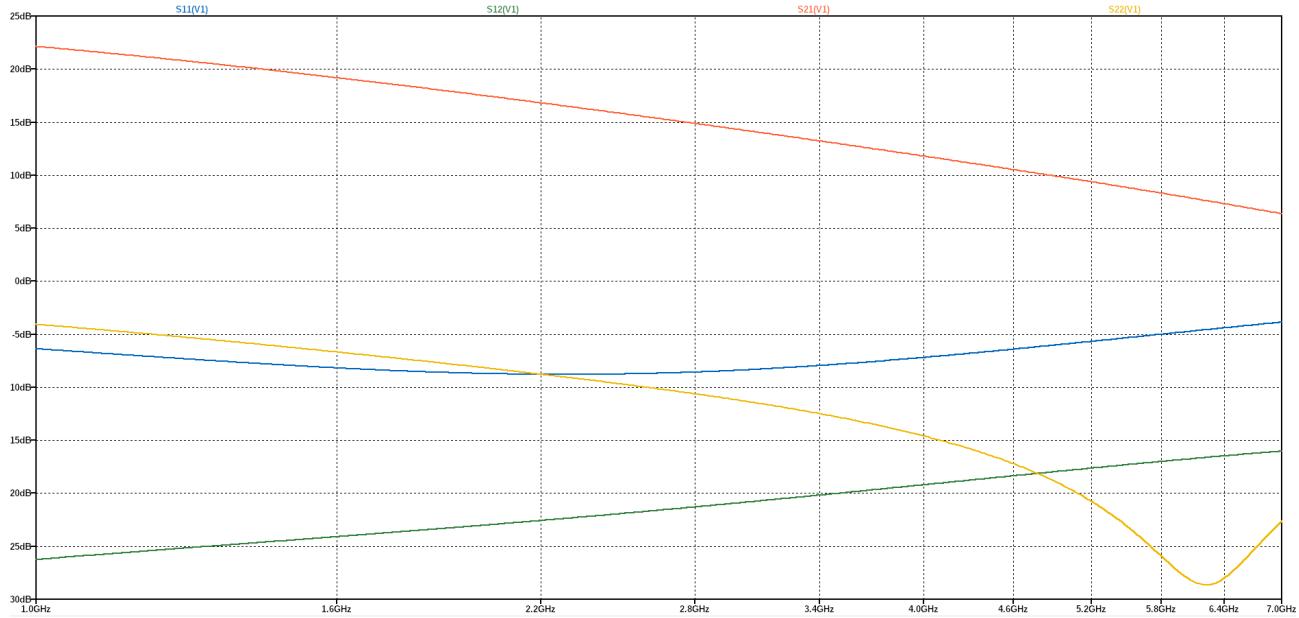
### 3.2 Simulation without matching networks

As mentioned before, the first step in designing a matching network of an LNA is to know the S-parameters of the amplifier circuit for the range of frequencies, so, switching to an AC analysis of the LNA circuit, and adding both the source and the load ( $50\Omega$ ), the schematic of the simulated circuit in LTSpice is shown in Figure 34.



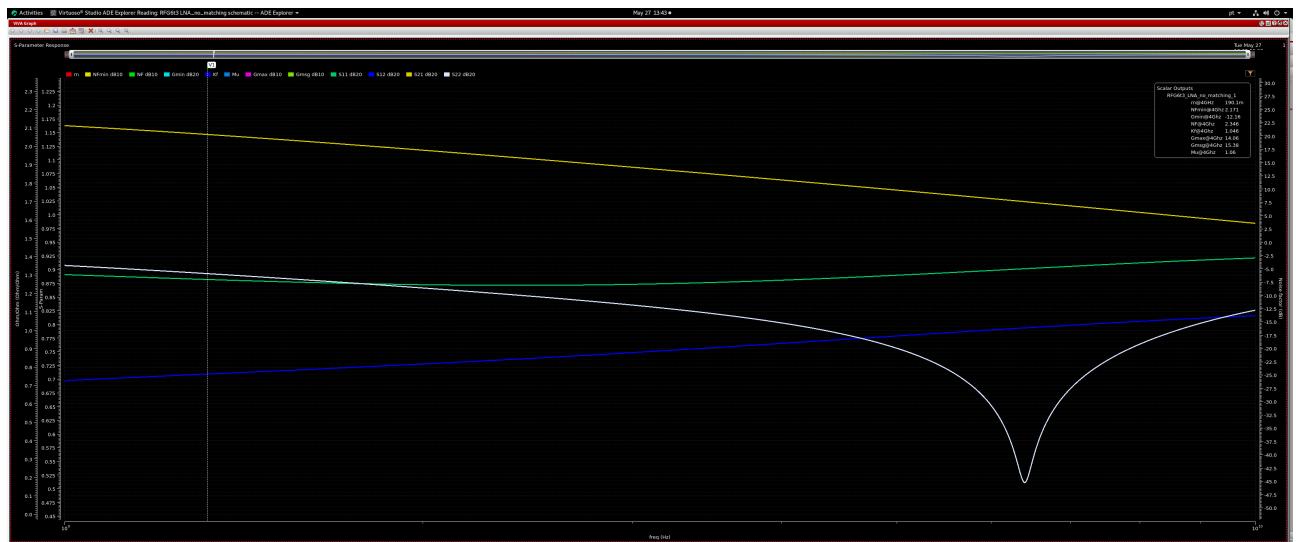
**Figure 34:** Circuit for the S-parameters

The resulting S-parameters obtain in LTSpice were extracted to a s2p file and further processed in a Python script [A](#), the resultant s-parameters without matching networks in LTSpice can be seen in Figure 35.



**Figure 35:** S-parameters for the LNA circuit

The same simulation was done in Cadence, and the results can be seen in Figure 36.



**Figure 36:** S-parameters for the LNA circuit in Cadence.

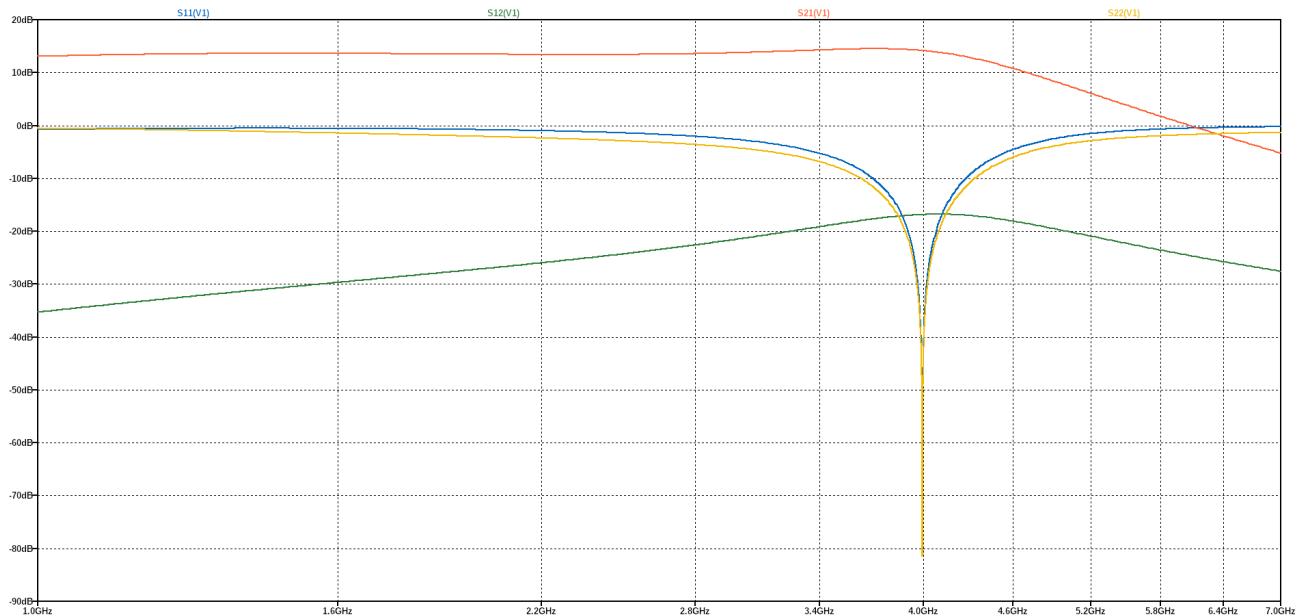
### 3.3 Simulation for Maximum Gain Adaptation

After assuming a working frequency of 4GHz at the previous section, the resulting matching networks for maximum gain were simulated, first in LTSpice and then in Cadence, in order to validate the results obtained.

### 3.3.1 Matching networks using Lumped circuit elements

The matching networks for input and output depicted in Figure 9 were used to perform the simulation and validate the results.

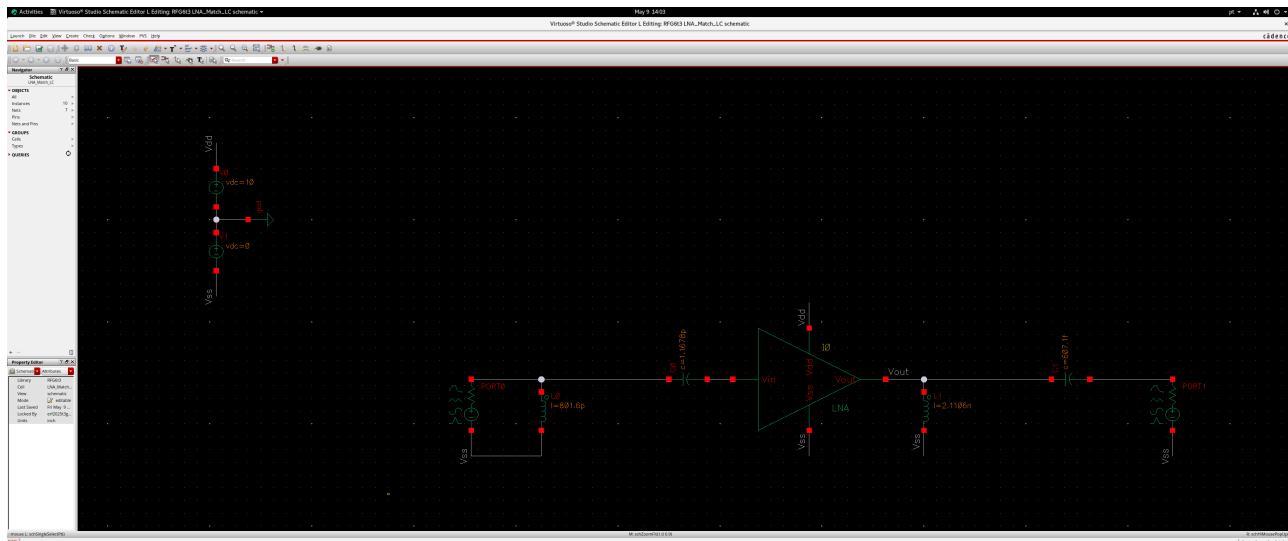
First, the simulation was done in LTSpice and the results can be seen in Figure 37.



**Figure 37:** Matching networks using lumped circuit elements in LTSpice.

After looking at the graphic above, it is possible to conclude that this matching network is working properly, since there is a sharp drop in both  $S_{11}$  and  $S_{22}$  at the desired frequency of  $4\text{GHz}$  as well as a high point in the  $S_{21}$  curve that is the maximum gain of the circuit, which is around  $14\text{dB}$  as expected.

For more accurate results, the same circuit was simulated in Cadence, and the schematic can be seen in Figure 38.



**Figure 38:** Matching networks using lumped circuit elements in Cadence.

The graphical results of the simulation in Cadence can be seen in Figure 39.



**Figure 39:** S-parameters for the matching networks using lumped circuit elements in Cadence.

In table 18 the results of the matching networks using lumped circuit elements are summarized.

**Table 18:** Matching network results using lumped circuit elements in Cadence.

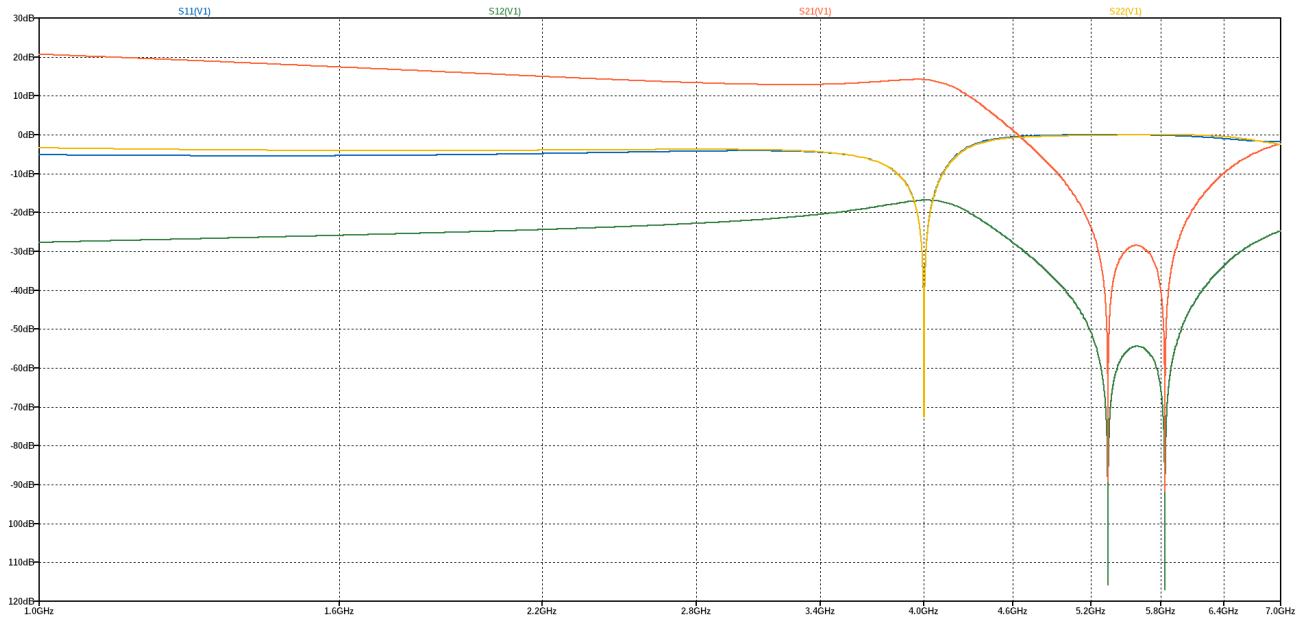
Parameter	Value
LTS spice $S21$	14.18dB
Cadence $S21$	14.06dB

Observing the results, it is possible to conclude that the matching networks using lumped circuit elements are working properly, since the  $S_{21}$  parameter is around  $14dB$  in both LTSpice and Cadence, which is close to the expected value of  $14, 17dB$  calculated in the previous section.

### 3.3.2 Matching networks using transmission lines and stubs

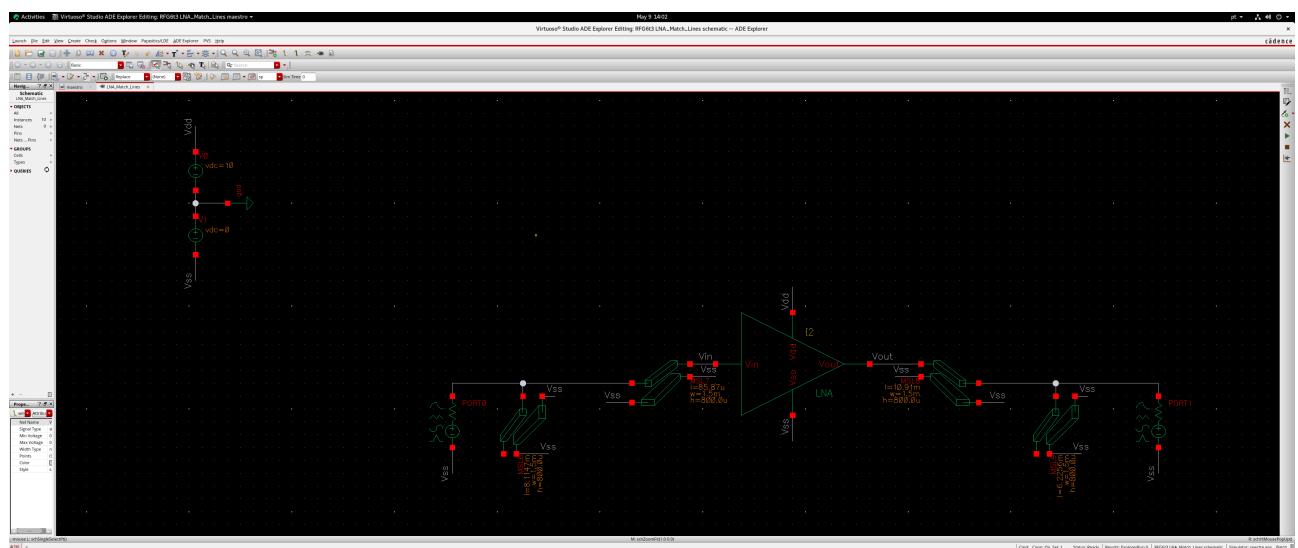
The matching networks for input and output depicted in Figure 20 were used to perform the simulation and validate the results.

First, the simulation was done in LTSpice and the results can be seen in Figure 40.



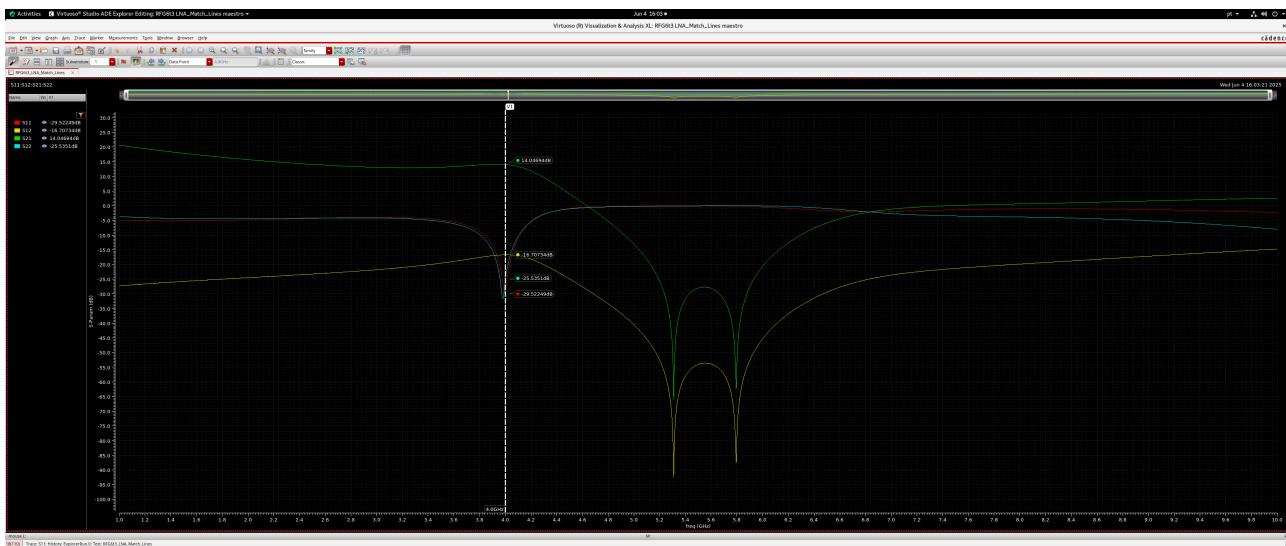
**Figure 40:** Matching networks using transmission lines and stubs in LTSpice.

In cadence, the circuit for using transmission lines and stubs is depicted in Figure 41.



**Figure 41:** Matching networks using transmission lines and stubs in Cadence.

The graphical results of the s-parameters simulation in Cadence can be seen in Figure 42.



**Figure 42:** S-parameters for the matching networks using transmission lines and stubs in Cadence.

Similarly to the first matching networks, the drop in both  $S_{11}$  and  $S_{22}$  can also be seen, as well as the same approximated value of  $S_{21}$ , so, this matching network using transmission lines and stubs is correctly working.

The summarized results of the matching networks using transmission lines and stubs can be seen in table 19.

**Table 19:** Matching network results using transmission lines and stubs in Cadence.

Parameter	Value
LTS spice $S_{21}$	14.18dB
Cadence $S_{21}$	14.05dB

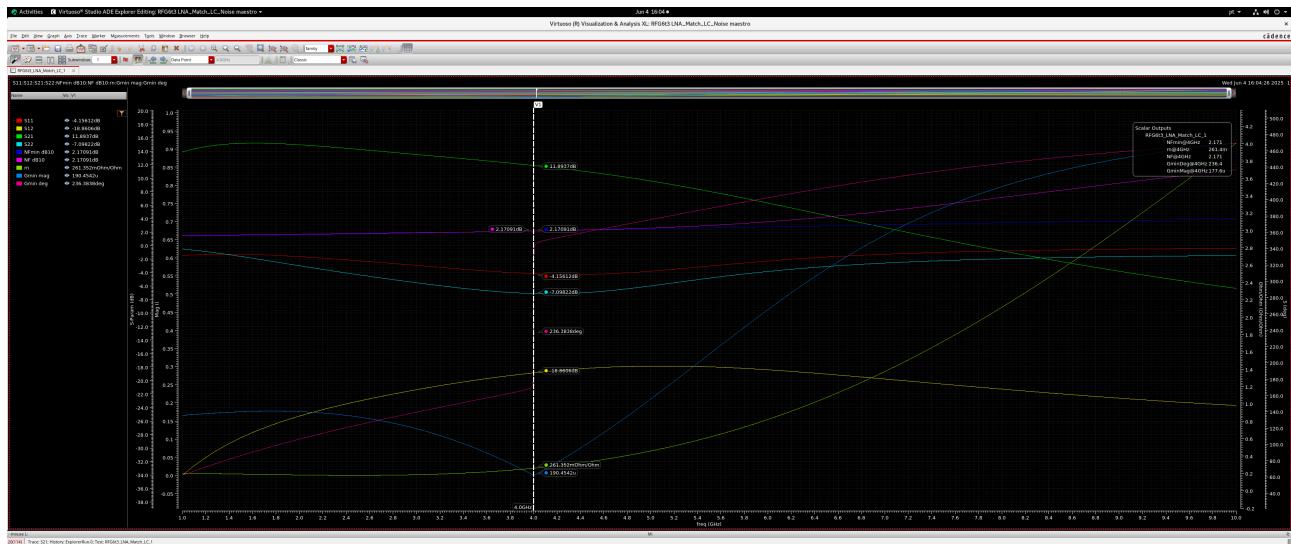
### 3.4 Simulation for Minimum Noise Adaptation

In order to adapt the LNA for minimum noise figure, the matching networks were designed to minimize the noise figure at the desired frequency of  $4\text{GHz}$ , in this section the design matching networks were simulated and validated in Cadence.

#### 3.4.1 Matching networks using Lumped circuit elements

The matching networks for input and output depicted in Figure 24 were used to perform the simulation and validate the results.

The results of the simulation in Cadence can be seen in Figure 43.



**Figure 43:** Matching networks using lumped circuit elements for minimum noise in Cadence.

In table 21 the summarized results of the matching networks using lumped circuit elements for minimum noise can be seen.

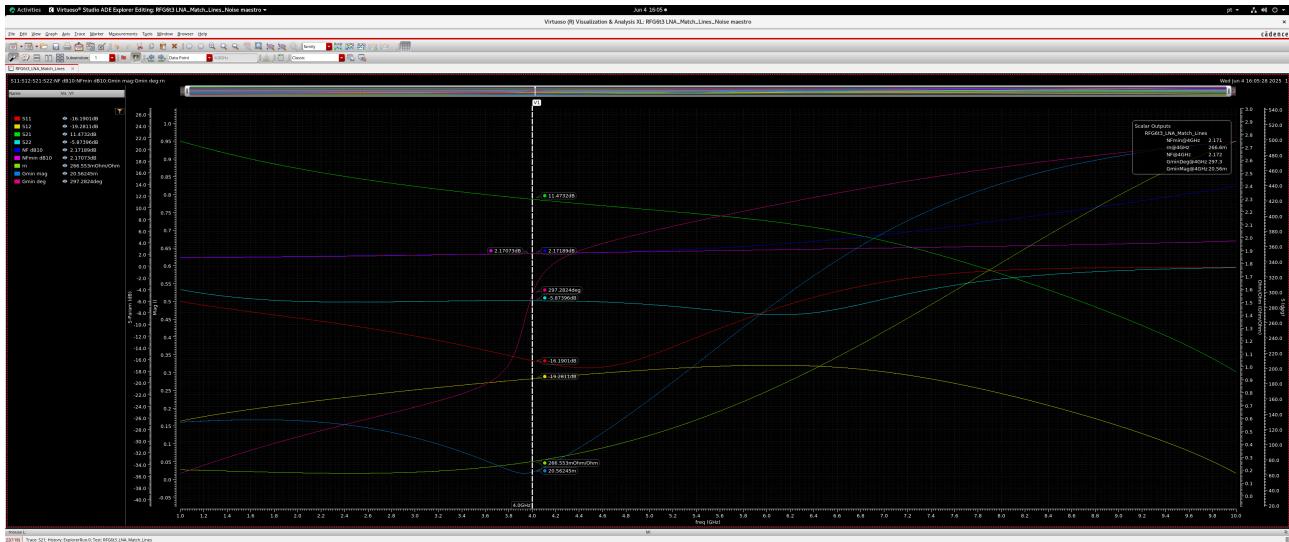
**Table 20:** Matching network results for minimum noise in Cadence.

Parameter	Value
Theoretical Noise Factor	2.17dB
Cadence Noise Factor	2.17dB

### 3.4.2 Matching networks using transmission lines and stubs

The matching networks for input and output depicted in Figure 25 were used to perform the simulation and validate the results.

The results of the simulation in Cadence can be seen in Figure 44.



**Figure 44:** Matching networks using transmission lines and stubs for minimum noise in Cadence.

In table 21 the summarized results of the matching networks using transmission lines and stubs can be seen.

**Table 21:** Matching network results for minimum noise in Cadence.

Parameter	Value
Theoretical Noise Factor	2.17dB
Cadence Noise Factor	2.17dB

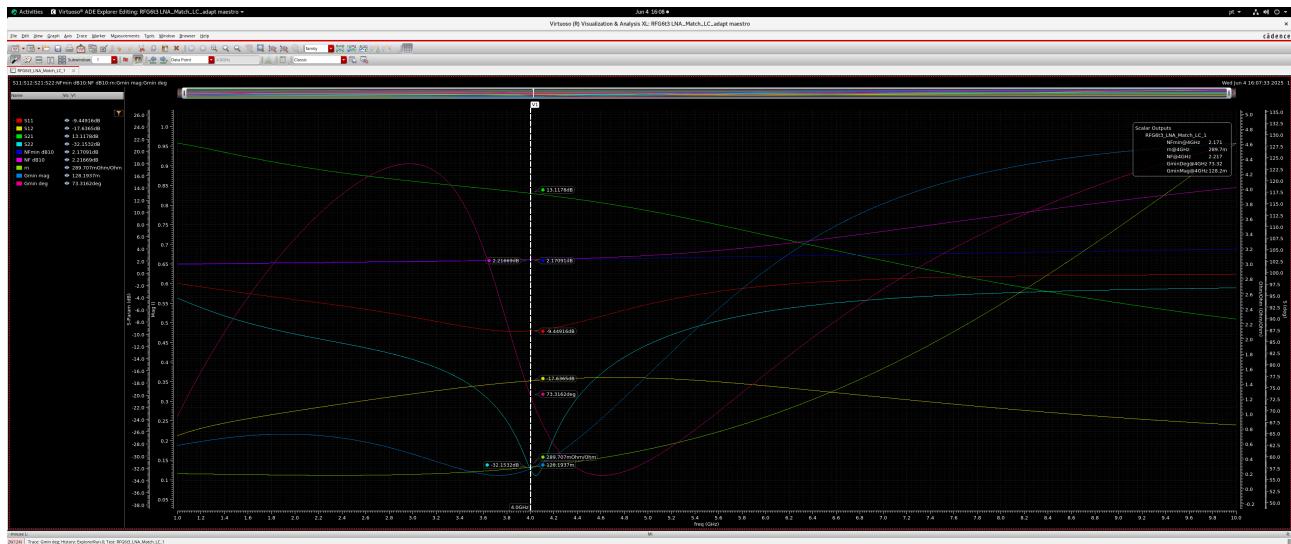
### 3.5 Simulation for Noise-Gain Adaptation

In order to adapt the LNA for minimum noise figure and maximum gain, the matching networks were designed to minimize the noise figure at the desired frequency of  $4GHz$  and maximize the gain at the same frequency, in this section the design matching networks were simulated and validated in Cadence.

#### 3.5.1 Matching networks using Lumped circuit elements

The matching networks for input and output depicted in Figure ?? were used to perform the simulation and validate the results.

The results of the simulation in Cadence can be seen in Figure 45.



**Figure 45:** Matching networks using lumped circuit elements for minimum noise and maximum gain in Cadence.

In table 22 the summarized results of the matching networks using lumped circuit elements for minimum noise and maximum gain can be seen.

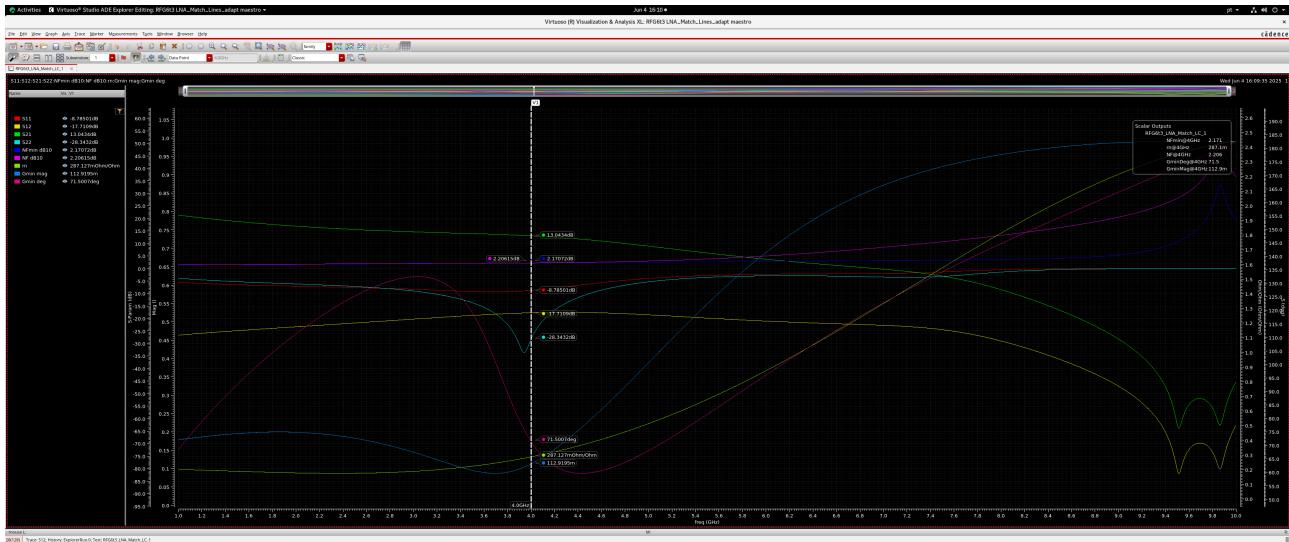
**Table 22:** Lumped elements Matching network results for minimum noise and maximum gain in Cadence.

Parameter	Value
Theoretical Noise Factor	3dB
Cadence Noise Factor	2.2dB
Theoretical Gain	13.22dB
Cadence Gain	13.11dB

### 3.5.2 Matching networks using transmission lines and stubs

The matching networks for input and output depicted in Figure 29 were used to perform the simulation and validate the results.

The results of the simulation in Cadence can be seen in Figure 46.



**Figure 46:** Matching networks using transmission lines and stubs for minimum noise and maximum gain in Cadence.

In table 23 the summarized results of the matching networks using transmission lines and stubs for minimum noise and maximum gain can be seen.

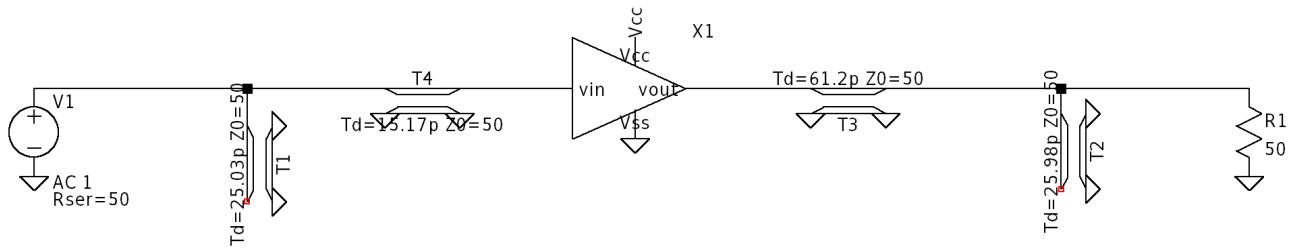
**Table 23:** Lines and Stubs Matching network results for minimum noise and maximum gain in Cadence.

Parameter	Value
Theoretical Noise Factor	3dB
Cadence Noise Factor	2.2dB
Theoretical Gain	13.22dB
Cadence Gain	13.04dB

The results obtain alongside this section show that the type of matching network used does not affect the noise figure of the circuit or the gain, since both types of matching networks obtained results very close to the theoretical values. The choice of implementation of the matching networks will depend on the application and the available components, since the lumped circuit elements are easier to implement, but the transmission lines and stubs are more suitable for high frequency applications, like this one.

## 4 Final Circuit

The final circuit design for the Low Noise Amplifier (LNA) using the BFP420 transistor is shown in Figure 47. The circuit has been optimized to achieve a low noise figure and high gain at the desired frequency of 4 GHz.



**Figure 47:** Final Circuit Design for the LNA using BFP420 Transistor.

The matching networks were implemented using microstrip lines due to their advantages in high-frequency performance, ease of fabrication, and seamless integration with other RF components. The design includes optimized input and output matching networks to ensure maximum power transfer while minimizing reflections. Compared to lumped components, microstrip lines offer lower parasitic effects, better power handling, and improved thermal stability. Additionally, their planar structure allows for compact routing, reduced sensitivity to manufacturing tolerances, and lower insertion losses, contributing to overall higher efficiency in the LNA design.

The final results of the circuit are shown in Table 24, which includes the noise figure, gain, and other relevant parameters.

**Table 24:** Final Results of the LNA Circuit Design

Parameter	Value
Noise Figure (NF)	2.2 dB
Gain (S21)	13.04 dB
Frequency	4 GHz
$I_C$	8.83 mA
$V_{CE}$	5.094 V
$V_{BE}$	1.012 V

## 5 Conclusion

In this report, we have explored the design and simulation of an LNA using a BFP420 transistor. The design process involved determining the biasing conditions, and optimizing the circuit for low noise figure and high gain. The simulation results demonstrated that the LNA meets the design specifications, achieving a noise figure of 2.2 dB and a gain of 13 dB at a frequency of 4 GHz, which are satisfactory results.

The design process also highlighted the importance of careful component selection to minimize noise and maximize performance. The use of simulation tools allowed us to validate our design choices and make necessary adjustments before finalizing the circuit.

The final circuit design, which includes optimized input and output matching networks, was successfully designed using microstrip lines. This choice of microstrip implementation provided

several advantages, such as lower parasitic effects, better power handling, and improved thermal stability, contributing to the overall efficiency of the LNA.

The results of this project demonstrate the effectiveness of the design and simulation process in achieving the desired performance metrics for an LNA. Future work could involve further optimization of the circuit, exploring different transistor models, or implementing additional features to enhance performance.

## References

- [1] D. M. Pozar, *Microwave engineering*, 4th ed. John Wiley and Sons, Inc, 2012.
- [2] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Prentice Hall, 1997.
- [3] L. Oliveira, “Class slides,” 2025.

## A Appendix A: Python Script

The Python script used for the design and simulation of the Low Noise Amplifier (LNA) is provided below. This script utilizes the ‘scikit-rf’ library for RF circuit analysis and design.

GitHub repository: <https://github.com/MartimAgostinho/ERF-Lab2.git>