

MEEC/MEMN

2024 / 2025

Course: Electrónica de Rádio Frequência

Low Noise Amplifier - Part 1

Goal:

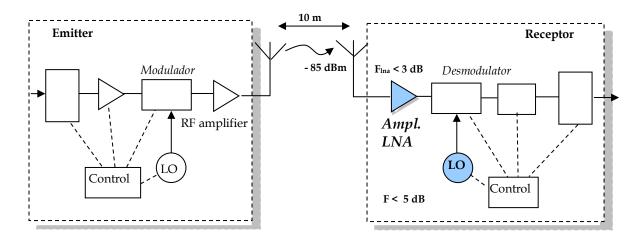
Analysis and design of a LNA with lumped and distributed elements.

http://moodle.fct.unl.pt

Version 1.0 Date: 6th April 2025 Author: Luís Oliveira 2024 / 2025 ERF- Final Project

Motivation

Modern telecommunications systems use high-frequencies with high data-rates. In the receiver path the critical block is the LNA, since, it needs to deal with very low amplitude signals. The LNA has stringent specifications in terns of gain, noise, IM3, P-1dB... In this Project it is expected that the students will understand in detail all these aspects designing an LNA for a ISM (industrial, scientific and medical) band.



Specifications

The LNA for ISM band should fulfill the following specifications:

- ➤ S11 < 10 dB (with Matching networks);
- ➤ S22 < -10 dB (with Matching networks);
- \triangleright F < 3 dB;
- ➤ Gain = MAG = S21 dB (with Matching networks);
- \triangleright 50 Ω load and source.
- \triangleright Characteristic impedance: 50 Ω
- Operation frequency: 3-6 GHz (Bipolar design) (check stability and available gain) please contact professor before start);

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Project assignment

The students should form groups of three. All the groups will use the same transistor BPF420 (form Infineon), with different bias point. Therefore, each group will use a different S-parameter file.

Group	Transistor BFP420	Group	Transistor BFP420	Group	Transistor BFP420
P1G1	IC = 5 mA VCE = 3 V	P2G1	IC = 7 mA VCE = 4 V	P3G1	IC = 10 mA VCE = 5 V
P1G2	IC = 11 mA VCE = 3 V	P2G2	IC = 9 mA VCE = 4 V	P3G2	IC = 8 mA VCE = 5 V
P1G3	IC = 7 mA VCE = 3 V	P2G3	IC = 6 mA VCE = 4 V	P3G3	IC = 12 mA VCE = 5 V
P1G4	IC = 13 mA VCE = 3 V	P2G4	IC = 11 mA VCE = 4 V	P3G4	IC = 7 mA VCE = 5 V
P1G5	IC = 9 mA VCE = 3 V	P2G5	IC = 4 mA VCE = 4 V	P3G5	IC = 14 mA VCE = 5 V
P1G6	IC = 15 mA VCE = 3 V	P2G6	IC = 13 mA VCE = 4 V	P3G6	IC = 9 mA VCE = 5 V
P1G7	IC = 17 mA VCE = 3 V	P2G7	IC = 18 mA VCE = 4 V	P3G7	IC = 20 mA VCE = 5 V

Components

> Transistors

Documents about the BFP420 transistor: Datasheet, spice models are available in the moodle.

Design procedure

1- Project:

<u>LNA</u>

- a. Design the LNA according with the specifications, with a detailed explanation about:
 - i. Design Transistor Bias network;
 - ii. Obtain S-parameters with packaging effects;
 - iii. Transistor validation for the given bias point;
 - iv. Stability.
 - v. Design the input and output matching networks.
 - vi. Determine the gain and NF.

b. Simulation:

- i. Validate the LNA designs using LTSpice.
- ii. Investigate the possibility of changing the input matching, according with the previous specifications of Gain and NF.

2- Report

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- a. The report should have:
 - i. Detailed justification about the options done during the project.
 - ii. Circuit schematics, simulations files, plot, simulation results.
- b. Structure:
 - i. First page with the group number and students identification.
 - ii. Introduction
 - 1. objective
 - iii. Main Body
 - 1. Design
 - 2. Simulations
 - 3. Final circuit
 - 4. Analysis of Results
 - iv. Conclusions

3- Delivery

a. Date: 10-05-2025

b. Place: upload in moodle

Contacts

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