NOVA SCHOOL OF SCIENCE & TECHNOLOGY

MIEEC/MIEMN

2024 / 2025

Course : **Electrónica de Rádio Frequência**

Low Noise Amplifier – Part 2

Goal:

Analysis and design of a CMOS LNA.

http://moodle.fct.unl.pt

Version 1.0
Date: 12th May 2025
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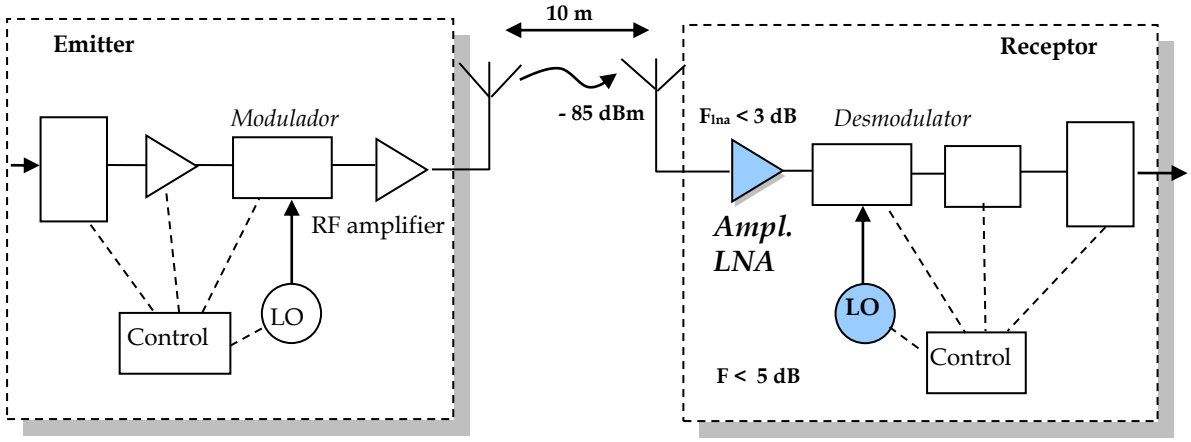
Motivation

Modern telecommunications systems use high-frequencies with high data-rates. In the receiver path the critical block is the LNA, since, it needs to deal with very low amplitude signals. The LNA has stringent specifications in terns of gain, noise, IM3, P^{-1}dB... In this Project it is expected that the students will understand in detail all these aspects designing an LNA for a ISM (industrial, scientific and medical) band.



Specifications

The LNA should fulfill the following specifications:

- S11 < - 10 dB;
- S22 < -10 dB;
- F < 3 dB;
- Gain > 10dB (= MAG 1st part);
- 0.1 - 2 GHz with 350 nm CMOS and 65nm (5GHz) and 45 nm (10 GHz);

Project assignment

Group	Transistor 350 nm CMOS	Group	Transistor 350 nm CMOS	Group	Transistor 350 nm CMOS
P1G1	VDD = 3 V n = 1.75	P2G1	VDD = 3.3 V n = 1.75	P3G1	VDD = 2.5 V n = 1.75
P1G2	VDD = 3 V n = 2	P2G2	VDD = 3.3 V n = 2	P3G2	VDD = 2.5 V n = 2
P1G3	VDD = 3 V n = 2.25	P2G3	VDD = 3.3 V n = 2.25	P3G3	VDD = 2.5 V n = 2.25
P1G4	VDD = 3 V n = 2.5	P2G4	VDD = 3.3 V n = 2.5	P3G4	VDD = 2.5 V n = 2.5
P1G5	VDD = 3 V n = 2.75	P2G5	VDD = 3.3 V n = 2.75	P3G5	VDD = 2.5 V n = 2.75
P1G6	VDD = 3 V n = 3	P2G6	VDD = 3.3 V n = 3	P3G6	VDD = 2.5 V n = 3
P1G7	VDD = 3 V n = 3.25	P2G7	VDD = 3.3 V n = 3.25	P3G7	VDD = 2.5 V n = 3.25

Optional: a) technology 65nm (cadence) VDD=1.2 V, b) technology of 45nm (LTSPICE) VDD = 1 V

Components

- **Transistors**

Using 350 nm and optional: 45 nm CMOS technology in simulator LTSPICE and 65nm (cadence in Lab)

Design procedure

1- Project:

LNA

a. Design the LNA using the circuit topology combined CG + CS stages.
   i. Design Transistor Bias and sizing for CG and CS (each stage gain = MAG or > 10 dB).
   ii. Determine the gain and NF.
   iii. Implement the ratio n between CG and CS gm.
   iv. Implement the LNA with minimum L (350nm) and compare with 130nm (optional) and 45 nm technology.
   v. Design the output buffer for output Z0 match.

b. Simulation:
   i. Validate LNA design using Spice.
   ii. Simulate ratio n between CG and CS gm and check the differences in Gain, NF and Power consumption.
   iii. Compare the results between different CMOS technologies.

2- Report

a. The report should have:
    i. Detailed justification about the options done during the project.
    ii. Circuit schematics, simulations files, plot, simulation results.

b. Structure:
    i. First page with the group number and students identification.
    ii. Introduction
        1. Objective
        2. Motivation
    iii. Main Body
        1. Design
        2. Simulations
        3. Final circuit
        4. Analysis of Results
        5. Comparison between bipolar and CMOS design.
    iv. Conclusions

3- Delivery

a. Date: 12-06-2025
b. Place: upload in moodle

Contacts

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