NOVA SCHOOL OF
SCIENCE & TECHNOLOGY

MEEC/MIEEC

Radio Frequency Electronics

Low Noise Amplifier - Part II

Authors:

Martim Duarte Agostinho (70392) md.agostinho@campus.fct.unl.pt
Francisco Simões Coelho Sá da Costa (70386) fsc.costa@campus.fct.unl.pt
Sofia Margarida Mafra Dias Inácio (58079) sm.inacio@campus.fct.unl.pt

2024/2025 – 2nd Semester, DEEC

Contents

List of Figures

1 Introduction

1.1 Objectives

The main goal of this project is to analyze and design a Low Noise Amplifier (LNA) using 350 nm CMOS technology, with a comparison using more advanced technologies such as 45 nm and 65 nm. The LNA must comply with key performance specifications, including a gain greater than 10 dB, a noise figure (NF) below 3 dB, and proper input/output impedance matching (S11 and S22 less than -10 dB).

In table 1, the specifications for the LNA are summarized. The design will be validated through circuit simulations using LTSpice, and the results will be compared with theoretical expectations.

Table 1: LNA Specifications

Specification	**Value**
Gain (S21)	> 10 dB
Noise Figure (NF)	< 3 dB
Input Impedance (S11)	< -10 dB
Output Impedance (S22)	< -10 dB
Technology Node	350 nm, 65 nm, 45 nm
Frequency (350 nm)	0.1 GHz to 2 GHz
Frequency (65 nm)	5 GHz
Frequency (45 nm)	10 GHz
VDD (350nm, 65nm, 45 nm)	2.5V, 1.2V, 1V
K constant (350nm, 65nm, 45 nm)	200?μ, 244.961?μ, 50?μ
L_{min} (350nm, 65nm, 45 nm)	350?nm, 65?nm, 45?nm
n (g_m ratio)	3

1.2 Motivation

Modern telecommunication systems operate at high frequencies and data rates, and the LNA plays a critical role in the receiver chain, as it amplifies weak incoming signals while minimizing noise. A well-designed LNA ensures signal integrity, energy efficiency, and compliance with communication standards. This project gives students the opportunity to apply theoretical knowledge of analog and RF electronics by developing and validating a practical CMOS-based LNA using circuit simulation tools such as LTSpice.

2 LNA Architecture

In this section, we present the architecture of the Low Noise Amplifier (LNA) designed, the complete architecture is shown in Figure 1.

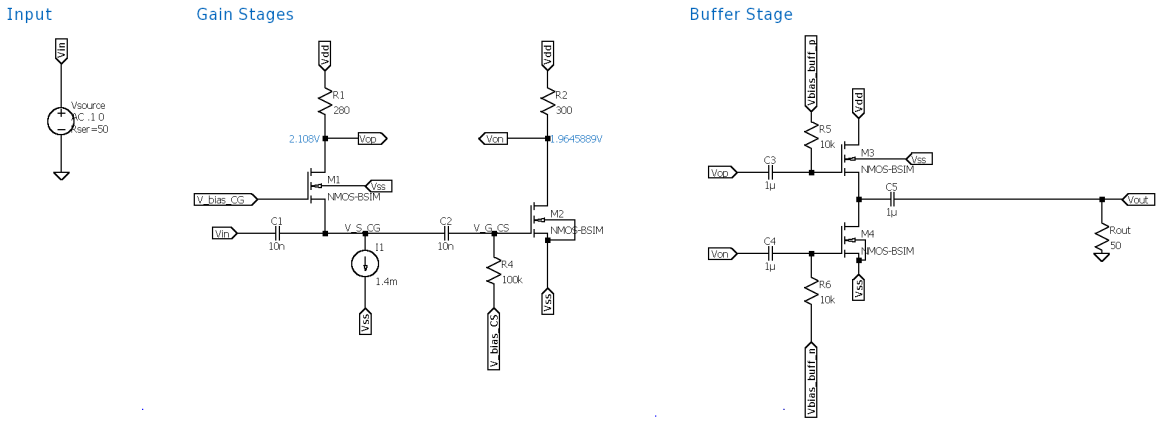

Figure 1: Schematic of the gain stages in the proposed LNA architecture.

2.1 Common Gate and Common Source combination gain stages

The Low Noise Amplifier (LNA) implemented in this project adopts a wideband balun-LNA topology, which combines a common-gate (CG) stage and a common-source (CS) stage operating in parallel, as depicted in Figure 2. This configuration, proposed in [1], is particularly advantageous because it simultaneously enables input matching, output balancing, noise cancellation, and distortion suppression.

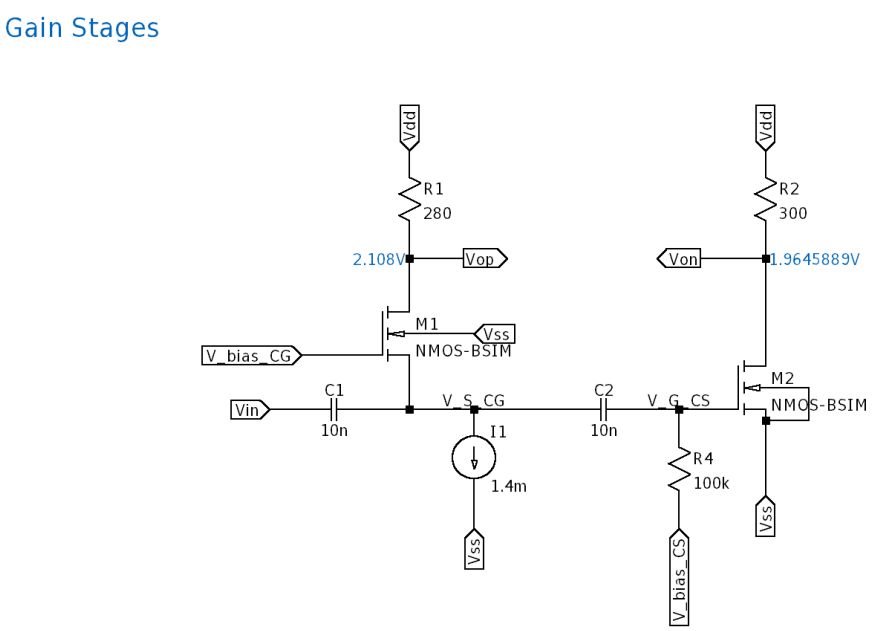

Figure 2: Schematic of the gain stages in the proposed LNA architecture.

Analyzing the circuit in Figure 2, the input signal is amplified by two separate stages, the common-gate stage, where transistor M1 is used, and the common-source stage, where transistor M2 is used. The output is differential, with the positive signal taken from the drain of M1 and the negative signal from the drain of M2. The capacitors are used to couple the AC signals while blocking DC, ensuring that the DC biasing of the transistors does not affect the AC performance.

2.1.1 Common Gate Stage

The CG stage, depicted in Figure 3, provides a single-ended input with low input impedance, which makes it ideal for broadband input matching—specifically to 50Ω source impedance.

However, most receiver chains operate differentially, requiring a conversion from single-ended to differential signals. In this topology, the differential output is achieved by adding the CS stage in parallel with the CG stage, and balancing the gains of both paths with opposite polarities. This results in a balun behavior, allowing the circuit to simultaneously amplify and convert the input signal to differential form.

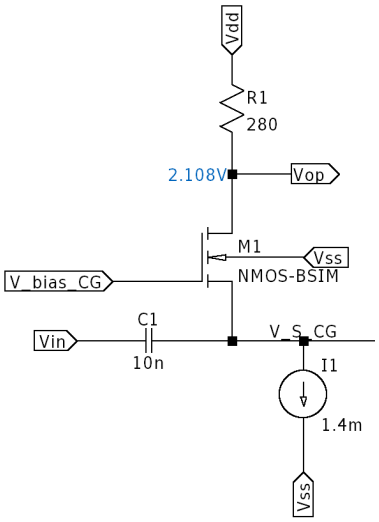

Figure 3: Schematic of the common-gate stage in the proposed LNA architecture.

2.1.2 Common Source Stage

The CS stage, shown in Figure 4, provides a high input impedance and is typically used for voltage amplification. In this architecture, the CS stage is designed to operate in parallel with the CG stage, allowing for differential output while maintaining high gain. The CS stage also contributes to the overall noise figure and linearity of the LNA.

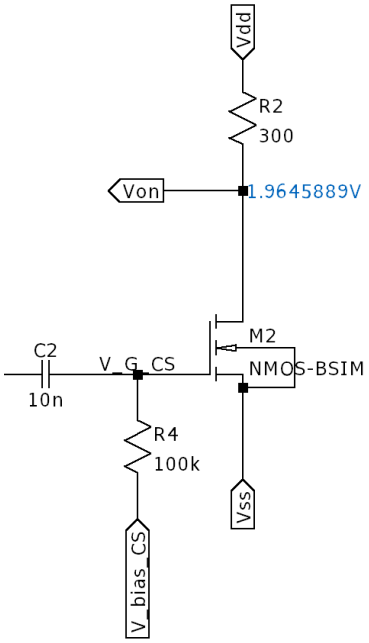

Figure 4: Schematic of the common-source stage in the proposed LNA architecture.

The noise produced by the CG transistor, mainly thermal noise, is a major contributor to the total noise figure in traditional designs. However, by carefully matching the gain of the CG and CS paths, the noise from the CG stage appears as a common-mode signal at the differential output and is effectively canceled. This cancellation occurs because the CG noise contributes identically to both outputs, while the CS stage contributes with opposite polarity. The result is a significantly reduced noise figure.

In addition to noise, the nonlinear distortion of the CG stage can also be canceled using this structure. When both paths have matched amplitude and phase but opposite sign, the nonlinear distortion generated by the CG stage also appears in-phase at both outputs and is canceled in the differential signal. As a result, the overall linearity is determined by the CS stage. The CS stage can then be optimized independently for linearity, allowing the design to achieve high dynamic range while maintaining wideband operation.

2.2 Buffer Stage

In the proposed LNA architecture, an output buffer, depicted in Figure 5, is included following the differential outputs of the common-gate and common-source stages. The buffer plays a crucial role in ensuring impedance matching, signal integrity, and measurement convenience.

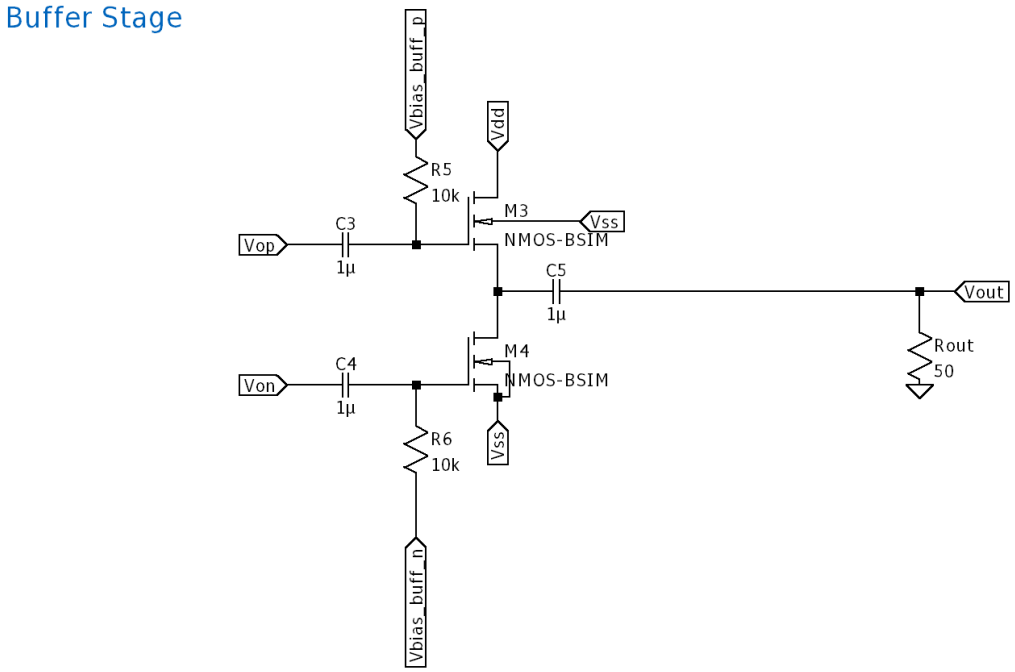

Figure 5: Schematic of the output buffer in the proposed LNA architecture.

Analyzing the circuit the differential signal enters through the gates of both transistors, M3 in a common-drain configuration and M4 in a common-source configuration. Ideally, both configurations have a gain of 1, resulting in a single-ended output signal with a gain equal to the gain of the input signals. As in the previous circuit, the capacitors are used to couple the AC signals while blocking DC, ensuring that the DC biasing of the transistors does not affect the AC performance.

Firstly, in typical RF systems, the LNA output often needs to interface with 50Ω measurement equipment or subsequent stages (e.g., mixers) that have specific impedance requirements. The output buffer, provides a low output impedance while maintaining a high input impedance, effectively isolating the LNA core from the load. This allows the LNA to drive a standard 50Ω load without compromising its gain or linearity performance.

Secondly, the buffer helps to preserve the voltage gain achieved by the LNA. Without buffering, any mismatch or loading at the output could attenuate the signal and degrade performance. The buffer thus ensures that the full gain developed across the load devices is delivered to the output.

Thirdly, for testing and characterization purposes, the buffer is particularly important. In the measurement setup described in [2], the output buffer is integrated with a balun/voltage combiner to enable single-ended measurements of the differential output. This facilitates direct connection to spectrum analyzers or vector network analyzers without the need for additional external components.

Finally, the inclusion of the buffer also contributes to robustness against variations in the following stage, whether in simulation or practical implementation, ensuring consistent performance across different configurations.

3 Design of the LNA

In this section, we present the design of the LNA architecture shown in Figure 1. The design process involves biasing conditions and ensuring the desired specifications are met.

3.1 Common Gate Stage Design

3.2 Common Source Stage Design

3.3 Buffer Stage Design

4 Simulation and Results analysis

In this section are presented the simulations performed on the LNA circuit in the three technologies mentioned before, including the analysis of the gain, noise figure, and input/output impedance. The simulations were conducted using LTSpice and Cadence, and the results are compared with theoretical expectations, and the technologies are compared in terms of performance metrics.

4.1 Simulation for 350 nm Technology

4.2 Simulation for 65 nm Technology

The simulations for this technology were done in Cadence.

4.2.1 1:1 g_m ratio

The circuit implemented in Cadence for the 65 nm technology with a 1:1 g_m ratio is shown in Figure 6. The simulation results are shown in Figure 7 summarized in Table 2.

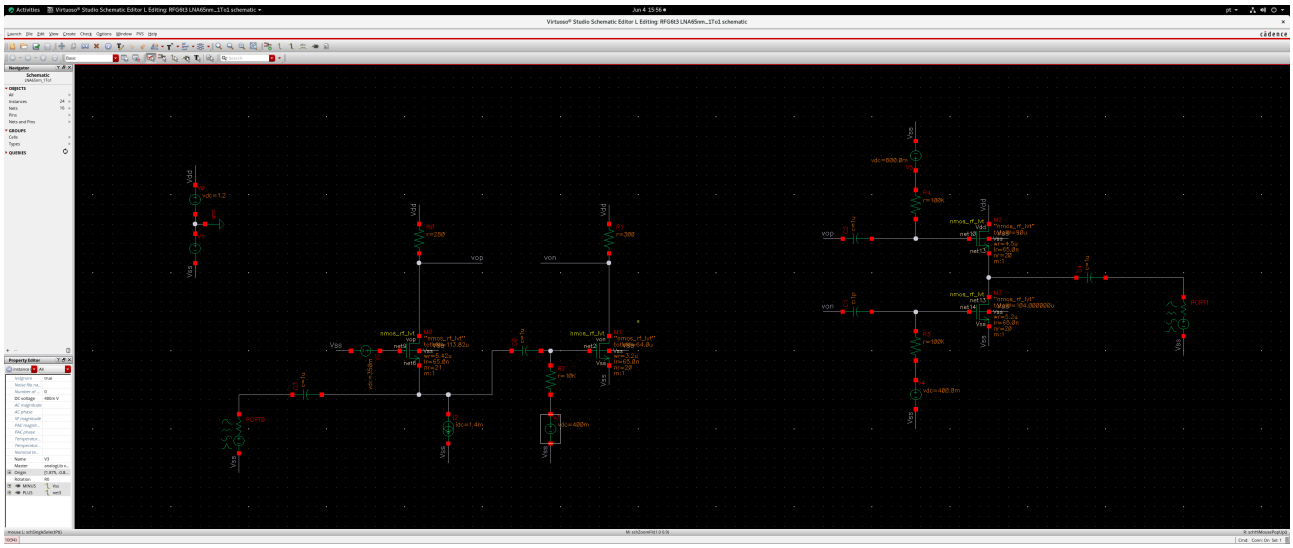

Figure 6: LNA Circuit for 65 nm Technology with 1:1 g_m Ratio

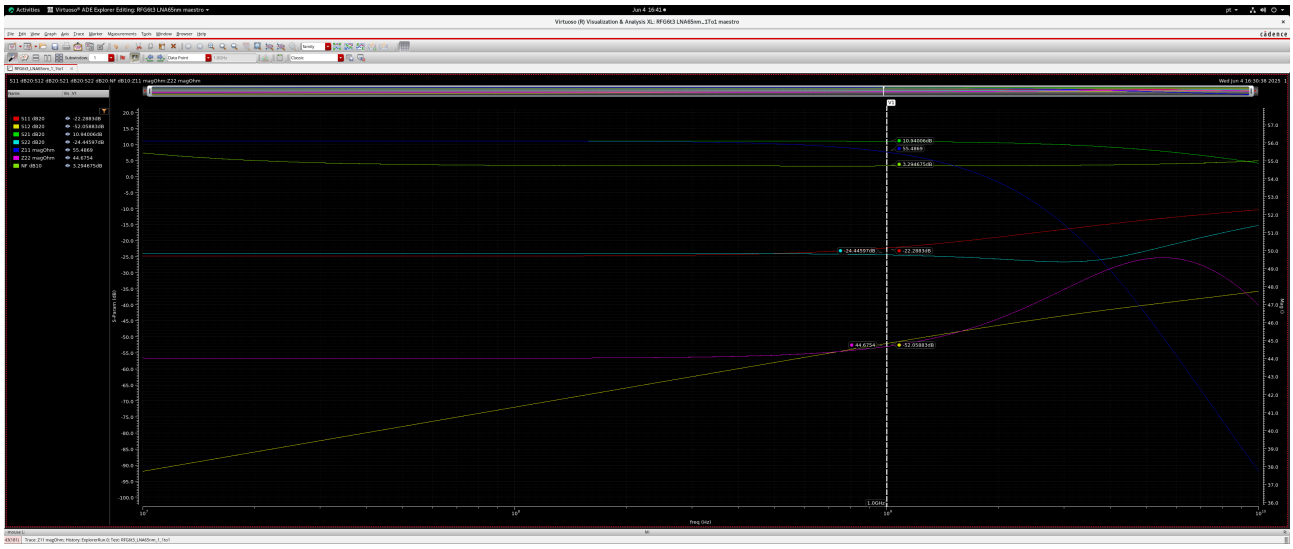

Figure 7: LNA Simulation for 65 nm Technology with 1:1 g_m Ratio

Table 2: Simulation Results for 65 nm Technology with 1:1 g_m Ratio

Parameter	Value
Gain (S21)	10.94dB
Noise Figure (NF)	3.29dB
Input Impedance (Z11)	44.68ohm
Output Impedance (Z22)	55.49ohm

4.2.2 1:n g_m ratio

The circuit implemented in Cadence for the 65 nm technology with a 1:n g_m ratio is shown in Figure 8. The simulation results are shown in Figure 9 summarized in Table 3.

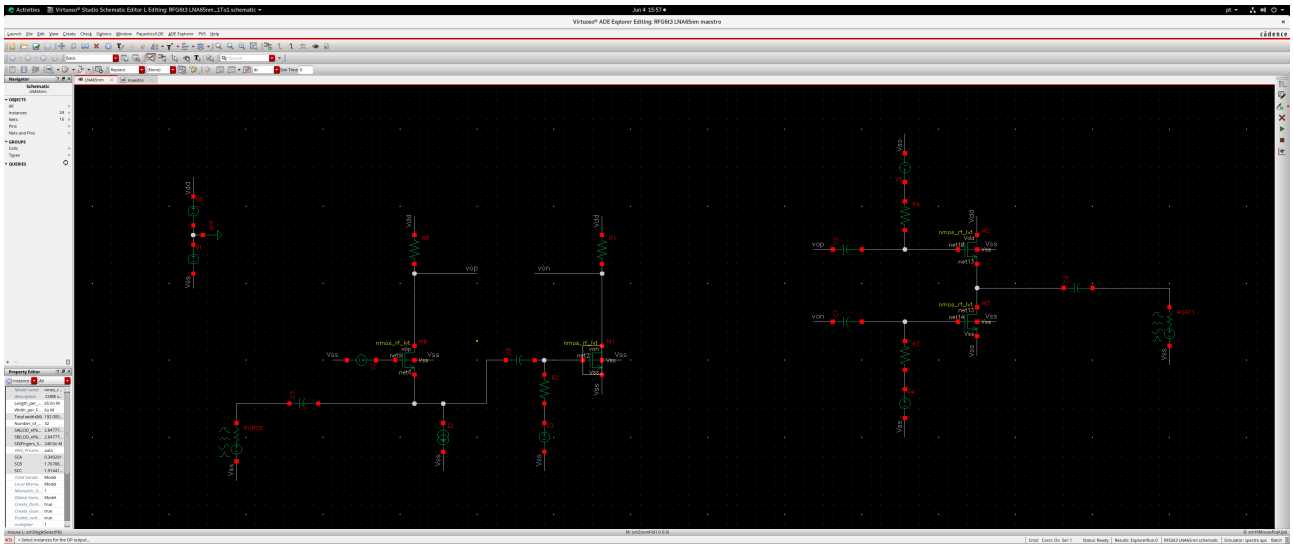

Figure 8: LNA Circuit for 65 nm Technology with 1:n g_m Ratio

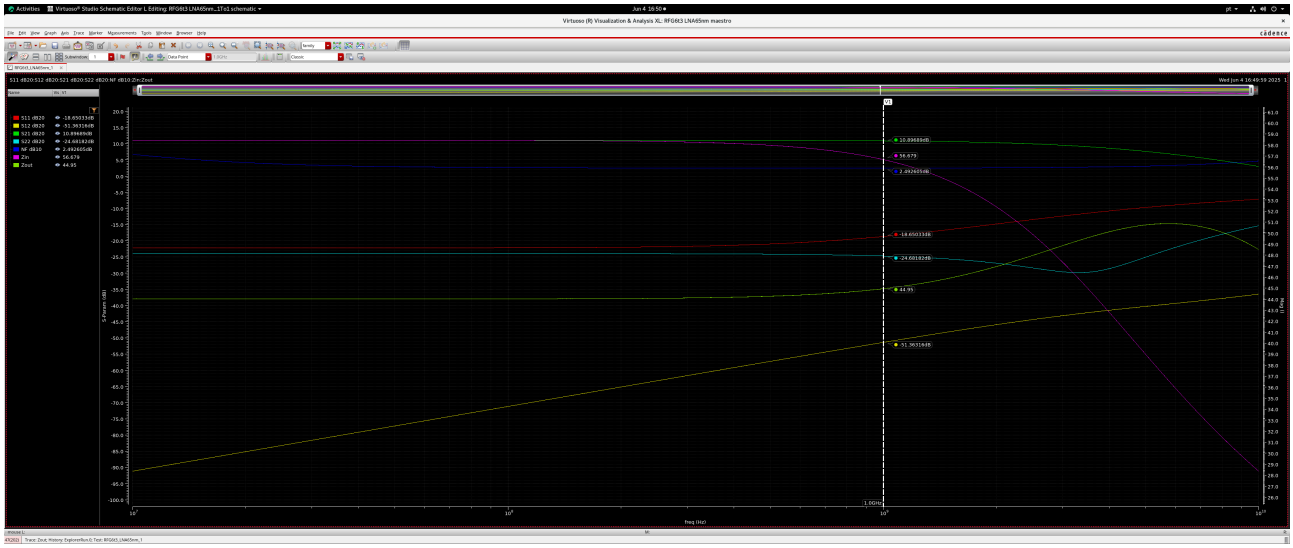

Figure 9: LNA Simulation for 65 nm Technology with 1:n g_m Ratio

Table 3: Simulation Results for 65 nm Technology with 1:n g_m Ratio

Parameter	Value
Gain (S21)	10.86dB
Noise Figure (NF)	2.49dB
Input Impedance (Z11)	56.68ohm
Output Impedance (Z22)	44.95ohm

References

[1] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-lna with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1349, 2008.

[2] I. Bastos, L. B. Oliveira, J. Goes, and M. Silva, "A low power balun lna with active loads for gain and noise figure optimization," *Analog Integrated Circuits and Signal Processing*, vol. 81, pp. 693–702, 2014.

A Appendix A: Python Script

The Python script used for the design and simulation of the Low Noise Amplifier (LNA) is provided below. This script utilizes the 'scikit-rf' library for RF circuit analysis and design.

GitHub repository: https://github.com/MartimAgostinho/ERF-Lab2.git