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A low power balun LNA with active loads for gain and noise figure optimization

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Abstract In this paper we describe a balun LNA with noise and distortion cancelling with active loads to boost the gain and reduce the noise figure (NF). Simulation and measurements results, with a 130 nm CMOS technology, show that the gain is enhanced by about 3 dB and the NF is reduced by at least 0.5 dB, with a negligible impact on the circuit linearity (IIP3 is about 0 dBm). The total power dissipation is only 4.8 mW, and the active area is less than 50×50 μm^2.

Keywords LNA · Active loads · Gain optimization

1 Introduction

Modern fully integrated receiver architectures (e.g. Low-IF and Zero-IF), require inductorless circuits to achieve their potential low area, low cost, and low power [9, 13, 16]. The LNA, which is a key block in such receivers, is investigated in this paper.

Narrowband LNAs [16] use inductors and have very low noise figure, but they occupy a large area and require a technology with RF options to obtain inductors with high Q. Wideband LNAs with multiple narrowband inputs have low noise, but their design is complex and the area and cost are high [13, 16]. RC LNAs are very simple and inherently wideband, but their conventional realizations have large noise figure (NF). Recently, wideband LNAs with noise and distortion cancelling, with passive loads [6, 7] have been proposed, which can have low NF, but have high power consumption.

In this paper our main goal is to obtain a very low area, low power, and low-cost LNA. We use the LNA architecture employed in [6], with noise and distortion cancelling, which combines a common-gate (CG) stage and a common-source (CS) stage. In [6] the resistor loads are used in these two stages. Here, we replace the resistor loads by MOS transistors, biased in moderate inversion and operating near the transition between triode and saturation, which allows the increase of the LNA gain (for the same voltage drop) and minimizes the circuit NF, without increasing the circuit die area; the active loads allow a supply voltage reduction, which can lead to a very low power consumption. Preliminary simulation results of this circuit have already been presented in the conference papers [3, 4]. In this paper we present an extended version of this work with measurement results.

Two circuit prototypes have been designed in a standard 130 nm CMOS technology to compare the conventional design with resistors [6], and the new implementation, with active loads. We demonstrate that the proposed design methodology leads to a gain boost of 3 dB and reduces the NF by 0.5 dB, with a minimum impact on circuit non-linearity.

This paper is organized as follows. In Sect. 2 we review the conventional balun LNA with passive loads [6]. In Sect. 3 we propose the use of active loads and present design guidelines to increase the gain and reduce the NF. In Sect. 4 we present the measurement results for the two

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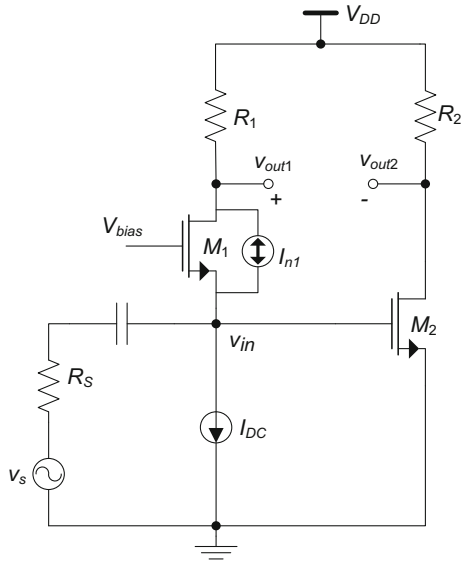

Fig. 1 Balun LNA with passive loads [6]

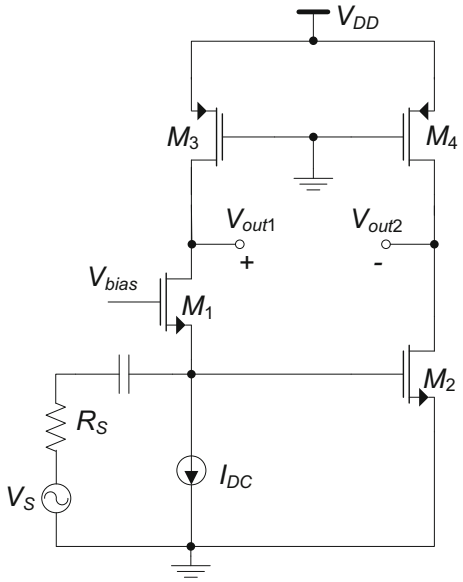

Fig. 2 Proposed LNA with active loads

circuit prototypes. Finally, in Sect. 5 we draw the conclusions.

2 Balun LNA with passive loads

The circuit in Fig. 1 [6] is a state-of-the-art inductorless LNA. This circuit is particularly attractive because it combines CG and CS stages performing a balun operation (single-ended to differential conversion) and it allows noise and distortion cancellation. A balun LNA is very advantageous, since the LNA is, typically, preceded by a filter or is directly coupled to an antenna, which have a single output (there are antennas with differential outputs, but these are not common in on-chip RF front-ends); thus, the LNA needs a single input. Since, the subsequent stage (e.g., mixer) usually has differential inputs, a balun is required in the case of a single ended LNA. A passive wideband balun has high losses, and a low-loss balun is narrowband and must be implemented externally.

Analyzing the circuit of Fig. 1 and assuming ideal transistors with infinite output resistance, all the input current flows in the CG stage through R_1, originating the output signal v_{out1}, which is in phase with v_{in}, and the gain A_{vCG} is roughly given by $g_{m1}R_1$. The input impedance Z_{in} of the CG stage, is approximately $1/g_{m1}$, and must be equal to R_S for input impedance matching. For proper balun operation, both stages must have equal voltage gains with opposite sign. This is possible, since the CS stage has voltage gain, A_{vCS}, given approximately by $-g_{m2}R_2$. The stages' gains are, therefore, given by

$$A_{vCG} = -A_{vCS} = R_1/R_S \tag{1}$$

The thermal noise produced by the CG stage (M_1), represented by current source i_{n1}, originates a noise voltage at the input $v_{n,in}$ since it flows into R_S. This generates noise voltages in phase at the CG output $v_{n,out1}$ and at the CS stage output $v_{n,out2}$. Thus, the CG stage thermal noise is cancelled and the gain of the LNA is doubled at the differential output. The gain matching of the two stages is critical, since the same gain is needed for full noise cancellation.

In addition to the noise, this structure also allows the cancellation of the non-linear distortion introduced by the CG stage, as shown in [6].

For the noise factor calculation, and in a first-order analysis, the transistors are assumed to have infinite output resistance (r_0) and the bias current source (I_{DC}) is assumed to be ideal. To achieve noise cancellation and balun operation the CG and CS's stages gain should be matched by making $g_{m1} = g_{m2} = g_m$ (neglecting the body effect) and $R_1 = R_2 = R_D$. Considering $r_{o1}g_{m1} \gg 1$ and that for the same current and length (L) of M_1 and M_2, their output resistances (r_o) are approximately equal, the total noise figure is given by [6]

$$F_{LNA} = 1 + \frac{k_f}{8kTR_SC_{ox}f^{\alpha_f}}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2}\right) + \frac{\gamma}{2R_Sg_m} + \frac{1}{R_SR_Dg_m^2} \tag{2}$$

where k is Boltzmann's constant, C_{ox} is the oxide gate capacitance per unite area, W_i and L_i are the transistor dimensions, T is the absolute temperature, γ is the transistors' excess noise factor, k_f and α_f are intrinsic process parameters, which depend on the size of the transistors [8, 15].

Table 1 Circuit design values

	I_D (mA)	g_m (mS)	W (μm)	L (μm)	V_{GS} (mV)
M_1	2	25.1	75.6	0.12	460
M_2	2	26.1	77	0.12	430
M_3	2	2	13.8	0.12	–
M_4	2	2	13.8	0.12	–

* $V_{BIAS} = 895$ mV

It is worth noting here that there is a tradeoff between power, area, and noise figure. It can be seen by inspection of (2), that if R_D is reduced and g_m is increased in the same proportion to achieve the same gain for proper noise cancellation, the noise factor is reduced. However, the increase of the transconductance requires a significant increase of the bias current of the CS stage, and/or increase of W/L ratio with minimum L, leading to a very low transistor output resistance.

3 Balun LNA with active loads

3.1 Circuit implementation

The proposed LNA with active loads is shown in Fig. 2, in which the load resistors are replaced by PMOS transistors (M_3, M_4).

If transistors M_3 and M_4 operate deeply in the triode region ($V_{DS} \ll V_{GS} - V_t$), they are modeled ideally by a resistor ($r_{ds} = 1/g_{ds}$) between the drain and source, where g_{ds} is the channel conductance.

The design procedure is divided into three steps:

1. Set g_m of transistor M_1 for 50 Ω input impedance matching. The bias current source (I_{DC}) is set to a value compatible with the acceptable power consumption (2 mA in our design, as shown in Table 1), and the value of W is calculated assuming minimum L to maximize the circuit bandwidth.
2. Consider the same current for the commons-source stage (2 mA), to minimize the total circuit power consumption, and obtain W of M_2, assuming minimum L. These values will be slightly different from transistor M_1 since M_2 does not suffer from body effect.
3. Optimize the value of the active loads in order to maximize the gain and reduce the NF.

3.2 Gain and noise figure

Once the resistors are replaced by MOSFETs, it becomes possible to optimize the circuit gain.

The incremental model of a MOS operating in saturation is a current source in parallel with a resistor. We can increase the incremental load resistance without increasing the DC voltage drop, thus increasing the gain with respect to the original circuit with resistor load. By simulation we find optimal gain point of the LNA, as shown in Fig. 3.

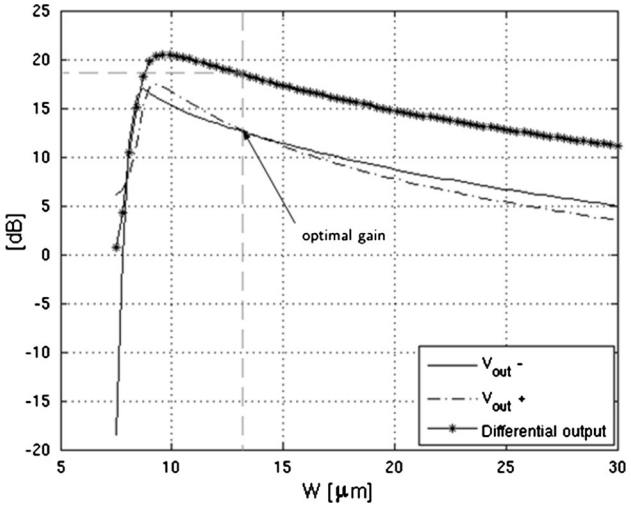

Fig. 3 LNA optimum gain point

The biasing and incremental parameters, for the circuit example, are shown in Table 1. By simulation we vary $W_3 = W_4$ (with $L_3 = L_4 = L_{min}$) and observe that the gains of the CG and CS stages, increase until a point is reached for which the gains are no longer almost equal; after that point the gains diverge, thus, violating the cancellation condition. This is the optimal gain point, shown in Fig. 3. It is easy to see that the corresponding biasing is in triode, but not far from the saturation region.

Since M_3 and M_4 have the same size and biasing voltage, their incremental resistances are $r_{ds3} = r_{ds4}$, and the LNA gain is

$$A_{vLNA} = g_{m1}(r_{ds1}//r_{ds3}) + g_{m2}(r_{ds2}//r_{ds4}) \tag{3}$$

If we compare Eqs. (3) and (1) we obtain a higher gain in (3) since the value of $r_{ds3} = r_{ds4}$ is higher than the value of $R_1 = R_2$.

If we assume that $g_{m1} = g_{m2} = g_m$, and $r_{ds3} = r_{ds4} = r_{ds}$ then the noise factor equation can be simplified to

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S C_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2} + \frac{1}{W_3 L_3} + \frac{1}{W_4 L_4}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} \tag{4}$$

Comparing Eq. (4), with Eq. (2) we can conclude that we will have higher flicker noise due to the extra contributions of transistors M_3 and M_4, but the last term of Eq. (4) is lower since r_{ds} is higher than R_D. Thus, we can reduce the noise figure without changing the value of g_m, without any penalty in terms of area and power dissipation.

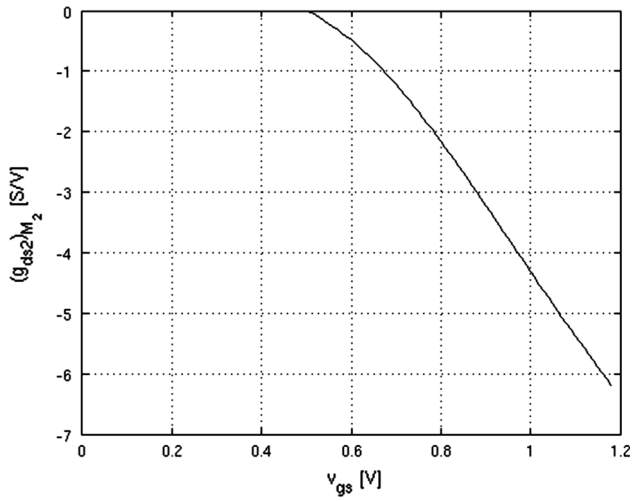

Fig. 4 Second order cefficient (g_{ds2}) of transistor M_2

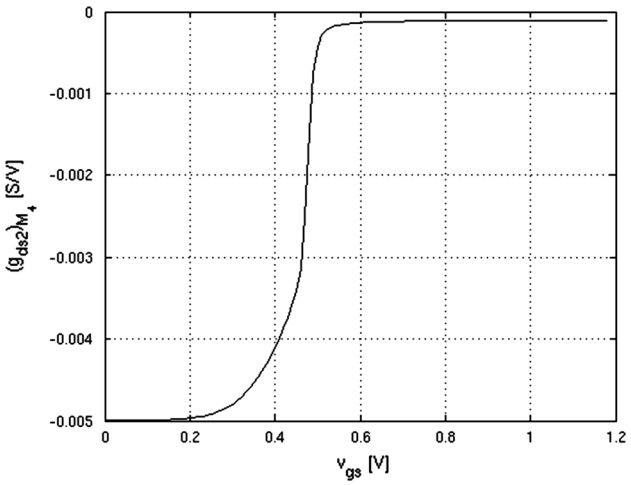

Fig. 5 Second order coefficient (g_{ds2}) of transistor M_4

3.3 Distortion analysis

Since non-linear MOS devices have replaced the load resistors, suitable linearity of the LNA should be ensured for the entire gain range. We will now investigate how to improve the linearity by proper biasing.

The nonlinearity of the CS stage (M_2, M_4) is of special concern, since the distortion of the CG stage is cancelled out. The transistor equation can be represented by a Taylor series expansion [6] in the form:

$$\begin{aligned} i_d(v_{gs}, v_{ds}) = {} & g_{m1}v_{gs} + g_{ds1}v_{ds} + g_{m2}v_{gs}^2 + g_{ds2}v_{ds}^2 \\ & + g_{11}v_{gs}v_{ds} + g_{m3}v_{gs}^3 + g_{12}v_{gs}v_{ds}^2 + g_{21}v_{gs}^2v_{ds} \\ & + g_{ds3}v_{ds}^3 \end{aligned} \tag{5}$$

where,

$$g_{mk} = \frac{1}{k!}\frac{\partial^k i_{DS}}{\partial V_{GS}^k}, g_{dsk} = \frac{1}{k!}\frac{\partial^k i_{DS}}{\partial V_{DS}^k}, g_{jk} = \frac{1}{j!k!}\frac{\partial^{j+k} i_{DS}}{\partial V_{GS}^j \partial V_{DS}^k}$$

Since M_4 has $v_{gs} = 0$, the distortion originated by this transistor is only due to v_{ds}. In Figs. 4 and 5 we compare the simulated second order coefficients of M_2 and M_4, as a function of V_{GS} of M_2.

Coefficient g_{ds2} of M_2 is more than 100 times higher than g_{ds2} of M_4, and the difference is even higher for the third order coefficients, as can be confirmed by electrical simulations. Thus, M_4 does not introduce significant distortion. M_4 defines the CS stage gain, but its influence on IIP2 and IIP3 is negligible.

The output voltage of the CS stage is $v_{ds} = -i_d\, r_{ds}$, and we can express v_{ds} as a non-linear function of v_{gs},

$$v_{ds} = -\left(c_1 v_{gs} + c_2 v_{gs}^2 + c_3 v_{gs}^3\right) \tag{6}$$

By substituting (6) in (5) we obtain

$$i_d = k_1 v_{gs} + k_2 v_{gs}^2 + k_3 v_{gs}^3 \tag{7}$$

where the coefficients, k_1, k_2, and k_3 are [6]:

$$k_1 = \frac{g_{m1}}{1 + g_{ds1}r_{ds}} r_{ds} \tag{8}$$

$$k_2 = \frac{g_{m2} + g_{ds2}c_1^2 r_{ds}^2 - g_{11}c_1 r_{ds}}{1 + g_{ds1}r_{ds}} r_{ds} \tag{9}$$

$$\begin{aligned} k_3 = \Bigg[& \left(g_{m3} + g_{12}c_1^2 r_{ds}^2 + 2g_{ds2}c_1 c_2 r_{ds}^2 - g_{11}c_2 r_{ds}\right. \\ & \left. - g_{21}c_1 r_{ds} - g_{ds3}c_1^3 r_{ds}^3\right)\left(\frac{1}{1 + g_{ds1}r_{ds}}\right)\Bigg] r_{ds} \end{aligned} \tag{10}$$

For different M_2 bias we extract the transistor parameters in (5) by simulation and we use (8) to (10) to obtain k_1, k_2 and k_3.

In Fig. 6 the gain coefficient k_1 in (8) is represented as a function of V_{GS2}. The gain was set previously by the optimization procedure (Fig. 3). To have proper balun operation and noise cancellation, the CS stage gain must be equal to the gain of the CG stage. Thus, we have two possibilities, V_{GS2} either near 430 mV or near 515 mV. In Figs. 7 and 8 the nonlinearity coefficients k_2 and k_3 are shown. To minimize k_2 and k_3, V_{GS2} should be below 450 mV. Thus, the optimal biasing point adopted for M_2 is 430 mV.

4 Simulation and measurement results

As already stated, the value of g_{m1} is set by the required 50 Ω input impedance (approximately equal to g_{m1}^{-1}). The transconductance of M_2 should be equal to that of M_1, which with equal loads lead to equal gains as required for gain matching and noise cancellation.

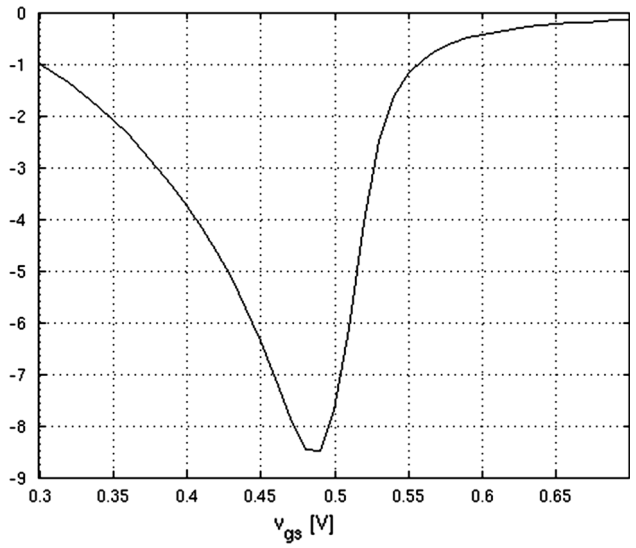

Fig. 6 Coeficient k_1 (gain) as a function of V_{GS2}

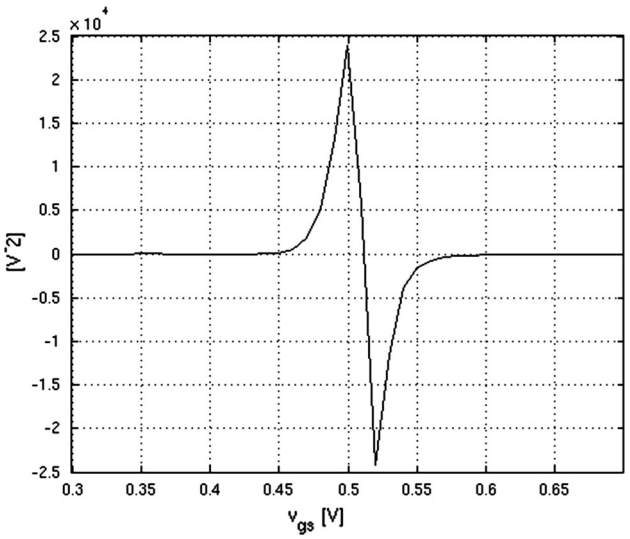

Fig. 8 Coeficient $k3$ as a function of V_{GS2}

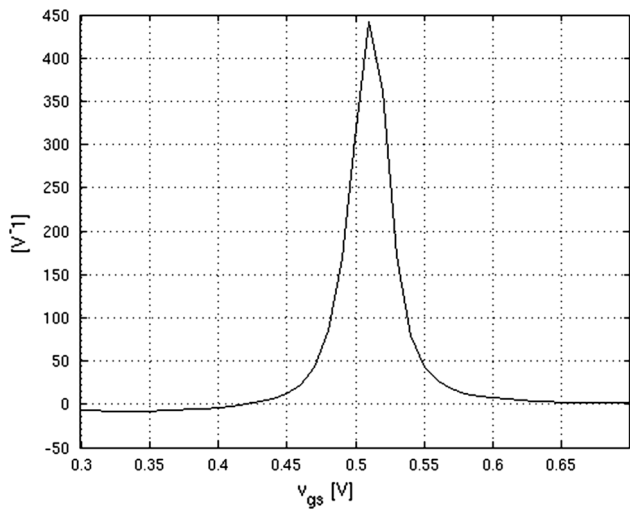

Fig. 7 Coeficient k_2 as a function of V_{GS2}

The final transistor widths are set to $W_1 = 80$ µm, $W_2 = 89.6$ µm and $W_3 = W_4 = 12.3$ µm (values obtained from post-layout simulations including the biasing and buffer circuits). For maximum speed all transistors have the minimum channel length (120 nm). The bias voltage V_{B1} is 930 mV and it sets the value of V_{GS2}, since V_{GS1} is defined by the current source I_{B1}.

For a fair comparison, we consider equal voltage drop in the load devices in the two cases, and we have resistances of about 200 Ω, similar to the work in [6], and transistors as active loads ($g_{ds} = 3.9$ mS), using the maximum gain point of Fig. 3. The active loads are not in saturation. The equivalent resistance is increased from 200 to 256 Ω (active load). For each case results of schematic level and post-layout simulation, and measurements are presented for comparison. Both circuit prototypes use the same test setup biasing circuitry and internal balun/output buffer (as shown in Fig. 9), and they are built together in the same MWP run. In Fig. 10 the layout and die photo of the two circuits are shown. The area of each chip is 198 × 390 µm (including pads), and two chips have approximately the same area, since there is a negligible difference between the areas of the load transistor and of the load resistor.

The bias current source is implemented employing a simple current mirror, and a biasing circuitry is used for biasing the gate terminal of transistor M_1. At the output an internal balun/voltage-combiner [11] is used for differential to single-ended conversion and for matching the 50 Ω standard impedance of the measuring equipment. This allows testing with the LNA directly connected to the vector and spectrum analyzer for measuring S-parameters, Gain, NF, and IIP3. A photo of the board is shown in Fig. 11. We have used a direct wirebonding and microstrips and SMA conectors for testing the two LNAs with active and passive loads.

In Figs. 12, 13, 14, and 15 the results of gain and NF for the two LNAs are presented. The fluctuations in the curves are due to the external interference captured by the test boards, due to a strong WiFi signal: they are not due to our integrated circuit prototype.

To compare the two cases, a figure of merit (FoM) is used [18]:

$$FOM\left[mW^{-1}\right] = \frac{Gain[abs]}{(NF-1)[abs]P_{DC}[mW]} \tag{11}$$

In Table 2 a comparison is presented between the traditional version with passive loads and the proposed

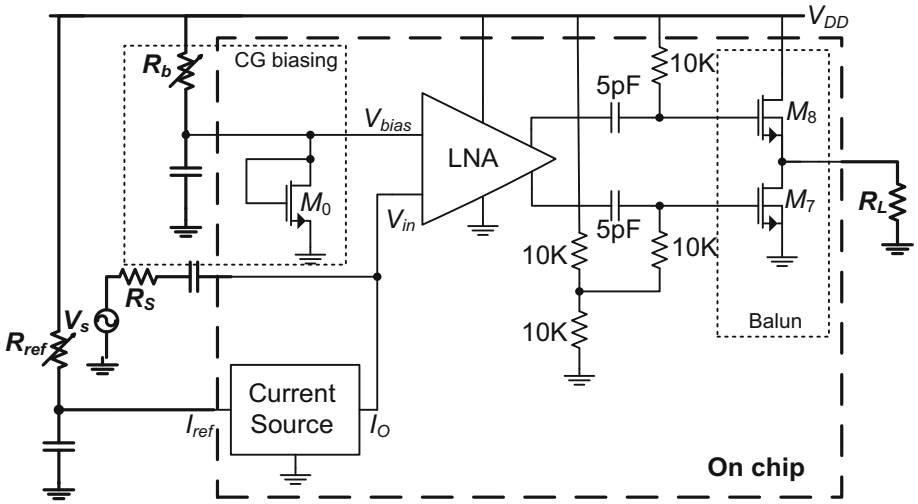

Fig. 9 LNA test setup for evaluation of the integrated prototypes

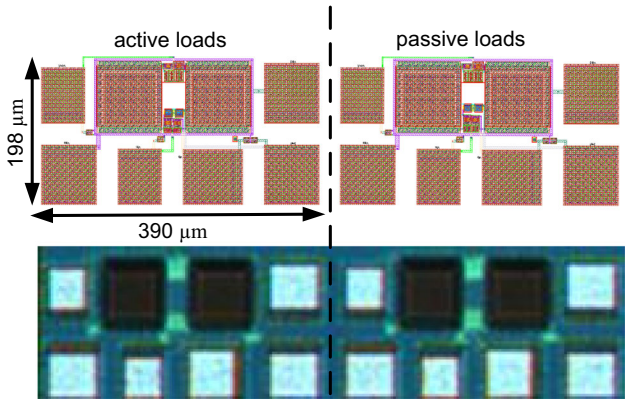

Fig. 10 Layouts and die photo of the test circuit (active and passive loads)

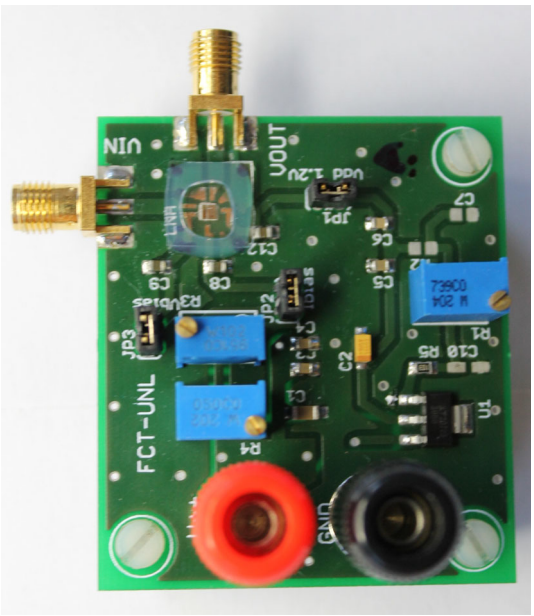

Fig. 11 LNA test board

version with active loads. From Table 2 and Figs. 17 and 18, we can conclude that the proposed circuit has a higher measured gain (up to 3 dB improvement) and lower NF (about 0.5 dB reduction), with similar performance in terms of non-linearity. This circuit is suitable for, in the region up to 1.5 GHz, ISM bands (450 MHz, 900 MHz), and WMTS band (600 MHz and 1.4 GHz) [12].

An example at 600 MHz is considered, and similar results are obtained for the remaining bands as shown in Figs. 16 and 17.

The proposed LNA has a low power than the work [6] (14 mW), in which the bias current of CS stage is four times that in the CG stage.

We have implemented the current source I_{DC}, which is responsible for about 1 dB degradation in the NF, whereas the authors of the work in [6], have used an inductor in connected to the source of the CG stage.

In order to simplify the measurement we have included in the test circuit a balun/buffer, which leads only to 0.3 dB increase in the LNA NF. We have performed a simulation in which we have plotted the noise summary for the 10 major noise sources, at 600 MHz, and the contribution of the gate noise current and of the biasing circuit of the CG stage are negligible (below 1 % of the total output noise).

Measuring the LNAs with a double-layer PCB board using wirebonding, two micro-strips, and two SMA connectors, and with a DC block at the LNA input, leads two more than 1 dB NF degradation with respect to post-layout simulations for both circuit prototypes. This NF degradation with respect to the post-layout simulations could be strongly reduced by using a probe station with on-wafer testing, but this is not available in our lab.

These cumulative NF degradation explains the differences between the NF measured in [6] and the results obtained in Table 2.

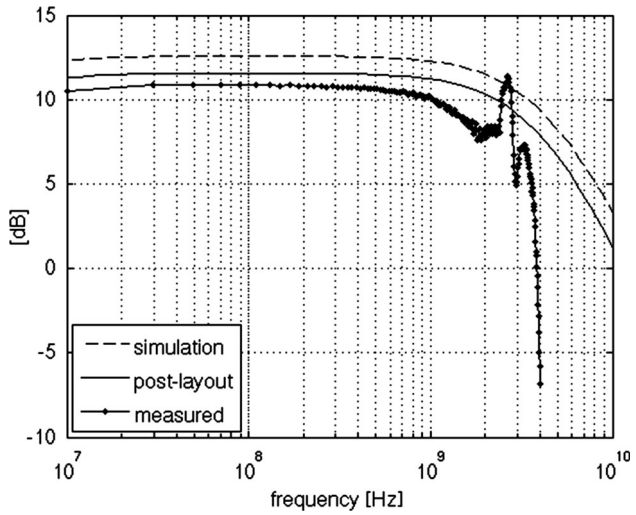

Fig. 12 Power gain of the LNA with active loads (Fig. 2)

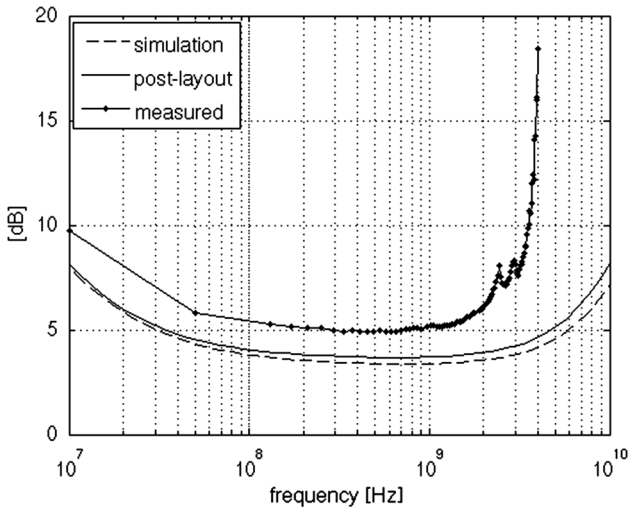

Fig. 14 NF of the LNA with active loads (Fig. 2)

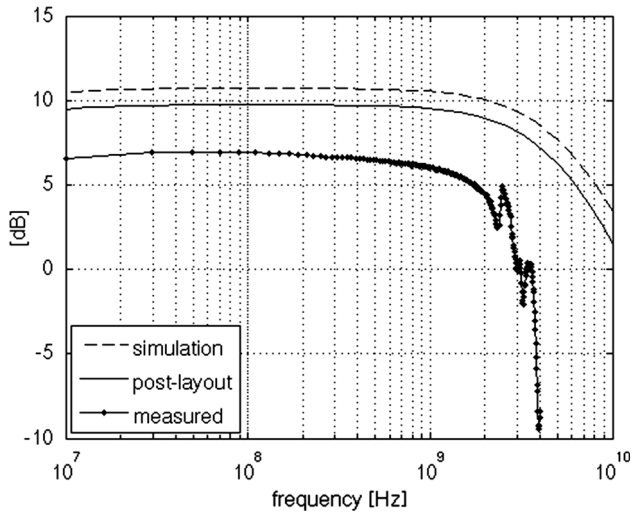

Fig. 13 Power gain of the LNA with passive loads (Fig. 1)

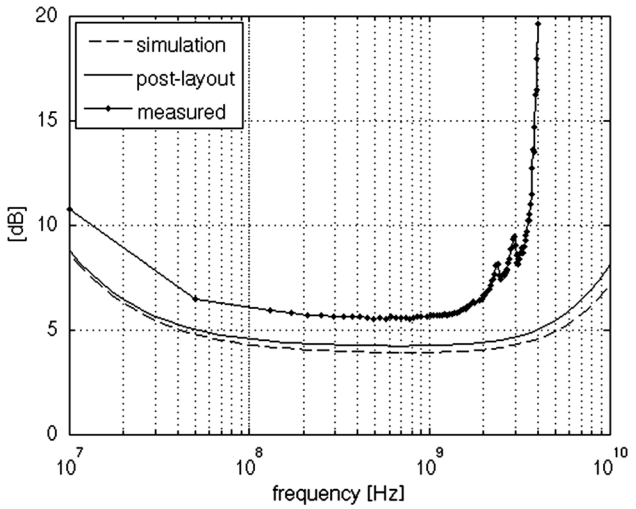

Fig. 15 NF of the LNA with passive loads (Fig. 1)

From Table 2 and Figs. 16 and 17, we can conclude that the proposed circuit has a higher gain (up to 3 dB improvement) and lower NF (about 0.5 dB reduction), with similar performance in terms of non-linearity. The improvement in NF is due to the increased gain, since the noise contributions of the resistor and of the transistor loads are similar. In Table 3, the performance of this circuit is compared with some state-of-the art LNAs.

An LNA with passive resonating load might have a lower NF. The circuit prototype proposed here is a low area, low cost wideband LNA, and can be built in a standard CMOS technology. Since it is wideband, a steeper band selection filter may be required.

The performance is worse than that of a resonating load LNA, but the circuit is wideband and can cover all the ISM and WMTS bands, from 450 MHz to 1.5 GHz. A passive resonating load circuit only works for a single frequency band; dual-band or multi-band approaches would have a large overhead in area and cost.

Table 2 Circuit measurements for active and passive loads considering WMTS biomedical application [12]

Loads	Freq. (GHz)	Power gain (dB)	NF (dB)	IIP3 (dBm)	PDC (mW)	FOM (mW^{-1})
Passive loads	0.6	7	5.4	−3.8	4.8	0.4
Active loads	0.6	10.8	4.9	1.5	4.8	0.7

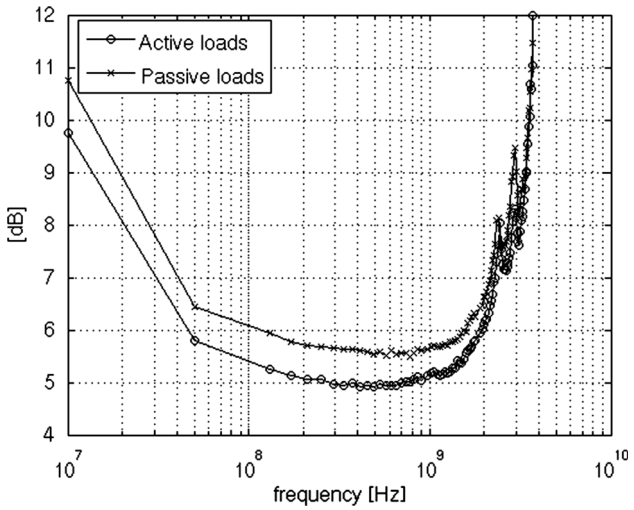

Fig. 16 Comparison of measured LNA NF with active and passive loads

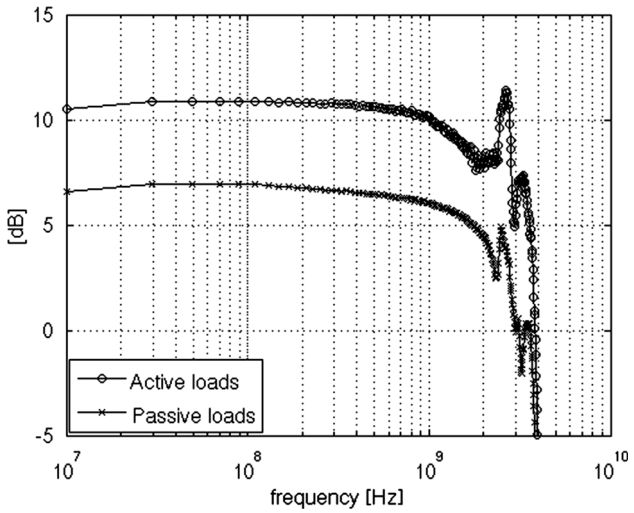

Fig. 17 Comparison of measured LNA gain with active and passive loads

Table 3 Comparison with state-of-the-art LNAs

	Tech (nm)	Band (GHz)	Voltage gain (dB)	NF (dB)	Power (mW)	FOM (mW−1)
[3]	65	0.2–5.2	13-15.6	<3.5	14	0.4
[18]	90	0.5–8.2	22–25	<2.6	42	0.5
[2]	90	0.8-6	18–20	<3.5	12.5	0.6
[14]	90	0.1–1.9	20.6	<2.7	9.6	1.3
[1]	130	0.2–3.8	11.2	<2.8	1.9	2.1
[17]	180	0.5–0.9	16	<4.3	22	0.2
[10]	180	0.1–0.9	15	<4.2	10	0.3
This work	**130**	**0.1–2**	**16.8**	**<5**	**4.8**	**0.7**

5 Conclusions

In this paper we presented the implementation of a low power LNA with noise and distortion cancelling [6] based on the combination of common-gate stage and a common-source stage using active loads. The replacement of resistor loads by transistors reduces the area and cost and adds a new degree of freedom in the design, which can be used to maximize the LNA gain and minimize the noise figure with a minimum impact on linearity.

This improvement is due to the higher dynamic output resistance of the active loads for the same DC voltage drop. Although not used here, active loads allow the control the LNA gain [4] and the reduction of supply voltage [5].

Measurement results of an LNA implemented in a 130 nm CMOS technology have been presented. For comparison, we have also shown the performance of a conventional LNA with resistor loads. For a fair comparison, both circuits have the same power consumption of 4.8 mW, and the same test circuitry. For the LNA with active loads we obtain a gain improvement of about 3 dB, and a NF reduction of about 0.5 dB with an IIP3 higher than 0 dBm.

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