Overview

The IObundle KNN core includes a configurable hardware accelerator for the KNN machine learning algorithm. It is written in Verilog and includes a C software driver. The user may change the size of the module to fit in its own FPGAs balancing the compromise between desired performance and space available. The IP is currently supported for use in FPGAs.

Features

- Verilog KNN machine learning algorithm accelerator
- C software driver.
- Reset, enable, data and test point send and neighbour read functions.
- IOb-SoC native CPU interface.
- AXI4 Lite CPU interface (premium option).

Benefits

- Compact hardware implementation
- Can adapt the instances to different size FPGAs
- Can adapt to the algorithm parameters of the user
- Low power consumption ???

Deliverables

- Verilog source code
- User documentation for easy system integration
- Example integration in IOb-SoC (premium)
- FPGA synthesis and implementation scripts (premium)
- ASIC synthesis and place and route scripts (premium)

Block Diagram

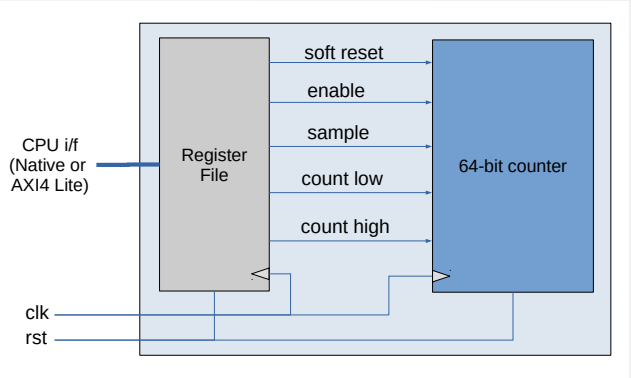

Figure 1: High-level block diagram

FPGA Results

The following are FPGA implementation results for two FPGA device families.

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.