A Fail-Safe Microprocessor Using Dual Synthesizable Processor Cores

Kotaro Shimamura, Shin'ichiro Yamaguchi*, Nobuyasu Kanekawa, Naoto Miyazaki+,
Hiromichi Yamada, Yoshitaka Takahashi, Teppei Hirotsu, Katsuichi Tomobe++,
Kazuyoshi Satoh++, Takashi Hotta, Ryo Fujita

Hitachi Research Laboratory, Hitachi, Ltd., (MD#230) 7-1-1, Omika-cho, Hitachi-shi, Ibaraki-ken, 319-1292, Japan
* Research & Development Center, Hitachi Building Systems Co. Ltd., 1070, Ichige, Hitachinaka-shi, Ibaraki-ken, 312-8506, Japan
+ Mito Transportation Systems Product Div., Power & Industrial Systems Group, Hitachi, Ltd., 1070, Ichige, Hitachinaka-shi, Ibaraki-ken, 312-8506, Japan
++ Device Development Center, Hitachi, Ltd., 16-3, Shinmachi 6-chome, Ome-shi, Tokyo, 198-8512, Japan
E-mail: shimamur@hrl.hitachi.co.jp

Abstract

A chip level redundant self-checking fail-safe microprocessor has been developed using a 0.35 μm CMOS embedded gate array. The microprocessor integrates two synthesizable processor cores and a self-checking comparator in a single chip. A full-custom processor core was transformed into each of the synthesizable cores for this purpose. Design methodologies suitable for reusing synthesizable processor cores has also been developed. Developed synthesizable processor cores and design methodologies reduce the cost of process migration of the chip. Migrating to the newer process improves the performance of the developed microprocessor with low development cost.

1. Introduction

Industrial controller systems require good reliability, and many systems introduce self-checking microprocessors to provide this. One approach to realize a self-checking microprocessor is applying special self-checking circuits to the microprocessor[1]. This approach requires redesign of the whole microprocessor, so the development cost is high. Second approach is adding some kind of redundant circuits to each of the functional units of the microprocessor[2]. This approach also requires redesign of the significant part of the microprocessor, which leads to high development cost. Third approach is utilizing commercial off-the-shelf microprocessor chips and a dedicated comparator chip[3]. As this approach requires design of only the comparator chip, the development cost is lower than the former ones. But the third approach utilizes several chips for one microprocessor function, and this becomes a bottleneck for minimizing the system size.

We applied synthesizable processor cores to the third approach and realized a single chip self-checking microprocessor with low development cost. Utilizing the synthesizable cores also facilitates application-specific customization of the microprocessor in the future, such as changing RAM size, adding ECC to RAM, and improving operating frequencies by way of process migration. A full-custom processor core was transformed into each of the synthesizable cores for this purpose.

This paper describes the developed self-checking microprocessor. The developed design methodologies suitable for reusing synthesizable processor cores are described in detail.

2. Processor Configuration

Fig. 1 shows the configuration of the developed microprocessor. Each of the two processor cores (MP(A) and MP(B)) contains a central processing unit (CPU), 16KB of SRAM (RAM) and peripheral modules. The two processor cores execute the same software in the synchronized fashion. The self-checking comparator[4]

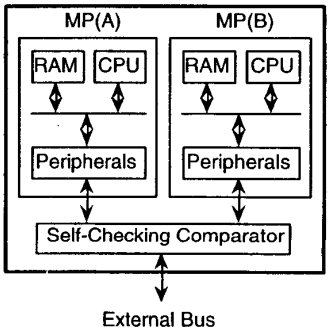


Fig. 1. Configuration of the Developed Microprocessor

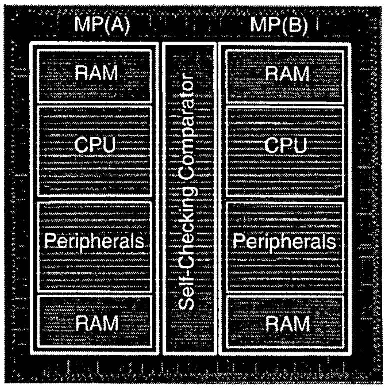


Fig. 2. Chip Photograph

Table 1. Chip Characteristics

Process	0.35 μm 5 Metal CMOS
Hard Macros	PLL x 2, RAM(40KB)
Random Logic	740k gates
Chip Size	14.75 mm□
Operating Frequency	60 MHz
Power Dissipation	2.6W @ 60MHz
Package	479pin BGA

compares the outputs of the two processor cores. When it detects any differences between the data, the comparator stops the two processor cores. The comparator has the ability to detect any faults in the two processor cores and the comparator itself, which greatly improves the reliability of the system using it. Fig. 2 shows a photograph of the chip.

Table 1 lists the characteristics of the developed chip. The chip utilizes a 0.35 μm 5-layer metal CMOS embedded gate array. The master chip contains two PLLs, 40KB of SRAM, and 1,150k random gates in 14.75 x 14.75 chip size. The developed chip uses 740k of 1,150k random gates. It operates at 60 MHz and dissipates 2.6W when operating at 60MHz. BGA package is utilized to quicken heat radiation.

3. High Reliable Architecture

Fig. 3 shows the configuration of the self-checking comparator[4][5]. The test pattern generator generates test patterns for each bit of the input data so that the comparator detects differences between the two inputs at the predetermined period. When the comparator outputs a waveform of the predetermined period, it means that input A and input B are equal and the comparator is good. When the comparator does not output a waveform of the predetermined period, it means that either input A and input B are different or the comparator has some faults. Thus the self-checking comparator can detect not only faults in the input, but also faults in the comparator itself.

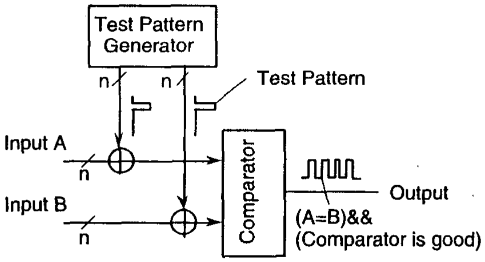
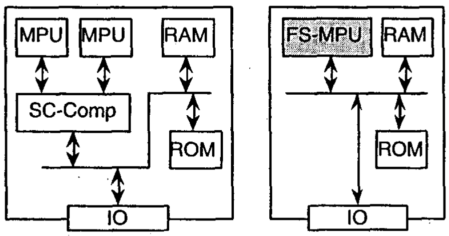


Fig. 3. Self-Checking Comparator (Reproduced from Reference [4] Fig. 1)

SC-Comp: Self-Checking Comparator
FS-MPU: Fail-Safe Microprocessor



(a) Conventional Fail-Safe Controller (b) Developed Chip Application

Fig. 4. Sample Application of the Developed Microprocessor

Fig. 4 shows a sample application of the developed fail-safe microprocessor. A conventional fail-safe controller (Fig. 4 (a)) consists of replicated microprocessors (MPUs), a self-checking comparator (SC-Comp), RAM, ROM and IO circuit (IO). The developed fail-safe microprocessor (FS-MPU) replaces the two MPUs and the SC-Comp in the conventional controller. Utilizing developed microprocessor has following advantages:

(a) Area reduction: smaller number of parts leads to smaller printed circuit board area and makes system integration easier. As the developed microprocessor operates just the same as a single microprocessor in normal conditions, it can easily be applied to currently non fail-safe systems to improve reliability.

(b) Fault rate reduction: smaller number of parts leads to lesser solder junctions on the printed circuit board and reduces the rate of permanent faults. As the solder junctions hold the significant part of the fault rate of the board, this improves the overall system availability.

4. Design Methodology

Table 2 shows the design methodologies of the developed processor core. The data path of the original core contains many kinds of customized circuits and cells, and re-coding of the entire data path is needed to improve process portability of the core. Waveform comparison with the original core helps to detect timing related bugs in an early stage of core development. Characterize-compile synthesis facilitates the change of the floor plan and the target operating frequency. The parametrized floor plan methodology was developed to reuse the floor plan know-how of the designers of the original core. Static timing analysis reduces the time for the timing verification, but the developed core contains some asynchronous logic which cannot be verified with the static timing analysis. The full-timing simulation is utilized for the timing verification of the asynchronous logic. The scan-based manufacturing test is used to reduce the time of test design.

Table 2. MP-Core Design Methodologies

Logical Design	Re-coding data path
Functional Verification	Waveform comparison with the original core
Synthesis	Characterize-compile
Floor Plan	Parametrized floor plan
Timing Verification	Static timing analysis and full-timing simulation
Manufacturing Test	Scan-based test (full scan)

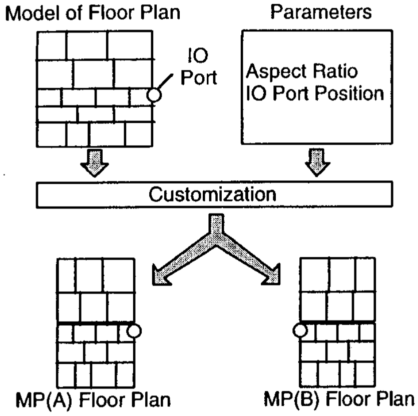


Fig. 5. Parametrized Floor Plan

Fig. 5 shows the developed parametrized floor plan methodology. The floor plan model was developed from the floor plan of the original core and contains the know-how of the designers of the original core. The customization step modifies the model in accordance with the parameters such as aspect ratio and IO port position. In the MP(A) floor plan, the aspect ratio was modified while preserving the relative position of the blocks. In MP(B) floor plan, the horizontal position of the blocks was reversed to make the IO port sit in the left edge of the core. This methodology allows reuse of know-how to create the floor plan customized for the present chip as well as for future applications of the core.

5. Development Cost Evaluation

Fig. 6 shows the development cost evaluation result. The core design portion means the cost to transform the original full-custom core into the synthesizable cores, and consists of re-coding of the data path, functional verification and timing design of the processor cores. The chip integration portion consists of the chip level functional verification, timing design and physical design including the scan-based manufacturing test design.

Reusing the design property of the original core such as the HDL code of control logic and the verification environment reduced the core design portion of the development cost of this work. About 80 % of the core design portion was used for the re-coding of the data path. Reusing the design property of the self-checking comparator reduced the chip integration part of the development cost. Reusing the design property cuts 75% of the development cost of the developed chip.

In the future process migration, the re-coding of the data path is not needed. The developed design methodologies such as characterize-compile synthesis and parametrized floor plan also reduces the cost of the process migration. The development cost of the process migration is estimated to be 20% of the developed chip.

Fig. 7 shows the effect of process migration on operating frequency, internal RAM capacity and power dissipation. As the developed chip utilizes rather old 0.35

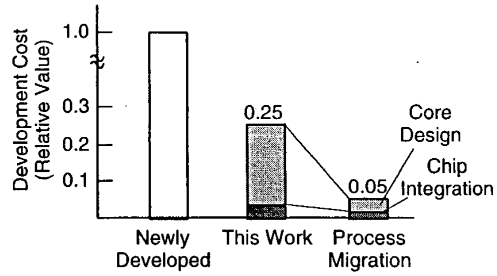


Fig. 6. Development Cost Evaluation

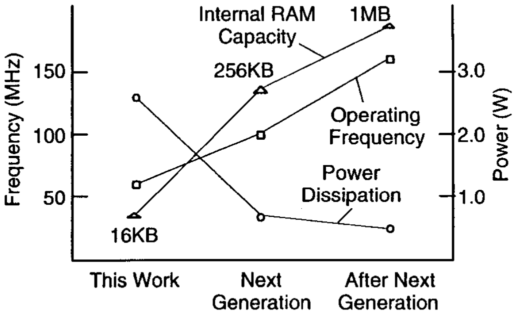


Fig. 7. Effect of Process Migration

μm process, the after next generation chip can be obtained in less than a year. The after next generation chip is estimated to operate at 160MHz, contain as much as 1MB of internal RAM and dissipate 0.5W at 160MHz. The internal RAM capacity augmentation is especially large because more area can be allocated to the RAM as the area of the random logic reduces by the process migration.

The large capacity of internal memory is especially important for controller application. As many systems utilize less than 1MB of memory area, the total memory area can be contained in the internal RAM of the after next generation chip. This eliminates the performance overhead of accessing the external RAM and greatly improve performance. This also allows to remove the RAM in Fig. 4 (b), which leads to area and fault rate reduction.

6. Conclusions

A chip level .redundant self-checking fail-safe microprocessor has been developed using a 0.35 μm CMOS embedded gate array. The microprocessor integrates two synthesizable processor cores and a self-checking comparator in a single chip. A full-custom processor core was transformed into each of the synthesizable cores for this purpose. Design methodologies such as characterize-compile synthesis and parametrized floor plan has also been developed to facilitate the reuse of the synthesizable processor cores. Developed synthesizable processor cores and design methodologies reduce the cost of process migration of the chip. Estimated development cost of process migration is about 20% of the developed chip. Migrating to the after next generation process achieves 2.5 times of operating frequency, 64 times of internal memory and one fifth of power dissipation.

Acknowledgements

The authors wish to thank T. Baji, A. Kiuchi, K. Noguchi, S. Matsui and H. Ohsuga for the discussions about the processor core. They also acknowledge the support of T. Takahashi, T. Ichimaru, Y. Nagasaki, K. Osugi, H. Date, S. Tanaka, Y. Satoh, H. Kajiwara, S. Ueda, S. Takata, K. Ohshima, T. Hachinohe and T. Takehara.

References

[1] M.M. Taso, A.W. Wilson, R.C. McGarity, C.J. Tseng, and D.P. Siewiorek, "The Design of C.fast: Single Chip Fault Tolerant Microprocessor," Proceedings of the 12th Annual International Symposium on Fault-Tolerant Computing Systems, pp.63-69, June 1982

[2] G. Northrop, R. Averill, et al., "600MHz G5 S/390 Microprocessor," 1999 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp.88-89, Feb. 1999.

[3] D.A. Rennels, A. Avizienis and M. Ercegovac, "A Study of Standard Building Blocks for the Design of Fault-Tolerant Distributed Computer Systems," Proceedings of the 8th Annual International Symposium on Fault-Tolerant Computing Systems, pp.144-149, June 1978.

[4] N. Kanekawa, M. Nohmi, Y. Satoh, and H. Satoh, "Self-Checking and Fail-Safe LSIs by Intra-Chip Redundancy," Proceedings of the 26th International Symposium on Fault-Tolerant Computing, pp.426-430, June 1996.

[5] N. Kanekawa, T. Meguro, K. Isono, Y. Shima, N. Miyazaki, and S. Yamaguchi, "Fault Detection and Recovery Coverage Improvement by Clock Synchronized Duplicated Systems with Optimal Time Diversity," Proceedings of the 28th Annual International Symposium on Fault-Tolerant Computing, pp.196-200, June 1998.