

SoCe for Railway Trains&Railways

Xilinx
Webminar

Ver. 200617



Index

- Challenges and Use-cases
 - On-track Electronic Signaling
 - Rolling Stock
- **SoCe** Solutions
- R&D



On-track Electronic Signaling

- Demand for a network infrastructure:
 - Optimized in terms of:
 - Life cycle costs
 - Scalability
 - Data throughput
 - Featuring:
 - Highest levels of availability
 - Easy integration into existing infrastructures
 - Security
 - Safety



On-track Electronic Signaling

Field-buses converge on Ethernet...but...the application demands High-Availability

- Redundancy with Zero-delay recovery time
- Switch-less Ring Network topologies (HSR)
- Latency worst case known Ring Network topologies (HSR)
- Full compatibility with standard Ethernet (PRP)
- Seamless HSR-PRP merging
- Redundant PTP





On-track Electronic Signaling

Solutions based on Time-Sensitive Networking (TSN):

- Redundancy with Zero-delay recovery time (802.1CB)
- Network topology simplification:
 - Deterministic Ethernet
 - Advanced QoS for Real Time traffic: *Scheduled, Reserved, Best Effort*
 - OT/IT traffic integration in the same network

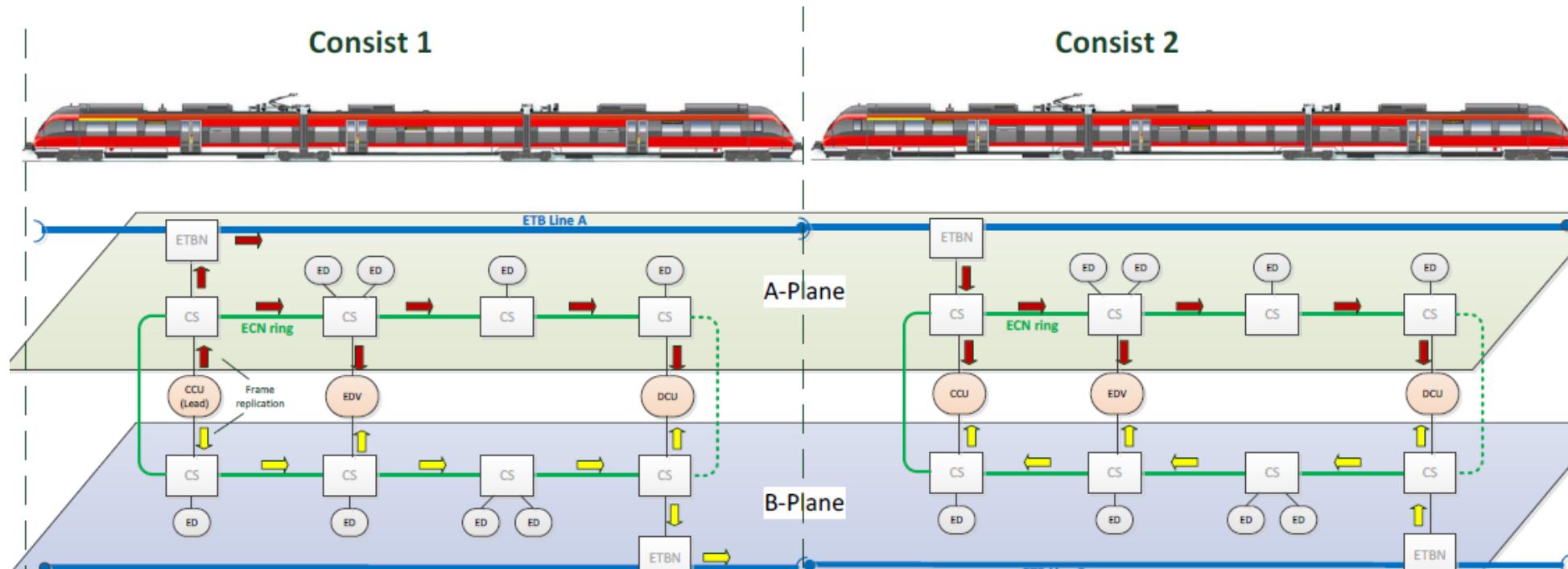
Rolling Stock

- Evolving TCN-Train Communication Networks with Time-Sensitive Networking (TSN):
 - Simpler Network Infrastructure
 - Simplified integration due Interoperability
 - Support for :
 - Controlled network latency (Deterministic Ethernet)
 - Zero-delay recovery time Redundancy



Rolling Stock

- Ethernet Train Backbone (ETB)
- Ethernet Consist Network (ECN)

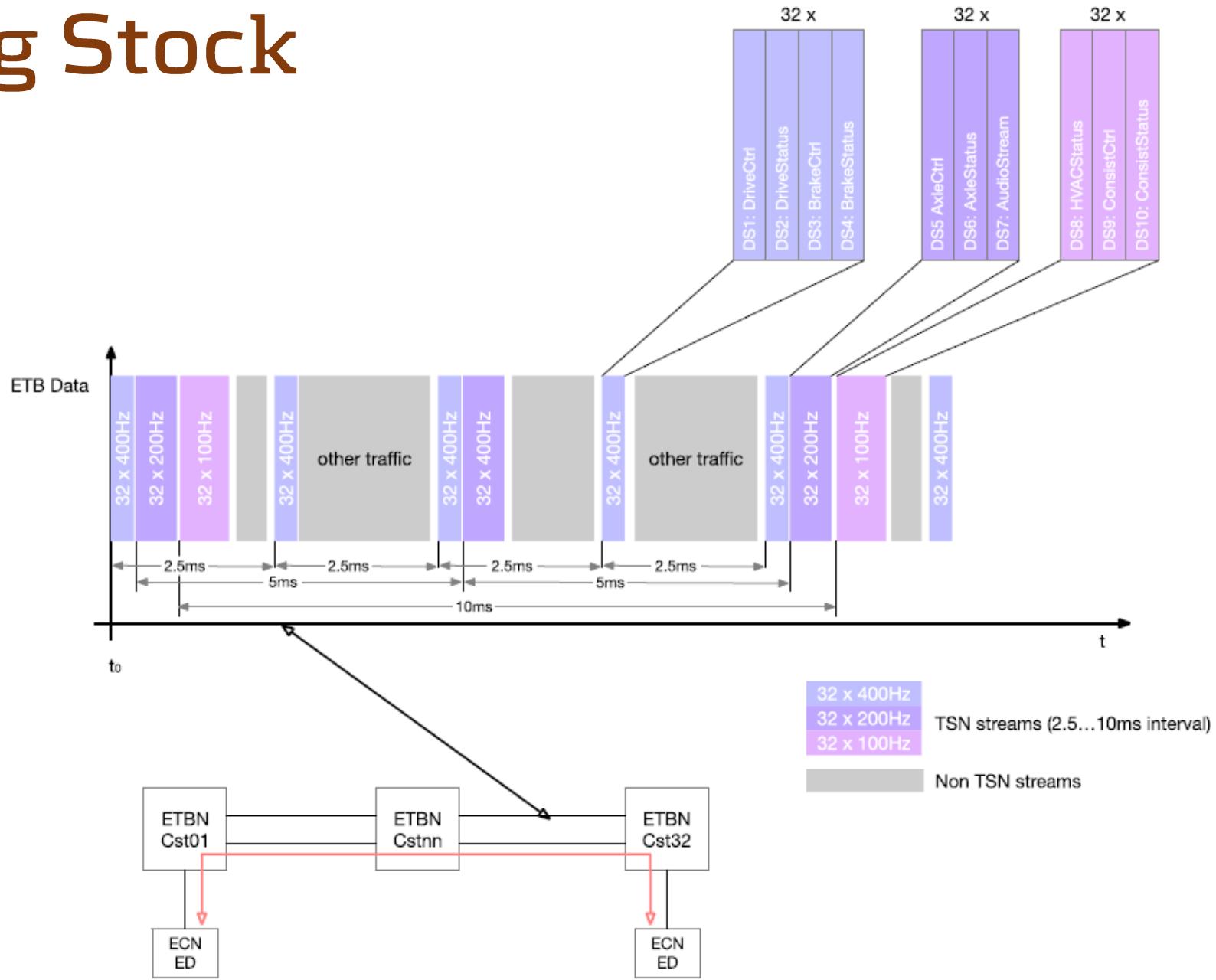


CCU	Consist Control Unit
CS	Consist Ethernet Switch
DCU	Door Control Unit
ECN	Ethernet Consist Network
ED	End Device
EDV	Electronic Distribution Valve (Brake)
ETB	Ethernet Train Backbone
ETBN	Ethernet Train Backbone Node

} Scheduled data traffic (TSN)

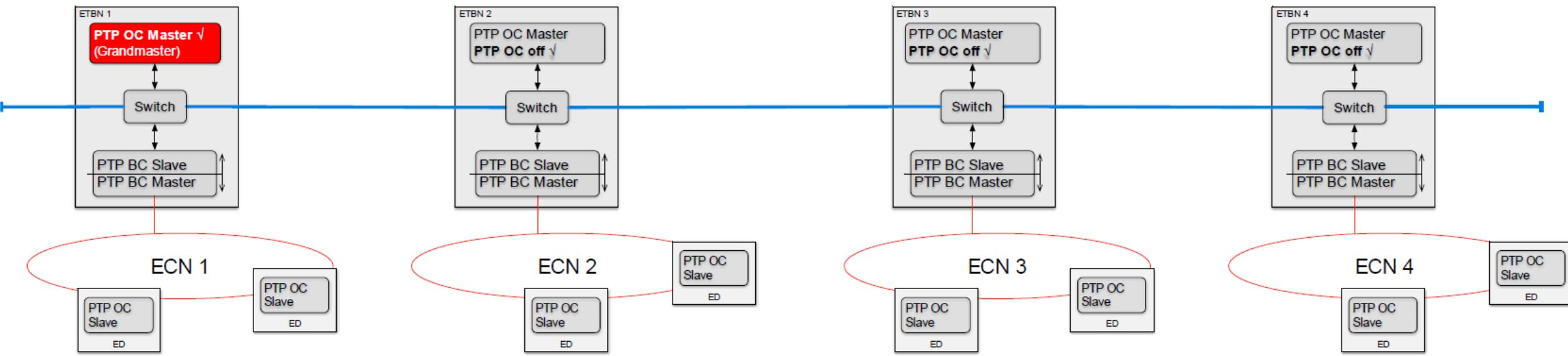
- TSN Streams over ETB (Source SAFE4RAIL D1.9)

Rolling Stock



Rolling Stock

- IEEE 1588 based accurate synchronization distribution



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- Challenges and Use-cases
- **SoCe Solutions**
 - 1G/10G Managed Ethernet Switch IP
 - Time-Sensitive Networking TSN IP
 - SoMs and Boards
 - MTSN IP integration example
 - Wire-speed security for Ethernet
- R&D



1G/10G Managed Ethernet Switch IP

- **Designed for Critical Systems:**
 - Scalable up-to 32 ports
 - No-frames lost at full-speed
 - Distributed memory for low-latency
 - IEEE 1588 Synchronization
 - Redundancy: (MR)STP, DLR, MRP, HSR/PRP)
- **Head-of-Line blocking free architecture to support:**
 - Full-speed switching at 10G
 - Switching availability even in congestion in output ports
 - Low-latency thanks to MAC queries parallelization



1G/10G Managed Ethernet Switch IP

- Enriched with Advanced Switching Features:
 - Ethernet Type based switching
 - Fully VLAN support
 - Multicast Filtering
 - Configurable Jumbo frame support
 - Complete Statistics



1G/10G Managed Ethernet Switch IP

- **Cybersecurity Support:**
 - Hardware filtering for IEEE 802.1X
 - Frame Rate Limiting
 - Broadcast Storm Protection
 - Embedded Port Mirroring capability
 - Optional Wire-speed security



1G/10G Managed Ethernet Switch IP

- Easing the integration for the designer:
 - Fully parametrizable in Xilinx Vivado
 - Software support: APIs and GUI
 - Reference Designs
 - SoMs and Development Platforms



Time-Sensitive Networking IP

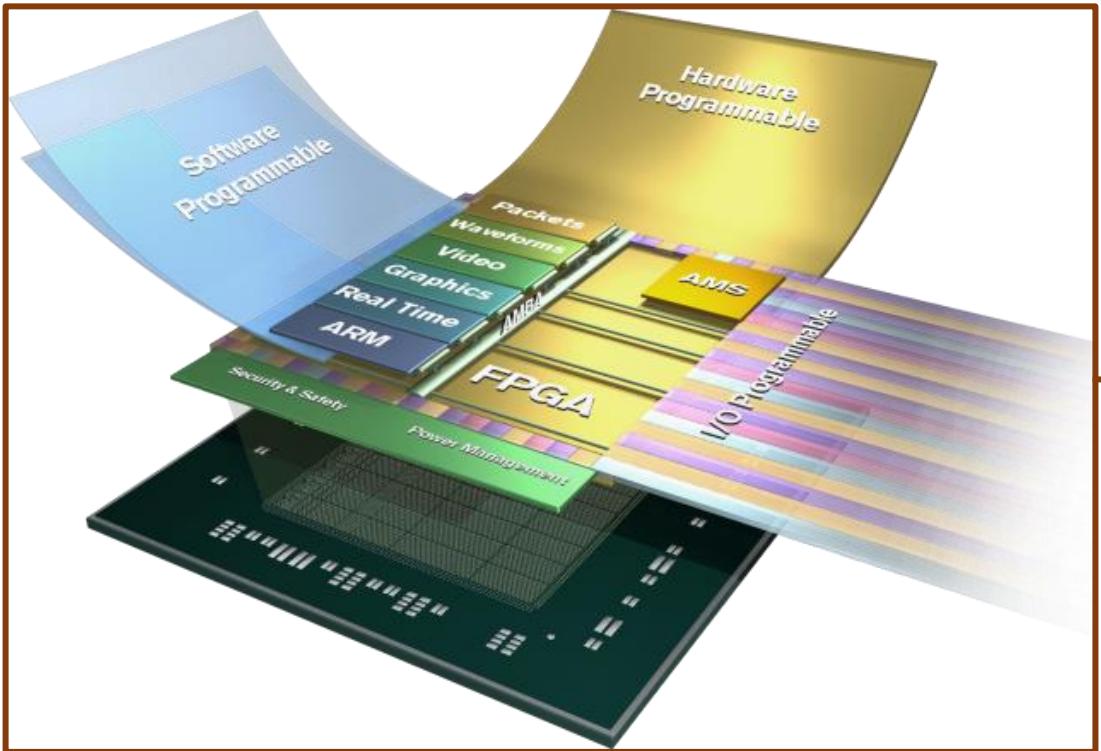
- All-in-one flexible solution for TSN:
 - Fully parametrizable in Xilinx tool
 - Number of ports
 - Desired TSN features
 - Software stacks supported
 - Reference Designs and Development Kits



Time-Sensitive Networking IP

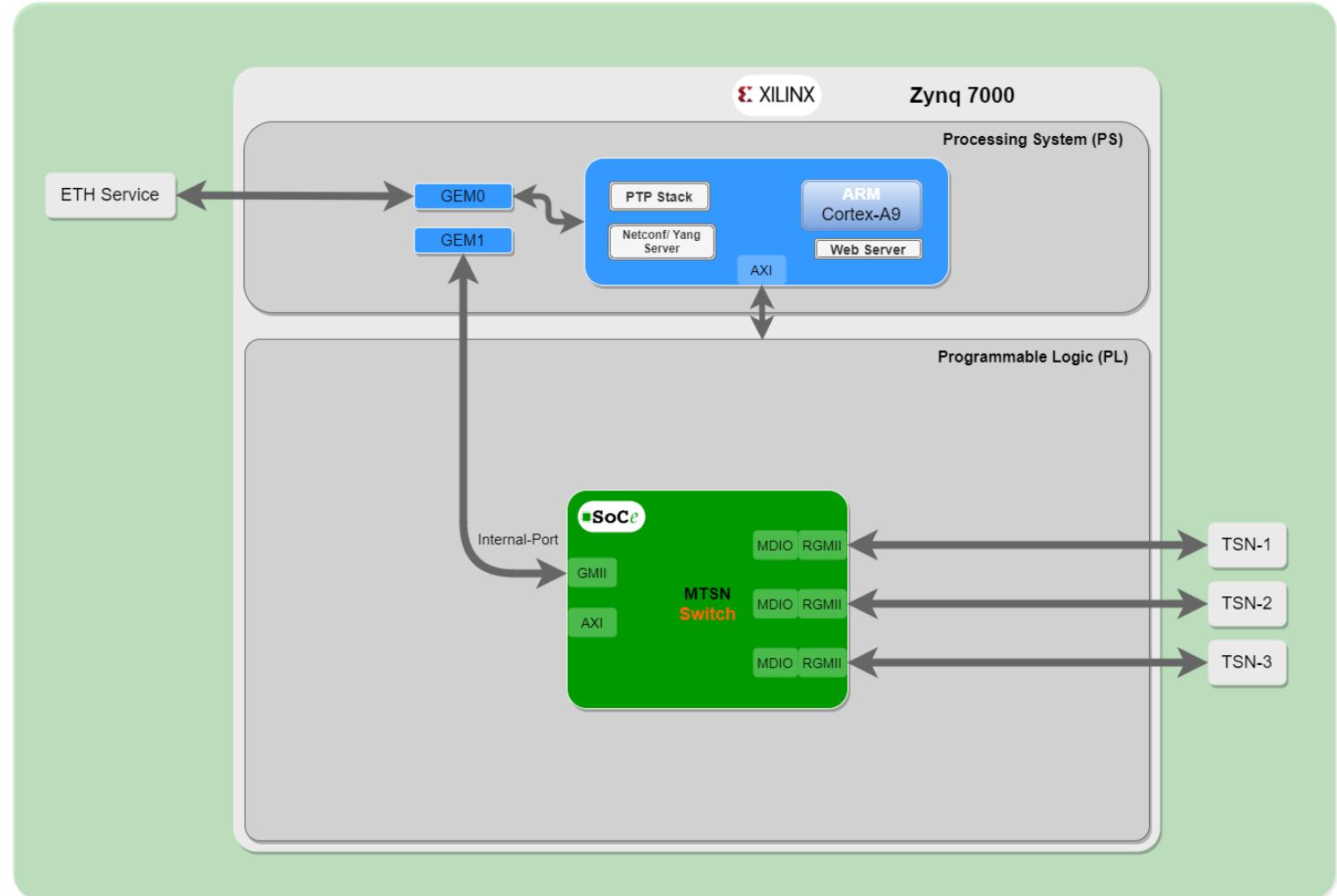
- Complete TSN features to build a node according to your Profile:
 - Time-aware Shaping
 - Credit-based Shaping
 - Redundancy
 - Pre-emption
 - Interoperable Configuration

MTSN Switch IP: Integration Examples on SoCs

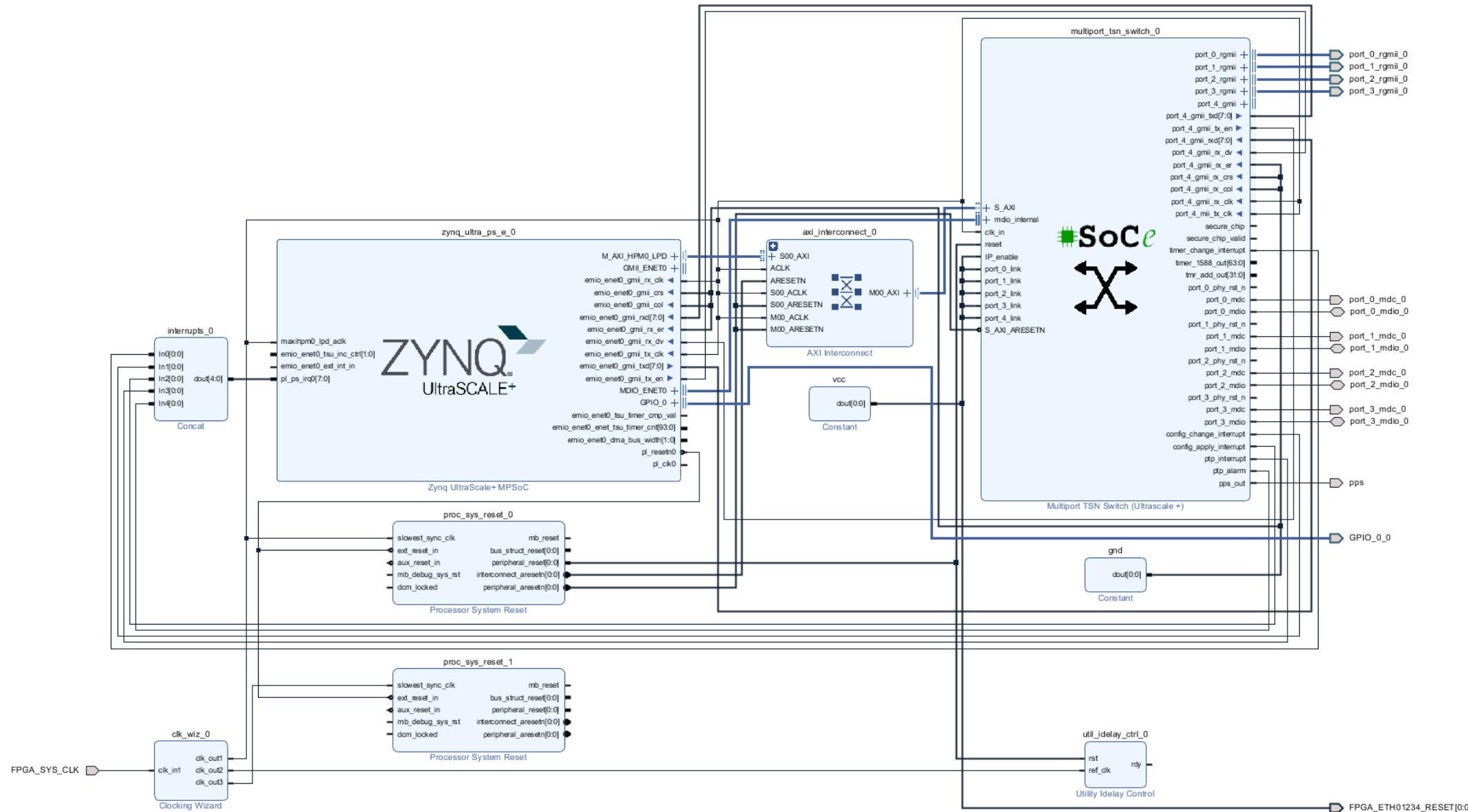


MTSN Switch IP: E.g. Multiport TSN Switch

- 4x port TSN Bridge implementation
- Linux + middleware ARM CPUs in PS
- PS GEM links MTSN switch in PL

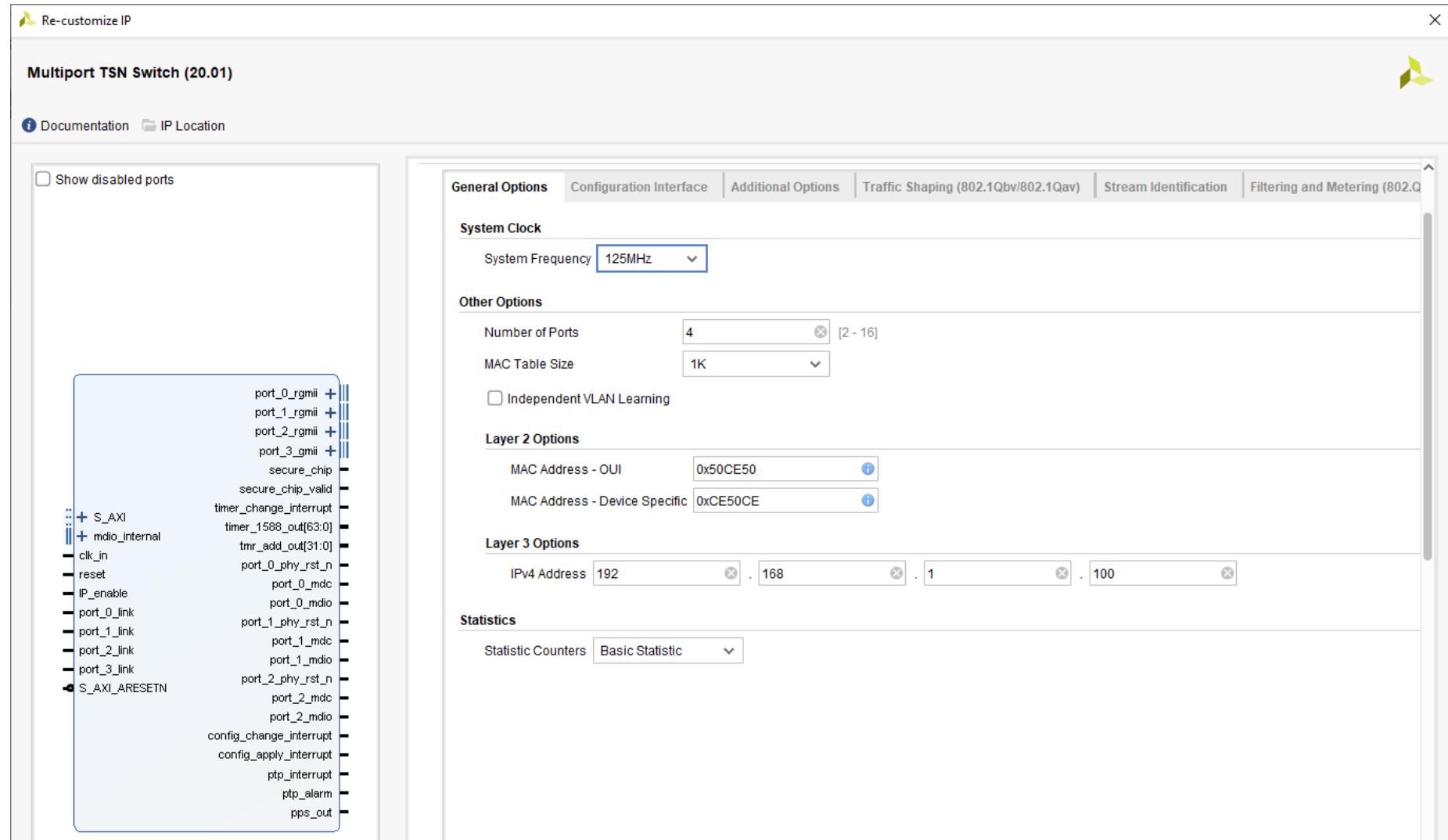


MTSN Switch IP: E.g. Multiport TSN Switch



MTSN Switch IP: Easy Customization and Integration

- How to define the General Options of the IP?



MTSN Switch IP: Easy Customization and Integration

- How to define the Stream Identification mechanisms?
- How to integrate seamless redundancy (CB)?
- How to optimize the IP?
 - Maximum Number of Slots
 - Credit Based Shaping

The screenshot shows the Stream Identification tab of a configuration interface. It includes settings for Stream Identification Function (Active Destination MAC and VLAN Stream Identification), Stream Handle Width (64 Stream Handle), and Stream Identification Table Size (1K). Below this is the Active Stream Translation section with a Translate Function dropdown set to VID.

The screenshot shows the Configuration Interface tab of a configuration interface. A checkbox labeled 'FRER Enable' is checked.

The screenshot shows the Traffic Shaping (802.1Qbv/802.1Qav) tab of a configuration interface. It includes TSN - Time Slot Settings (Supported Maximum Gate Control List Depth set to 256 Slots) and Credit Based Shaping (802.1Qav) (IEEE802.1Qav Enable checked).

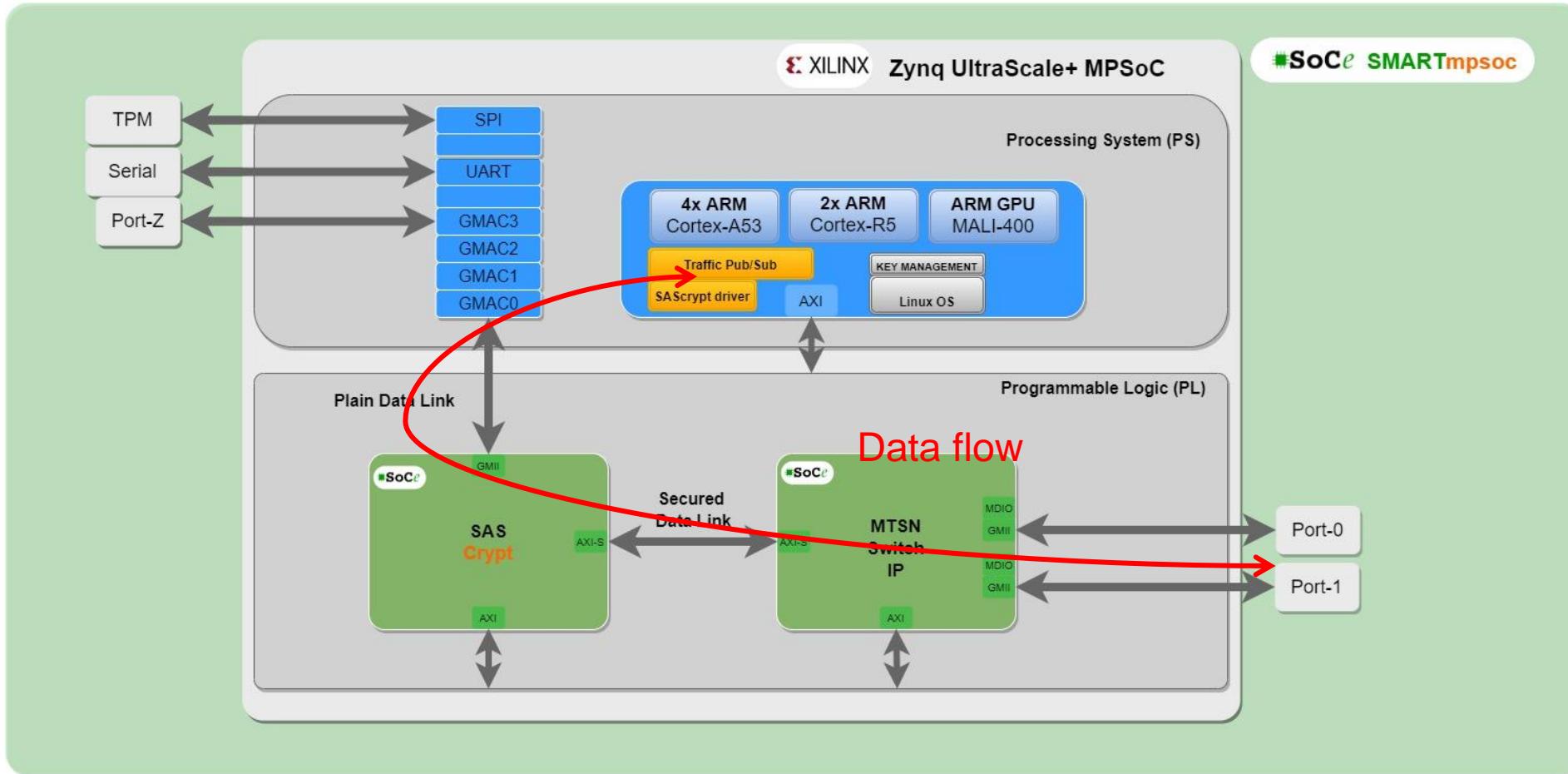


Wire-speed security for Ethernet

- Facing the challenge of securing real-time traffic:

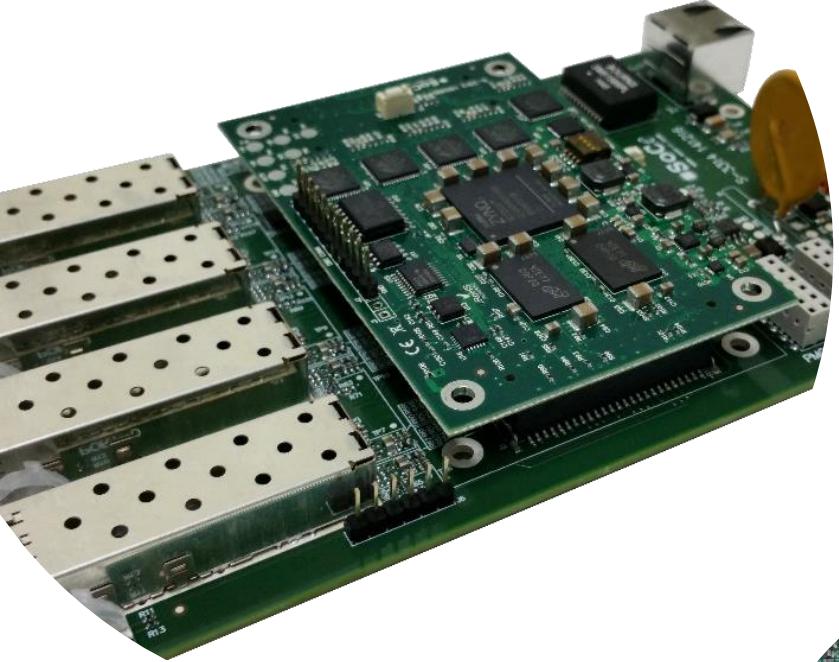
- Fixed and ultra-low latency
- AES-GCM based wire-speed cryptography
- Automatic Ethernet traffic type identification
- Fixed and small latency depending on Secure Frame Format
- Single core to support up to 16Gbps of data bandwidth
- Multiple parallel Security Keys management

MTSN Switch IP: E.g. Secure TSN Switch



- Wire-speed Cryptography for Scheduled Traffic





SoMs and Boards

- Focused on Networking applications:
 - Xilinx Zynq-7000, Ultrascale+ MPSoC, Artix-7
 - Evaluation, Reference and Production

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- Challenges and Use-cases
- SoCe Solutions
- R&D
 - Interoperability Events



Interoperability Events

- IEEE ISPCS 2011: Munich (Germany). Product qualified: Precise Time Basic on S6
- UCA Pre-testing for CIGRE 2012: Winterthur (Switzerland). Product qualified: HSR/PRP on S6
- CIGRÉ 2012: Paris (France). Product qualified: HSR/PRP on S6 in customer product
- IEEE ISPCS 2012: San Francisco (USA). Product qualified: 1588Tiny IP S6
- UCA Pre-testing for CIGRE 2014: Bilbao (Spain) Coordinated and hosted by SoCe 1GE HSR and IEEE 1588 test passed
- CIGRÉ 2014: Paris (France). Coordination Demo
- IEEE ISPCS 2014: Austin (USA) Products qualified: 1GE HSR/PRP with IEEE1588 running Power and Utility Profile
- IEEE ISPCS 2015: Beijing (China):PRP/HSR<-> HSR new BC. Secure 1588
- IEEE ISPCS 2016: Stockholm (Sweden): IEEE 1588 AS profile [AVB and TSN]
- IIC TSN TESTBED 2018: Erbach, Stuttgart, Hannover (Germany): QbV, AS profile, modules
- IIC TSN TESTBED 2019: Hannover, Stuttgart (Germany). Beasain (Spain): CB, YANG
- IIC TSN TESTBED 2020: Stuttgart (Germany): Network

R&D



Time Sensitive Networking - Flexible Manufacturing



Time Sensitive Networking (TSN) is key for industrial applications such as process and machine control where low communication latency and minimal jitter are critical to meeting closed loop control requirements. TSN is the first fully open, standard and interoperable way to fulfill these requirements.

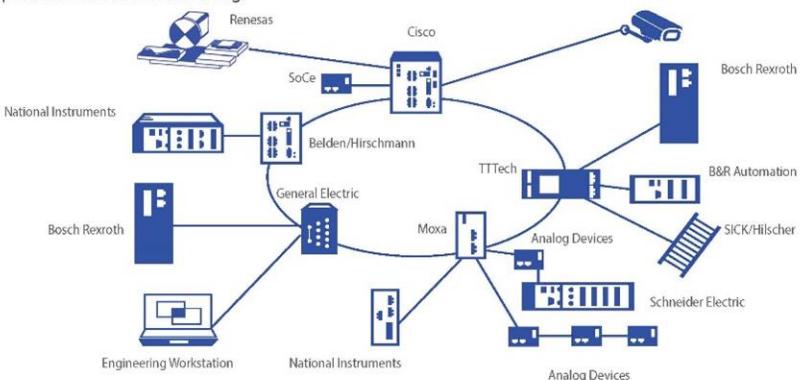
CHALLENGE

Manufacturing operations requires tight coordination of sensing and actuation to safely and efficiently perform closed loop control. Typically, these systems have been deployed using non-standard network infrastructure or air-gapped (unconnected) standard networks. This approach makes devices and data much harder to access and creates a technical barrier to IIoT which is predicated on the ability to consume data anywhere throughout the infrastructure.

To address these needs of IIoT all the way to the control system, the IEEE organization has been working to update the standards for Ethernet and wireless (IEEE 802) to support time sensitive networking.

SOLUTION

TSN enables a single, open network infrastructure supporting multi-vendor interoperability through standardization and IT and OT convergence through guarantee of service. The technology will be used to support real-time control and synchronization of high performance machines over a single, standard Ethernet network. This testbed showcases an early implementation of TSN. As such, it will show the value of the technology as well as some of the challenges in implementations from a number vendors. This testbed will not only document the value of TSN, but will provide feedback to the relevant standards organizations on areas of further clarification or improvement.



R&D



CONNECTA-2 & Safe4RAIL-2 joint TSN interoperability tests
14 June 2019

https://projects.shift2rail.org/s2r_ip1_n.aspx?p=CONNECTA-2

- CONNECTA-2 project Safe4Rail-2: Beasain on 27th, 28th and 29th May 2019 for the first TSN interoperability tests
- TSN IP cores to be used in Urban and Regional demonstrator of CONNECTA-2 project have been tested.
- These tests have validated the full interoperability of SoC-e IP with other TSN technologies, to be used in consist and train switches of the demonstrators
- The IP core from SoC-e to be used in the TSN controller deployed by CAF.

About SoC-e



- Provides IP cores, modules and end-equipment for
 - Networking:
 - Deterministic Ethernet:
 - MTSN, D-HSR
 - High-availability Ethernet:
 - HSR/PRP, MRP, S-HSR
 - Time-aware Ethernet:
 - MES, UES, Field-buses
 - Synchronization:
 - IEEE1588, Irigb
 - Real-time Cyber-security



Field-proven Technology in more than
25 countries worldwide

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