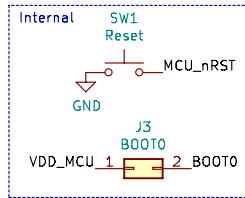
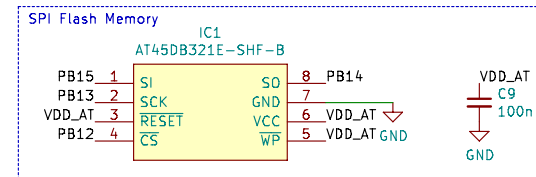
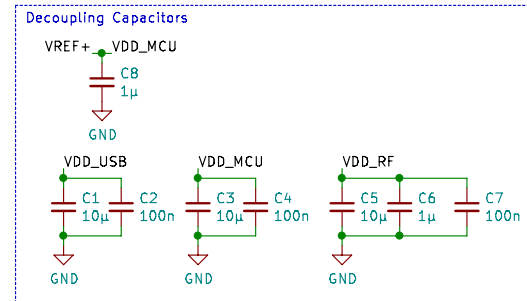
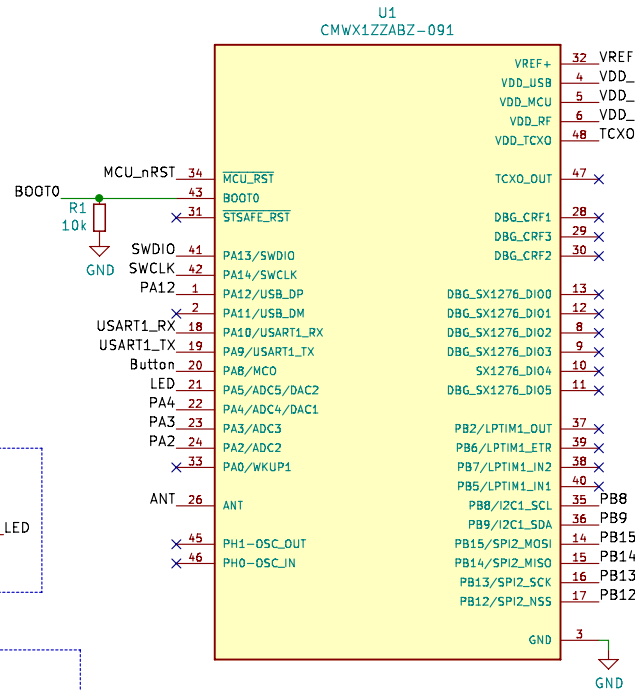
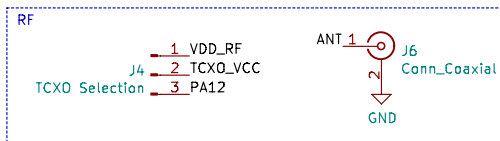
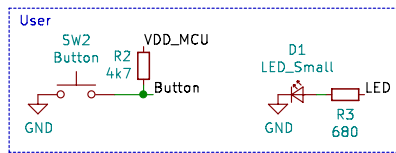
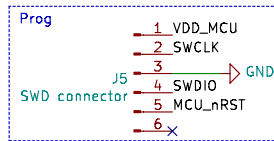


PWR_FLAG TCXO_VCC
PWR_FLAG VDD_AT
PWR_FLAG VDD_MCU
PWR_FLAG VDD_USB
PWR_FLAG VDD_RF
PWR_FLAG GND

J1
Pin1
1 USART1_RX
2 USART1_TX
3
4 PA4
5 PA3 GND
6 PA2
7 PB8
8 PB9



J2
Pin2
1 VDD_USB
2 VDD_MCU
3 VDD_RF
4 VDD_AT
5 PB15
6 PB14
7 PB13
8 PB12



- Module reset does not need external pull up
- VREF+ connected to VDD because battery powered and VDD may be fluctuating
- L1 C8 C9 as in Murata not used for ANT
- VDD_TCXO to PA12 to control TCXO on/off
- BOOT0 to select boot mode (Default Flash)
- Add external osc???
- 8Fx1L-254mm

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File: Master Thesis PCB.sch		
Title: LoRAWAN FUOTA		
Size: A4	Date: 2019-11-26	Rev: 1.1
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