Arithmetic Logic Unit

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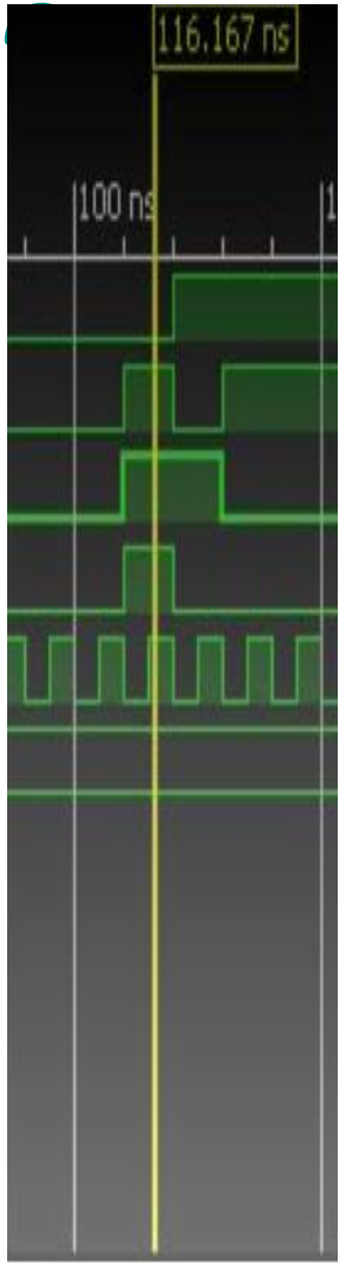
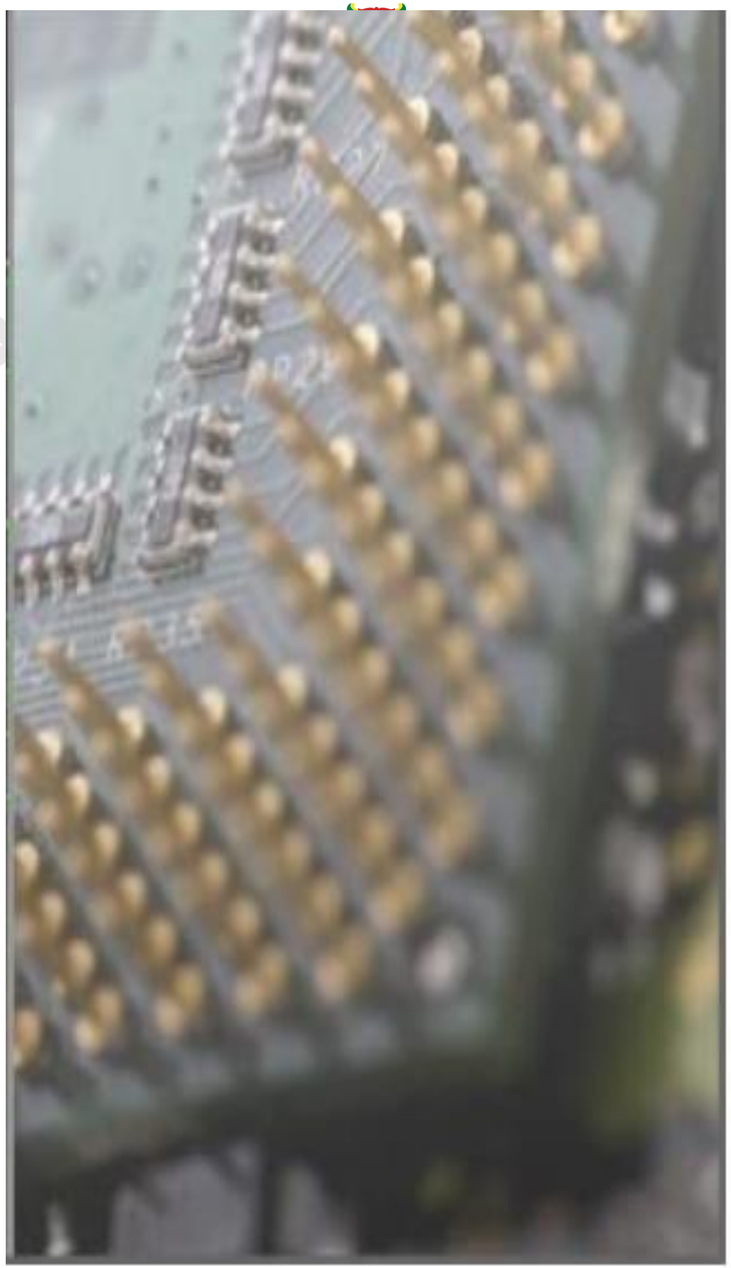
Agenda

- ALU

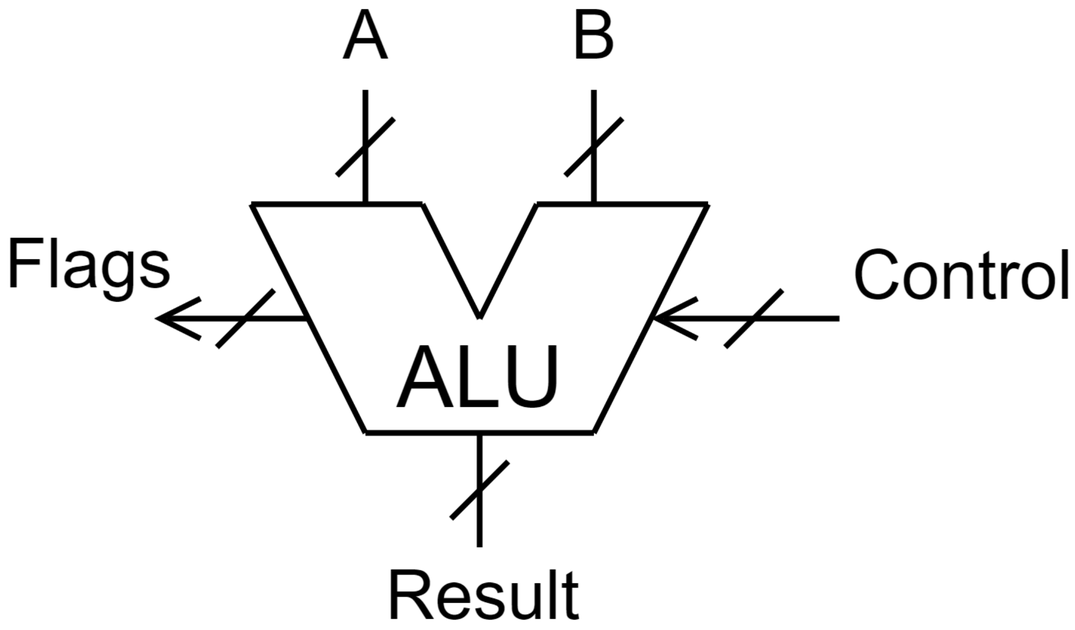


ALU



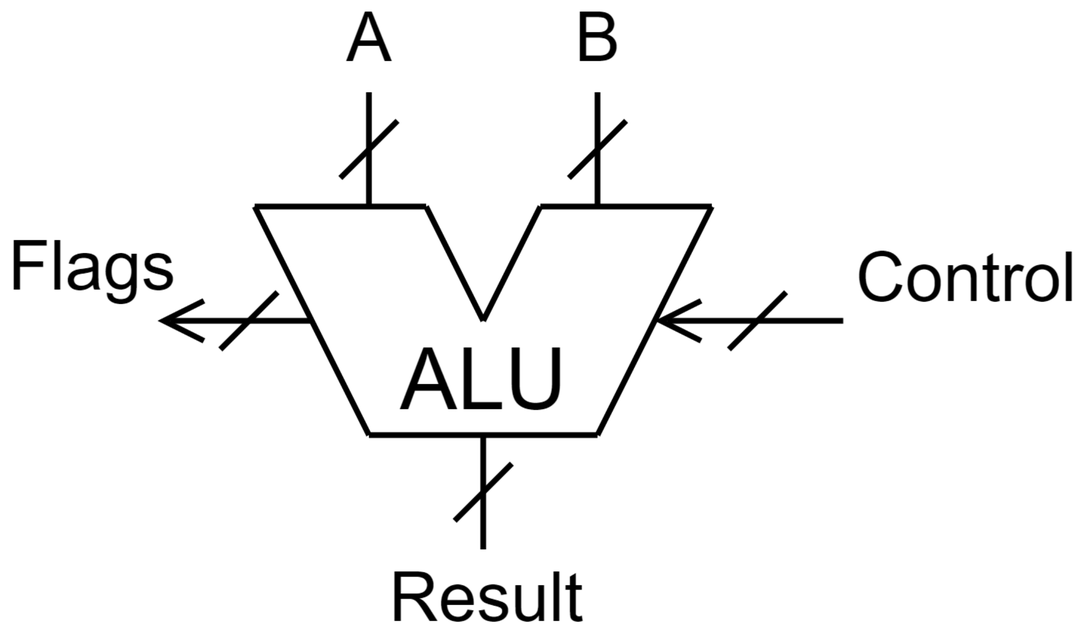
Arithmetic Logic Unit

An ALU (Arithmetic Logic Unit) is the fundamental building block of a processor (CPU) responsible for carrying out arithmetic (addition, subtraction, multiplication, division) and logical operations (comparisons, bitwise operations, etc.).



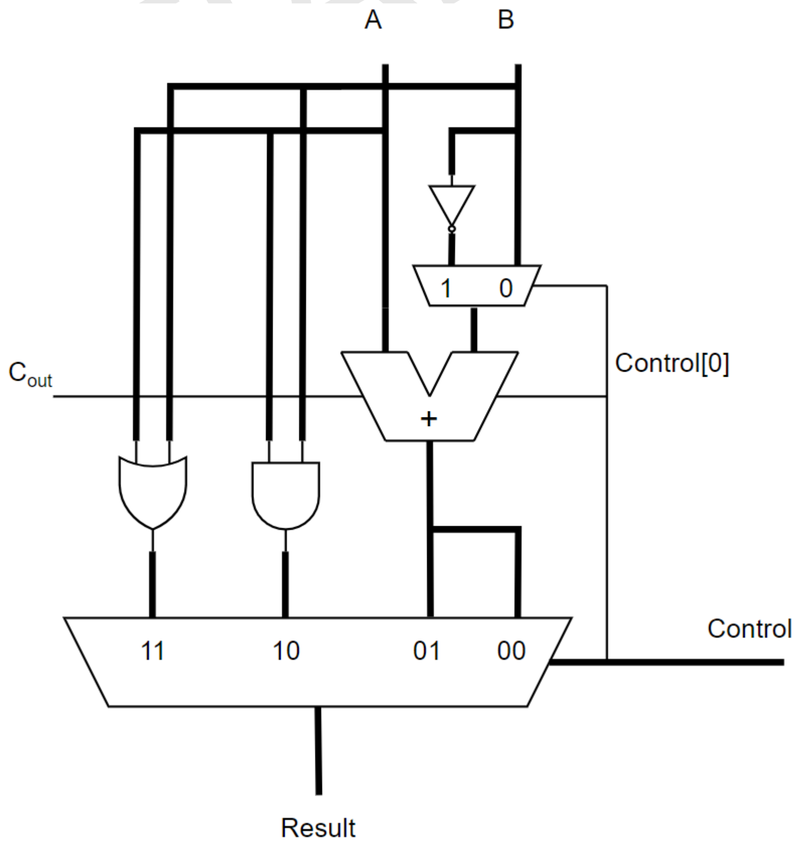
Arithmetic Logic Unit

Control signals select the operation to perform, and flags indicate the status of the result.



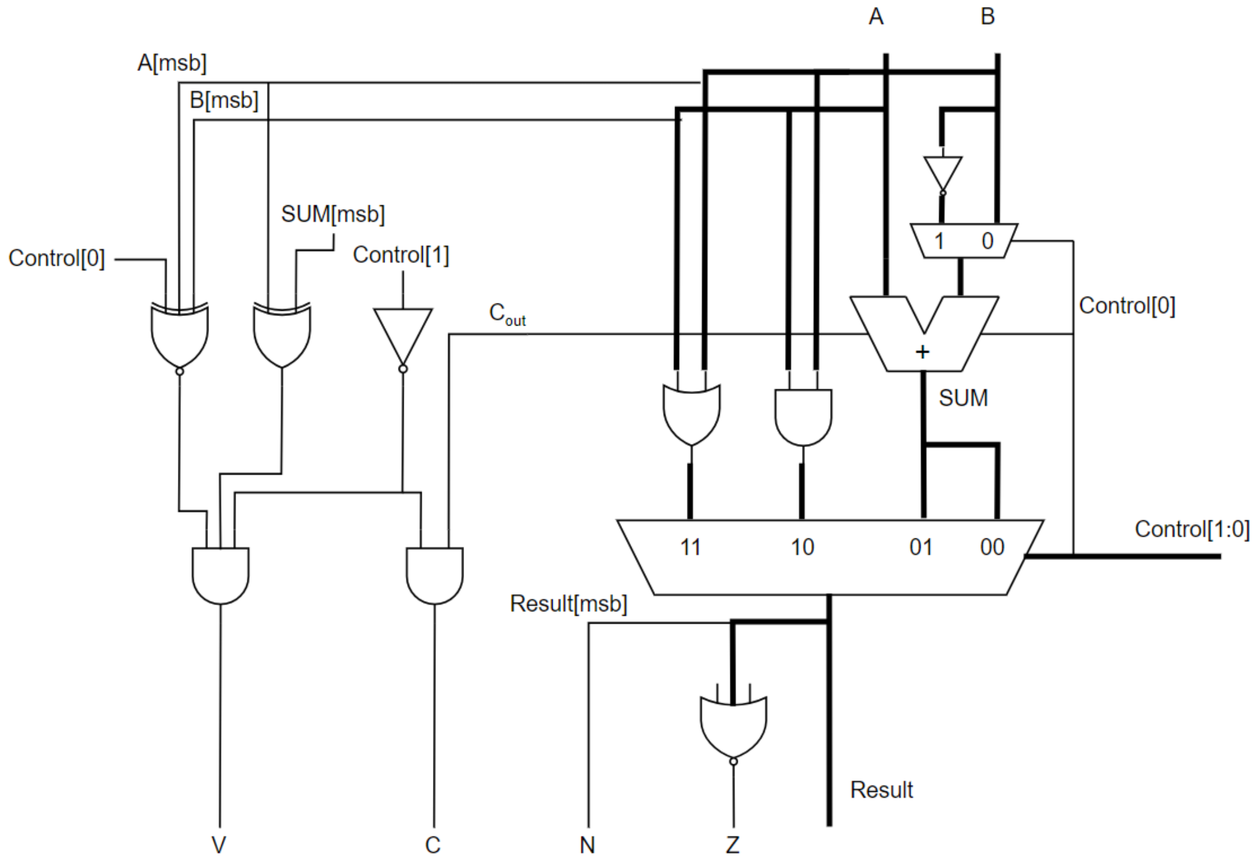
Basic ALU (Operations)

Control	Function
00	Add
01	Subtract
10	AND
11	OR

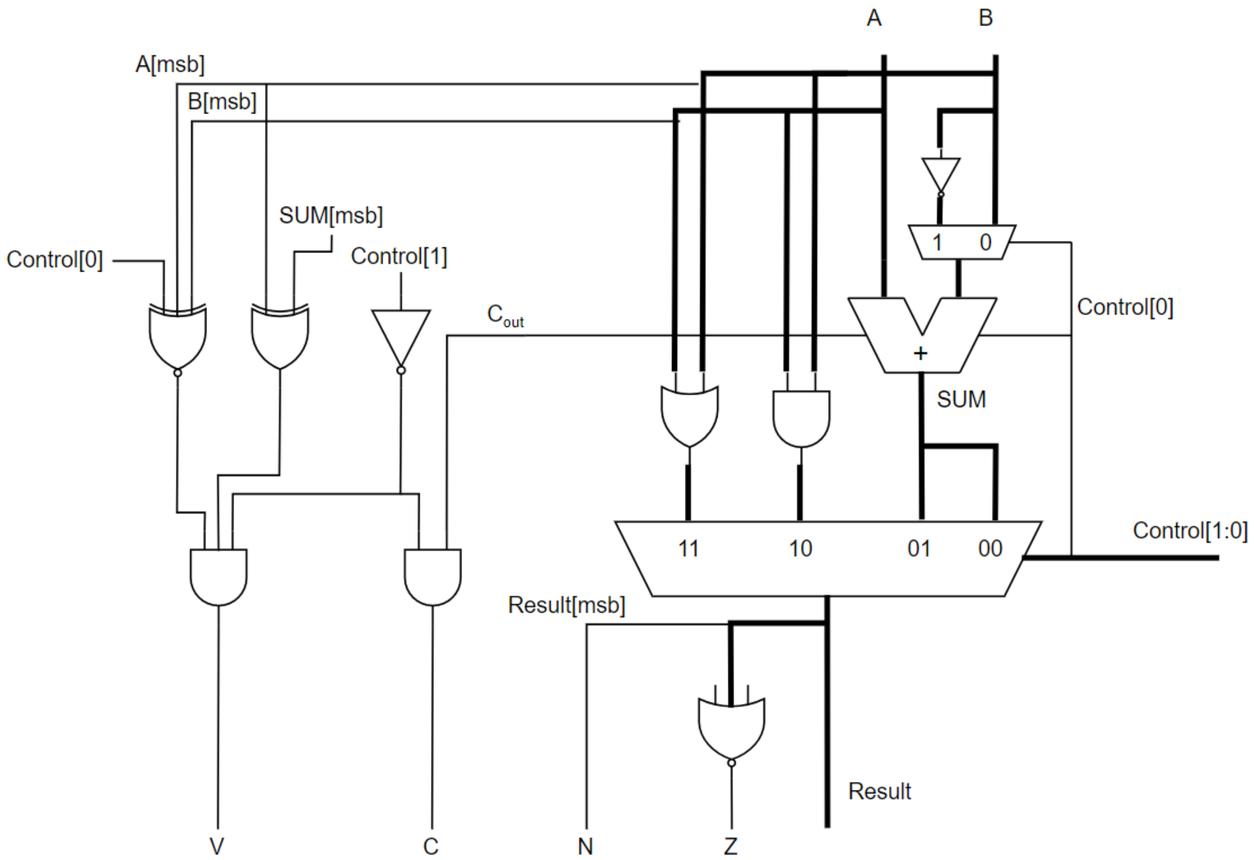


Basic ALU(flags)

Flag	Description
N	Result is Negative
Z	Result is zero
C	Adder produces carry out
V	Overflow

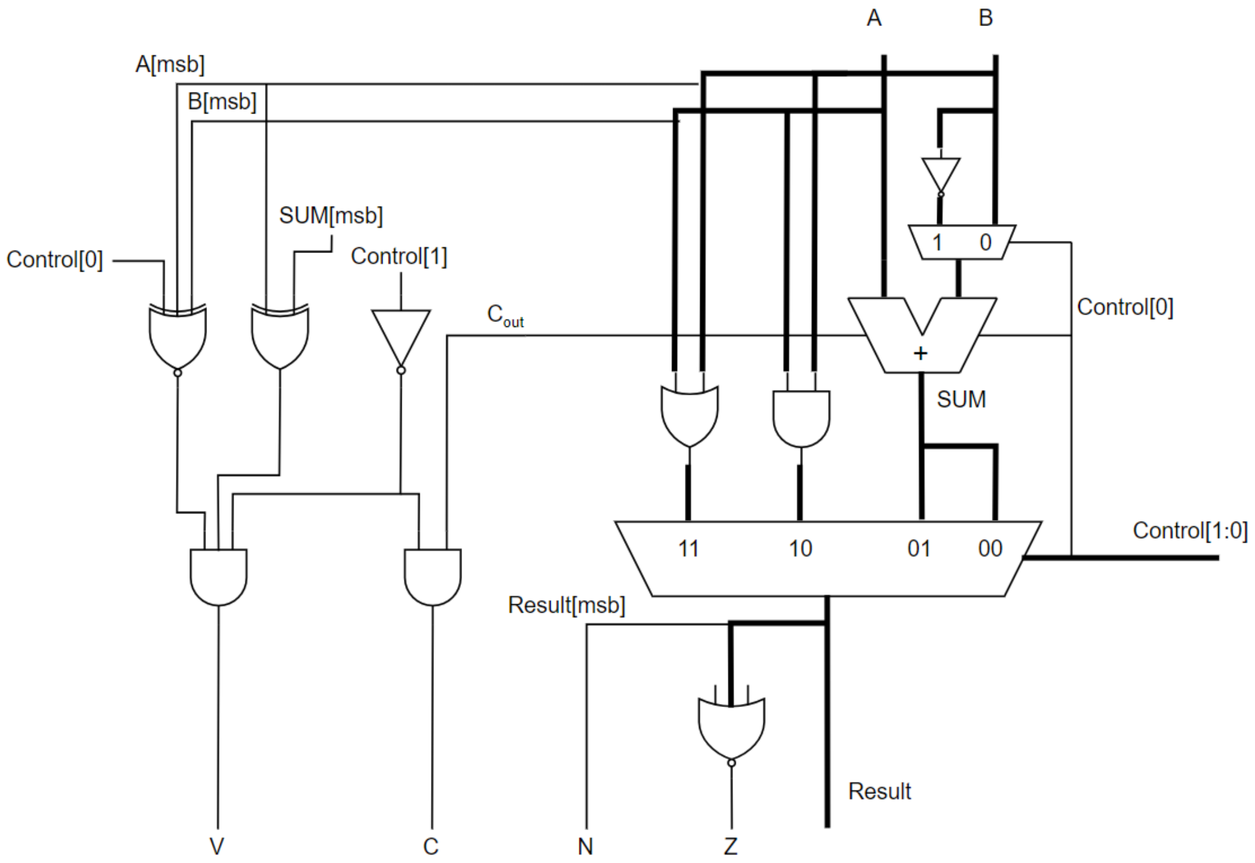


Basic ALU(flags)



N: sign can be determined by the msb of result.
Z: zero can be determined by checking that every bit of the result is 0.
C: carry can be determined when adder produces a carry out due to an addition or subtraction.

Basic ALU(flags)



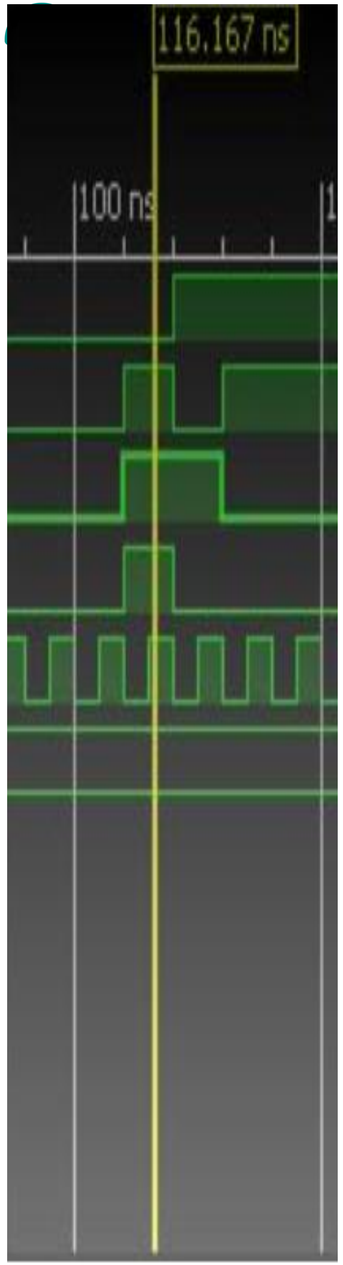
V: Overflow occurs when:

- Addition or subtraction is performed **(control[1]==0).**
- Only when 2 numbers with the same sign are added overflow is possible. **(A[msb]⊕B[msb]⊕[Control[0])**.
- Inputs of adder are different from output **(A[msb] ⊕ Sum[msb]).**

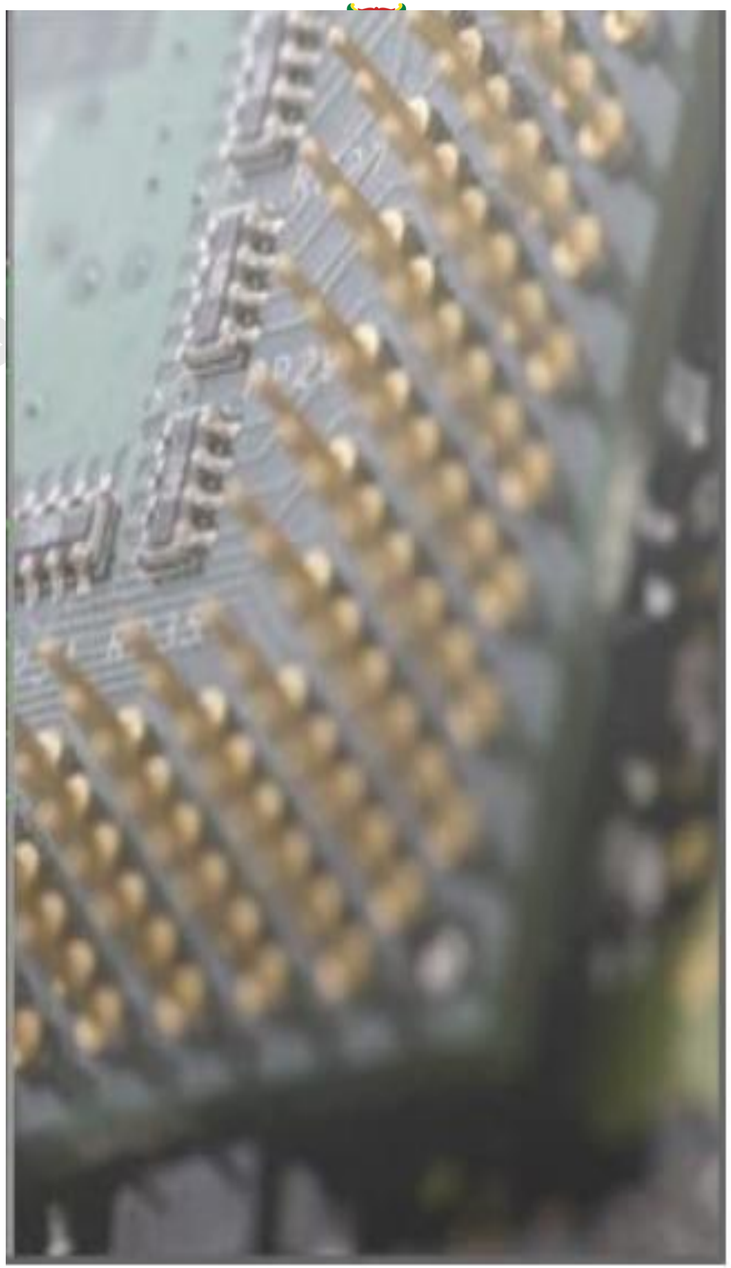
ALU comparisons using flags

When A-B operation is performed we can use flags to perform comparisons. The table show how flags can be used.

Comparison	Signed	Unsigned
==	Z	Z
<	N⊕V	$\bar{C}$
>	$\bar{Z}(\overline{N \oplus V})$	$\bar{Z}$C



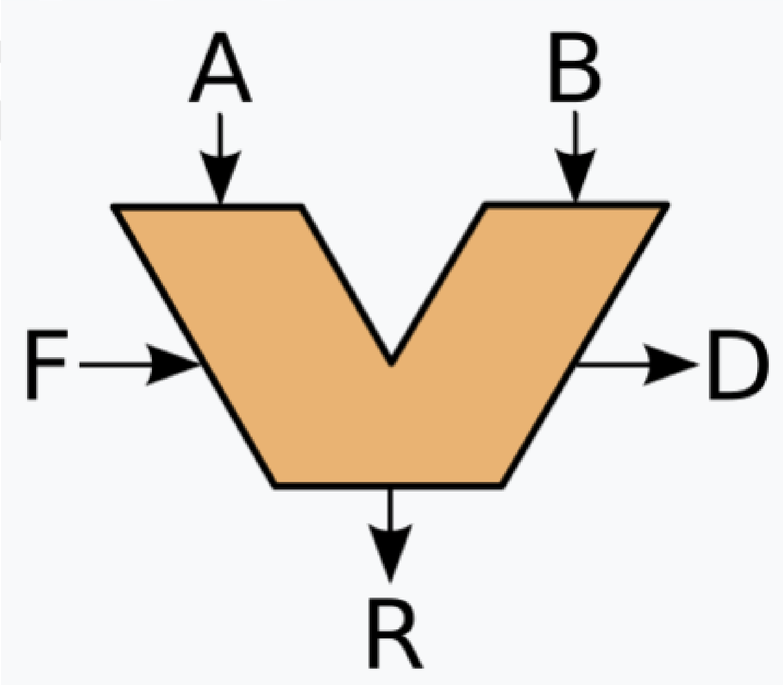
Lab



Labs

- **Lab: Arithmetic Logic Unit (ALU)**

ALU is the digital circuit responsible for performing arithmetic and logic operations within processors.



Arithmetic Logic Unit

Design an ALU with the following specifications.

Control bus	Function	Description
000	AND	Bitwise AND
001	OR	Bitwise OR
010	XOR	Bitwise XOR
011	SLL	Shift left logic input A
100	ADD	Arithmetic addition A+B
101	SUB	Arithmetic subtraction A-B
110	SLTU	Set if less unsigned (A < B)
111	SEQ	Set if equal (A ==B)

Flag	Description
N	Result is Negative
Z	Result is zero
C	Adder produces carry out
V	Overflow