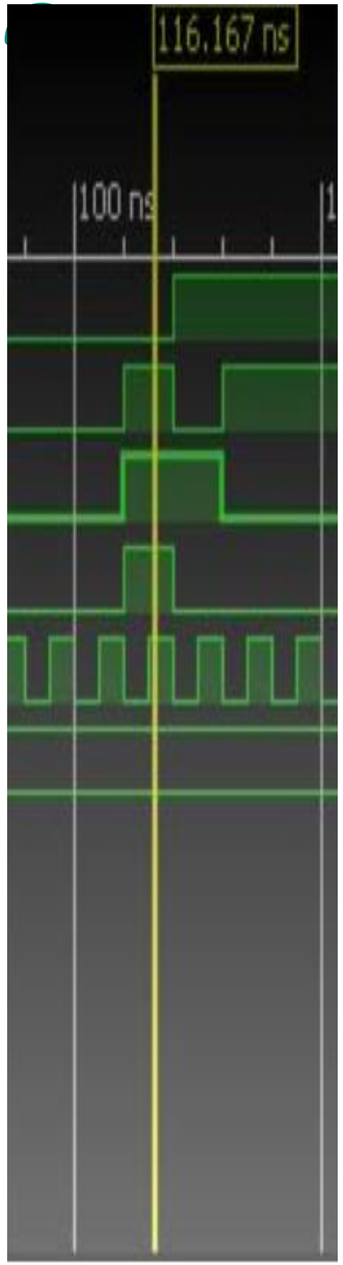
Combinational logic II

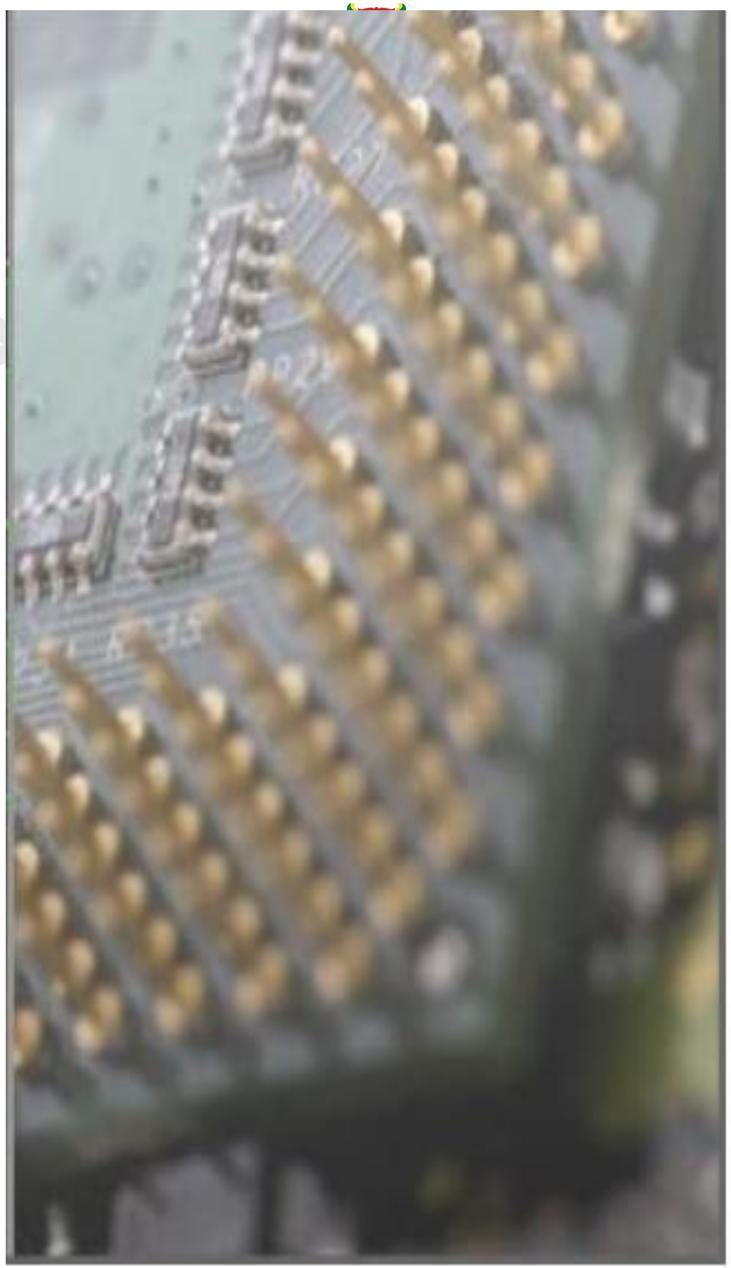
MC. Martin González Pérez

Agenda

- Z and X states
- Multiplexers
- Decoders
- Timing



X and Z states



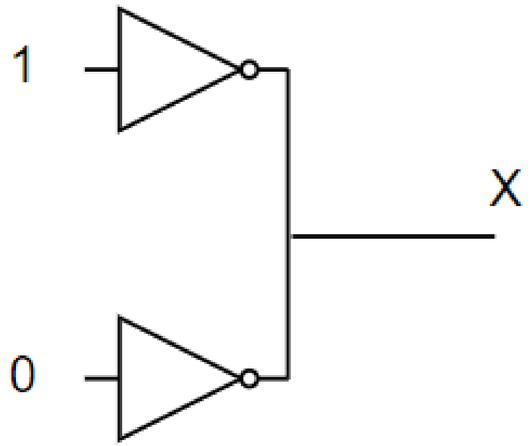
X and Z states

Boolean algebra is limited to 0's and 1's. However, real circuits can have illegal and floating values, this states are represented symbolically by X's and Z's.

Illegal values (X)

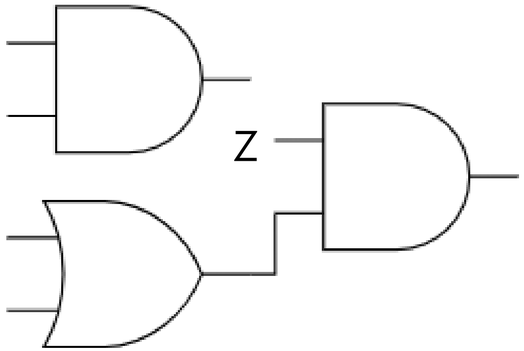
The symbol X indicates that the circuit node has an unknown or illegal value. This can happen if it is being driven to both 0 and 1 at the same time.

Don’t care symbol is also X, so be careful of don’t mix terms.



High impedance

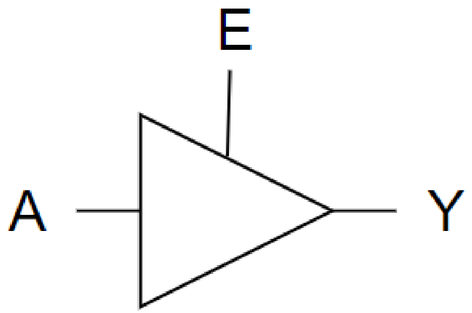
Symbol Z indicate that a node is being driven neither 1 or 0. The node is said to be floating or high impedance. A way to interpret this state is an unconnected input.

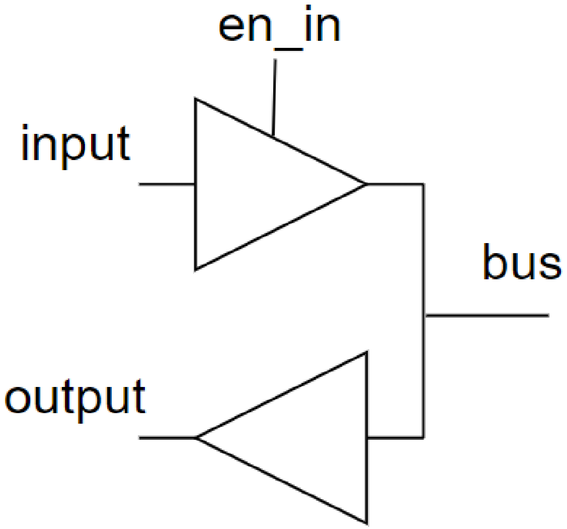


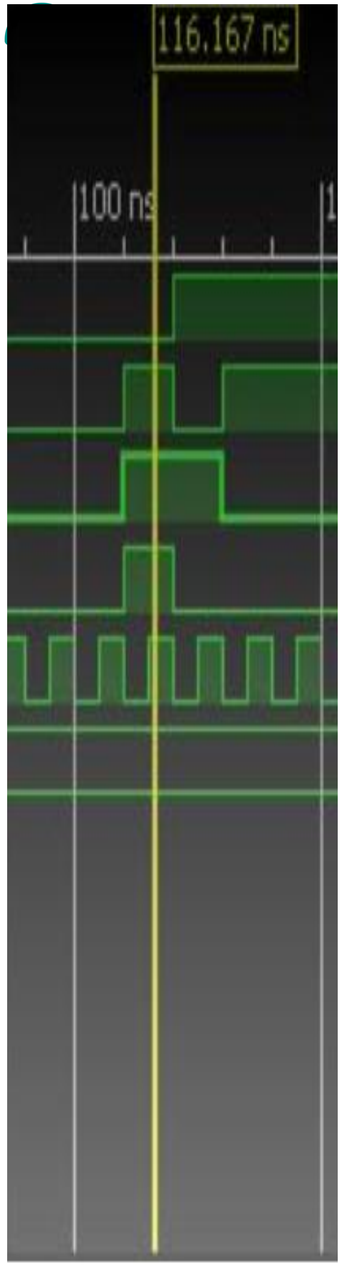
Tristate buffer

A tristate buffer has 3 possible states, 0, 1 and Z.

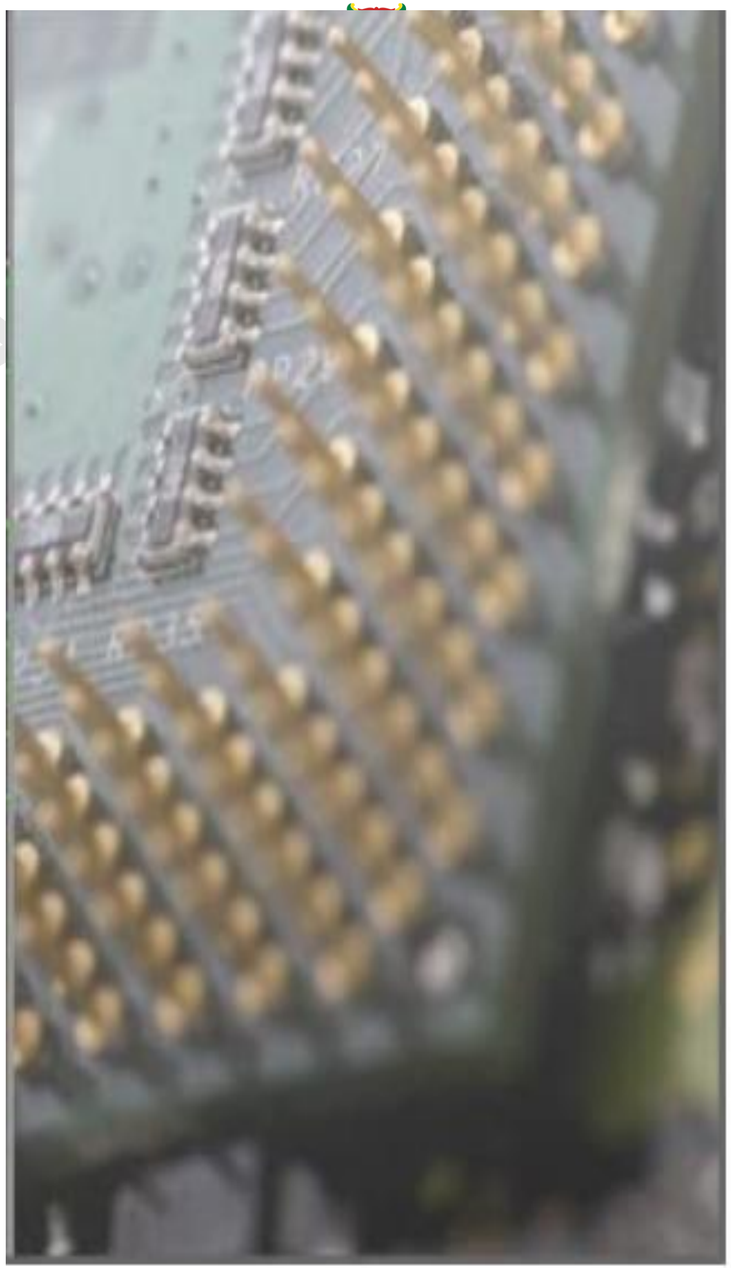
E	A1	Y
0	0	**Z**
0	1	**Z**
1	0	**0**
1	1	**1**







Multiplexers



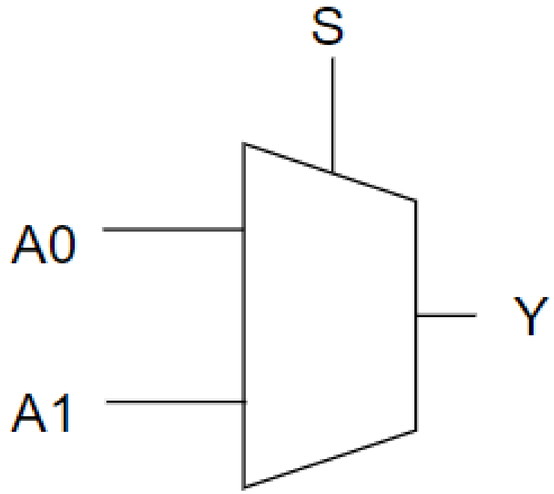
Multiplexers (Mux)

Multiplexers are one of the most commonly used combinational circuits. They choose an output from among several possible inputs, based on the value of a select signal.

S	A1	A0	Y
0	0	0	**0**
0	0	1	**1**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**0**
1	1	0	**1**
1	1	1	**1**

S	Y
0	A0
1	A1

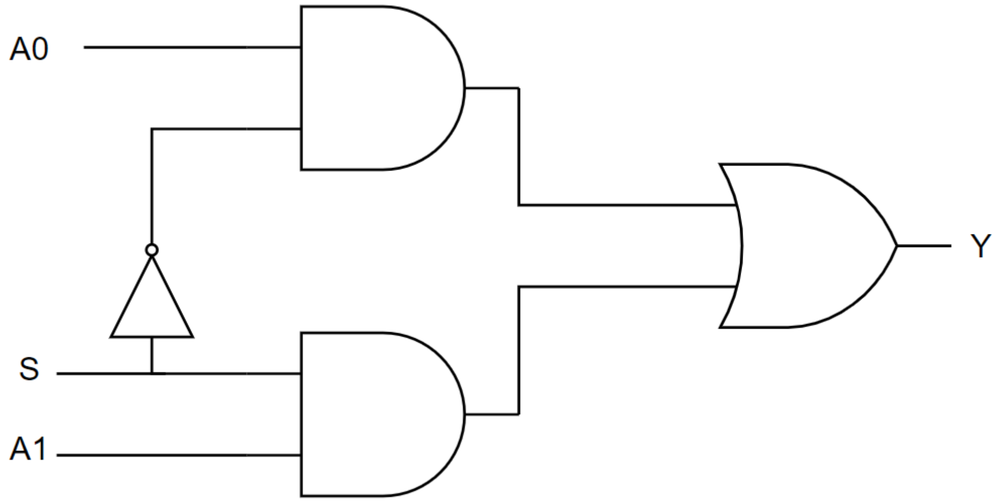
$$Y = A_0\bar{S} + A_1S$$



Mux implementation

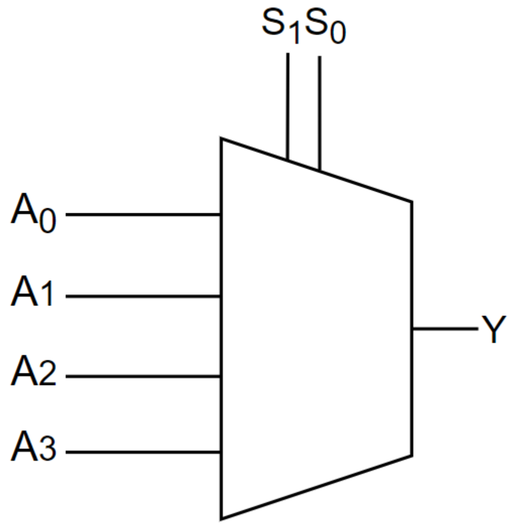
Logic gates

$$Y = A_0\bar{S} + A_1S$$



Exercise

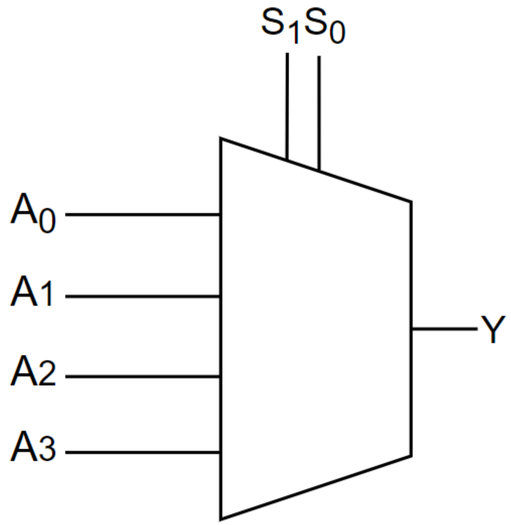
- Get the Boolean equation of a 4 inputs MUX.



Exercise

- Get the Boolean equation of a 4 inputs MUX.

S1	S0	Y
0	0	**A0**
0	1	**A1**
1	0	**A2**
1	1	**A3**



$$Y = A_0\overline{S_0}\ \overline{S_1} + A_1 S_0\ \overline{S_1} + A_2\ \overline{S_0} S_1 + A_3 S_0 S_1$$

Look up tables

A **Look-Up Table (LUT)** is a data structure (usually an array or table) that stores a set of precomputed values or results for a specific set of inputs. Instead of recalculating a function or result each time, the system quickly retrieves the precomputed value from the table.

n	2^n
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Look up tables

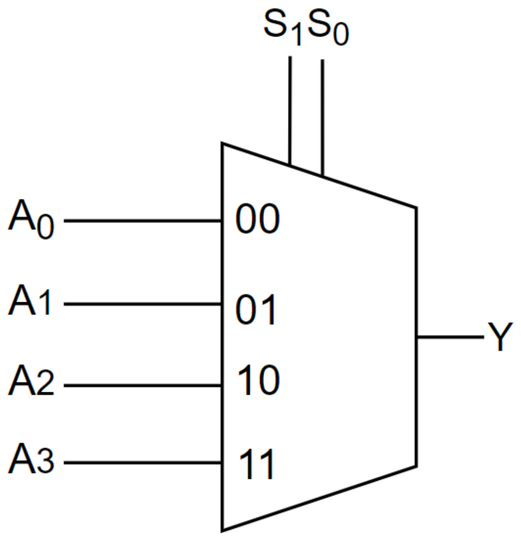
A **Look-Up Table (LUT)** is a data structure (usually an array or table) that stores a set of precomputed values or results for a specific set of inputs. Instead of recalculating a function or result each time, the system quickly retrieves the precomputed value from the table.

n	2^n
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

LUTs are one of the basic building blocks of FPGAs.

Mux as LUT

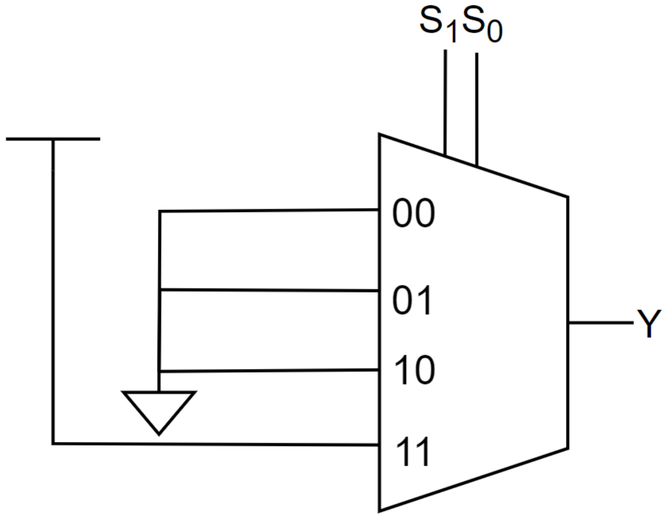
How can we implement a 2-input AND logic with a 4-input MUX?



Mux as LUT

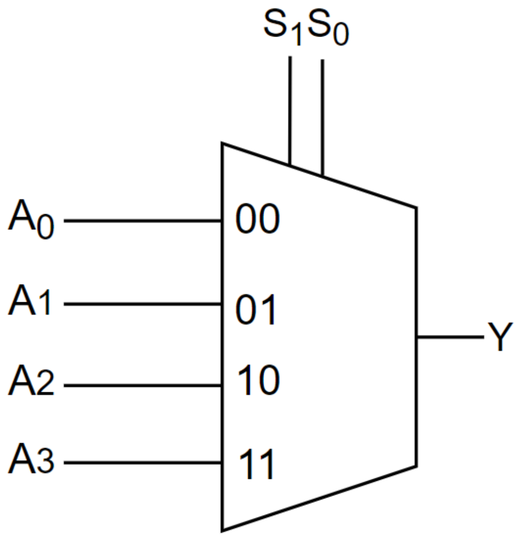
How can we implement a 2-input AND logic with a 4-input MUX?

Answer!!



Mux as LUT

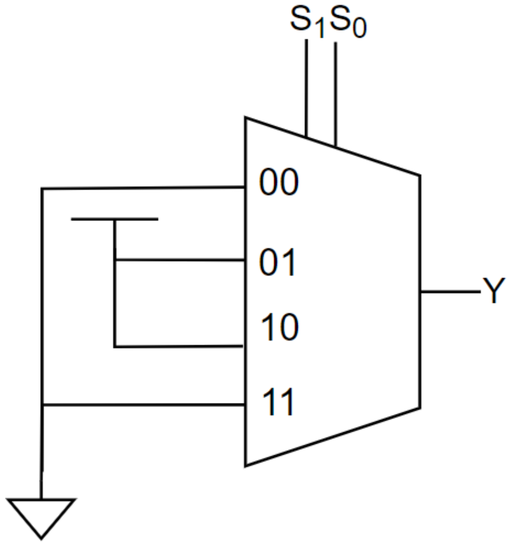
What about a 2-input XOR?



Mux as LUT

What about a 2-input XOR?

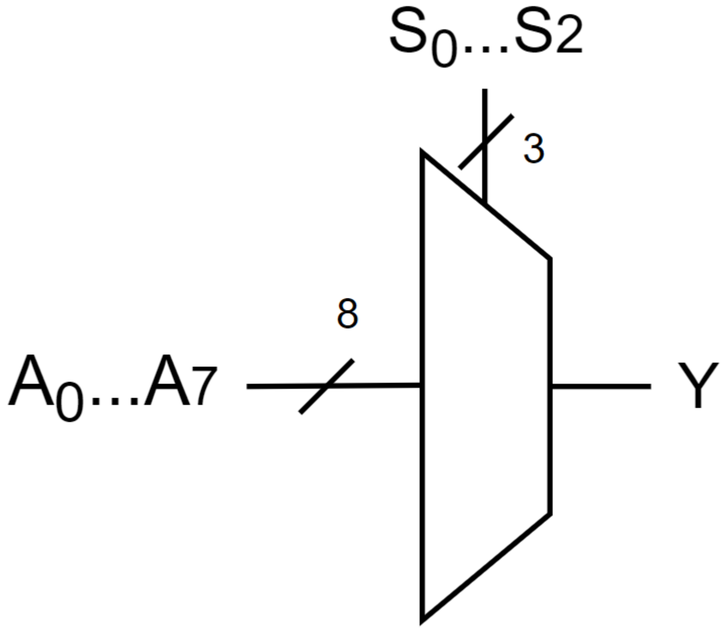
Answer!!



Mux as LUT

And this truth table?

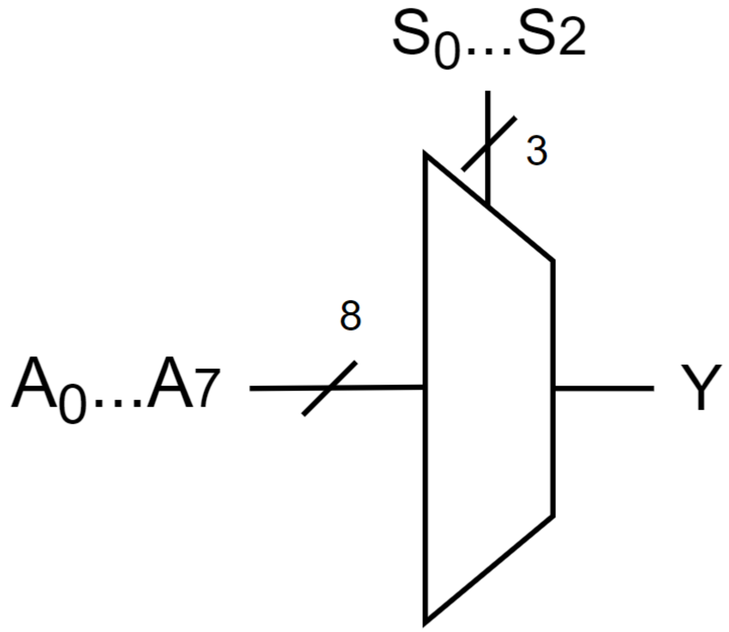
S2	S1	S0	Y
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**0**
1	0	0	**1**
1	0	1	**1**
1	1	0	**0**
1	1	1	**0**



Mux as LUT

And this truth table?

S2	S1	S0	Y
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**0**
1	0	0	**1**
1	0	1	**1**
1	1	0	**0**
1	1	1	**0**

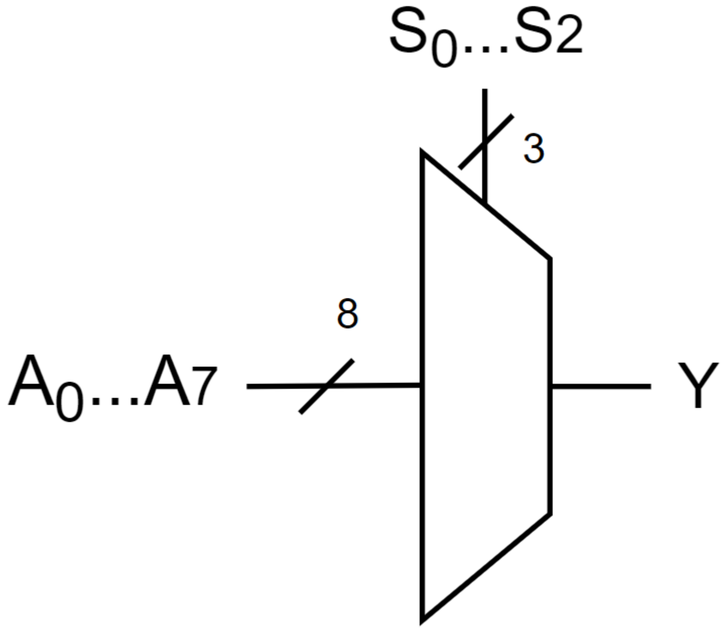


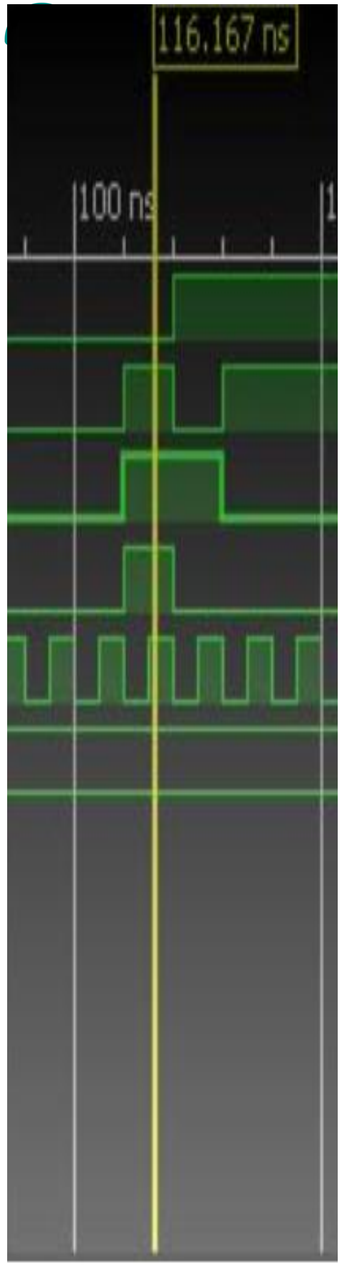
Answer!!

A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**1**	**1**	**0**	**1**	**0**	**0**

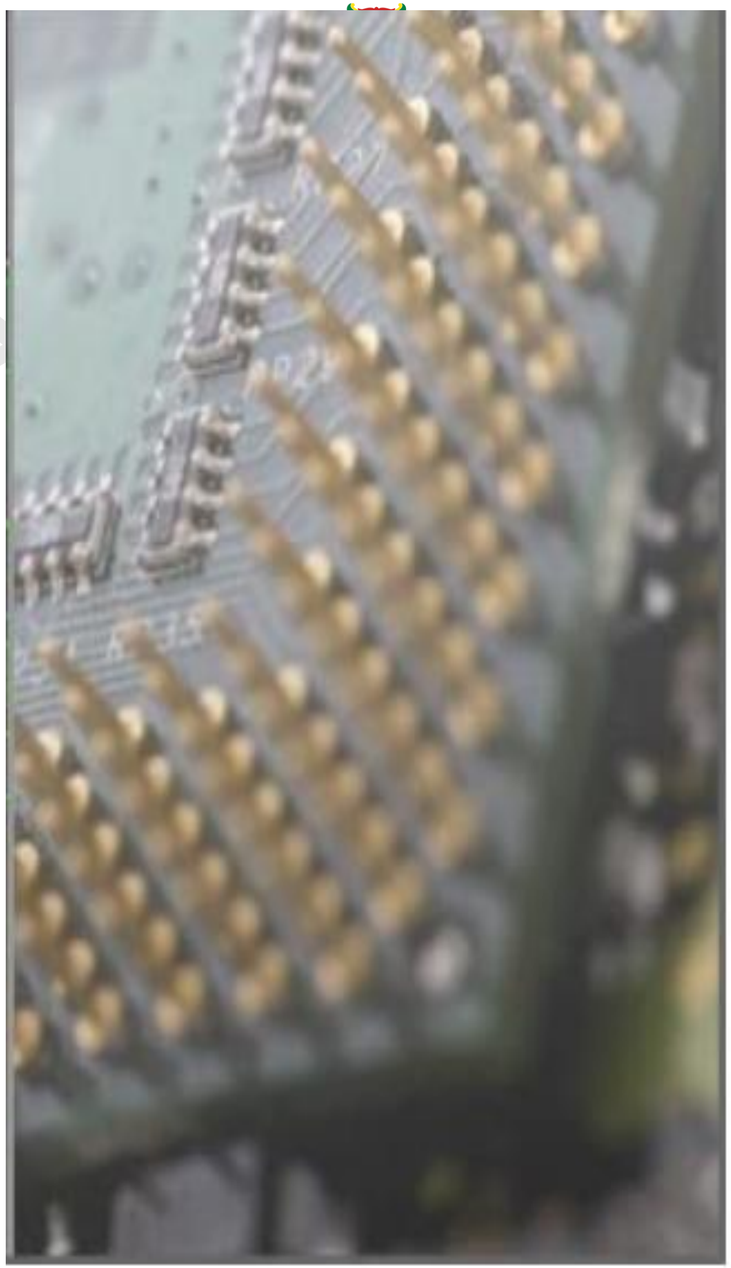
ALUT

Making "**A**" bus configurable we can create a Adaptative Look Up Table, this is basic principle for FPGA configurability.



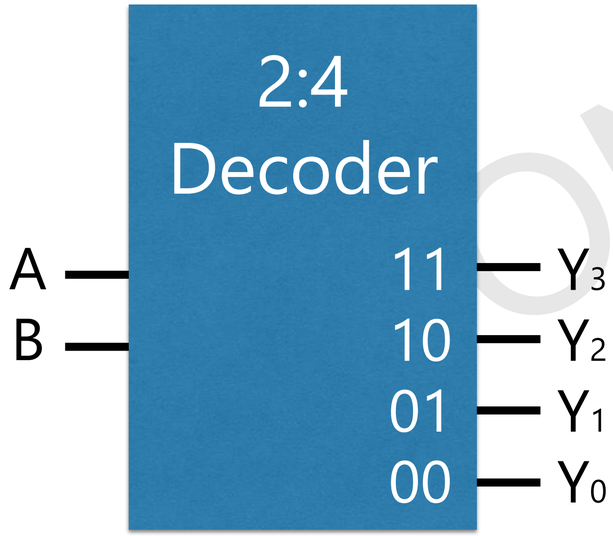


Decoders

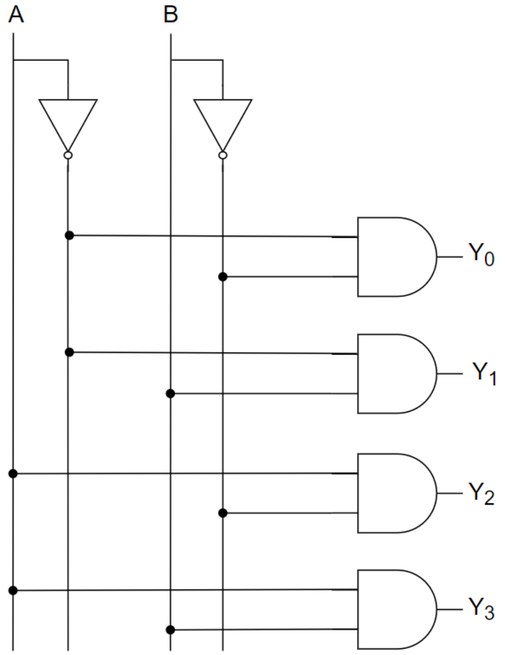


Decoder

A decoder is a combinational circuit that has N inputs and M outputs (where M ≤ 2^N). It assert exactly one of its outputs depending on the input combination. The output are called ***one hot.***

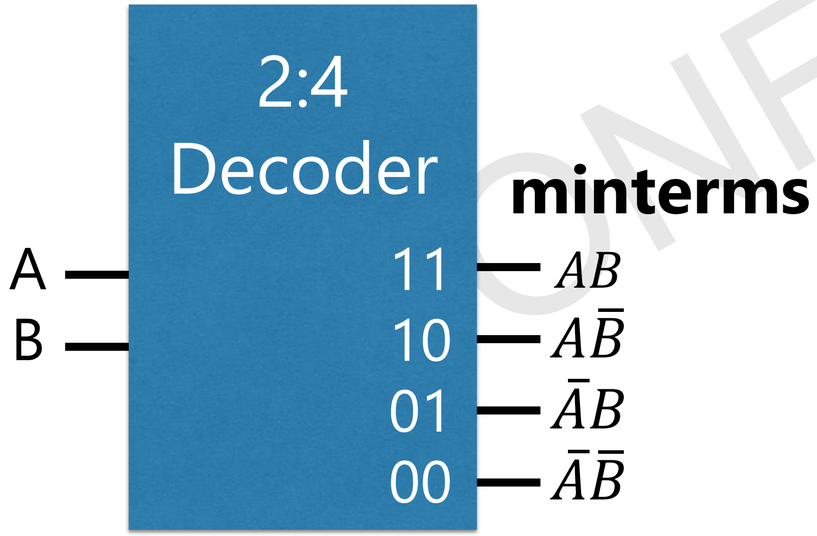


A	B	Y3	Y2	Y1	Y0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



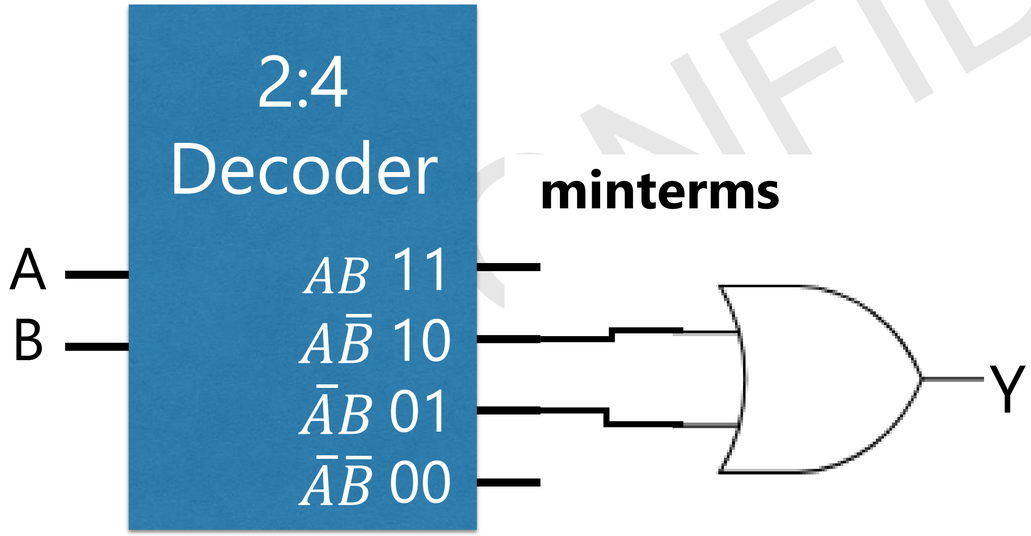
Decoder

Decoder outputs can be seen as minterms, so we can add **OR** logic to build logic functions.

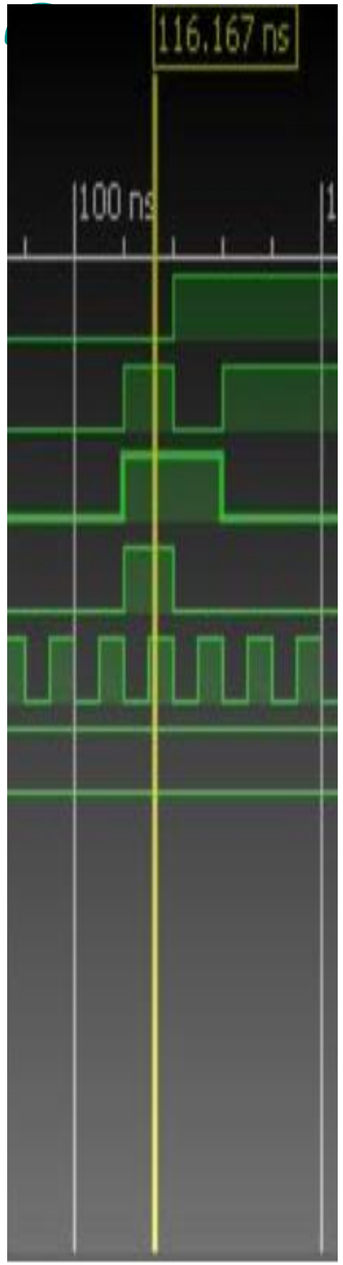


Decoder

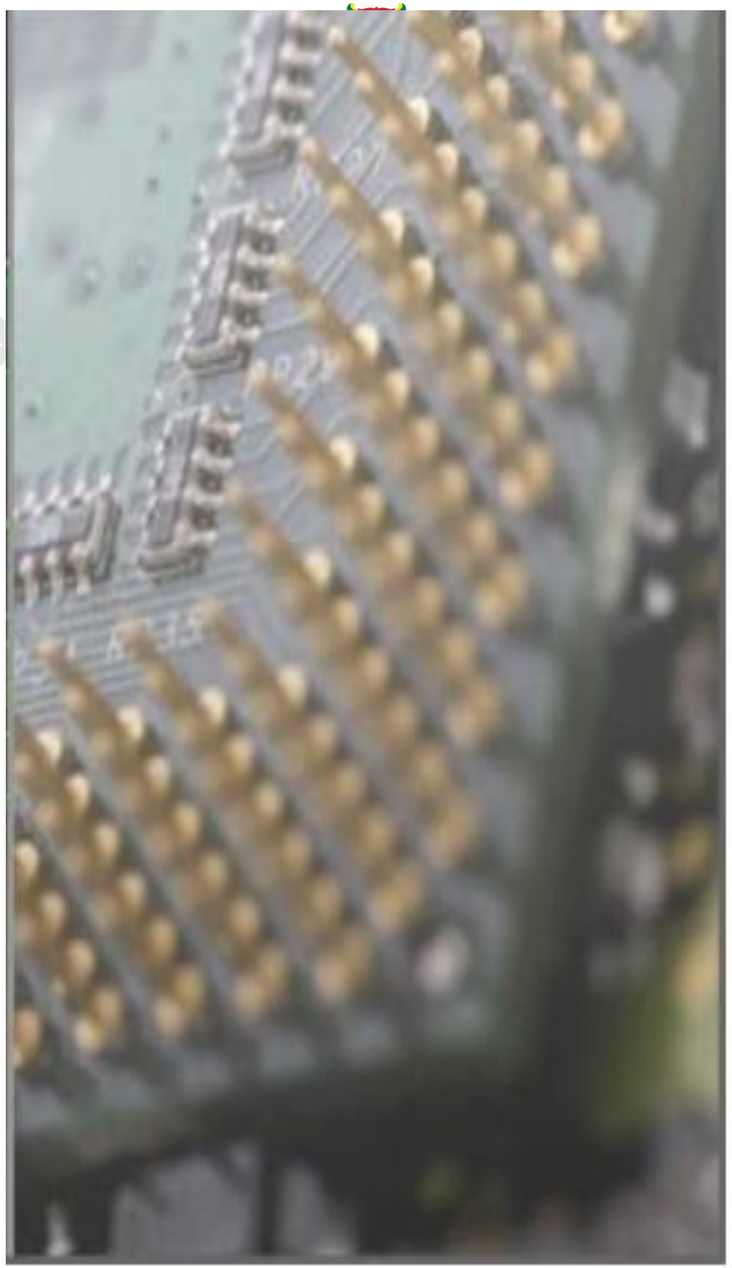
- Build a XOR gate using 2:4 decoder



$$Y = A \oplus B = \bar{A}B + A\bar{B}$$



Timing (Overview)

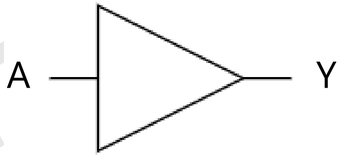


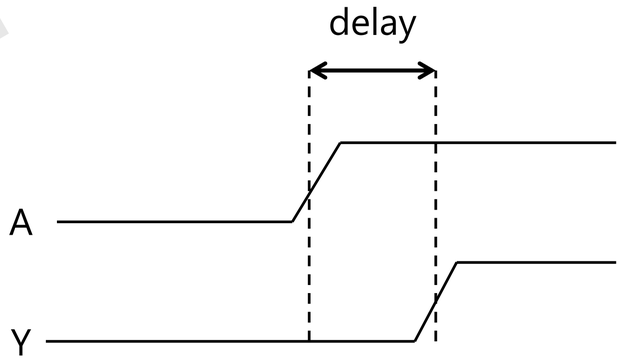
Delay

Delay is the time between input change and output changing.

Delay is caused by:

- Capacitance and resistance in a circuit
- Rising and falling delays
- Physics limitation

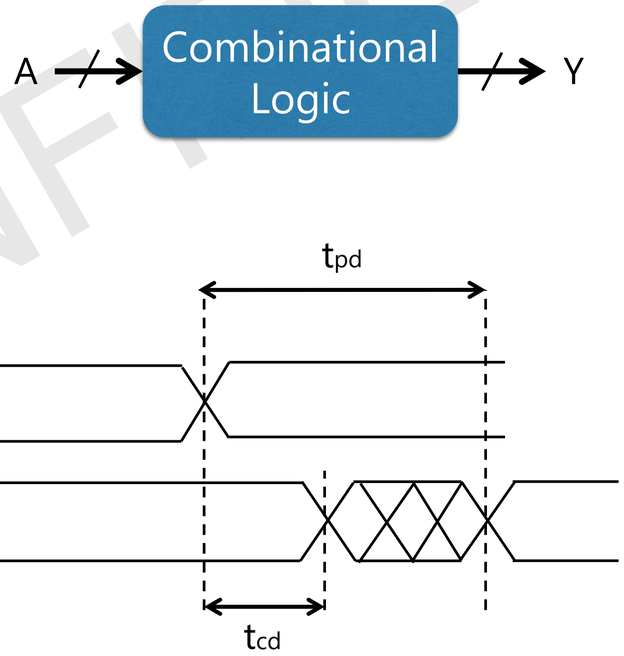




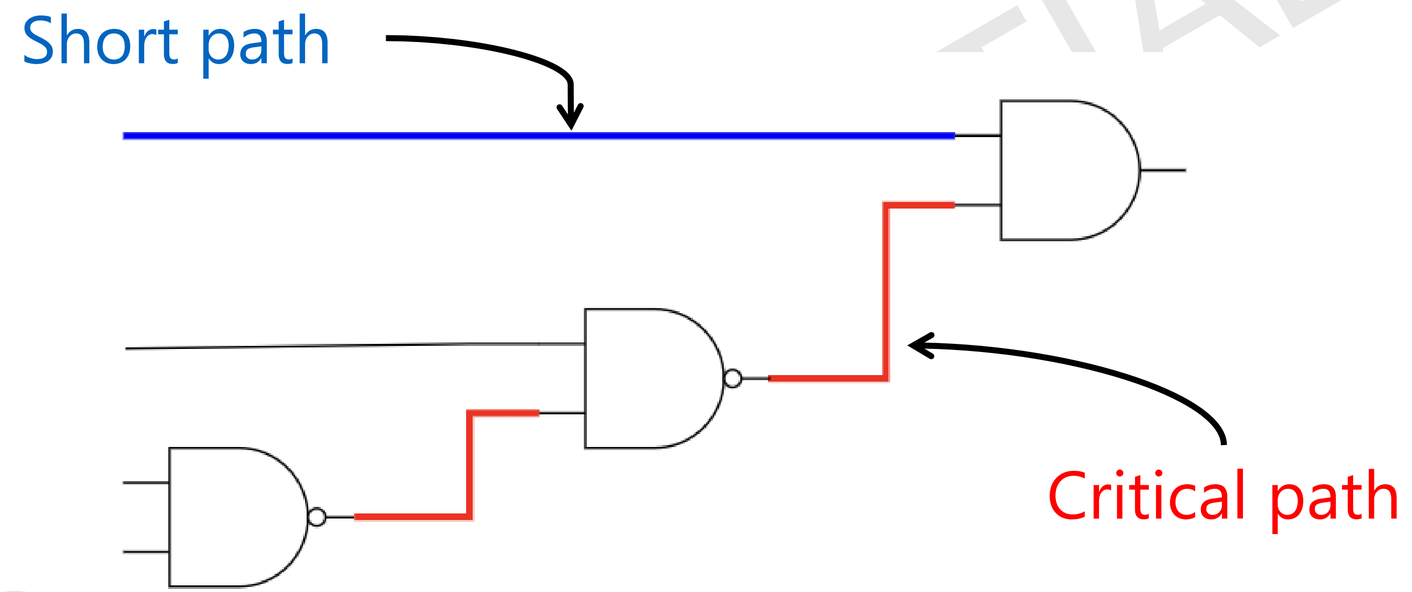
Propagation and contamination delay

Propagation delay (t_{pd}): is the max delay from input(s) to output(s).

Contamination delay(t_{cd}): is the min delay from input(s) to output(s).



Delay



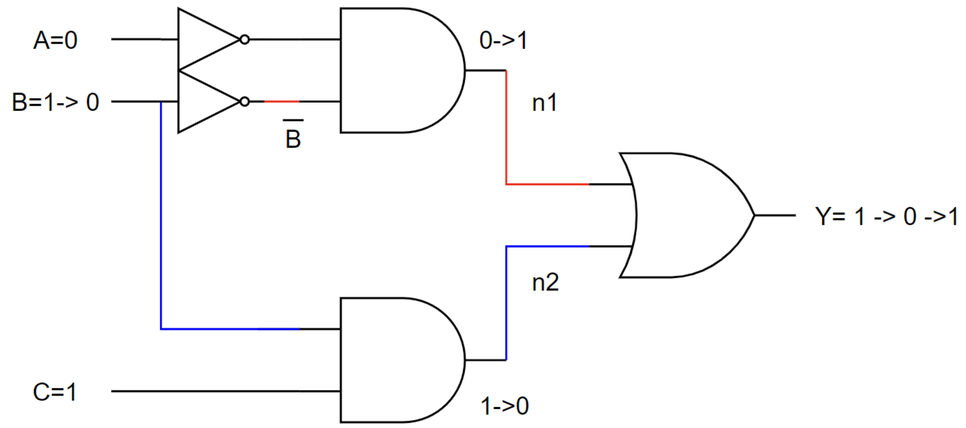
Critical Path: $t_{pd} = 2t_{pd\_NAND} + t_{pd\_AND}$ (max delay)

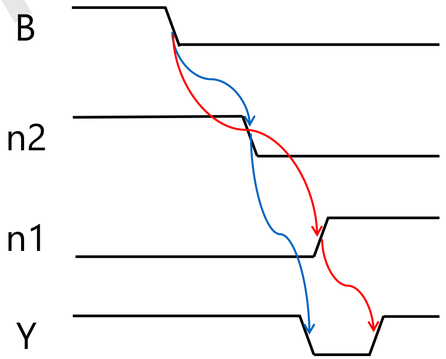
Short Path: $t_{cd} = t_{cd\_AND}$ (min delay)

For a logic gate rise and fall can be different. We consider as t_{pd} the highest delay.

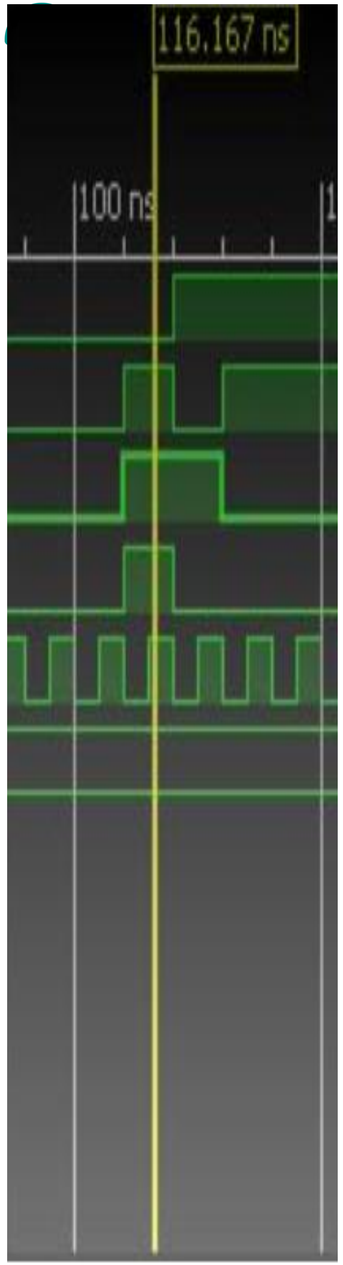
Glitch

When a single input change causes an output to change multiple times.

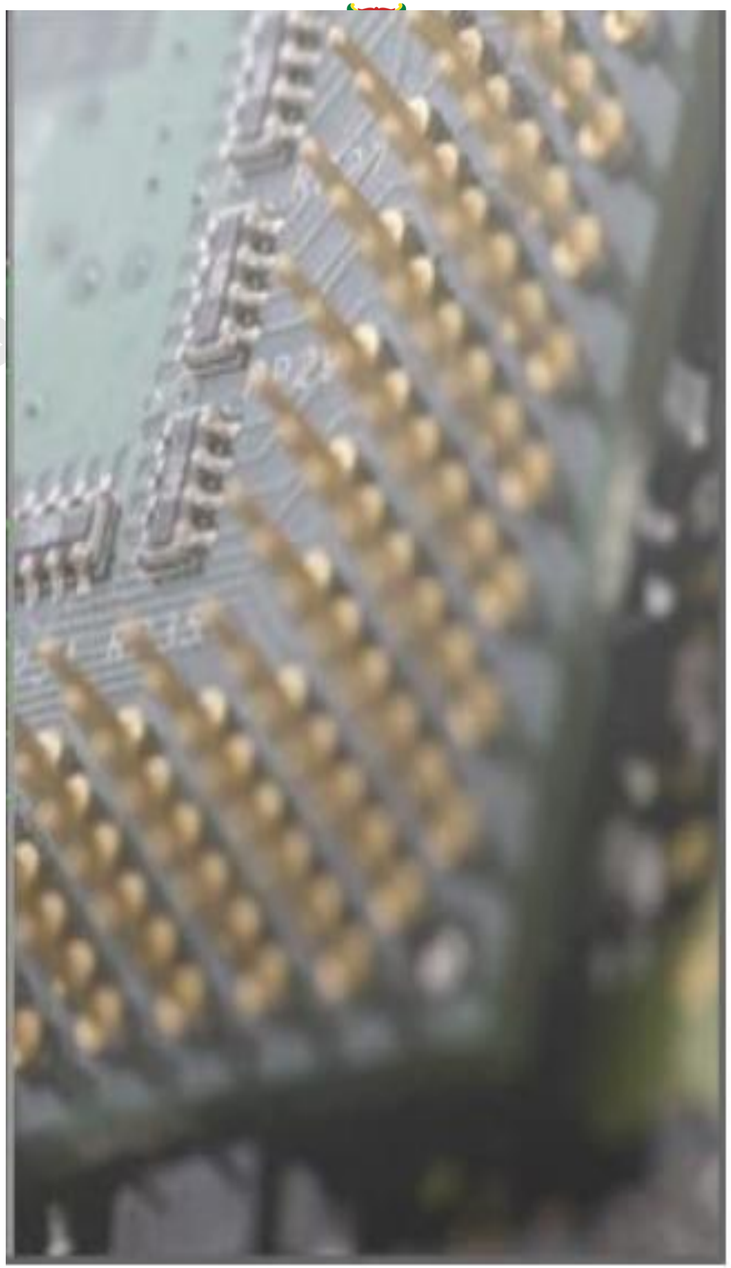




We can't get rid of all glitches but it's important recognize a glitch in simulations or on oscilloscope.



Exercises



Exercises

Create the next circuits using logic gates.

- Detector de igualdad.
- Parity check de 8 bits.
- Sumador completo de 4 bits.
- Majority circuit (3 inputs).