Subtractor

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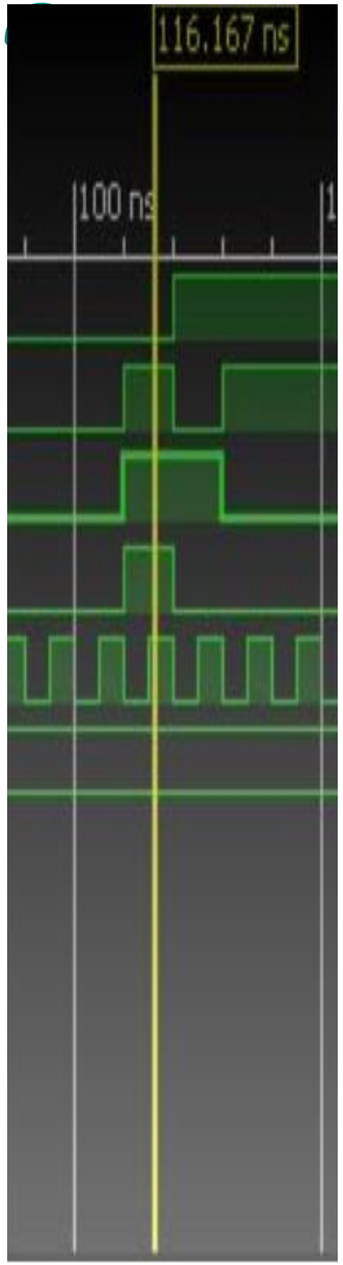
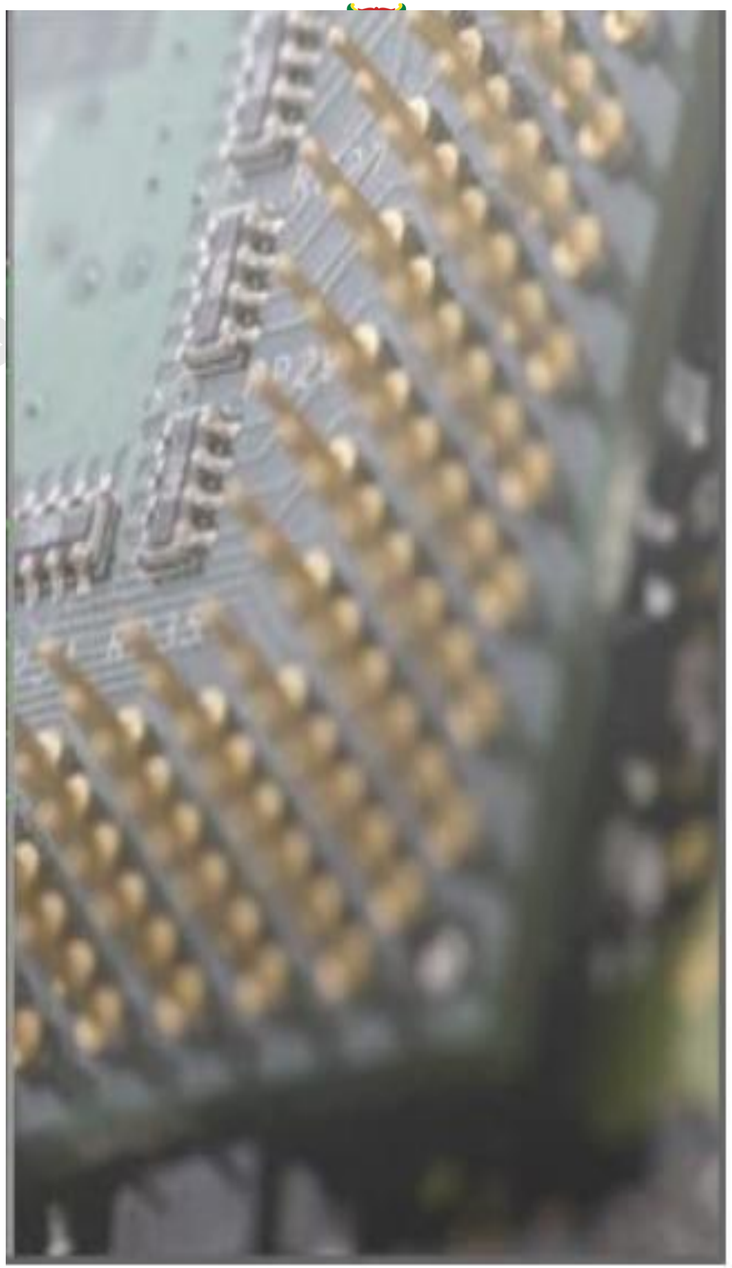
Agenda

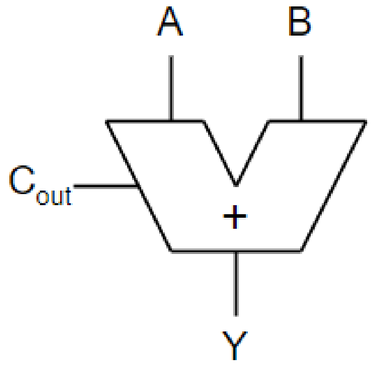
- Addition
- Subtraction



Addition



Half adder

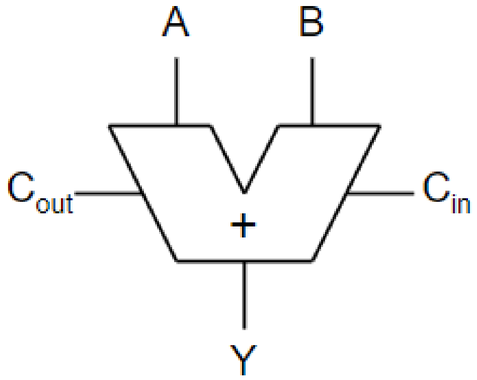


$$Y = A \oplus B$$

$$C_{out} = AB$$

A	B	C_{out}	Y
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Full adder



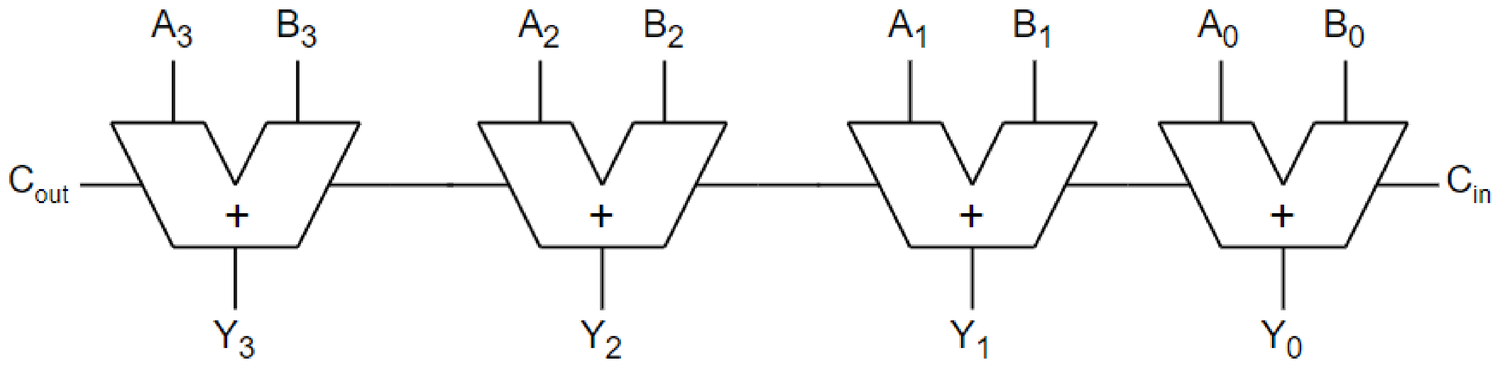
C_{in}	A	B	C_{out}	Y
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

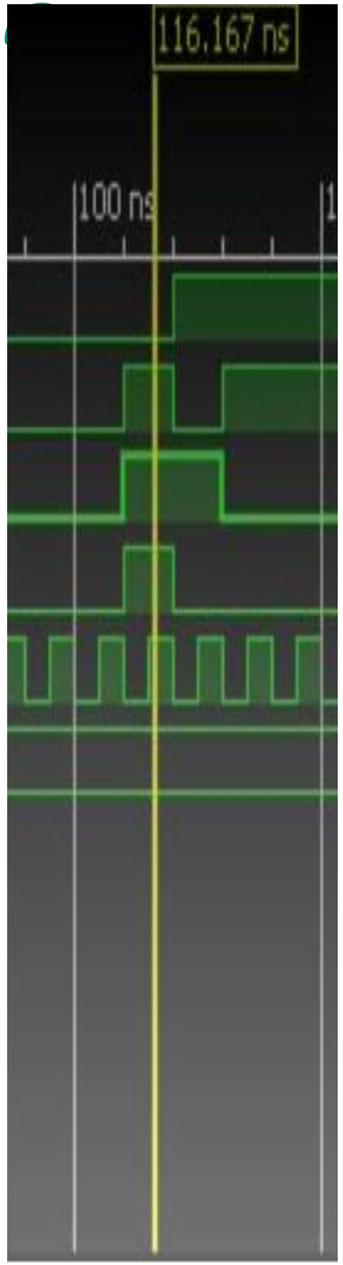
$$Y = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + AC_{in} + BC_{in}$$

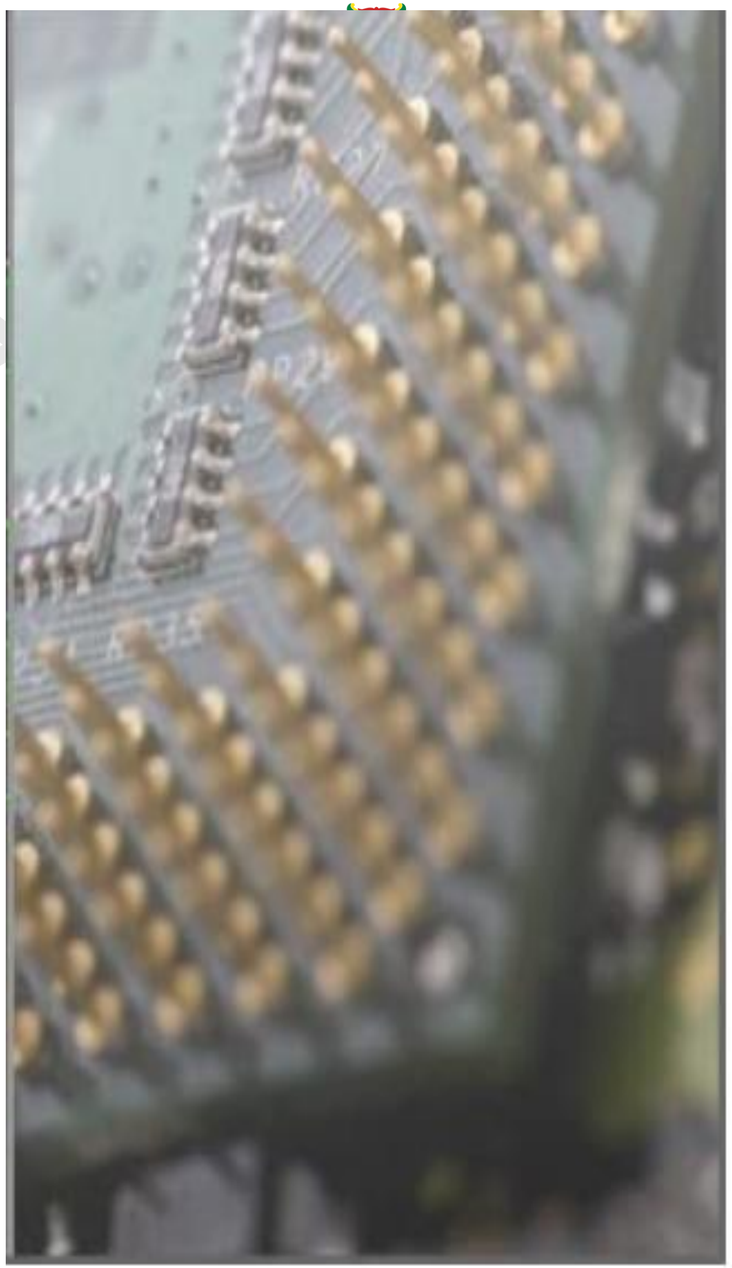
N-bits Full adder

The figure show the simplest way to build a N-bits adder. This is called **Ripple-Carry Adder**. This adder has the disadvantage that is slow when N is large.



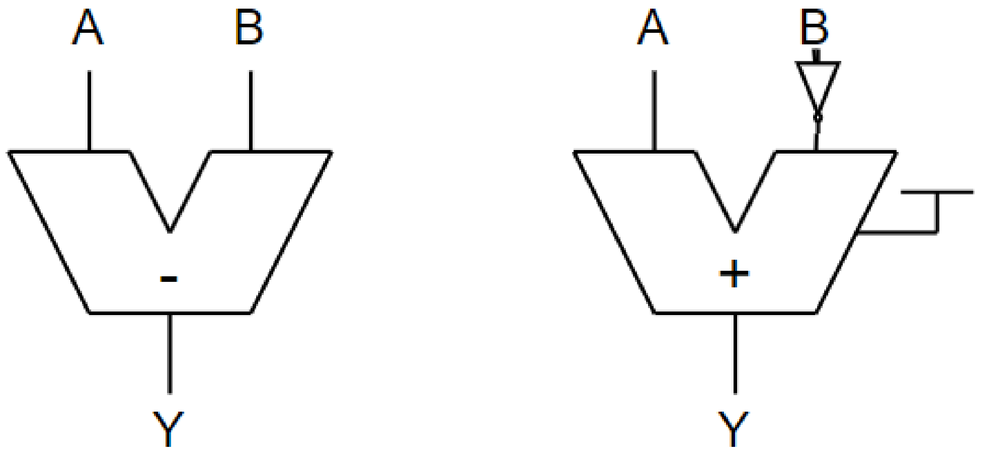


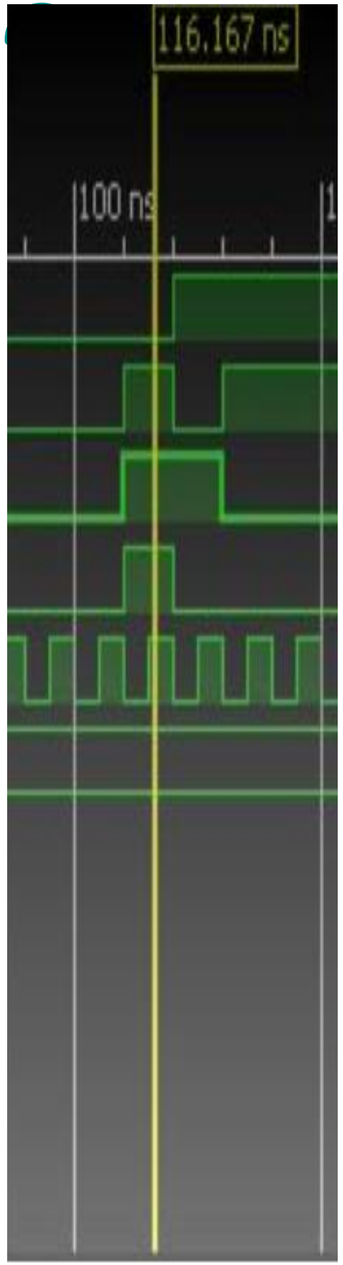
Subtraction



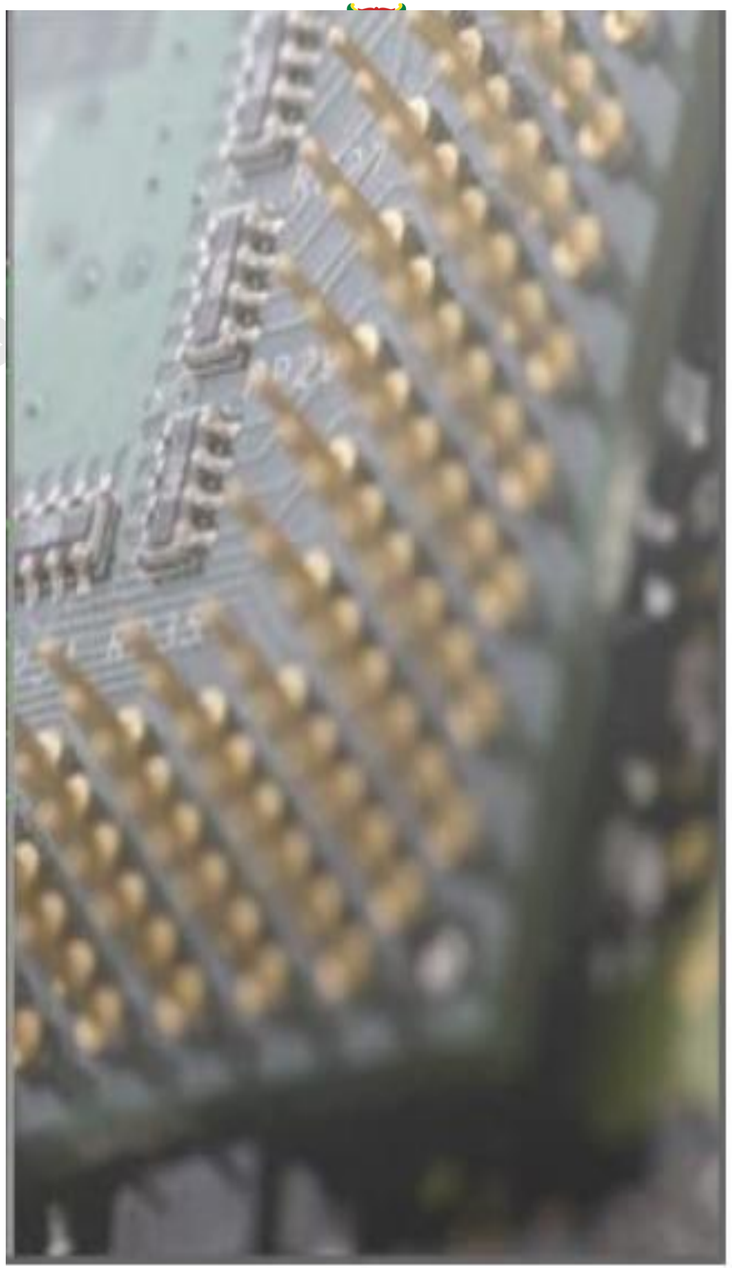
Subtractor

Adders can add positive and negative numbers in two’s complement representation. We can change a sign to a number to preform a subtraction.





Lab



LAB2: Subtractor.

Design a parametrizable subtractor with the next features using Verilog:

- The inputs will be represented in two's complement format.
- The output must be in two's complement format.
- If an overflow occurs, it must be indicated with a single bit.