Introduction to Digital Design with Verilog

MC. Martin González Pérez

Agenda

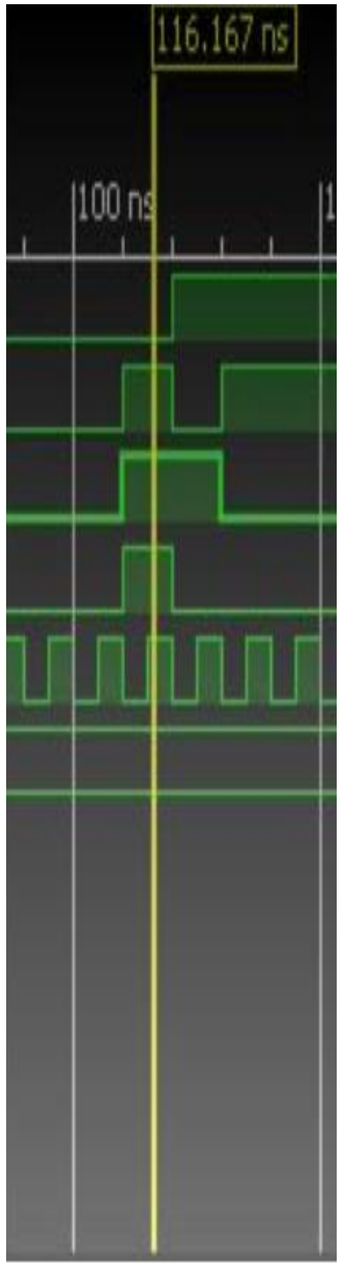
- Introduction
- About this course
  - Topics
  - Goals
  - Labs
- Bibliography

Self introduction

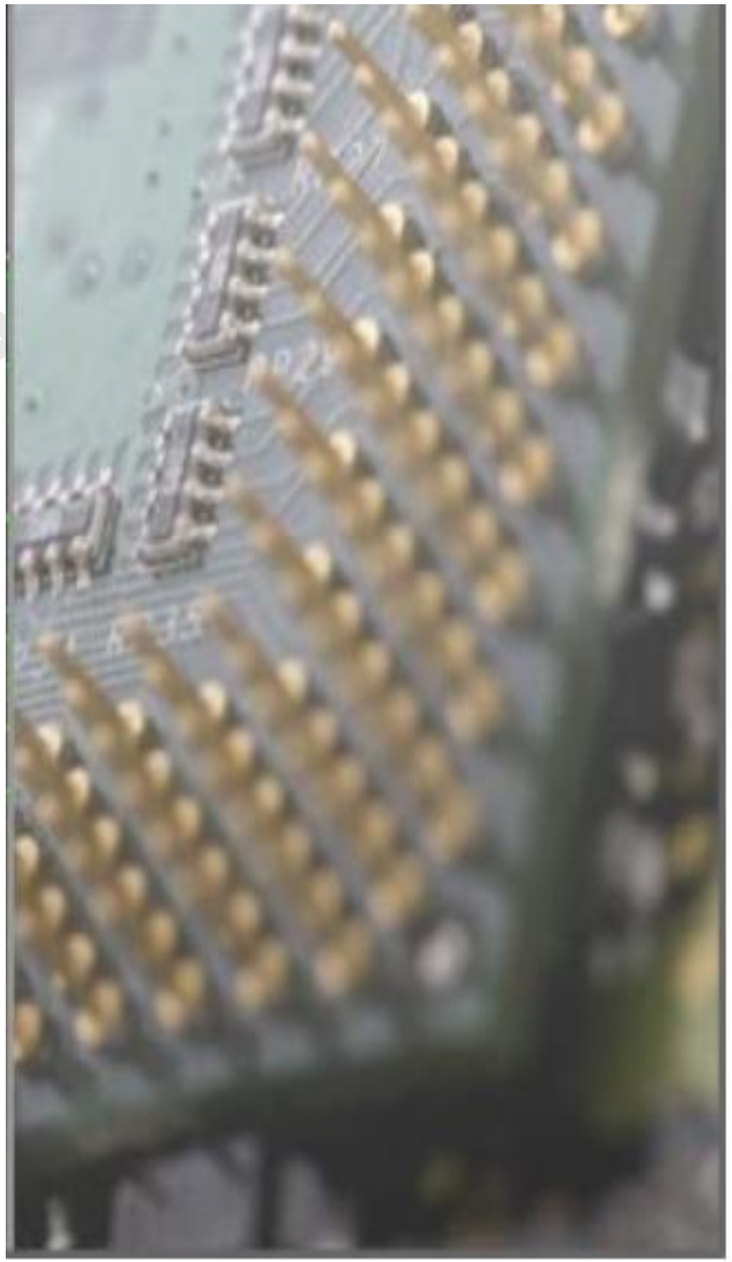
- **Martin González Pérez**
  - MC in Electrical Engineering, CINVESTAV Unidad Guadalajara
  - BS in Mechatronics Engineering, Instituto Tecnológico de Tepic

- **Research interest**
  - Computer architecture
  - Hardware/Software cooperation
  - Architectures for AI computing
  - VLSI digital design verification

What about you?



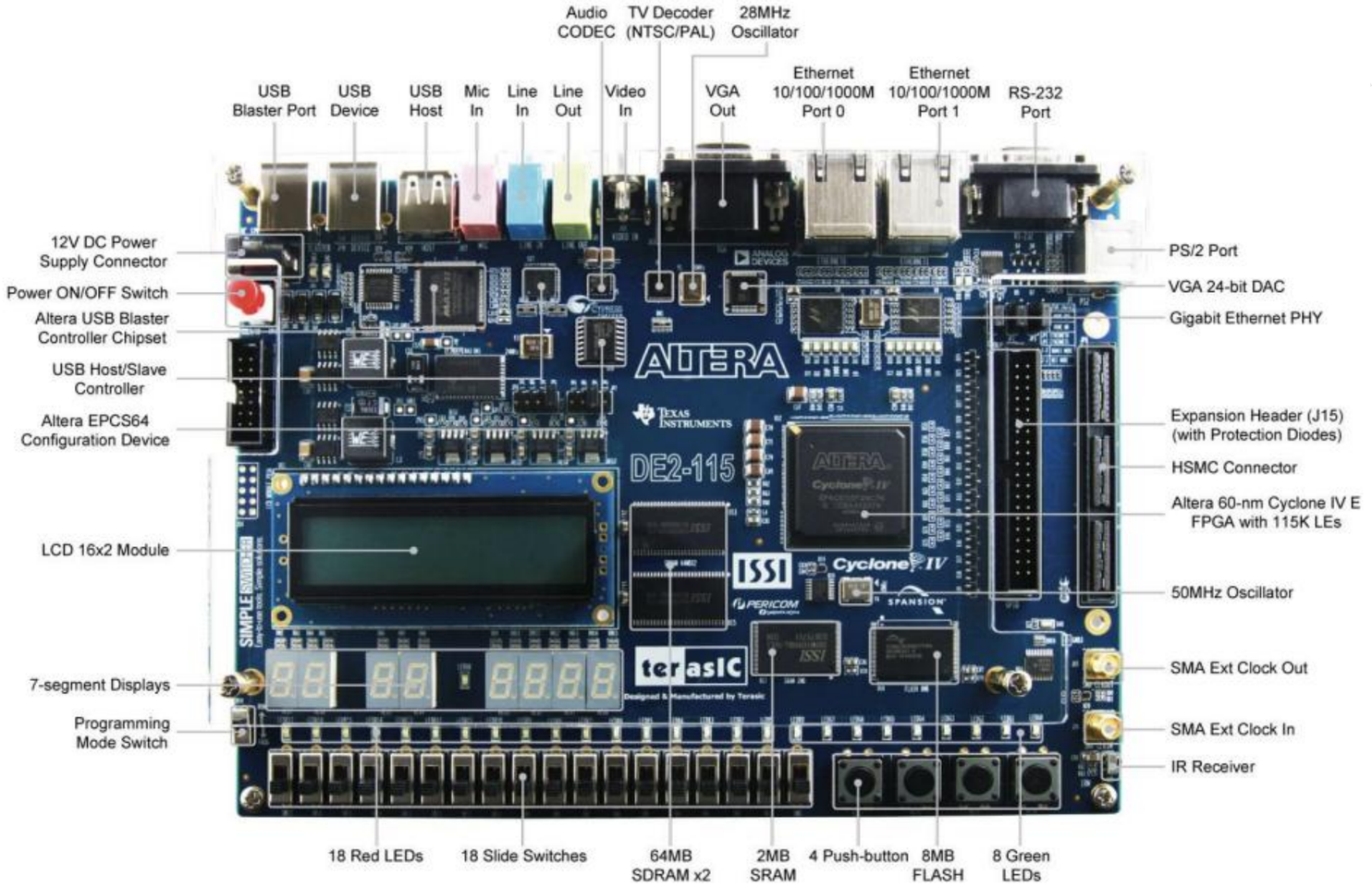
About this course



Goals

- Introduce students to the fundamentals of digital circuit design.
- Introduce students to HDL with Verilog
- Develop skills for designing combinational and sequential circuits using Verilog through practical exercises.

Labs: our FPGA Board



DE2-115

https://www.terasic.com.tw/attachment/archive/502/DE2_115_User_manual.pdf

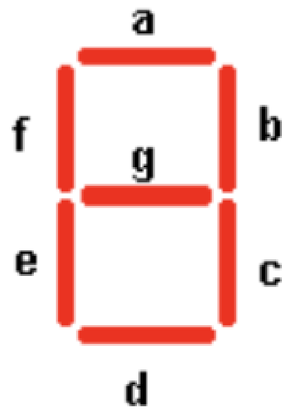
Let’s create working groups

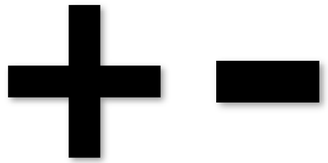
You will work in groups of three:

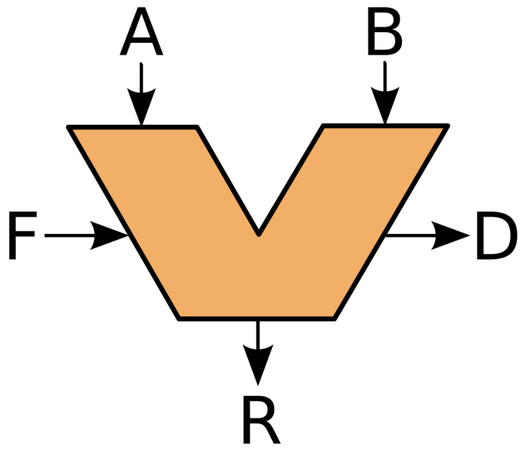
- Option 1: Choose your partners
- Option 2: Get randomly assigned to a partner.

Labs

- **Lab 1: 7-seg Display**
- **Lab 2: Adder-subtractor**
- **Lab 3: ALU**

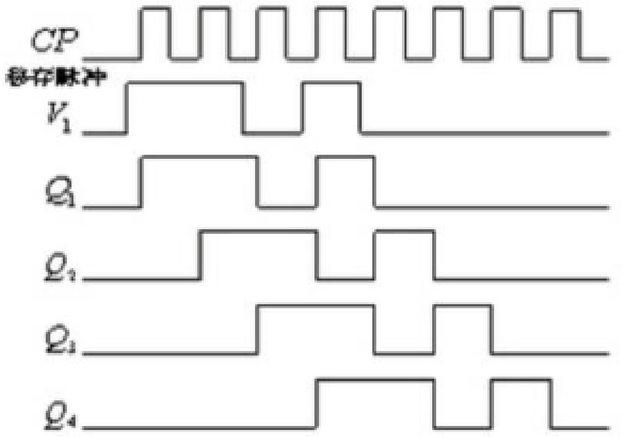






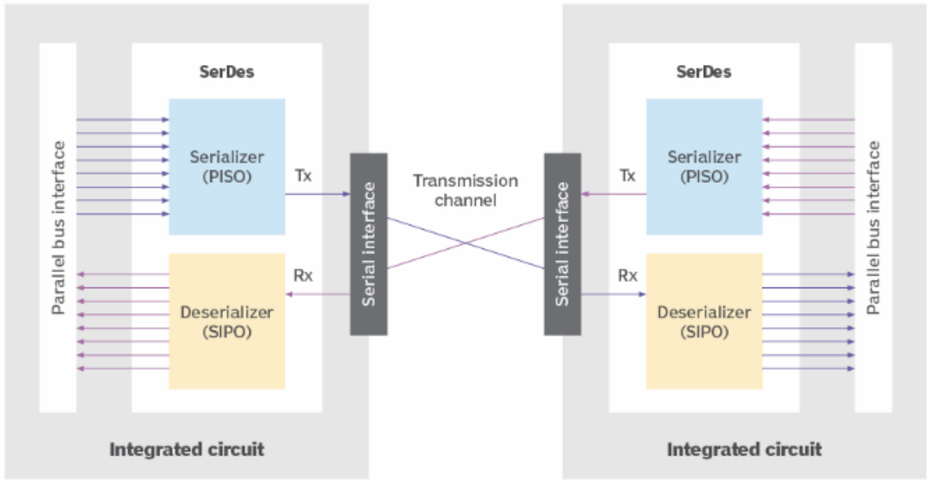
Labs

- **Lab 4: Shift register**



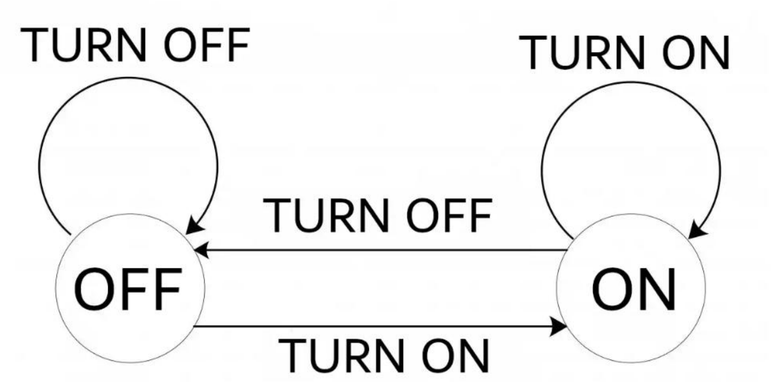
- **Lab 5: Counters**

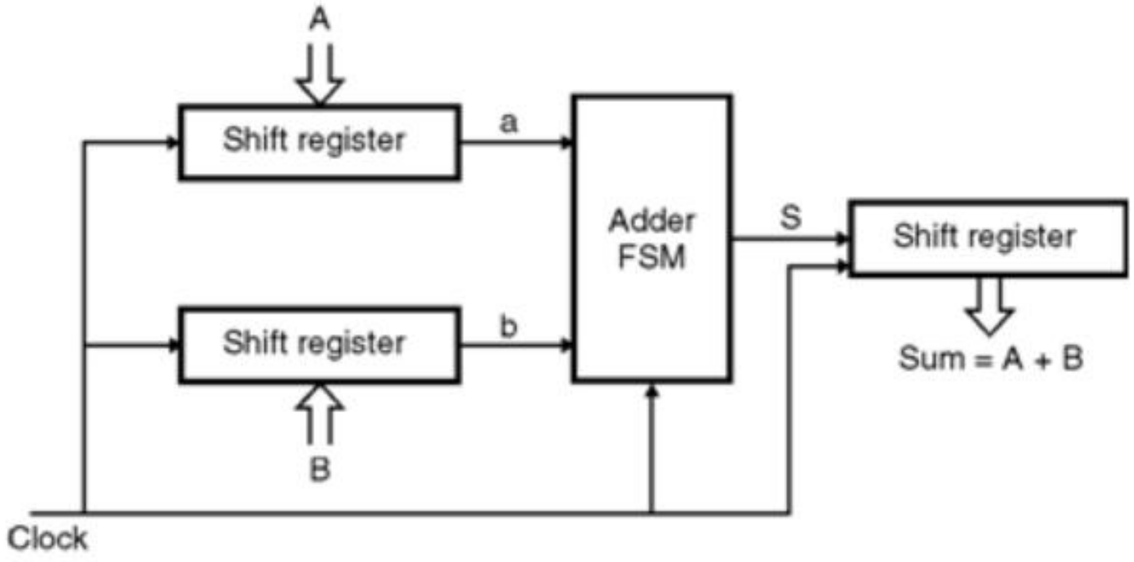
- **Lab 6: PISO-SIPO**



Labs

- **Lab 7: Finite state machines**
- **Lab 8: Serial Adder**



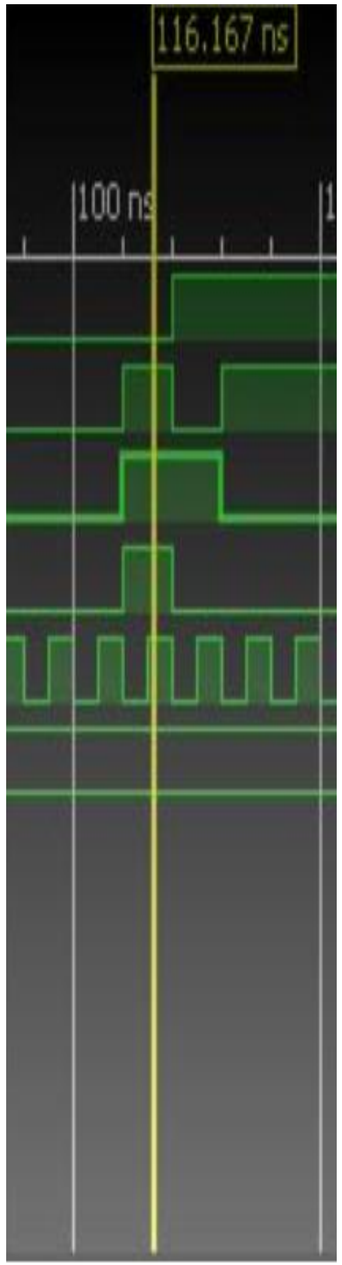


Rubric

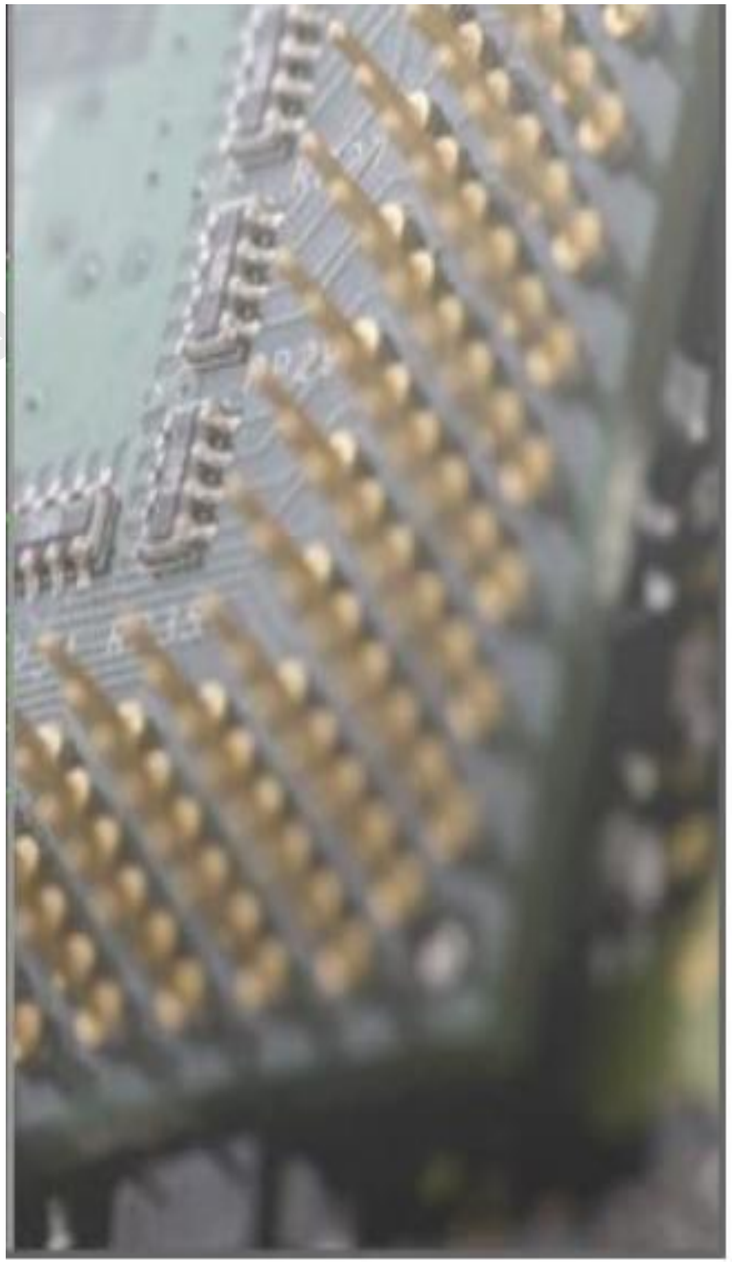
Rubric				
Criteria	Excelent	Good	Fair	Poor
Report	The report provides a clear and concise description of lab development.	The report correctly describes the lab development	The report lacks clear and logical organization of ideas.	The report's information does not correspond to the actual lab work
Schematic	A well-organized schematic, where different functions are clearly separated, easy to follow, and uses submodule instances to reduce schematic complexity	A well-organized schematic, where different functions are clearly separated, and the circuit is easy to follow.	Understandable schematic	disorganized schematic (hard to follow)
Functionality	The circuit operates correctly and includes all intended functionalities.	The circuit demonstrates partial functionality, with most features operating as intended.	Only principal circuit's features work correctly.	The circuit does not work.
Total	90-100	75-89	60-74	0-59

Evaluation criteria

Laboratories	80%
Participation	20%



Bibliography



Bibliography

- Sarah L. Harris, David Harris (2022). *Digital Design and Computer Architecture RISC-V Edition*, Morgan Kaufmann – ISBN: 978-0-12-820064-3.
- Stuart Sutherland (2017). RTL modeling with SystemVerilog for simulation and synthesis using SystemVerilog for simulation for ASIC and FPGA design. ISBN-13:978-1-5467-7634-5.
- Charles H., Lizy Kurian (2008). *Digital System Design Using VHDL*, Thompson. - ISBN: 13: 978-0-534-38462-3
- Floyd, T. L. (2006). *Fundamentos de Sistemas Digitales*, 9ª. Edición. Pearson educación S.A. ISBN 13: 978-84-832-2720-6
- Intel. (2019, diciembre). Intel® Quartus® Prime Standard Edition User Guide (v19.4).

Contact

For questions contact me:

E-Mail : martin.perez@cinvestav.mx

Questions?