ECSE 325

LAB 5 REPORT

Martin Kruchinski Almeida
(260915767)
Menad Kessaci
(260807381)

Group 35

G35_timestamper System:

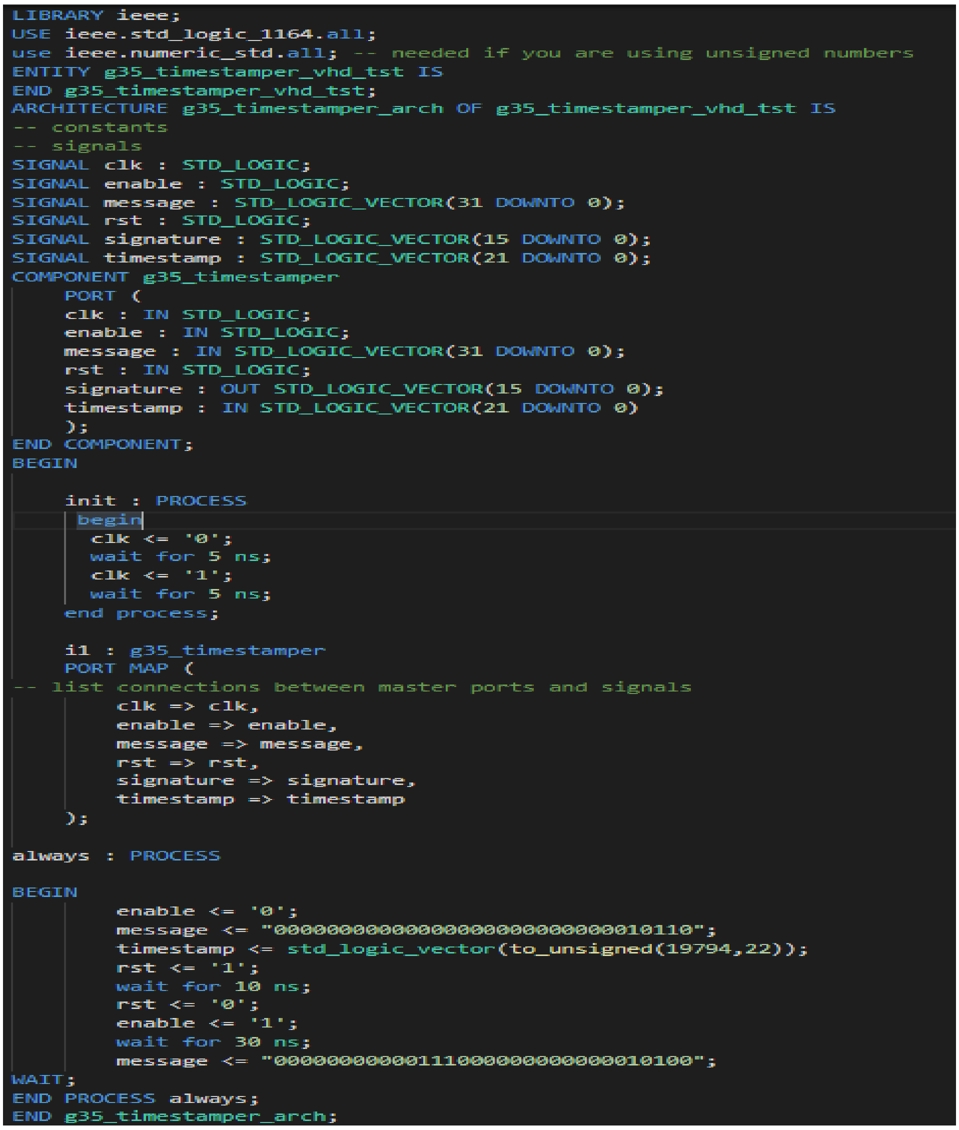
Introduction – Description of the circuit:

In this lab, we worked on the creation of a circuit that acts as a time-stamper. The circuit takes a message from a source, generates a time-stamp for it, and affixes a digital signature to the message. Then, the circuit outputs a digital signature.

Formally speaking, the time-stamper circuit has 4 inputs: a clock signal, a reset signal, an enable signal, a message, and a timestamp. The clock, the reset and the enable signals are all 1-bit signals. The message is a 32-bit vector while the timestamp is a 22-bit vector representing the number of hours since year 2000. The circuit has 1 output: a signature that is 16-bits wide.

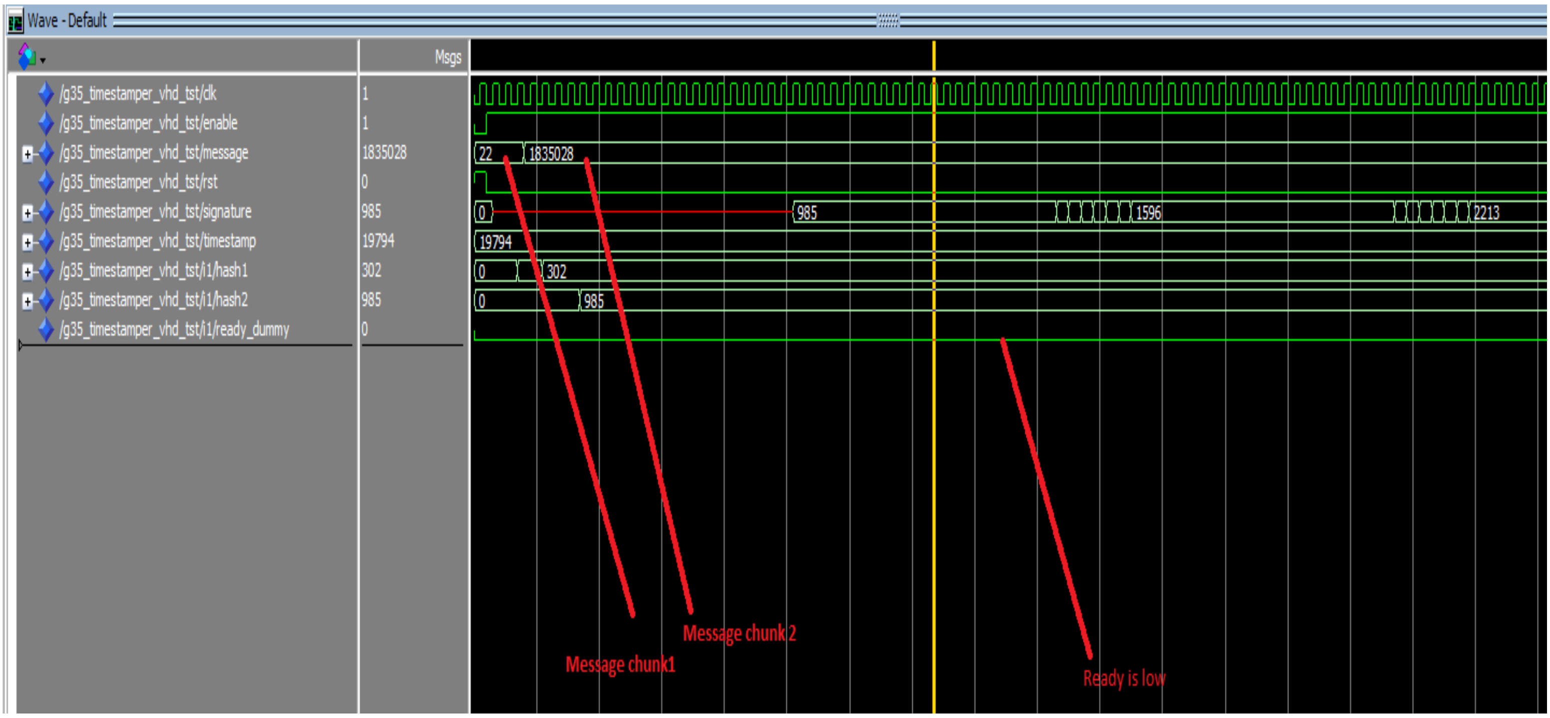
It is worth noting that the timestamp used as an input for the time-stamper is generated by another circuit: g35_Hash10. In summary, the latter takes a message and produces a hash for the input message.

VHDL Testbench code:

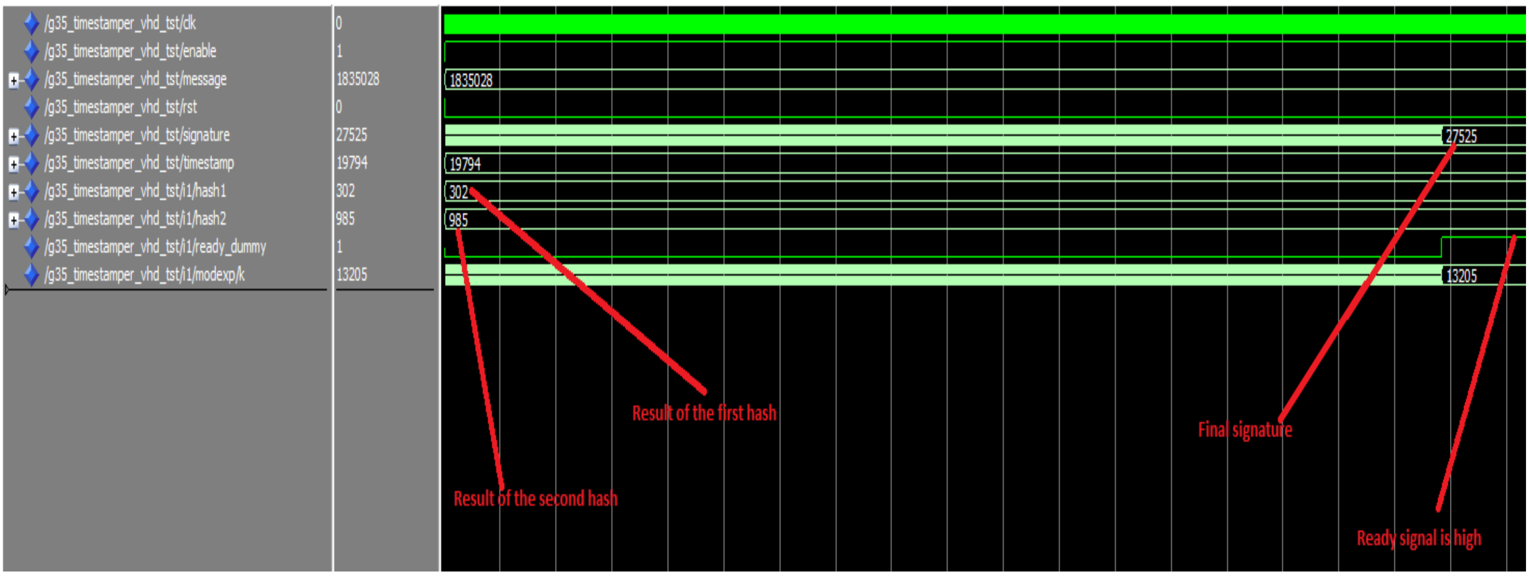


```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
use ieee.numeric_std.all; -- needed if you are using unsigned numbers
ENTITY g35_timestamper_vhd_tst IS
END g35_timestamper_vhd_tst;
ARCHITECTURE g35_timestamper_arch OF g35_timestamper_vhd_tst IS
-- constants
-- signals
SIGNAL clk : STD_LOGIC;
SIGNAL enable : STD_LOGIC;
SIGNAL message : STD_LOGIC_VECTOR(31 DOWNTO 0);
SIGNAL rst : STD_LOGIC;
SIGNAL signature : STD_LOGIC_VECTOR(15 DOWNTO 0);
SIGNAL timestamp : STD_LOGIC_VECTOR(21 DOWNTO 0);
COMPONENT g35_timestamper
    PORT (
    clk : IN STD_LOGIC;
    enable : IN STD_LOGIC;
    message : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
    rst : IN STD_LOGIC;
    signature : OUT STD_LOGIC_VECTOR(15 DOWNTO 0);
    timestamp : IN STD_LOGIC_VECTOR(21 DOWNTO 0)
    );
END COMPONENT;
BEGIN

    init : PROCESS
     begin
      clk <= '0';
      wait for 5 ns;
      clk <= '1';
      wait for 5 ns;
    end process;

    i1 : g35_timestamper
    PORT MAP (
-- list connections between master ports and signals
        clk => clk,
        enable => enable,
        message => message,
        rst => rst,
        signature => signature,
        timestamp => timestamp
    );

always : PROCESS

BEGIN
        enable <= '0';
        message <= "00000000000000000000000000010110";
        timestamp <= std_logic_vector(to_unsigned(19794,22));
        rst <= '1';
        wait for 10 ns;
        rst <= '0';
        enable <= '1';
        wait for 30 ns;
        message <= "00000000000111000000000000010100";
WAIT;
END PROCESS always;
END g35_timestamper_arch;
```

<u>**Simulation results (all the results are unsigned decimals):**</u>



	Msgs
/g35_timestamper_vhd_tst/clk	1
/g35_timestamper_vhd_tst/enable	1
/g35_timestamper_vhd_tst/message	1835028
/g35_timestamper_vhd_tst/rst	0
/g35_timestamper_vhd_tst/signature	985
/g35_timestamper_vhd_tst/timestamp	19794
/g35_timestamper_vhd_tst/i1/hash1	302
/g35_timestamper_vhd_tst/i1/hash2	985
/g35_timestamper_vhd_tst/i1/ready_dummy	0



/g35_timestamper_vhd_tst/clk	0
/g35_timestamper_vhd_tst/enable	1
/g35_timestamper_vhd_tst/message	1835028
/g35_timestamper_vhd_tst/rst	0
/g35_timestamper_vhd_tst/signature	27525
/g35_timestamper_vhd_tst/timestamp	19794
/g35_timestamper_vhd_tst/i1/hash1	302
/g35_timestamper_vhd_tst/i1/hash2	985
/g35_timestamper_vhd_tst/i1/ready_dummy	1
/g35_timestamper_vhd_tst/i1/modexp/k	13205