Novoptel

Laser Unit
LU1000

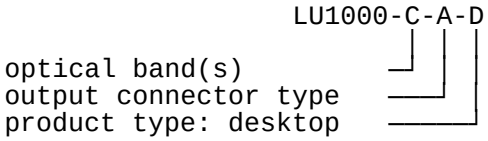
Revision history

Version	Date	Remarks	Author
0.5.0	20.11.2015	Draft version	B. Koch

General description

- 1 or 2 lasers, tunable in steps of 50 GHz (or tbd)
- 10 dBm output power (or more tbd)
- C & L band available, optionally at common output
- Desktop unit
- Operation via control buttons or via USB using Graphical User Interface, Matlab, Labview or similar.

Ordering information



For example, the type LU1000-CL-A-D covers optical C and L band, has FC/APC connector(s), and comes as a desktop unit.

Novoptel GmbH
EIM-E
Warburger Str. 100
33098 Paderborn
Germany
www.novoptel.com

Novoptel reserves the right to change module and specifications.

Absolute maximum ratings

Parameter	Value	Remarks/Conditions
Supply voltage	−0.3...+5.5 V	
Voltage at all logical ports	−0.3...+3.6 V	
Storage temperature	−40...+85°C	
Operating temperature	−10...+70°C	

Characteristics

Parameter	Value	Remarks/Conditions
Supply voltage	+4.75...5.25 V	
Supply current	2 A or tbd	
Logical port levels	LVCMOS33	3.3 V CMOS logic

Connector types

Type	Function
N	none
F	FC/UPC
A	FC/APC
L	LC/UPC
S	SC/PC
E	E2000

First letter specifies input connector, second letter specifies output connector(s).

Serial peripheral interface (SPI)

The module starts operation without SPI. The user doesn't have to use the SPI at all. While the module starts operation without SPI, this serial interface can be used to control function, modify parameters, read back these commands as well as debug register contents.

Transmission starts with falling edge of CS and ends with rising edge of CS. After falling edge of CS, the command is transmitted. SDI is sampled with rising edge of SCK. Maximum SCK frequency is 500 kHz. Command and data word length is 16 bit each. MSB of command and data word is sent first, LSB last. If a valid *register read* (RDREG) command is received, the SDO output register shifts with falling edge of SCK to transmit the requested data word. Otherwise SDO remains in high impedance state. Data transfer to the device continues directly after transmitting a *register write* (WRREG) command.

Each SPI register has 16 bit. Upon power-on, all registers are reset to default.

For a possible remote debugging, content of all defined registers needs to be read and sent to Novoptel.

All registers in the 12-bit address space that are not defined below are reserved, and should not be written into!

Serial peripheral interface (SPI) commands

Command	Code	Data	Function
RDREG	0XXXh	OUT	Read register XXXh (for definition see below)
WRREG	1XXXh	IN	Write register XXXh (for definition see below)

Register address coding

Bits	Function
11..9	Reserved. Leave “000”.
8..7	“00”: Common registers “01”: Laser 1 registers “10”: Laser 2 registers (optional) “11”: Laser 3 registers (optional)
6..0	Register address 0..127

Common registers

Register address	Name	Bit(s)	Read/ Write	Function
0	ALM			Internal alarm code. The alarm can be cleared by writing “0” to this register. This is successful only if the alarm condition is no longer present.
		0	R/W	tbd.
		1	R/W	tbd.
		2	R/W	tbd.
		4	R/W	Critical temperature.
1	BUSY	0	R	“1”: Controller module is busy
2	NLAS	15..0	R	Number of installed laser modules
19	UPDIS	0	R/W	“1” (default) : Enable internal register update
20	WRADDR	7..0	W	Write address for external register access
21	WRDATA	15..0	W	Data word for external register access
22	WRTRIG	0	W	“1”: External write operation on registers of laser 1.
		1	W	“1”: External write operation on registers of laser 2.
23	RDADDR	7..0	W	Read address for external register access
24	RDTRIG	0	W	“1” triggers read operation on all installed lasers.
25	DOUT1	15..0	R	Data word read from laser 1
26	DOUT2	15..0	R	Data word read from laser 2
51	TMPR	15..0	R	Controller module temperature in Celsiusx16
64	FW	15..0	R	Firmware version as 4 digit BCD
65	SN	15..0	R	Controller module serial number
68 … 83	MODTYP	15..0	R	Module Type as 32 character string. Beginning at 512+144, each Register contains two bytes, representing two ASCII-coded characters.
85	DDNA1	15..0	R	Device DNA word 3 (DNA bits 63...48) (same as read via JTAG)
86	DDNA2	15..0	R	Device DNA word 2 (DNA bits 47...32) (same as read via JTAG)
87	DDNA3	15..0	R	Device DNA word 1 (DNA bits 31...16) (same as read via JTAG)
88	DDNA4	15..0	R	Device DNA word 0 (DNA bits 15...0) (same as read via JTAG)

Laser control registers

Register address	Name	Bit(s)	Read/ Write	Function
0	NOP	15..8	R	Pending Operation Flags. 0 indicates that there are no currently pending operations
		4	R	“1” indicates that the module is ready for its output to be enabled
		3..0	R	Error condition according to OIF-ITLA-MSA-01.0
1	LBUS	1	R	“1”: Serial interface of laser is busy.
		0	R	“1”: Serial interface of laser is has a timeout exception.
48	Channel	15..0	R/W	Sets or returns the laser module’s current channel.

49	PWR	15..0	R/W	Sets or returns the laser module's current optical power in dBm*100
50	ResEna	15..0	R/W	Sets or returns the laser module's current status. Supported commands: 0x00: Laser output disabled 0x08: Laser output enabled
52	GRID	15..0	R	Grid spacing in GHz*10
53	FCF1	15..0	R	First channel's frequency, THz
54	FCF2	15..0	R	First channel's frequency, GHz*10
64	LF1	15..0	R	Returns channel's frequency as THz
65	LF2	15..0	R	Returns channel's frequency as GHZ*10
66	OOP	15..0	R	Returns the optical power encoded as dBm*100
67	CTemp	15..0	R	Returns the current temperature encoded as °C*100.
80	OPSL	15..0	R	Minimum possible optical power setting
81	OPSH	15..0	R	Maximum possible optical power setting
82	LFL1	15..0	R	Laser's first frequency, THz
83	LFL2	15..0	R	Laser's first frequency, GHz*10
84	LFH1	15..0	R	Laser's last frequency, THz
85	LFH2	15..0	R	Laser's last frequency, GHz*10
86	LGrid	15..0	R	Laser's minimum supported grid spacing, GHz*10

Serial peripheral interface (SPI) timing

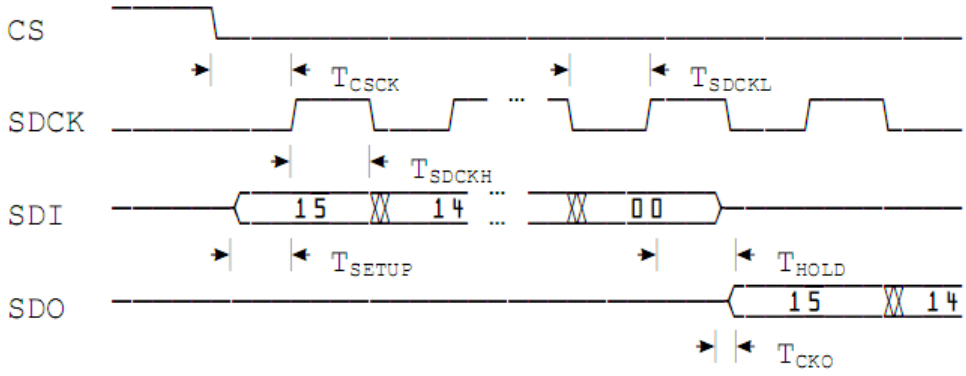


Fig. 1: Timing of SPI port.

Symbol	Description	Min	Max	Units
T_{CSCK}	CS low to SDCK high	120	–	ns
T_{CKCS}	SDCK low to CS high	120	–	ns
T_{SDCKL}	SDCKL low time	1	–	µs
T_{SDCKH}	SDCKL high time	1	–	µs
T_{SETUP}	SDI egde to SDCK high (setup time)	30	–	ns
T_{HOLD}	SDCK to SDI edge (hold time)	30	–	ns
T_{CKO}	SDCK edge to stable SDO	–	100	ns

USB transfer protocol

All SPI registers described above can also be accessed via USB. All communication is initiated by the host, e.g. the connected PC. Writing to a register uses a 9 byte data packet. Each byte represents an ASCII-coded character. The packet starts with the ASCII-character "W" and ends with the ASCII-code for carriage return:

"W"	A(2)	A(1)	A(0)	D(3)	D(2)	D(1)	D(0)	^CR

The 12 bit register address A is sent using 3 bytes, each containing the ASCII-character of the hexadecimal numbers 0 to F which represents the 4 bit nibble. The character of the most significant

nibble is sent first. The 16 bit data, which should be written into the register, is sent with 4 bytes using the same coding as the register address.

Reading data from a register requires the host to send a request data packet to the instrument. The packet starts with the ASCII-character “R”, followed by the register address coded the same way as in write data packets:

“R”	A(2)	A(1)	“0”	“0”	“0”	“0”	“0”	^CR

After receiving the request data packet, the instrument sends the requested data packet to the host:

D(3)	D(2)	D(1)	D(0)	^CR

Firmware upgrading

Via the JTAG port the user can upgrade the firmware. Note that the upgrading firmware must be obtained from Novoptel on a per-module basis because the firmware is encrypted and authenticated. For this purpose, Novoptel needs to be told the device DNA of the FPGA, which also serves as the serial number of the module. The user can find out the device DNA remotely via SPI (as long as the firmware is working) or via JTAG (in any case, which is therefore recommended). During firmware upgrading, polarization control is not possible.

The schematic and timing of the JTAG port correspond to that detailed in Spartan-3 Generation Configuration User Guide UG332 (v1.6) October 26, 2009 from Xilinx (www.xilinx.com). A schematic is given in Fig. 2.

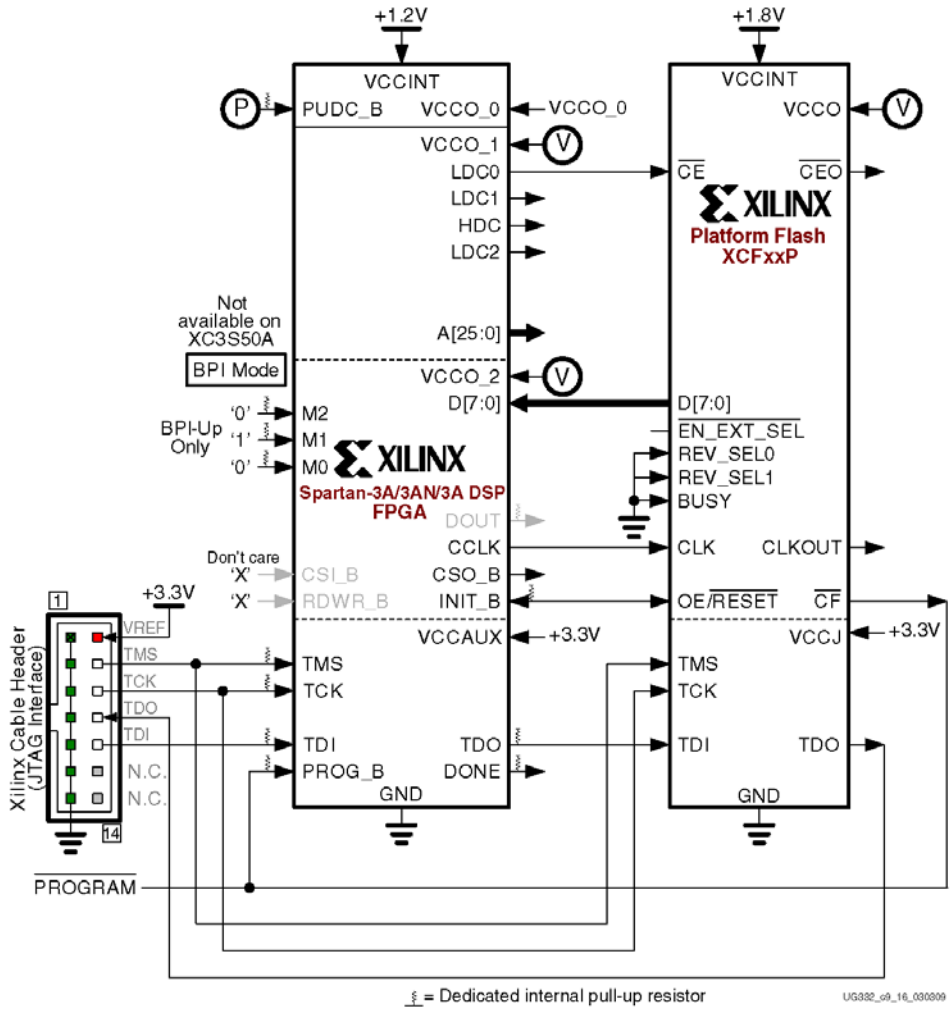


Figure 5-6: **Master BPI Mode Using Xilinx Parallel Platform Flash PROMs (XCFxxP)**

- The diagram in Figure 5-6 shows an Extended Spartan-3A family FPGA, but the same approach also works with Spartan-3E FPGAs.
- The Xilinx Parallel Platform Flash PROM family is in-system programmable using JTAG, similar to the FPGA.
- See XAPP483, *Multiple-Boot with Platform Flash PROMs*
- The FPGA's LDC2, LDC1, LDC0, and HDC outputs actively drive during configuration. Use the LDC0 output to enable the Platform Flash PROM during

Fig. 2: Schematic of JTAG port, adopted from Xilinx. However, instead of the Xilinx Cable Header the JTAG connections are part of the module connector.

JTAG Timing

Fig. 3 shows timing definitions of the JTAG port signals (source: Platform Flash Product Specification DS123 (v2.16) November 14, 2008 from XILINX (www.xilinx.com)).

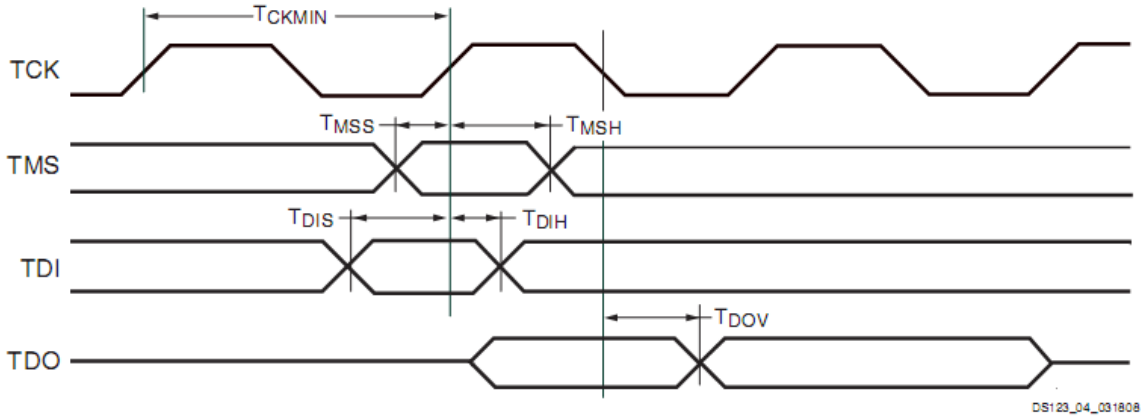


Fig. 3: Timing of JTAG port, adopted from Xilinx.

Symbol	Description	Min	Max	Units
T_{CKMIN}	TCK minimum clock period	67	–	ns
T_{MSS}	TMS setup time	8	–	ns
T_{MSH}	TMS hold time	25	–	ns
T_{DIS}	TDI setup time	8	–	ns
T_{DIH}	TDI hold time	25	–	ns
T_{DOV}	TDO valid delay	–	22	ns

Miscellaneous

This module is designed for industrial applications only. It must not be used if human life depends on its correct functioning (e.g., medical applications).

Installation and use of the module have to comply with the corresponding regulations for the operation of electrical and optical installations of the country where the module is to be used.

Diversion contrary to German law is prohibited. In addition, diversion contrary to USA law is prohibited. Module hardware is subject to compliance with all United States Export Administration Regularities. USA Regulations prohibit the transfer or reexport of module hardware, directly or indirectly, to restricted countries or entities.

You or anybody to whom you grant access may not reverse engineer, disassemble, decompile or decode the module, its hardware and software, except and only to the extent that such activity is expressly permitted by applicable law notwithstanding this limitation.

Fiber coatings are of Hytrel® or similar material. Module must therefore be protected against ultraviolet light exposure.