

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT541 Octal buffer/line driver; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Octal buffer/line driver; 3-state**74HC/HCT541****FEATURES**

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

$GND = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	$C_L = 15 \text{ pF}$; $V_{CC} = 5 \text{ V}$	10	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	37	39	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION

See "*74HC/HCT/HCU/HCMOS Logic Package Information*".

Octal buffer/line driver; 3-state

74HC/HCT541

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	bus outputs
20	V_{CC}	positive supply voltage

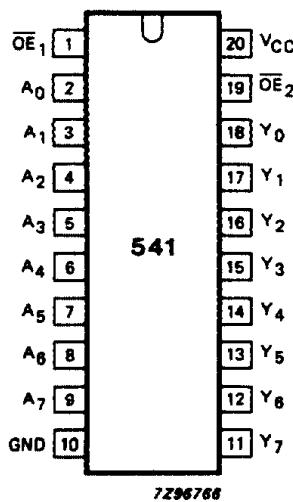


Fig.1 Pin configuration.

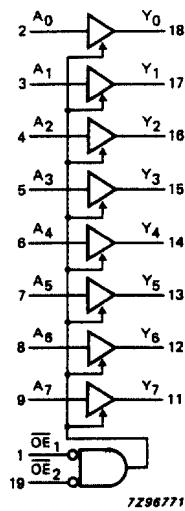


Fig.2 Logic symbol.

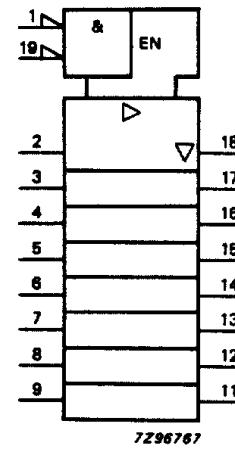


Fig.3 IEC logic symbol.

Octal buffer/line driver; 3-state

74HC/HCT541

FUNCTION TABLE

INPUTS		OUTPUT	
\overline{OE}_1	\overline{OE}_2	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

Notes

1. H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

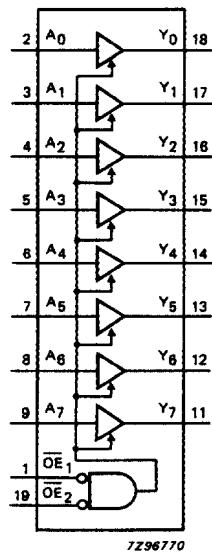


Fig.4 Functional diagram.

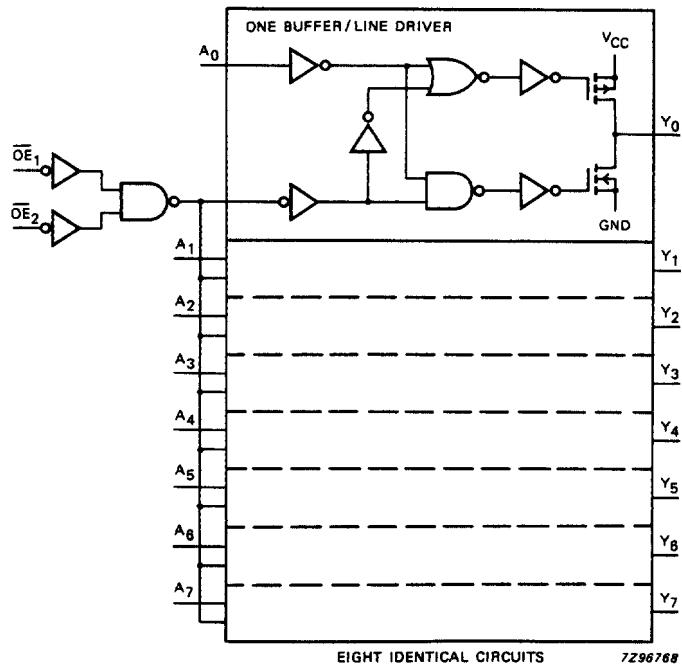


Fig.5 Logic diagram.

Octal buffer/line driver; 3-state

74HC/HCT541

DC CHARACTERISTICS FOR 74HCFor the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: bus driver

I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{cc} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n	33 12 10	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig.6		
t _{PZH} / t _{PZL}	3-state output enable time OE to Y _n	55 20 16	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.7		
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Y _n	61 22 18	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.7		
t _{THL} / t _{TLH}	output transition time	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6		

Octal buffer/line driver; 3-state

74HC/HCT541

DC CHARACTERISTICS FOR 74HCTFor the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: bus driver

I_{CC} category: MSI**Note to HCT types**The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
\overline{OE}_1	1.50
\overline{OE}_2	1.00
A _n	0.70

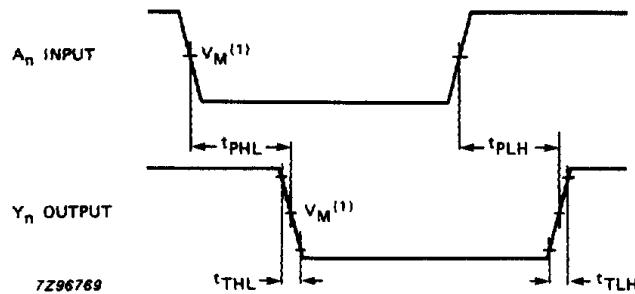
AC CHARACTERISTICS FOR 74HCTGND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n		15	28		35		42	ns	4.5	Fig.6	
t _{PZH} / t _{PZL}	3-state output enable time OE to Y _n		21	35		44		53	ns	4.5	Fig.7	
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Y _n		21	35		44		53	ns	4.5	Fig.7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6	

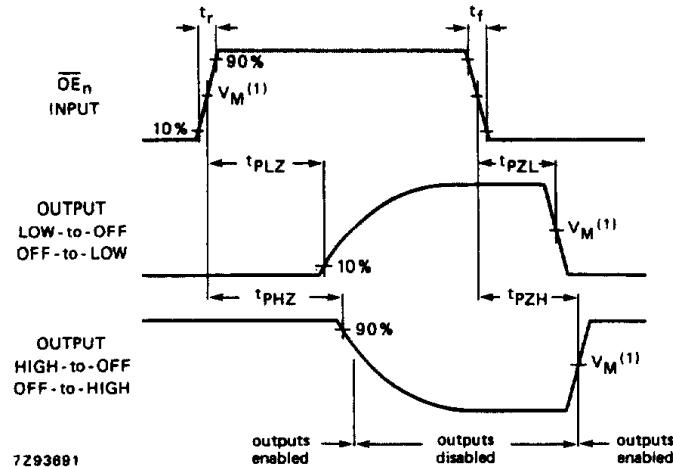
Octal buffer/line driver; 3-state

74HC/HCT541

AC WAVEFORMS



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.6 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.7 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".