

# 74HC590

8-bit binary counter with output register; 3-state

Rev. 02 — 28 April 2009

Product data sheet

## 1. General description

The 74HC590 is a high-speed Si-gate CMOS device and is pin compatible with Low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC590 is an 8-bit binary counter with a storage register and 3-state outputs. The storage register has parallel (Q0 to Q7) outputs. The binary counter features a master reset counter ( $\overline{MRC}$ ) and count enable ( $\overline{CE}$ ) inputs. The counter and storage register have separate positive edge triggered clock (CPC and CPR) inputs. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable. A ripple carry output ( $\overline{RCO}$ ) is provided for cascading. Cascading is accomplished by connecting  $\overline{RCO}$  of the first stage to  $\overline{CE}$  of the second stage. Cascading for larger count chains can be accomplished by connecting  $\overline{RCO}$  of each stage to the counter clock (CPC) input of the following stage. If both clocks are connected together, the counter state always is one count ahead of the register.

## 2. Features

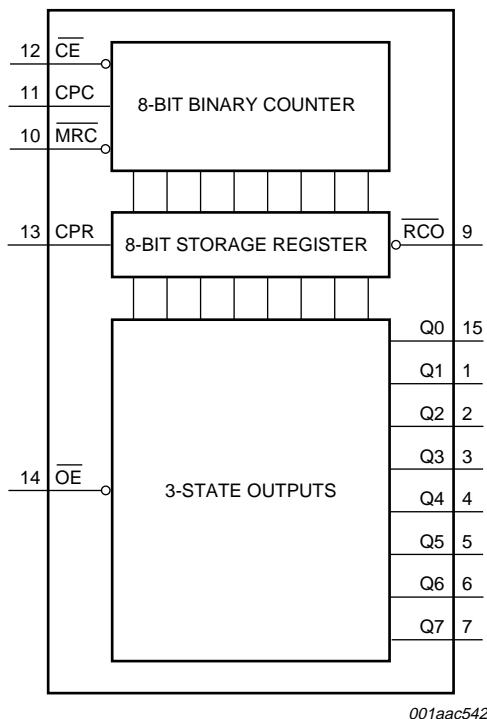
- Counter and register have independent clock inputs
- Counter has master reset
- Complies with JEDEC standard no. 7A
- Multiple package options
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 2000 V
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

## 3. Ordering information

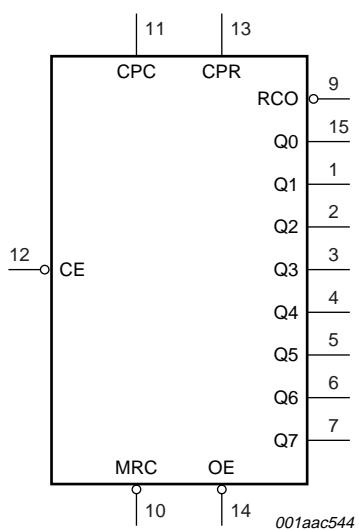
Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC590N	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	DIP16	plastic dual in-line package; 16 leads (300 mil)		SOT38-4
74HC590D	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm		SOT109-1
74HC590PW	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm		SOT403-1
74HC590BQ	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5 \times 3.5 \times 0.85$ mm		SOT763-1

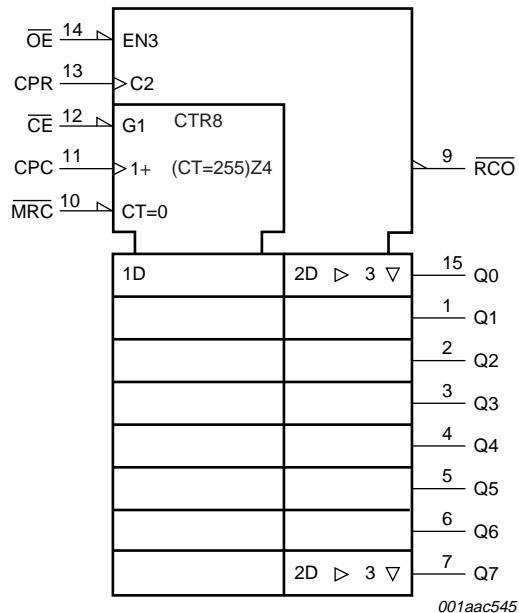
#### 4. Functional diagram



**Fig 1.** Functional diagram



**Fig 2.** Logic symbol



**Fig 3.** IEC logic symbol

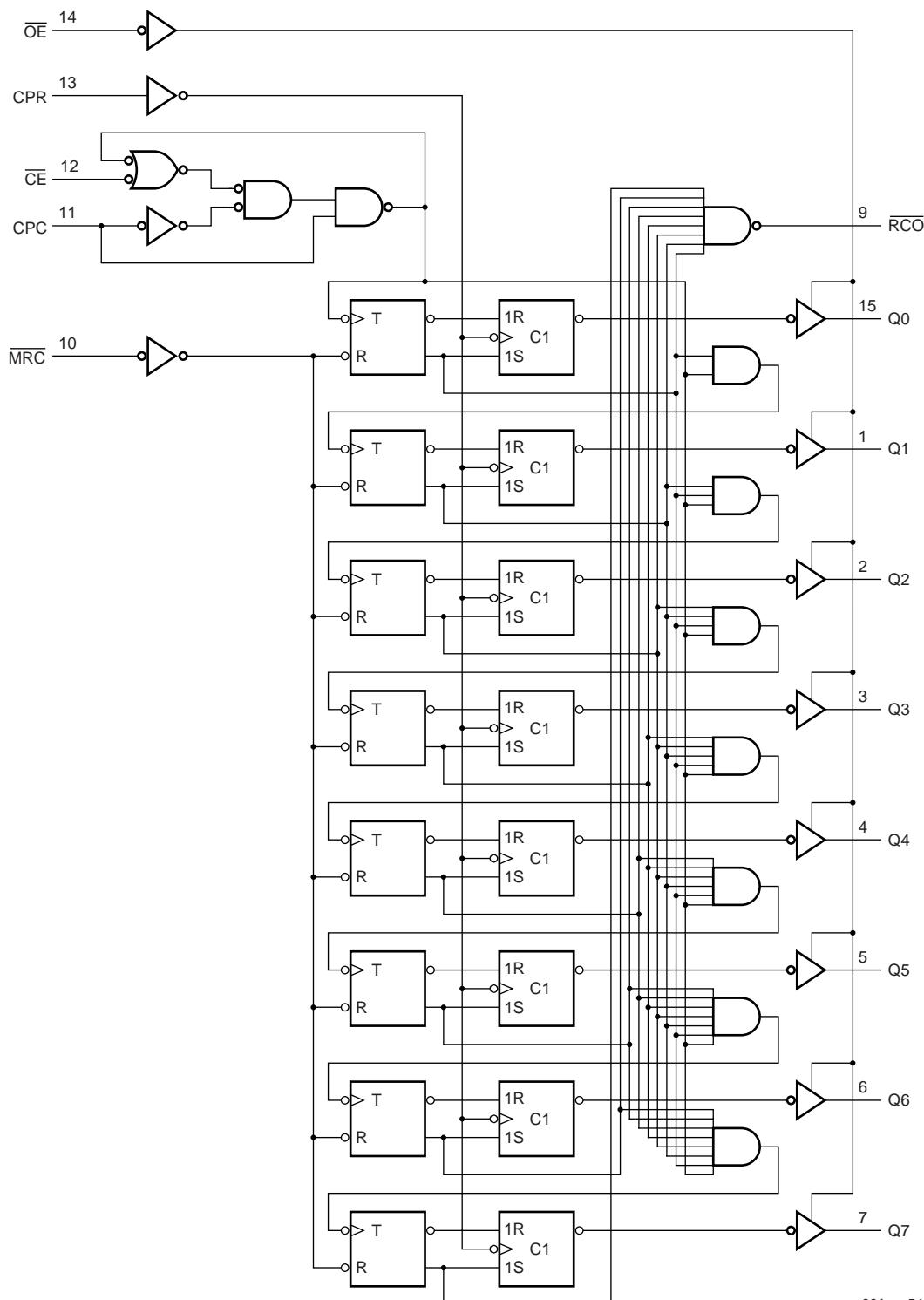


Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning

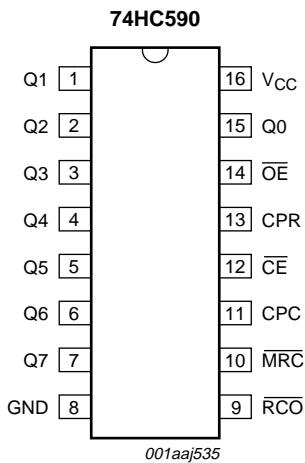


Fig 5. Pin configuration DIP16

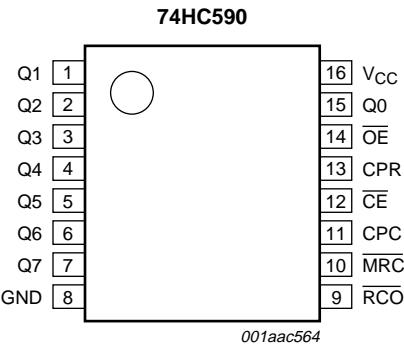
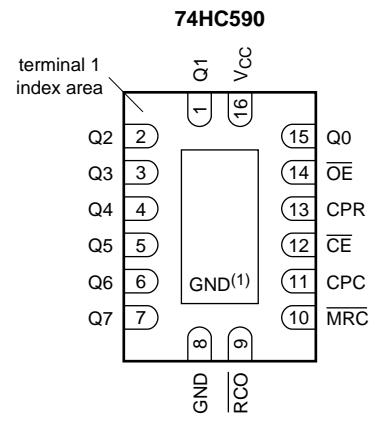


Fig 6. Pin configuration SO16 and TSSOP16



- (1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 7. Pin configuration DHVQFN16

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0 to Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
RCO	9	ripple carry output (active LOW)
MRC	10	master reset counter input (active LOW)
CPC	11	counter clock input (active HIGH)
CE	12	count enable input (active LOW)
CPR	13	register clock input (active HIGH)
OE	14	output enable input (active LOW)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup> <sup>[2]</sup>

Inputs					Description
OE	CPR	MRC	CE	CPC	
H	X	X	X	X	Q outputs disable
L	X	X	X	X	Q outputs enable
X	↑	X	X	X	counter data stored into register
X	↓	X	X	X	register stage is not changed
X	X	L	X	X	counter clear
X	X	H	L	↑	advance one count
X	X	H	L	↓	no count
X	X	H	H	X	no count

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

↑ = LOW-to-HIGH transition;

↓ = HIGH-to-LOW transition.

[2]  $RCO = \overline{Q0'} \cdot Q1' \cdot Q2' \cdot Q3' \cdot Q4' \cdot Q5' \cdot Q6' \cdot Q7'$  ( $Q0'$  to  $Q7'$  are internal outputs of the counter).

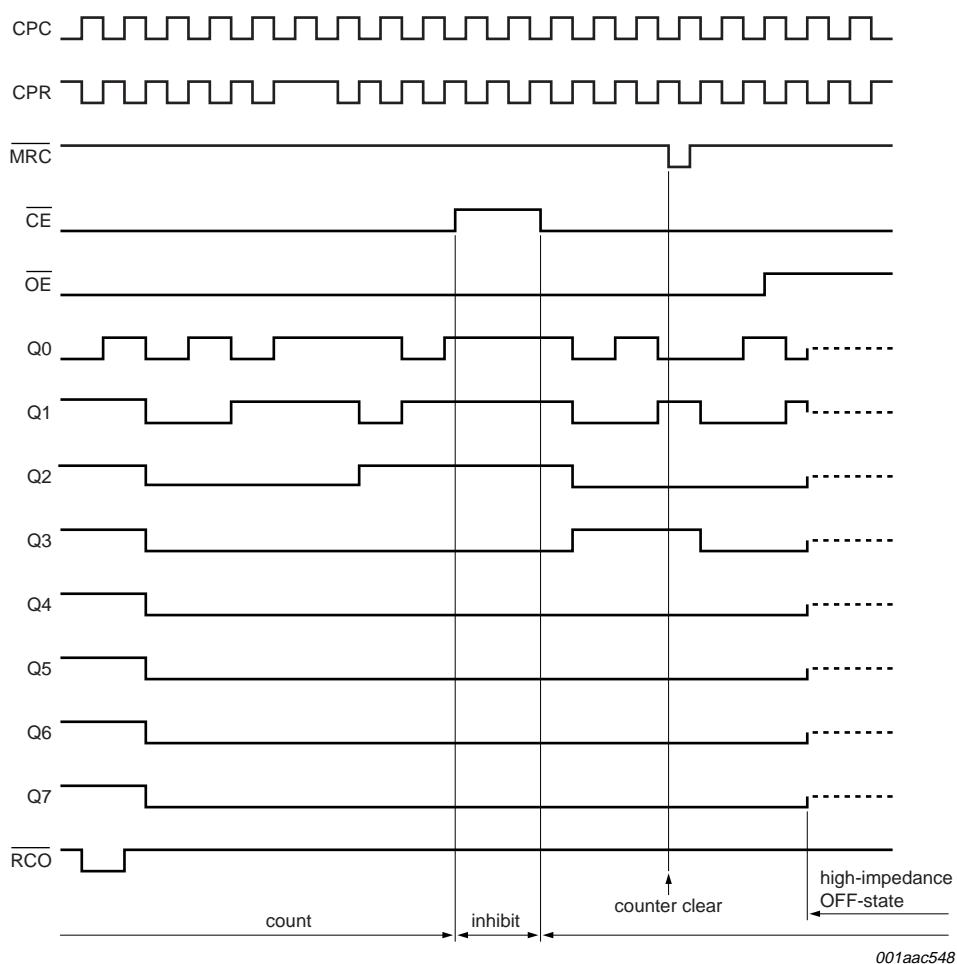


Fig 8. Typical timing sequence

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to V <sub>CC</sub> + 0.5 V			
		RCO standard output	-	±25	mA
		Qn bus driver output	-	±35	mA
I <sub>CC</sub>	supply current		-	70	mA
I <sub>GND</sub>	ground current		-70	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2]		
		DIP16 package	-	750	mW
		SO16 package	-	500	mW
		TSSOP16 package	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

For SO16 packages: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

For TSSOP16 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN16 packages: P<sub>tot</sub> derates linearly with 8 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	ns/V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5 \text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ all outputs								
		$I_O = -20 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu\text{A}; V_{CC} = 6.0 \text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$\overline{\text{RCO}}$ standard output								
		$I_O = -4 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.18	4.31	-	4.13	-	4.1	-	V
		$I_O = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.68	5.80	-	5.63	-	5.6	-	V
		Qn bus driver output								
		$I_O = -6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.18	4.31	-	4.13	-	4.1	-	V
		$I_O = -7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.68	5.80	-	5.63	-	5.6	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ all outputs								
		$I_O = 20 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu\text{A}; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$\overline{\text{RCO}}$ standard output								
		$I_O = 4 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.17	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.18	0.26	-	0.33	-	0.4	V
		Qn bus driver output								
		$I_O = 6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.17	0.26	-	0.33	-	0.4	V
		$I_O = 7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.18	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	per pin; $V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; other inputs at $V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	$\pm 0.5$	-	$\pm 5.0$	-	$\pm 10$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 6.0 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**GND (ground = 0 V); for test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	CPC to RCO; see <a href="#">Figure 9</a> [1]								
		V <sub>CC</sub> = 2.0 V	-	52	150	-	190	-	230	ns
		V <sub>CC</sub> = 4.5 V	-	19	30	-	38	-	45	ns
		V <sub>CC</sub> = 6.0 V	-	15	26	-	33	-	40	ns
		CPR to Qn; see <a href="#">Figure 10</a>								
	LOW to HIGH propagation delay	V <sub>CC</sub> = 2.0 V	-	50	140	-	175	-	210	ns
		V <sub>CC</sub> = 4.5 V	-	17	28	-	35	-	42	ns
		V <sub>CC</sub> = 6.0 V	-	14	24	-	30	-	36	ns
		MRC to RCO; see <a href="#">Figure 11</a>								
		V <sub>CC</sub> = 2.0 V	-	53	130	-	165	-	200	ns
$t_{en}$	enable time	V <sub>CC</sub> = 4.5 V	-	18	26	-	33	-	40	ns
		V <sub>CC</sub> = 6.0 V	-	14	22	-	28	-	34	ns
		OĒ to Qn; see <a href="#">Figure 12</a> [2]								
	disable time	V <sub>CC</sub> = 2.0 V	-	28	105	-	130	-	160	ns
		V <sub>CC</sub> = 4.5 V	-	13	21	-	26	-	32	ns
		V <sub>CC</sub> = 6.0 V	-	11	18	-	22	-	27	ns
$t_w$	pulse width	CPC and CPR; HIGH or LOW; see <a href="#">Figure 9</a> and <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 2.0 V	100	24	-	125	-	145	-	ns
		V <sub>CC</sub> = 4.5 V	20	9	-	25	-	29	-	ns
		V <sub>CC</sub> = 6.0 V	17	8	-	21	-	25	-	ns
		MRC; LOW; see <a href="#">Figure 11</a>								
	set-up time	V <sub>CC</sub> = 2.0 V	75	28	-	95	-	110	-	ns
		V <sub>CC</sub> = 4.5 V	15	8	-	19	-	22	-	ns
		V <sub>CC</sub> = 6.0 V	13	6	-	16	-	19	-	ns
		CPC to CPR; see <a href="#">Figure 14</a>								
	CĒ to CPC	V <sub>CC</sub> = 2.0 V	100	46	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	14	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	10	-	21	-	26	-	ns
	CĒ to CPC; see <a href="#">Figure 13</a>	CĒ to CPC; see <a href="#">Figure 13</a>								
		V <sub>CC</sub> = 2.0 V	100	44	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	11	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	9	-	21	-	26	-	ns

**Table 7. Dynamic characteristics ...continued**  
GND (ground = 0 V); for test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_h$	hold time	CE to CPC; see <a href="#">Figure 13</a>								
		V <sub>CC</sub> = 2.0 V	0	-	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-	-	0	-	0	-	ns
$t_{rec}$	recovery time	MRC to CPC; see <a href="#">Figure 11</a>								
		V <sub>CC</sub> = 2.0 V	75	28	-	95	-	110	-	ns
		V <sub>CC</sub> = 4.5 V	15	7	-	19	-	22	-	ns
$f_{max}$	maximum frequency	CPC or CPR; see <a href="#">Figure 9</a> and <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 2.0 V	6.6	16	-	5.2	-	4.4	-	MHz
		V <sub>CC</sub> = 4.5 V	33	52	-	26	-	22	-	MHz
$C_{PD}$	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub>	[4]	-	44	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$ ,  $t_{PLH}$ .

[2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[3]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

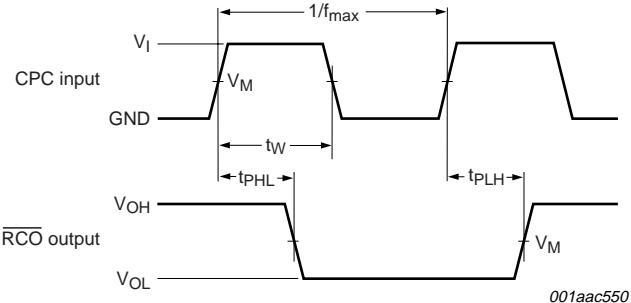
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

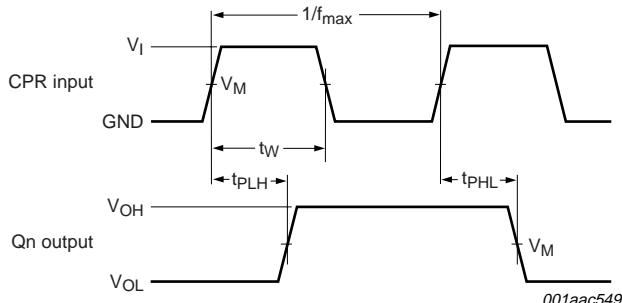
## 11. Waveforms



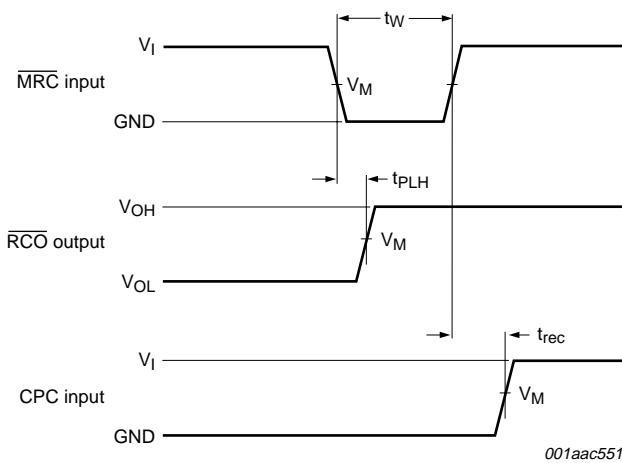
**Fig 9. Waveforms showing the propagation delays from the counter clock input (CPC) to ripple carry (RCO) output and the CPC pulse width**

**Table 8. Measurement points**

Type	Input	Output
	$V_I$	$V_M$
74HC590	$V_{CC}$	$0.5V_{CC}$
		$0.5V_{CC}$



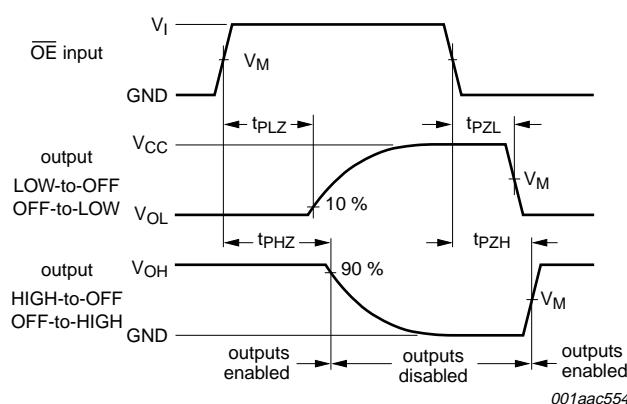
**Fig 10. Waveforms showing the propagation delays from the register clock input (CPR) to output (Qn) and the register clock pulse width**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

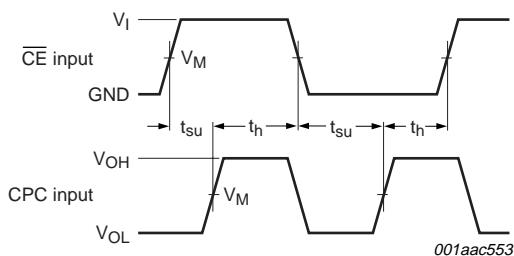
**Fig 11. Waveforms showing the propagation delays from the master reset counter input ( $\overline{MRC}$ ) to output ( $\overline{RCO}$ ), the  $\overline{MRC}$  pulse width and recovery time**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

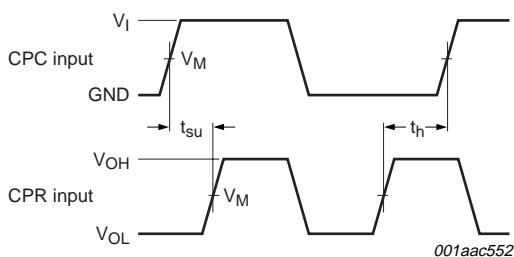
**Fig 12. Waveforms showing the 3-state enable and disable times**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

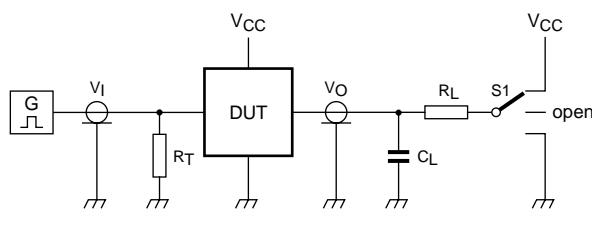
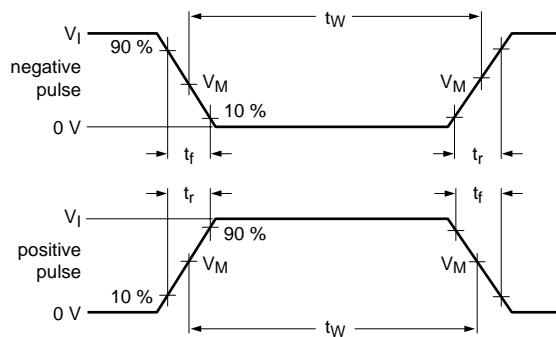
**Fig 13. Waveforms showing the set-up and hold times for the count enable input ( $\overline{CE}$ ) to the counter clock input (CPC)**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig 14. Waveforms showing the set-up and hold times for the counter clock input (CPC) to the register clock input (CPR)**



001aad983

Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig 15. Test circuit for measuring switching times**

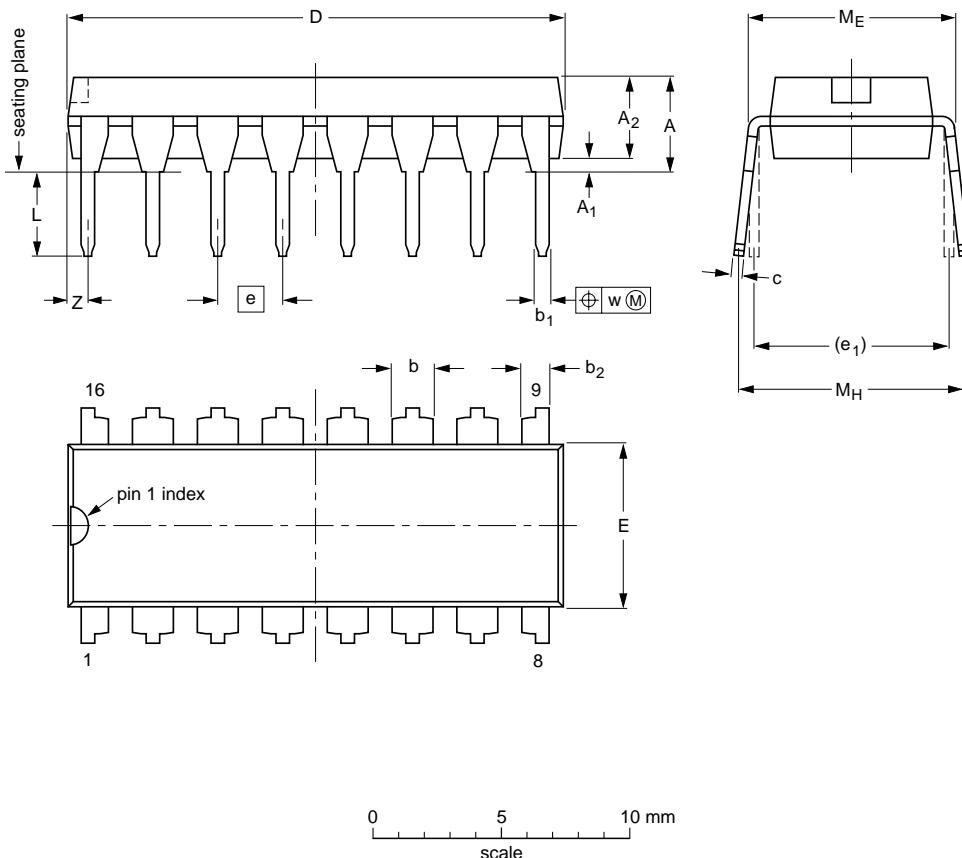
**Table 9. Test data**

Supply voltage	Input		Load		Switch position		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PZH</sub>	t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
2.0 V to 6.0 V	V <sub>CC</sub>	6 ns	50 pF	1 kΩ	open	GND	V <sub>CC</sub>

## 12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

### Note

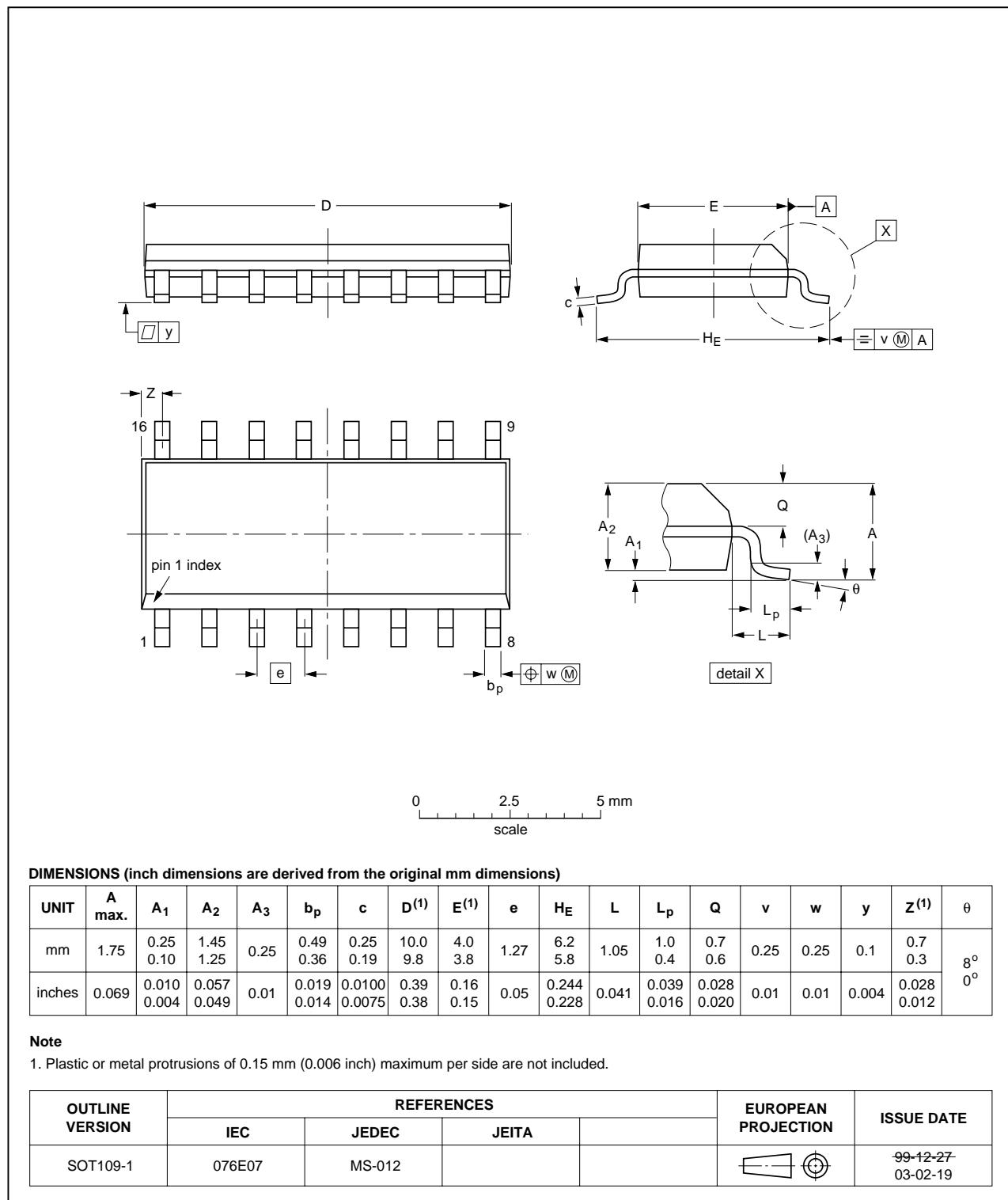
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 16. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 0.125	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0° 0°

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT109-1	076E07	MS-012			-99-12-27 03-02-19

**Fig 17. Package outline SOT109-1 (SO16)**

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

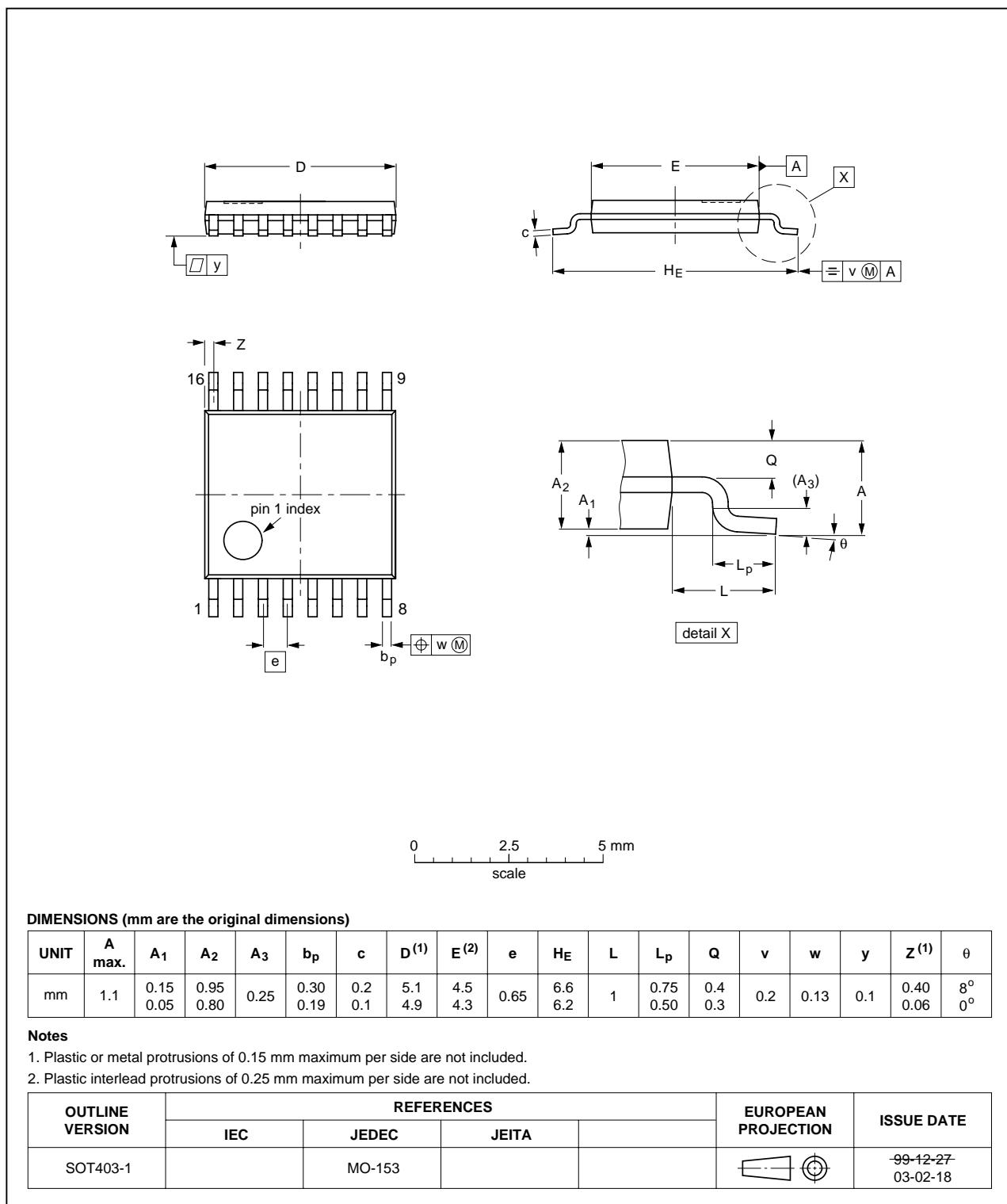


Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

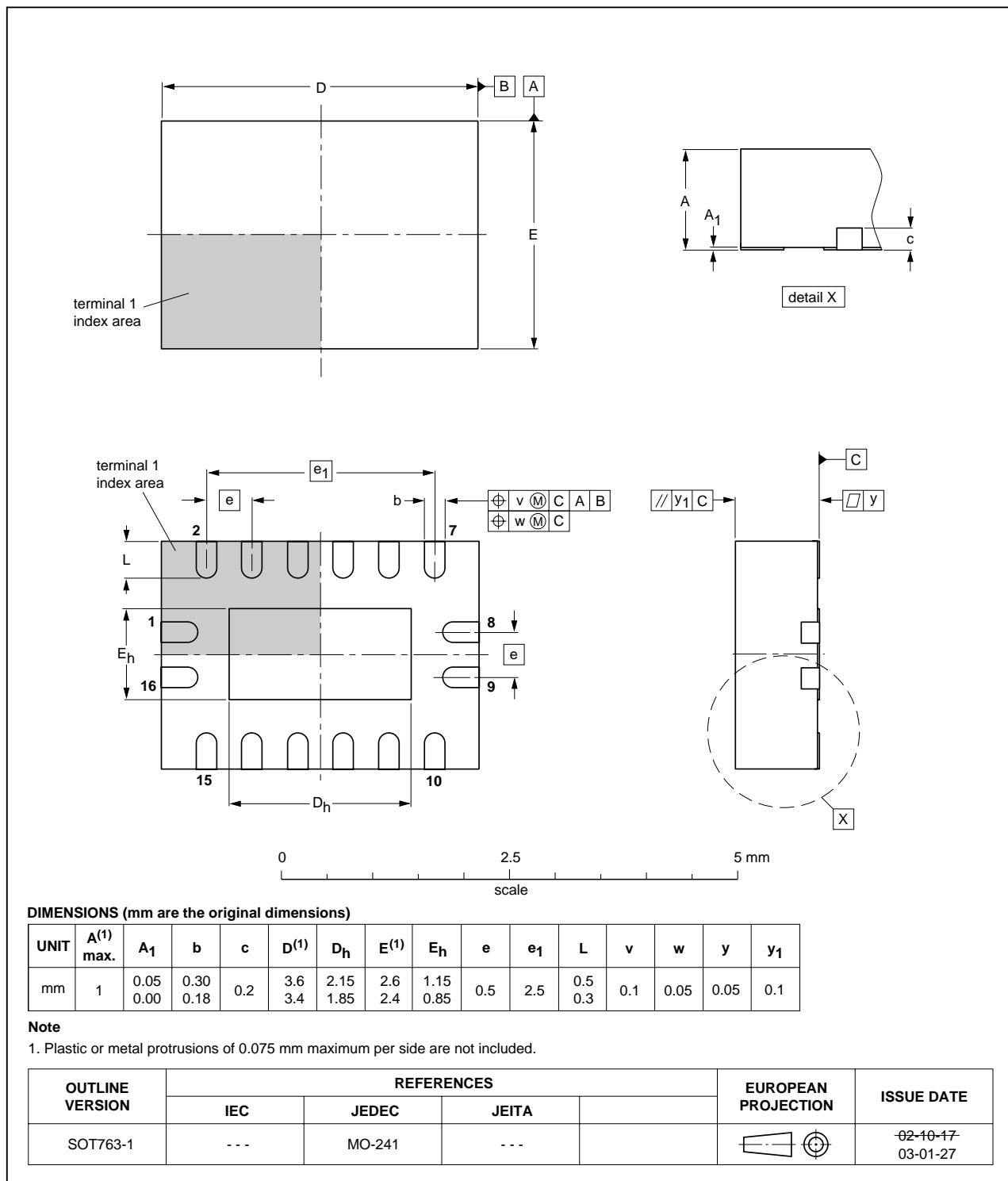


Fig 19. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC590_2	20090428	Product data sheet	-	74HC590_1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Quick reference data incorporated in to <a href="#">Section 9</a> and <a href="#">Section 10</a>.</li> <li>Added type number 74HC590N (DIP16 package)</li> </ul>			
74HC590_1	20050330	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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