



MOTOROLA

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

The SN54/74LS147 and the SN54/74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

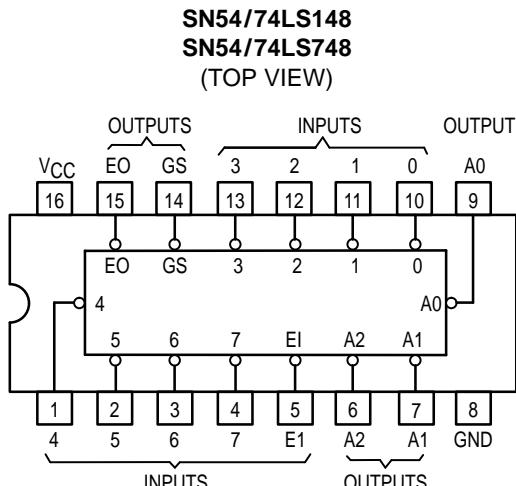
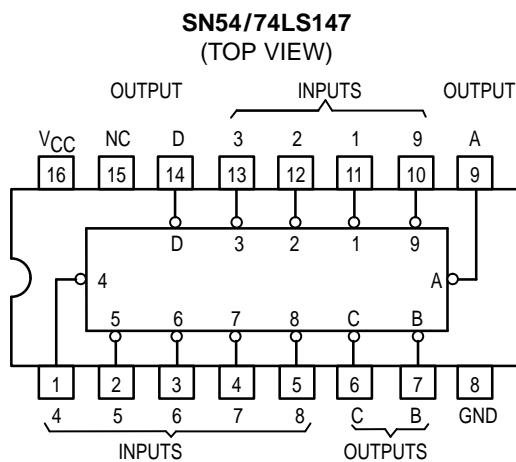
The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

The SN54/74LS748 is a proprietary Motorola part incorporating a built-in deglitcher network which minimizes glitches on the GS output. The glitch occurs on the negative going transition of the EI input when data inputs 0-7 are at logical ones.

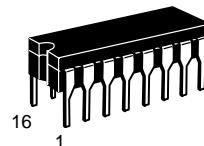
The only dc parameter differences between the LS148 and the LS748 are that (1) Pin 10 (input 0) has a fan-in of 2 on the LS748 versus a fan-in of 1 on the LS148; (2) Pins 1, 2, 3, 4, 11, 12 and 13 (inputs 1, 2, 3, 4, 5, 6, 7) have a fan-in of 3 on the LS748 versus a fan-in of 2 on the LS148.

The only ac difference is that t_{PHL} from EI to EO is changed from 40 to 45 ns.

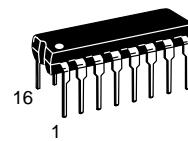


SN54/74LS147
SN54/74LS148
SN54/74LS748

**10-LINE-TO-4-LINE
AND 8-LINE-TO-3-LINE
PRIORITY ENCODERS**
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

**SN54/74LS147
FUNCTION TABLE**

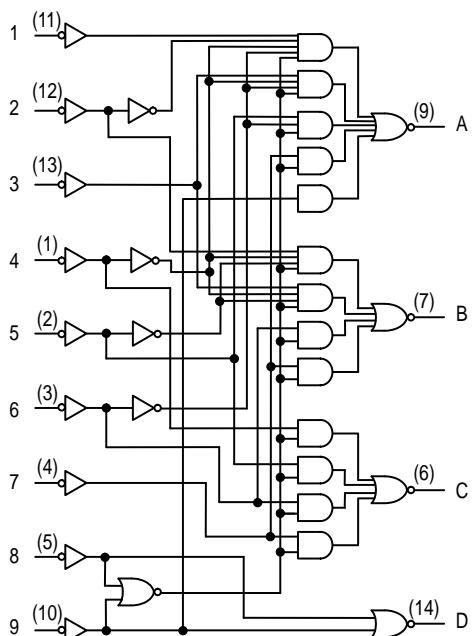
INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	X	L	H	H	H	L	L	H
X	X	X	X	X	L	H	H	H	H	L	H	L
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	L	H	H	H	H	H	H	H	H	L	L
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Logic Level, L = LOW Logic Level, X = Irrelevant

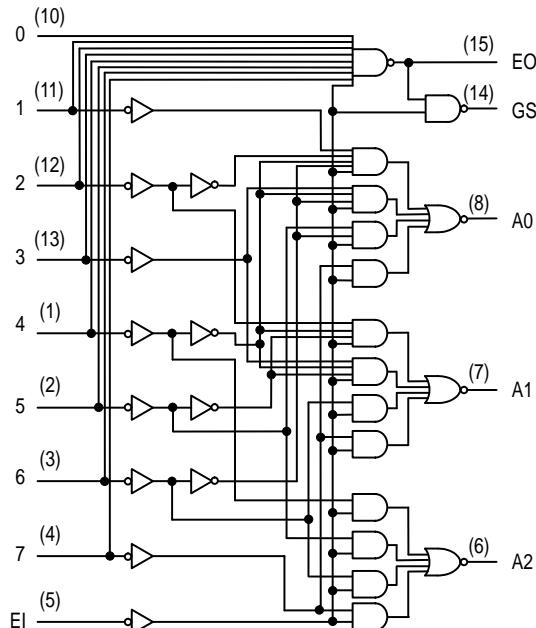
**SN54/74LS148
SN54/74LS748
FUNCTION TABLE**

INPUTS								OUTPUTS				GS	EO
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L	
L	X	X	X	X	X	X	X	L	L	L	L	H	
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	H	
L	X	X	X	L	H	H	H	H	H	L	H	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	H	
L	L	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

FUNCTIONAL BLOCK DIAGRAMS



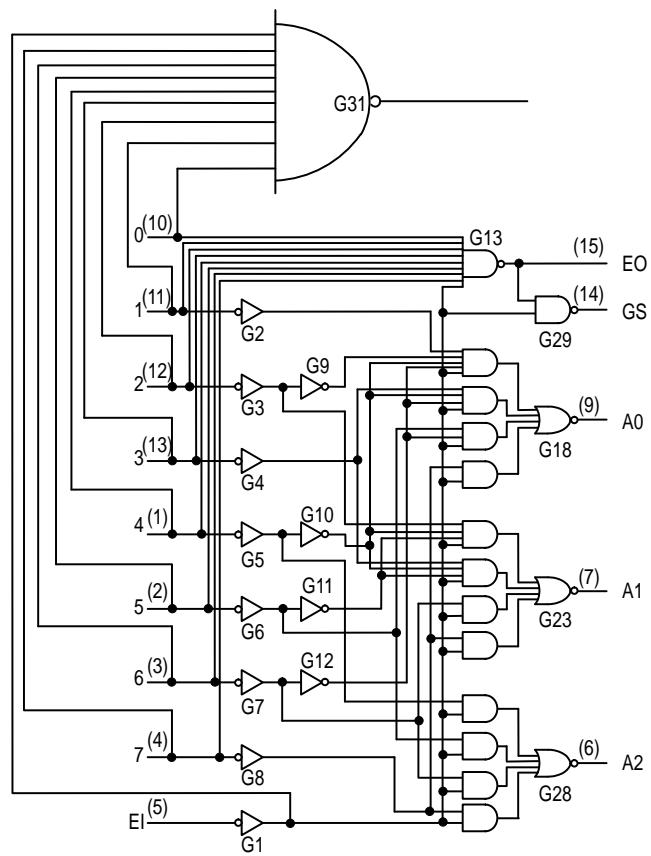
SN54/74LS147



SN54/74LS148

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

FUNCTIONAL BLOCK DIAGRAMS (continued)



SN54/74LS748

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25
T _A	Operating Ambient Temperature Range		54 74	-55 0	25 25	125 70
I _{OH}	Output Current — High	54, 74				-0.4
I _{OL}	Output Current — Low	54 74				4.0 8.0

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5	V	
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA
		74	0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)			20 40 40 60	µA	V _{CC} = MAX, V _{IN} = 2.7 V
	All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)			0.1 0.2 0.2 0.3	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)			-0.4 -0.8 -0.8 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CCH}	Power Supply Current Output HIGH			17	mA	V _{CC} = MAX, All Inputs = 4.5 V
I _{CCL}	Output LOW			20	mA	V _{CC} = MAX, Inputs 7 & E1 = GND All Other Inputs = 4.5 V

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

AC CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$)
SN54/74LS147

Symbol	From (Input)	To (Output)	Waveform	Limits			Unit	Test Conditions
				Min	Typ	Max		
t _{PLH}	Any	Any	In-phase output		12	18	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					12	18		
t _{PLH}	Any	Any	Out-of-phase output		21	33	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					15	23		

SN54/74LS148

SN54/74LS748

Symbol	From (Input)	To (Output)	Waveform	Limits			Unit	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
				Min	Typ	Max		
t _{PLH}	1 thru 7	A0, A1, or A2	In-phase output		14	18	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					15	25		
t _{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output		20	36	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					16	29		
t _{PLH}	0 thru 7	EO	Out-of-phase output		7.0	18	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					25	40		
t _{PLH}	0 thru 7	GS	In-phase output		35	55	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					9.0	21		
t _{PLH}	EI	A0, A1, or A2	In-phase output		16	25	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					12	25		
t _{PLH}	EI	GS	In-phase output		12	17	ns	$C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t _{PHL}					14	36		
t _{PLH}	EI	EO	In-phase output		12	21	ns	(LS148) (LS748)
t _{PHL}					28	40		
					30	45		