

**MOTOROLA**

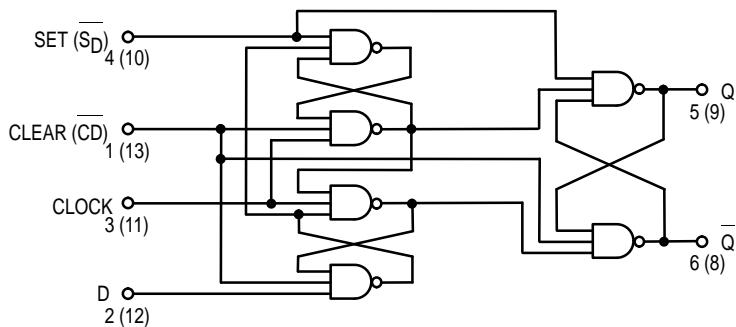
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and \bar{Q} outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

SN54/74LS74A

**DUAL D-TYPE POSITIVE
EDGE-TRIGGERED FLIP-FLOP**
LOW POWER SCHOTTKY

LOGIC DIAGRAM (Each Flip-Flop)**MODE SELECT — TRUTH TABLE**

OPERATING MODE	INPUTS			OUTPUTS	
	SD	SD	D	Q	\bar{Q}
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

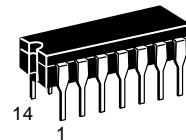
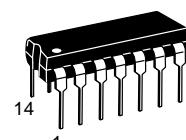
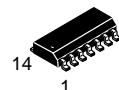
* Both outputs will be HIGH while both SD and CD are LOW, but the output states are unpredictable if SD and CD go HIGH simultaneously. If the levels at the set and clear are near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH} .

H, h = HIGH Voltage Level

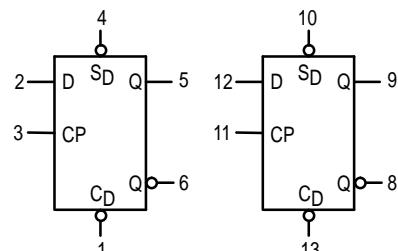
L, l = LOW Voltage Level

X = Don't Care

i, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

**J SUFFIX
CERAMIC
CASE 632-08****N SUFFIX
PLASTIC
CASE 646-06****D SUFFIX
SOIC
CASE 751A-02****ORDERING INFORMATION**

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

LOGIC SYMBOL

V_{CC} = PIN 14
GND = PIN 7

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GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5			
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input High Current Data, Clock Set, Clear			20 40	µA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Data, Clock Set, Clear			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Data, Clock Set, Clear			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Output Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			8.0	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

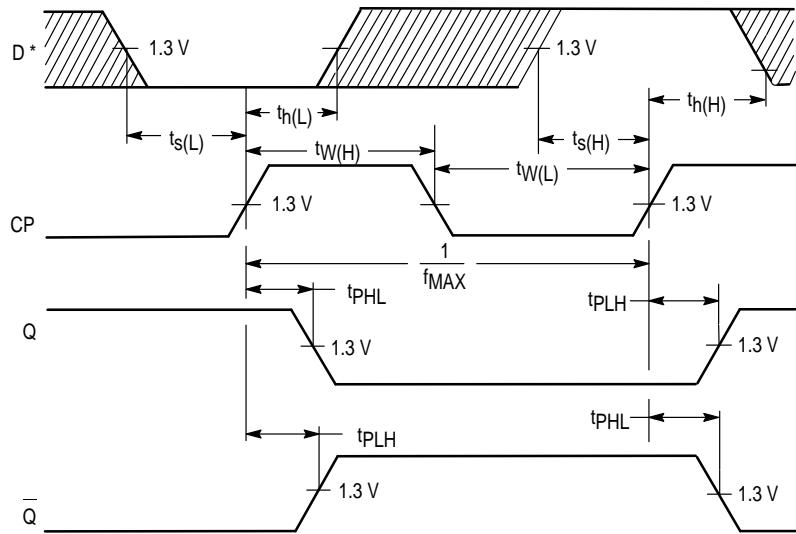
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	33		MHz	Figure 1
t _{PLH} t _{PHL}	Clock, Clear, Set to Output		13	25	ns	Figure 1
			25	40	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{W(H)}	Clock	25			ns	Figure 1
t _{W(L)}	Clear, Set	25			ns	Figure 2
t _s	Data Setup Time — HIGH LOW	20			ns	Figure 1
		20			ns	
t _h	Hold Time	5.0			ns	Figure 1

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AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width

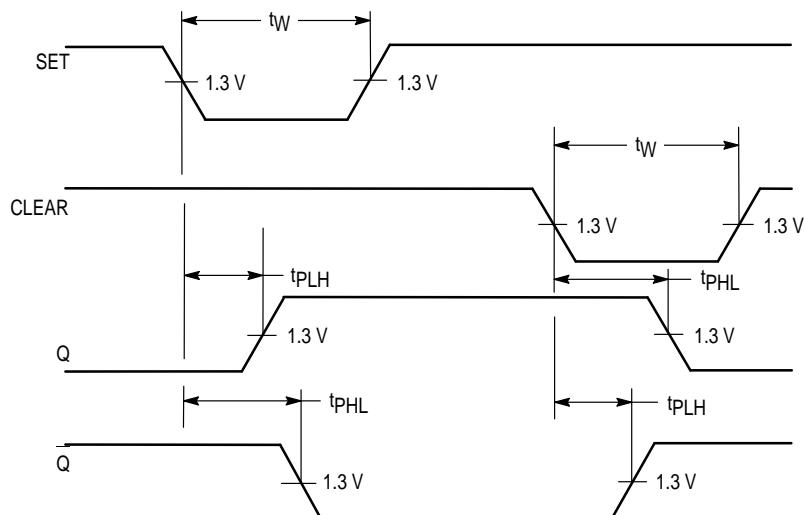


Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths