

# DATA SHEET

## **74LVC245A/74LVCH245A**

Octal bus transceiver with direction pin  
with 5-volt tolerant inputs/outputs  
(3-State)

Product specification  
Supersedes data of 1997 Dec 19  
IC24 Data Handbook

1998 May 20

# Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

# 74LVC245A 74LVCH245A

## FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when  $V_{CC} = 0V$
- Bushold on all data inputs (74LVCH245A only)

## DESCRIPTION

The 74LVC245A/74LVCH245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC245A/74LVCH245A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The '245' features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) input for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated.

The '245' is functionally identical to the '640', but the '640' has true (non-inverting) outputs.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	$C_L = 50pF$ $V_{CC} = 3.3V$	3.6	ns
$C_I$	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10.0	pF
$C_{PD}$	Power dissipation capacitance per buffer	Notes 1 and 2	33	pF

### NOTE:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
2. The condition is  $V_I = GND$  to  $V_{CC}$

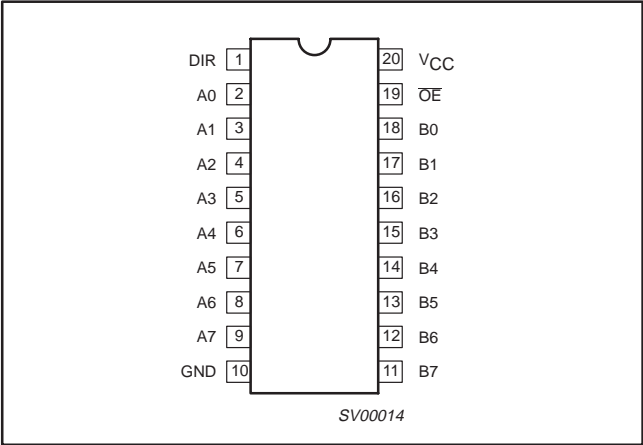
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	-40°C to +85°C	74LVC245A D	74LVC245A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to +85°C	74LVC245A DB	74LVC245A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to +85°C	74LVC245A PW	7LVC245APW DH	SOT360-1
20-Pin Plastic Shrink Small Outline (SO)	-40°C to +85°C	74LVCH245A D	74LVCH245A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to +85°C	74LVCH245A DB	74LVCH245A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to +85°C	74LVCH245A PW	LVCH245APW DH	SOT360-1

Octal bus transceiver with direction pin with  
5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

PIN CONFIGURATION



PIN DESCRIPTION

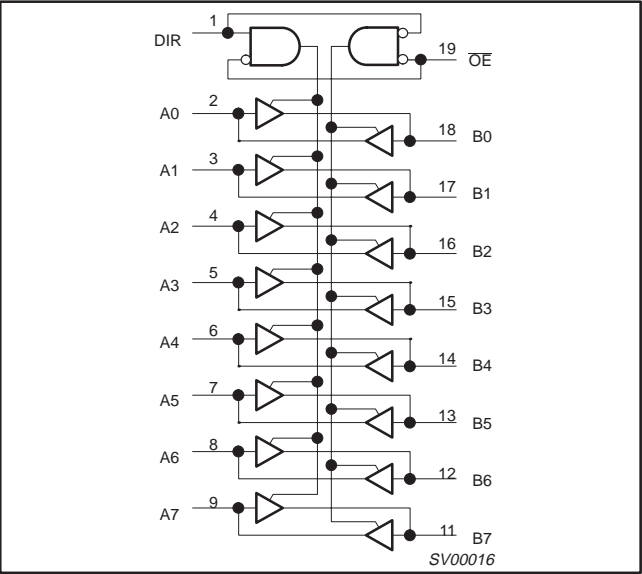
PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	Data inputs/outputs
19	$\overline{OE}$	Output enable input (active-Low)
20	V <sub>CC</sub>	Positive supply voltage

FUNCTION TABLE

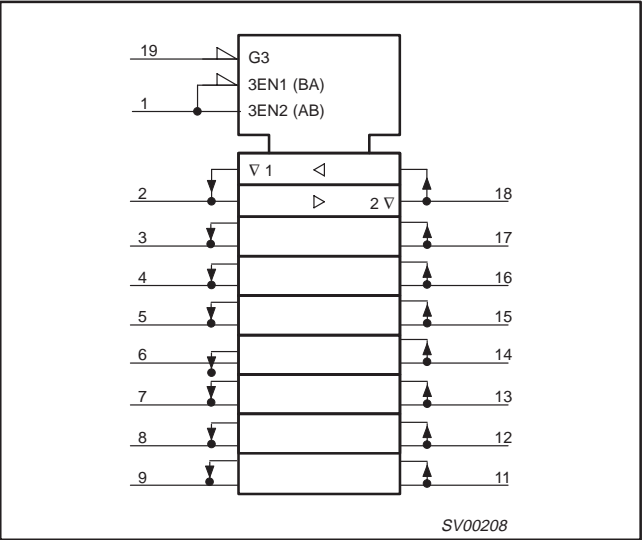
INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A <sub>n</sub>	B <sub>0</sub>
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level  
L = LOW voltage level  
X = Don't care  
Z = High impedance OFF-state

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



# Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
$V_I$	DC Input voltage range		0	5.5	V
$V_O$	DC Output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
	DC output voltage range; output 3-State		0	5.5	
$T_{amb}$	Operating ambient temperature range in free-air		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	Note 2	-0.5 to +6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
$V_O$	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	± 50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		± 100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package			mW
	– plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA			0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current <sup>6</sup>	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		± 0.1	± 5	μA
I <sub>OZ</sub>	3-State output OFF-state current <sup>6, 7</sup>	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	± 5	μA
I <sub>off</sub>	Power off leakage supply	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	± 10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	10	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA
I <sub>BHL</sub>	Bushold LOW sustaining current <sup>2, 3, 4</sup>	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V	75	—	—	μA
I <sub>BHH</sub>	Bushold HIGH sustaining current <sup>2, 3, 4</sup>	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V	-75	—	—	μA
I <sub>BHLO</sub>	Bushold LOW overdrive current <sup>2, 3, 5</sup>	V <sub>CC</sub> = 3.6V	500	—	—	μA
I <sub>BHHO</sub>	Bushold HIGH overdrive current <sup>2, 3, 5</sup>	V <sub>CC</sub> = 3.6V	-500	—	—	μA

### NOTES:

1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .
2. Valid for data inputs of bushold parts (LVCH-A) only.
3. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data input holds the input below the specified  $V_I$  level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bushold parts, the bushold circuit is switched off when  $V_I$  exceeds  $V_{CC}$  allowing 5.5V on the input terminal.
7. For I/O ports the parameter  $I_{OZ}$  includes the input leakage current.

Octal bus transceiver with direction pin with  
5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

AC CHARACTERISTICS

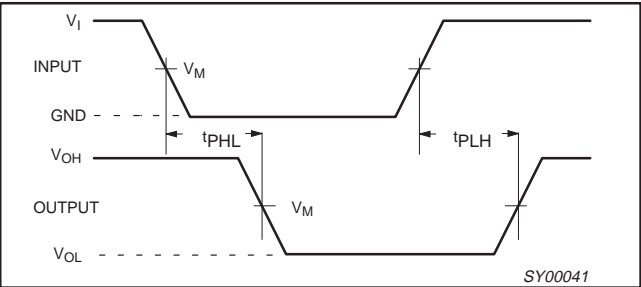
GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			$V_{CC} = 2.7\text{V}$		$V_{CC} = 1.2\text{V}$	
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	TYP	
$t_{\text{PHL}}$ $t_{\text{PLH}}$	Propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	1, 3	1.5	3.6	6.3	1.5	7.3	16	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	3-State output enable time $\text{OE}$ to $A_n$ ; $\text{OE}$ to $B_n$	2, 3	1.5	5.1	8.5	1.5	9.5	23	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	3-State output disable time $\text{OE}$ to $A_n$ ; $\text{OE}$ to $B_n$	2, 3	1.5	4.5	7.0	1.5	8.0	16	ns

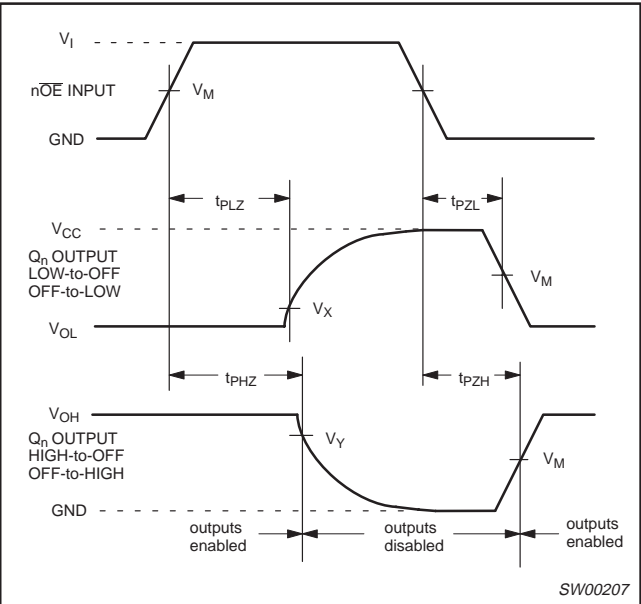
**NOTE:**  
1. Unless otherwise stated, all typical values are at  $V_{CC} = 3.3\text{V}$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

AC WAVEFORMS

$V_M = 1.5\text{V}$  at  $V_{CC} \geq 2.7\text{V}$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7\text{V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3\text{V}$  at  $V_{CC} \geq 2.7\text{V}$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7\text{V}$   
 $V_Y = V_{OH} - 0.3\text{V}$  at  $V_{CC} \geq 2.7\text{V}$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7\text{V}$

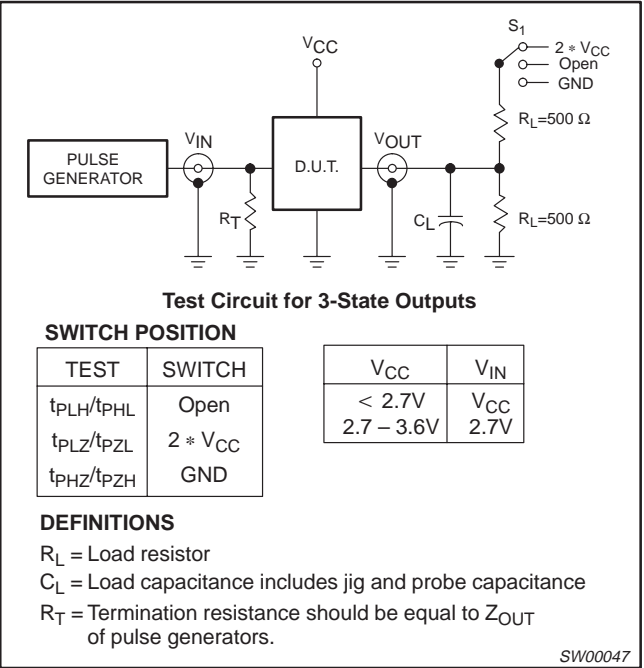


Waveform 1. Input ( $D_n$ ) to output ( $Q_n$ ) propagation delays.



Waveform 2. 3-State enable and disable times.

TEST CIRCUIT



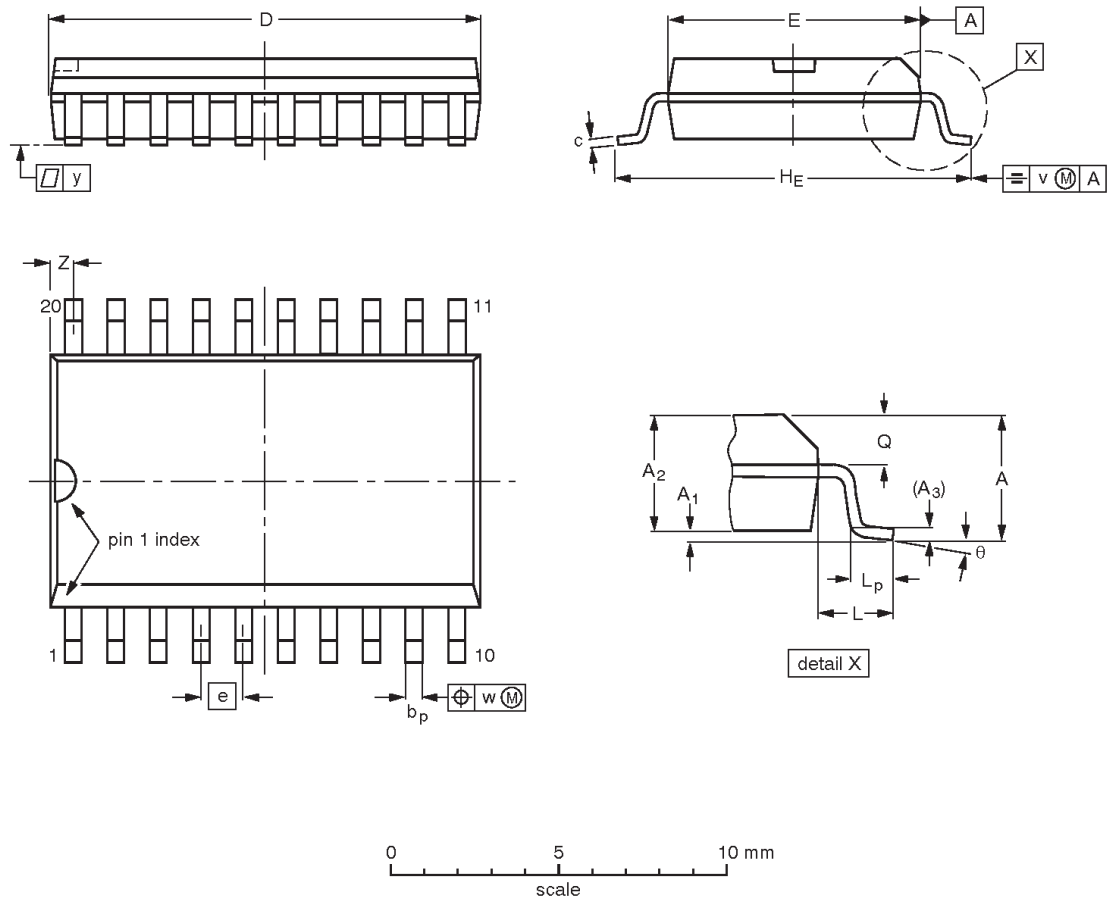
Waveform 3. Load circuitry for switching times.

Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**  
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

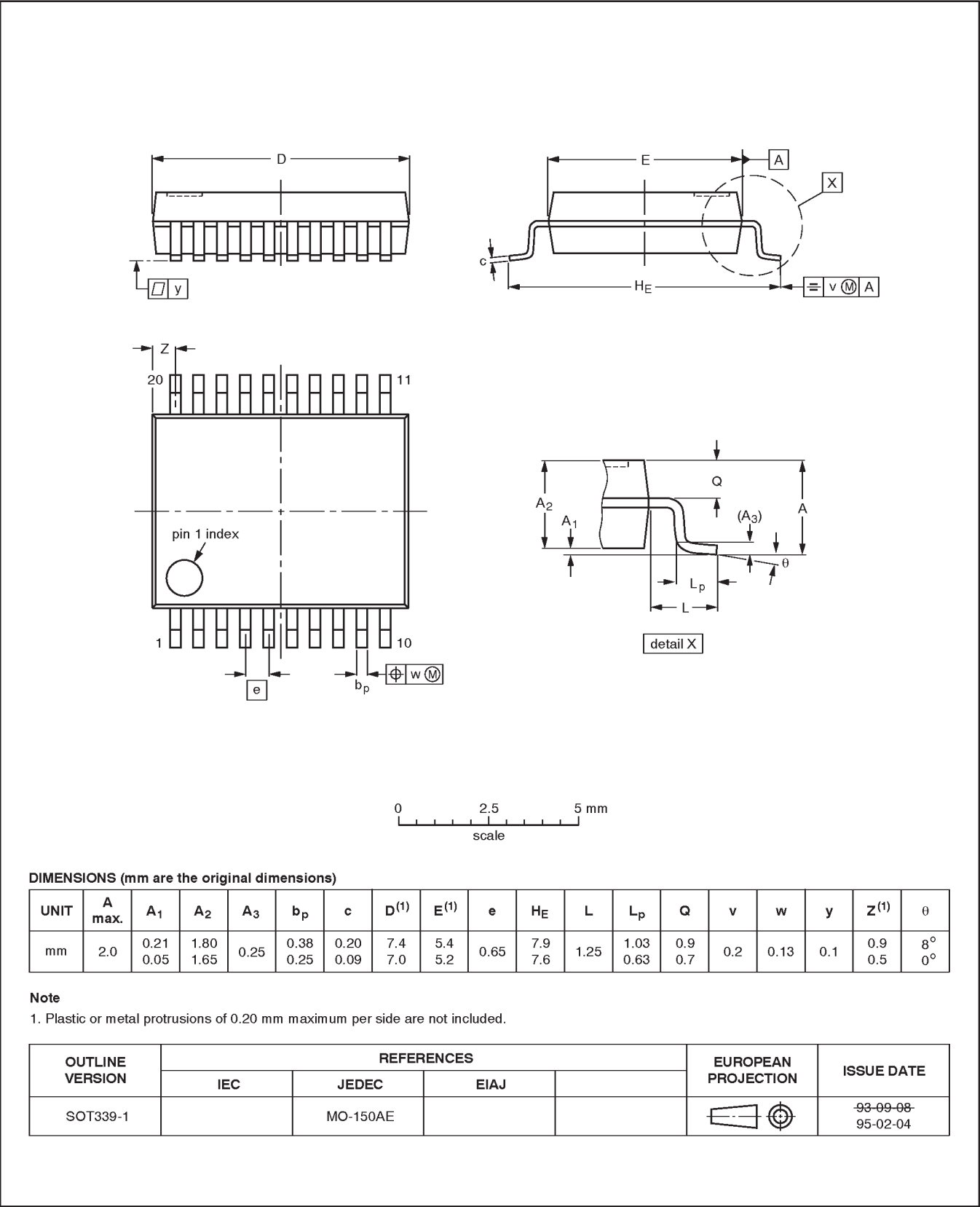
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

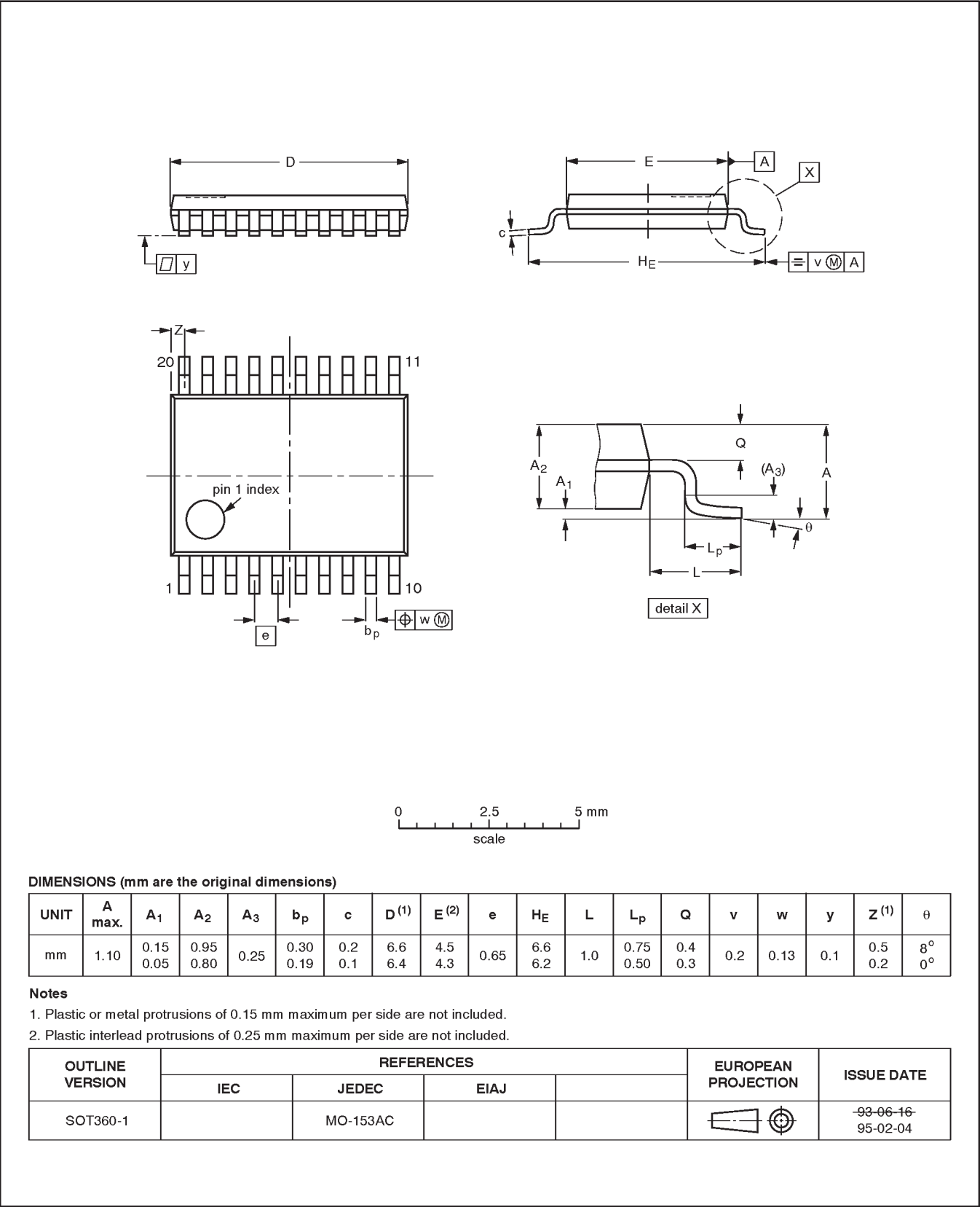


Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



# Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A  
74LVCH245A

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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