

74HC123; 74HCT123

Dual retriggerable monostable multivibrator with reset

Rev. 8 — 16 December 2011

Product data sheet

1. General description

The 74HC123; 74HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC123; 74HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\bar{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period ($nQ = \text{HIGH}$, $n\bar{Q} = \text{LOW}$) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input nRD , which also inhibits the triggering.
3. An internal connection from nRD to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input $n\bar{RD}$ as shown in the function table.

Schmitt-trigger action in the $n\bar{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The 74HC123; 74HCT123 are identical to the 74HC423; 74HCT423 but can be triggered via the reset input.

2. Features and benefits

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40°C to $+85^{\circ}\text{C}$ and from -40°C to $+125^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

| Type number | Package | Temperature range | Name | Description | Version |
|-------------|---------|-------------------|----------|--------------------------------------------------------------------------------------------------------------------------------|----------|
| 74HC123N | | −40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HCT123N | | | | | |
| 74HC123D | | −40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT123D | | | | | |
| 74HC123DB | | −40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT123DB | | | | | |
| 74HC123PW | | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT123PW | | | | | |
| 74HC123BQ | | −40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

4. Functional diagram

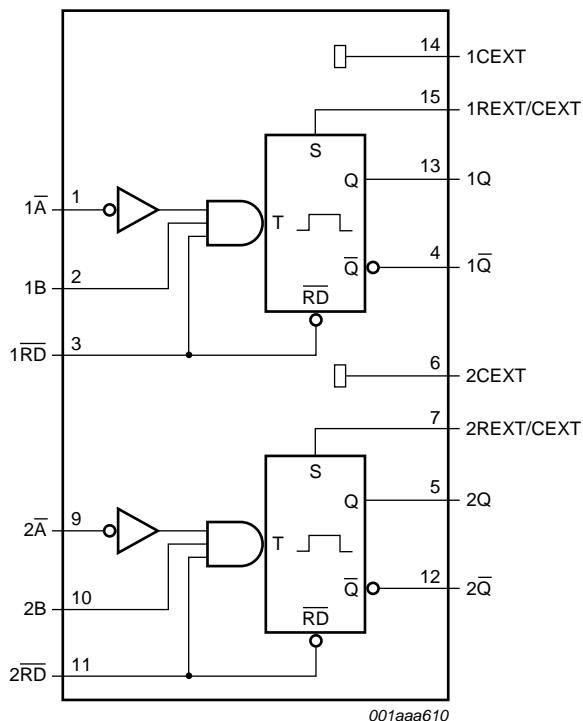


Fig 1. Functional diagram

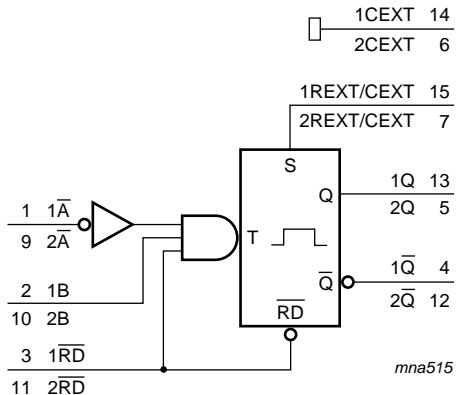


Fig 2. Logic symbol

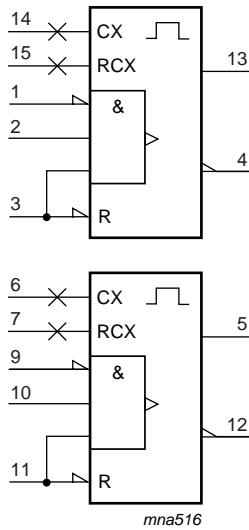


Fig 3. IEC logic symbol

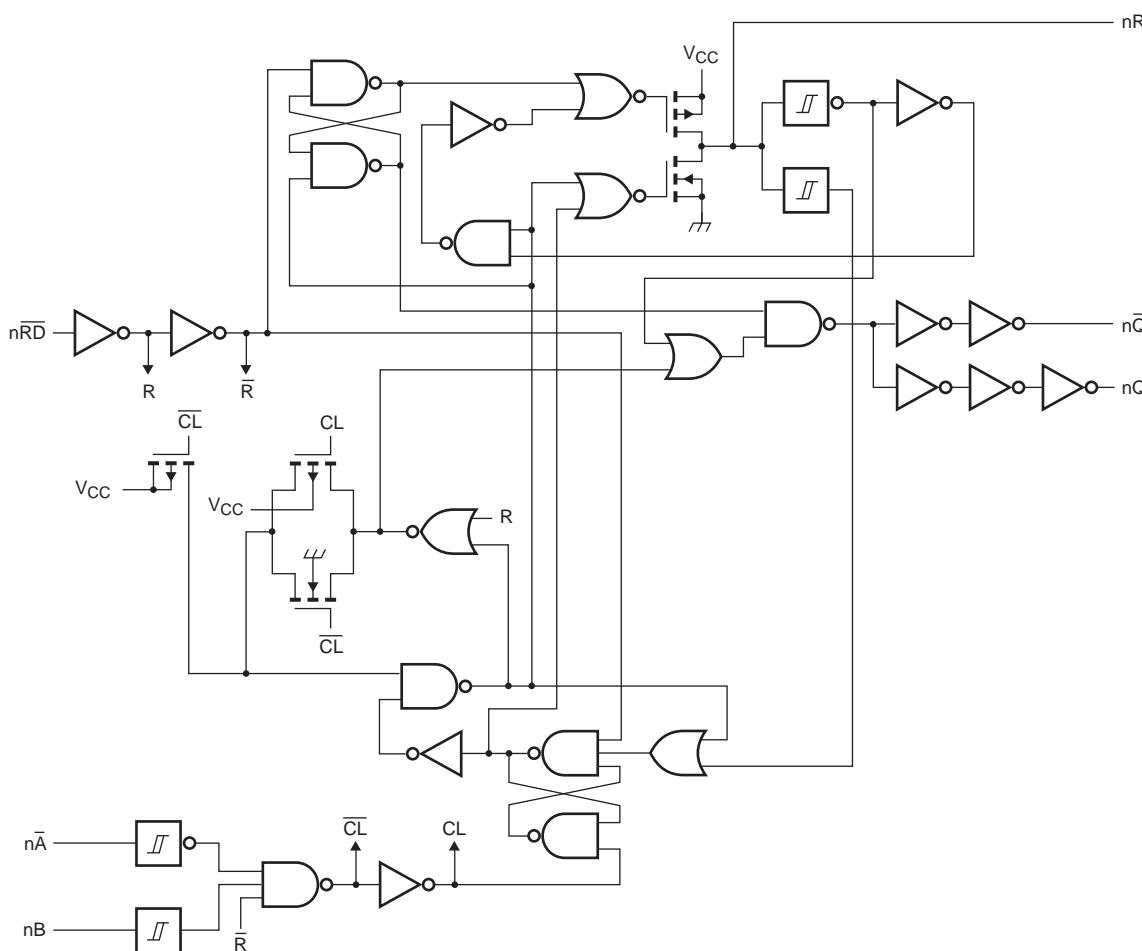


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

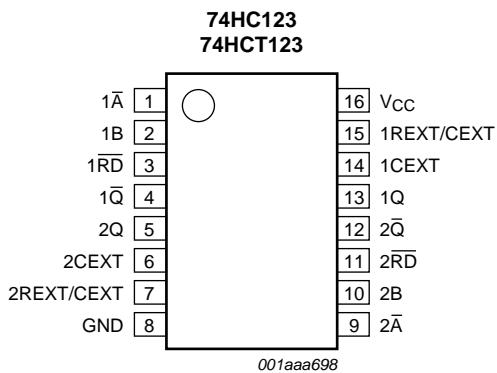
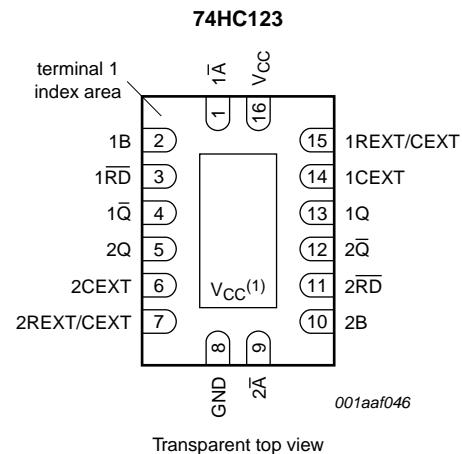


Fig 5. Pin configuration for DIP16, SO16, SSOP16 and TSSOP16



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input.

Fig 6. Pin configuration for DHVQFN16

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|-----|------------------------------------------------------|
| 1A | 1 | negative-edge triggered input 1 |
| 1B | 2 | positive-edge triggered input 1 |
| 1RD | 3 | direct reset LOW and positive-edge triggered input 1 |
| 1Q | 4 | active LOW output 1 |
| 2Q | 5 | active HIGH output 2 |
| 2CEXT | 6 | external capacitor connection 2 |
| 2REXT/CEXT | 7 | external resistor and capacitor connection 2 |
| GND | 8 | ground (0 V) |
| 2A | 9 | negative-edge triggered input 2 |
| 2B | 10 | positive-edge triggered input 2 |
| 2RD | 11 | direct reset LOW and positive-edge triggered input 2 |
| 2Q | 12 | active LOW output 2 |
| 1Q | 13 | active HIGH output 1 |
| 1CEXT | 14 | external capacitor connection 1 |
| 1REXT/CEXT | 15 | external resistor and capacitor connection 1 |
| V _{CC} | 16 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | | Output | |
|-------|----|----|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|
| nRD | nA | nB | nQ | nQ̄ |
| L | X | X | L | H |
| X | H | X |  [2] |  H[2] |
| X | X | L |  [2] |  H[2] |
| H | L | ↑ |  |  |
| H | ↓ | H |  |  |
| ↑ | L | H |  |  |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;

 = one HIGH level output pulse;  = one LOW level output pulse.

[2] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-------------------------------------------------------------------------------------|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | - | ±20 | mA |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V | - | ±20 | mA |
| I _O | output current | except for pins nREXT/CEXT; V _O = -0.5 V to (V _{CC} + 0.5 V) | - | ±25 | mA |
| I _{CC} | supply current | | - | 50 | mA |
| I _{GND} | ground current | | - | -50 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | | | | |
| | DIP16 package | ^[1] - | 750 | mW | |
| | SO16 package | ^[2] - | 500 | mW | |
| | SSOP16 package | ^[3] - | 500 | mW | |
| | TSSOP16 package | ^[3] - | 500 | mW | |
| | DHVQFN16 package | ^[4] - | 500 | mW | |

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | 74HC123 | | | 74HCT123 | | | Unit |
|---------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| $\Delta t/\Delta V$ | input transition rise and fall rate | nRD input | | | | | | | |
| | | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| T _{amb} | ambient temperature | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |
| | | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| | | | | | | | | | |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|-----------------|---------------------------|----------------------------------------------------------------------------------------|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC123 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = −20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = −20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = −20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = −4 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | I _O = −5.2 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT123 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = −20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| I _I | input leakage current | I _O = 4.0 mA | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | per input pin; I _O = 0 A; V _I = V _{CC} − 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | pins nA, nB | - | 35 | 125 | - | 160 | - | 170 | μA |
| C _I | input capacitance | pin nRD | - | 50 | 180 | - | 225 | - | 245 | μA |
| | | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|----------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC123 | | | | | | | | | | |
| t_{pd} | propagation delay | $n\overline{RD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; [1] $C_{EXT} = 0 \text{ pF}$; $R_{EXT} = 5 \text{ k}\Omega$; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | - | 83 | 255 | - | 320 | - | 385 | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 30 | 51 | - | 64 | - | 77 | ns |
| | | $V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 26 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 24 | 43 | - | 54 | - | 65 | ns |
| | | $n\overline{RD}$ (reset) to nQ or $n\overline{Q}$; $C_{EXT} = 0 \text{ pF}$; $R_{EXT} = 5 \text{ k}\Omega$; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | - | 66 | 215 | - | 270 | - | 325 | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 24 | 43 | - | 54 | - | 65 | ns |
| | | $V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 20 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 19 | 37 | - | 46 | - | 55 | ns |
| t_t | transition time | see Figure 9 [1] | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 6 | 13 | - | 16 | - | 19 | ns |
| t_w | pulse width | $n\overline{A}$ LOW; see Figure 10 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | 100 | 8 | - | 125 | - | 150 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | 20 | 3 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | 17 | 2 | - | 21 | - | 26 | - | ns |
| | | nB HIGH; see Figure 10 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | 100 | 17 | - | 125 | - | 150 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | 20 | 6 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | 17 | 5 | - | 21 | - | 26 | - | ns |
| | | $n\overline{RD}$ LOW; see Figure 11 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | 100 | 14 | - | 125 | - | 150 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | 20 | 5 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | 17 | 4 | - | 21 | - | 26 | - | ns |
| | | nQ HIGH and $n\overline{Q}$ LOW; [2] $V_{CC} = 5.0 \text{ V}$; see Figure 10 and 11 | | | | | | | | |
| | | $C_{EXT} = 100 \text{ nF}; R_{EXT} = 10 \text{ k}\Omega$ | - | 450 | - | - | - | - | - | μs |
| | | $C_{EXT} = 0 \text{ pF}; R_{EXT} = 5 \text{ k}\Omega$ | - | 75 | - | - | - | - | - | ns |

Table 7. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|-------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|------|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_{trig} | retrigger time | $n\bar{A}, nB; C_{\text{EXT}} = 0 \text{ pF};$ $R_{\text{EXT}} = 5 \text{ k}\Omega; V_{\text{CC}} = 5.0 \text{ V};$ see Figure 10 | [3][4] | - | 110 | - | - | - | - | ns |
| R_{EXT} | external timing resistor | see Figure 7 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 10 | - | 1000 | - | - | - | - | kΩ |
| C_{EXT} | external timing capacitor | $V_{\text{CC}} = 5.0 \text{ V};$ see Figure 7 | [4] | - | - | - | - | - | - | pF |
| | | per monostable; $V_I = \text{GND to } V_{\text{CC}}$ | [5] | - | 54 | - | - | - | - | pF |

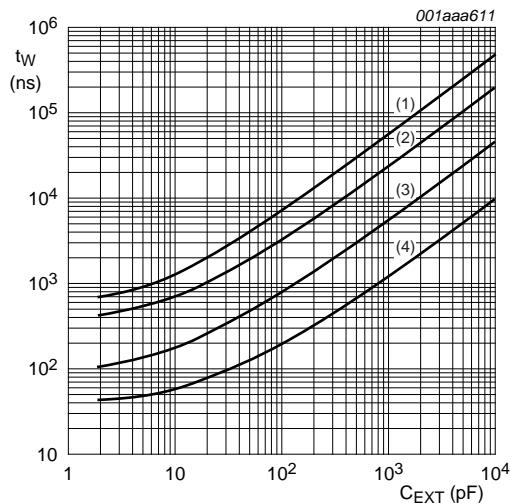
74HCT123

| | | | | | | | | | | | |
|------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----|----|----|----|----|----|----|----|
| t_{PHL} | HIGH to LOW propagation delay | $n\bar{D}, n\bar{A}, nB$ to nQ or $n\bar{Q}$; $C_{\text{EXT}} = 0 \text{ pF}; R_{\text{EXT}} = 5 \text{ k}\Omega;$ see Figure 9 | | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 30 | 51 | - | 64 | - | 77 | ns | |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 26 | - | - | - | - | - | ns | |
| | | $n\bar{D}$ (reset) to nQ or $n\bar{Q}$; $C_{\text{EXT}} = 0 \text{ pF};$ $R_{\text{EXT}} = 5 \text{ k}\Omega;$ see Figure 9 | | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 27 | 46 | - | 58 | - | 69 | ns | |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 23 | - | - | - | - | - | ns | |
| t_{PLH} | LOW to HIGH propagation delay | $n\bar{D}, n\bar{A}, nB$ to nQ or $n\bar{Q}$; $C_{\text{EXT}} = 0 \text{ pF};$ $R_{\text{EXT}} = 5 \text{ k}\Omega;$ see Figure 9 | | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 28 | 51 | - | 64 | - | 77 | ns | |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 26 | - | - | - | - | - | ns | |
| | | $n\bar{D}$ (reset) to nQ or $n\bar{Q}$; $C_{\text{EXT}} = 0 \text{ pF}; R_{\text{EXT}} = 5 \text{ k}\Omega;$ see Figure 9 | | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 23 | 46 | - | 58 | - | 69 | ns | |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 23 | - | - | - | - | - | ns | |
| t_t | transition time | $V_{\text{CC}} = 4.5 \text{ V};$ see Figure 9 | [1] | - | 7 | 15 | - | 19 | - | 22 | ns |

Table 7. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----|------|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_W | pulse width | $V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | | $n\bar{A}$ LOW; see Figure 10 | 20 | 3 | - | 25 | - | 30 | - | ns |
| | | nB HIGH; see Figure 10 | 20 | 5 | - | 25 | - | 30 | - | ns |
| | | $n\bar{R}\bar{D}$ LOW; see Figure 11 | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | nQ HIGH and \bar{nQ} LOW; [2] $V_{CC} = 5.0 \text{ V}$; see Figure 10 and 11 | | | | | | | | |
| | | $C_{EXT} = 100 \text{ nF};$ $R_{EXT} = 10 \text{ k}\Omega$ | | - | 450 | - | - | - | - | μs |
| | | $C_{EXT} = 0 \text{ pF};$ $R_{EXT} = 5 \text{ k}\Omega$ | | - | 75 | - | - | - | - | ns |
| t_{trig} | retrigger time | $n\bar{A}, nB; C_{EXT} = 0 \text{ pF};$ $R_{EXT} = 5 \text{ k}\Omega; V_{CC} = 5.0 \text{ V};$ see Figure 10 | [3][4] | - | 110 | - | - | - | - | ns |
| R_{EXT} | external timing resistor | $V_{CC} = 5.0 \text{ V}$; see Figure 7 | 2 | - | 1000 | - | - | - | - | kΩ |
| C_{EXT} | external timing capacitor | $V_{CC} = 5.0 \text{ V}$; see Figure 7 | [4] | - | - | - | - | - | - | pF |
| C_{PD} | power dissipation capacitance | per monostable; $V_I = \text{GND to } V_{CC}$ | [5] | - | 56 | - | - | - | - | pF |

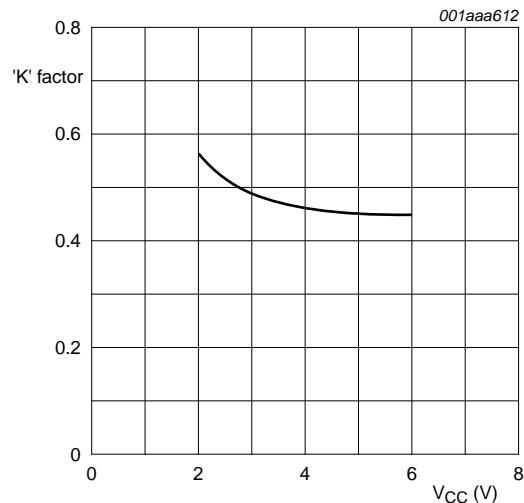
[1] t_{pd} is the same as t_{PHL} and t_{PLH} ; t_t is the same as t_{THL} and t_{TLH} [2] For other R_{EXT} and C_{EXT} combinations see [Figure 7](#). If $C_{EXT} > 10 \text{ nF}$, the next formula is valid. $t_W = K \times R_{EXT} \times C_{EXT}$, where: t_W = typical output pulse width in ns; R_{EXT} = external resistor in kΩ; C_{EXT} = external capacitor in pF; K = constant = 0.45 for $V_{CC} = 5.0 \text{ V}$ and 0.55 for $V_{CC} = 2.0 \text{ V}$.The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.[3] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT} . The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If $C_{EXT} > 10 \text{ pF}$, the next formula (at $V_{CC} = 5.0 \text{ V}$) for the setup time of a retrigger pulse is valid: $t_{trig} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where: t_{trig} = retrigger time in ns; C_{EXT} = external capacitor in pF; R_{EXT} = external resistor in kΩ.The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is 7 pF.[4] When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50 \text{ pF}$.[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where: f_i = input frequency in MHz; f_o = output frequency in MHz; D = duty factor in %; C_L = output load capacitance in pF; V_{CC} = supply voltage in V; C_{EXT} = timing capacitance in pF; $\sum(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.



$V_{CC} = 5.0 \text{ V}; T_{amb} = 25^\circ\text{C}.$

- (1) $R_{EXT} = 100 \text{ k}\Omega$
- (2) $R_{EXT} = 50 \text{ k}\Omega$
- (3) $R_{EXT} = 10 \text{ k}\Omega$
- (4) $R_{EXT} = 2 \text{ k}\Omega$

Fig 7. Typical output pulse width as a function of the external capacitor value

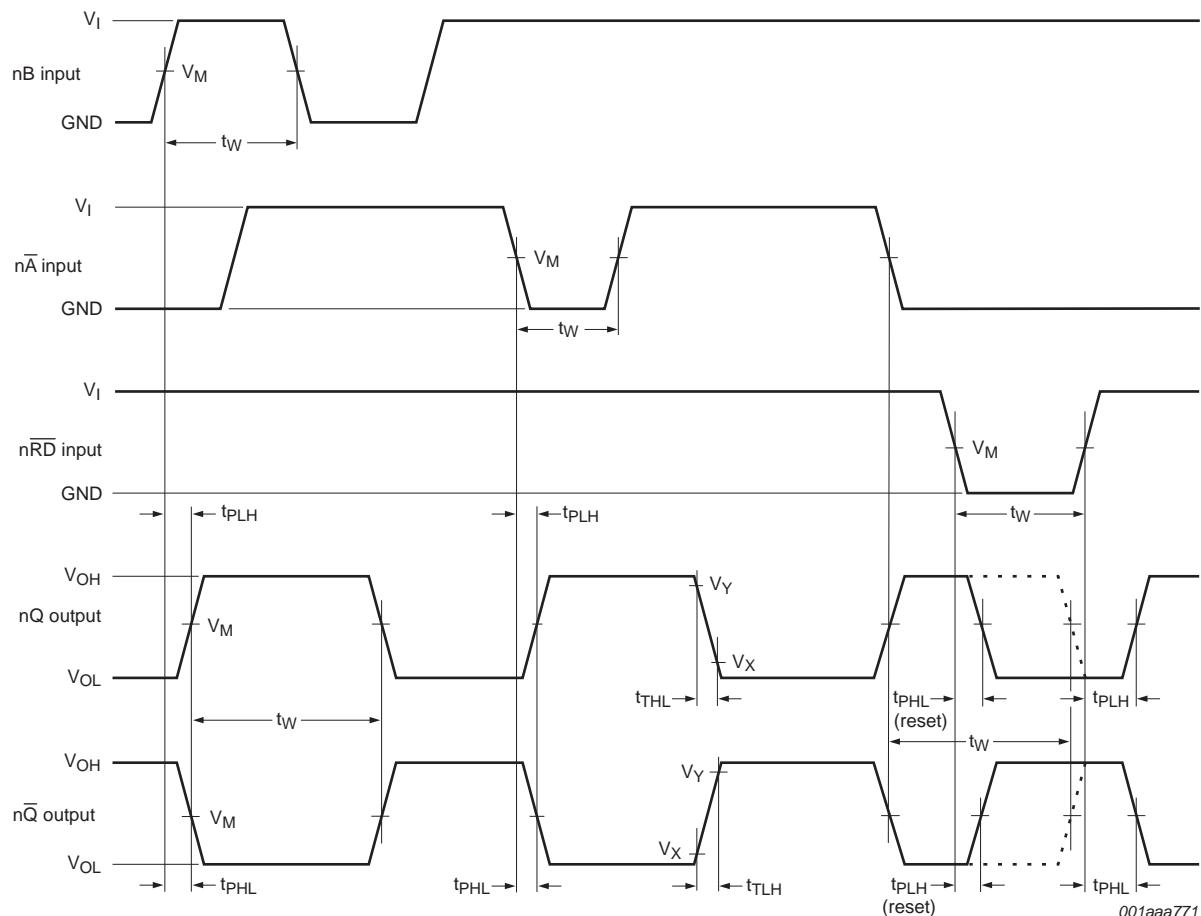


$C_{EXT} = 10 \text{ nF}; R_{EXT} = 10 \text{ k}\Omega \text{ to } 100 \text{ k}\Omega.$

$T_{amb} = 25^\circ\text{C}.$

Fig 8. 74HC123 typical 'K' factor as function of V_{CC}

11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Propagation delays from inputs ($n\bar{A}$, nB , $n\bar{R}\bar{D}$) to outputs (nQ , $n\bar{Q}$) and output transition times

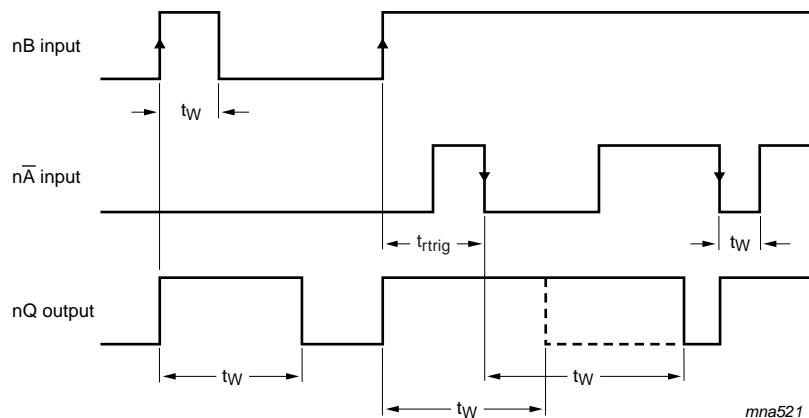


Fig 10. Output pulse control using retrigger pulse

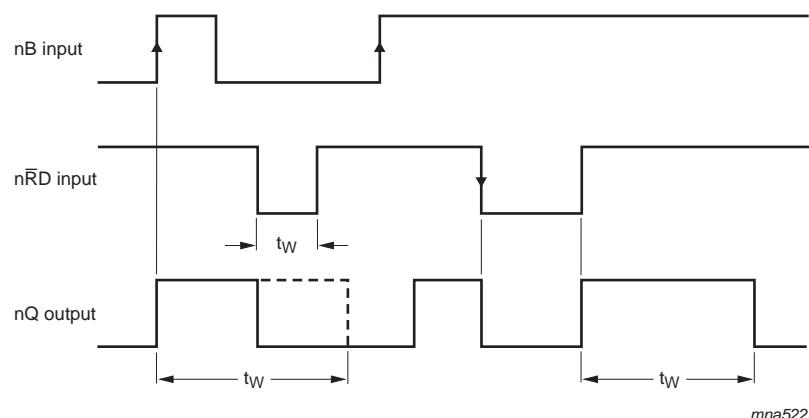
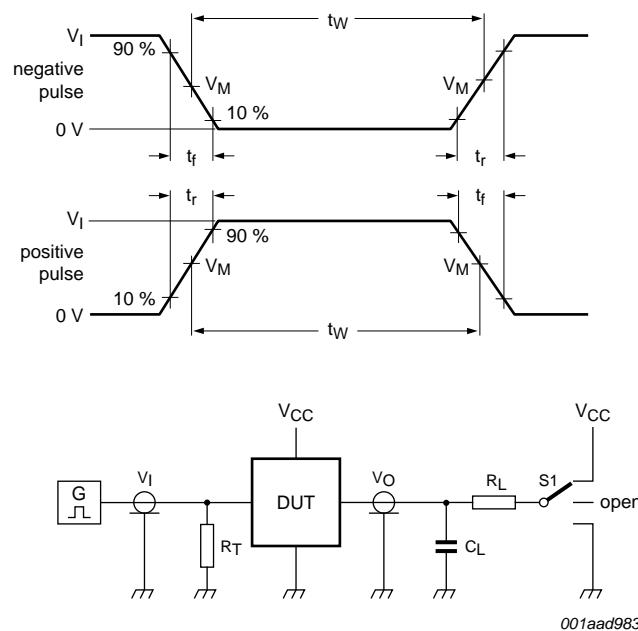


Fig 11. Output pulse control using reset input nRD



Test data is given in [Table 8](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 12. Test circuit for measuring switching times

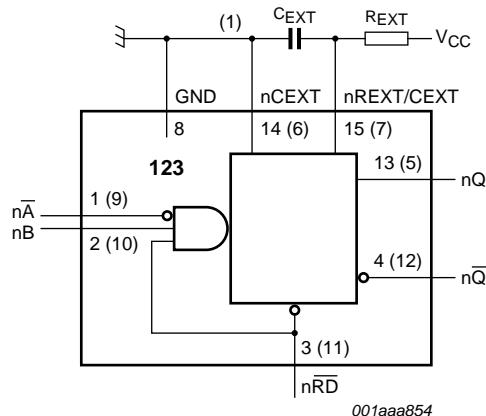
Table 8. Test data

| Type | Input | | Load | | S1 position |
|----------|----------|------------|--------------|--------------|-------------|
| | V_I | t_r, t_f | C_L | R_L | |
| 74HC123 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open |
| 74HCT123 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open |

12. Application information

12.1 Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT} .



- (1) For minimum noise generation it is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

Fig 13. Timing component connections

12.2 Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT} . This output pulse can be eliminated using the circuit shown in [Figure 14](#).

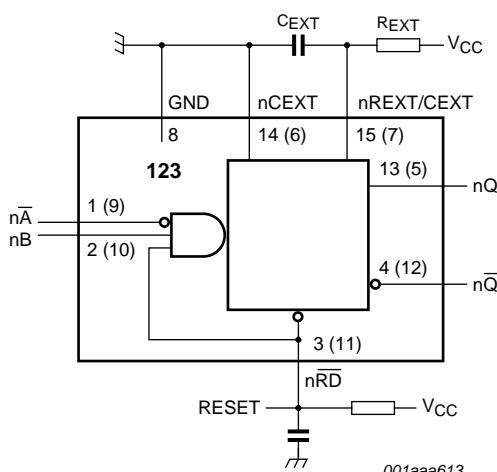
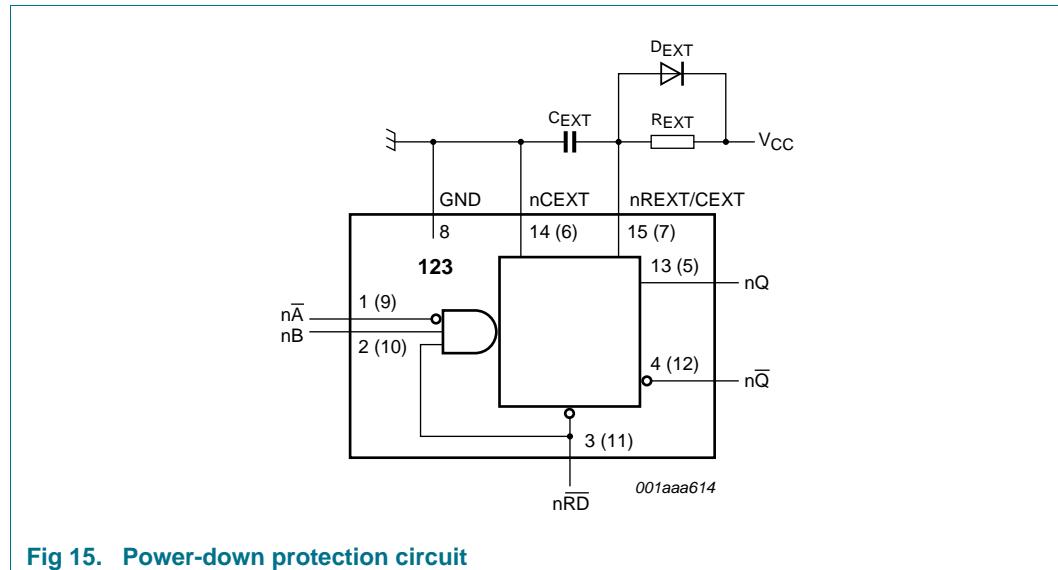


Fig 14. Power-up output pulse elimination circuit

12.3 Power-down considerations

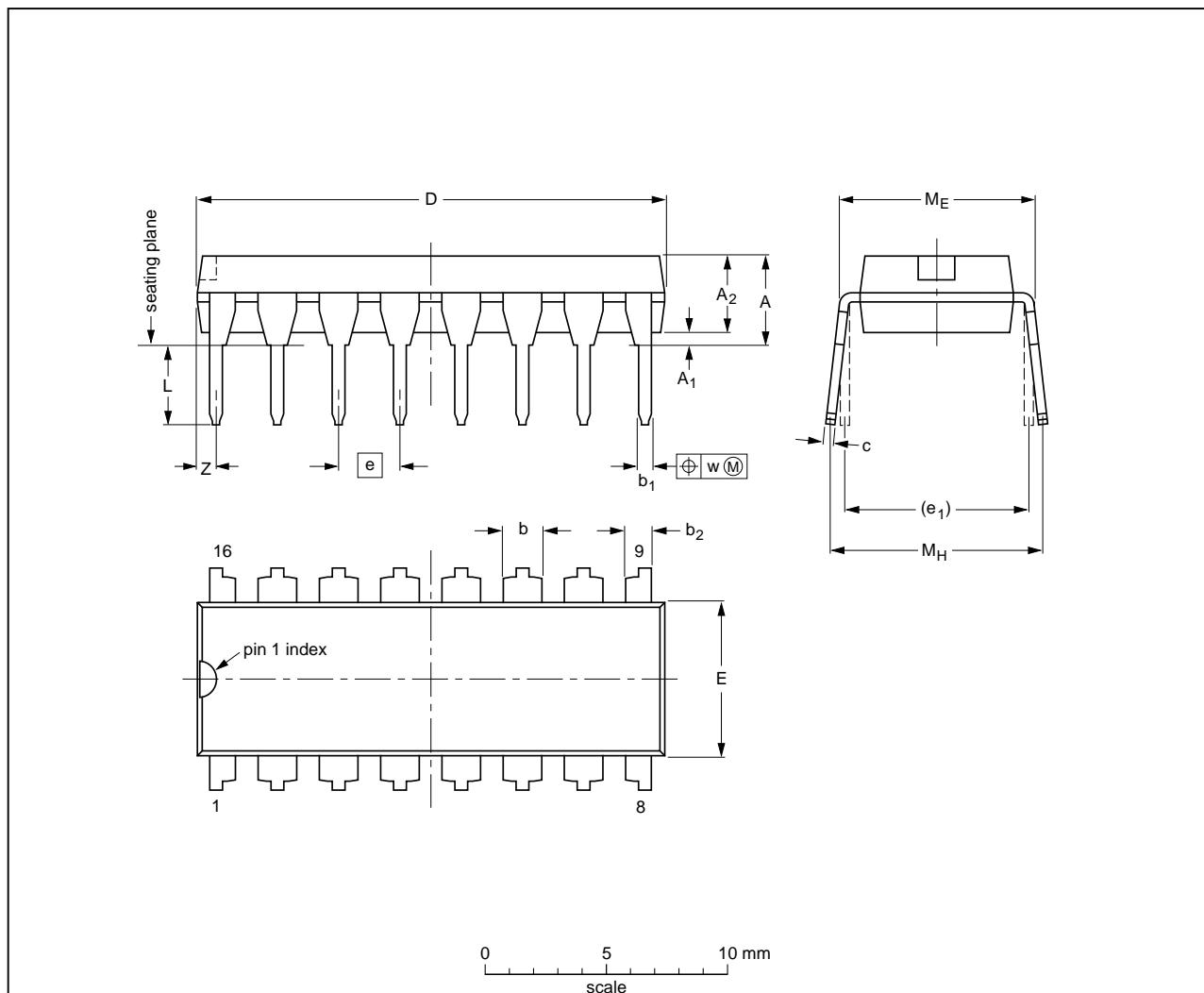
A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Figure 15](#).



13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|-----------|------------------------|------------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|--------------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.1 | 0.3 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.03 |

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|-------|--|------------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | 95-01-14 03-02-13 |

Fig 16. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

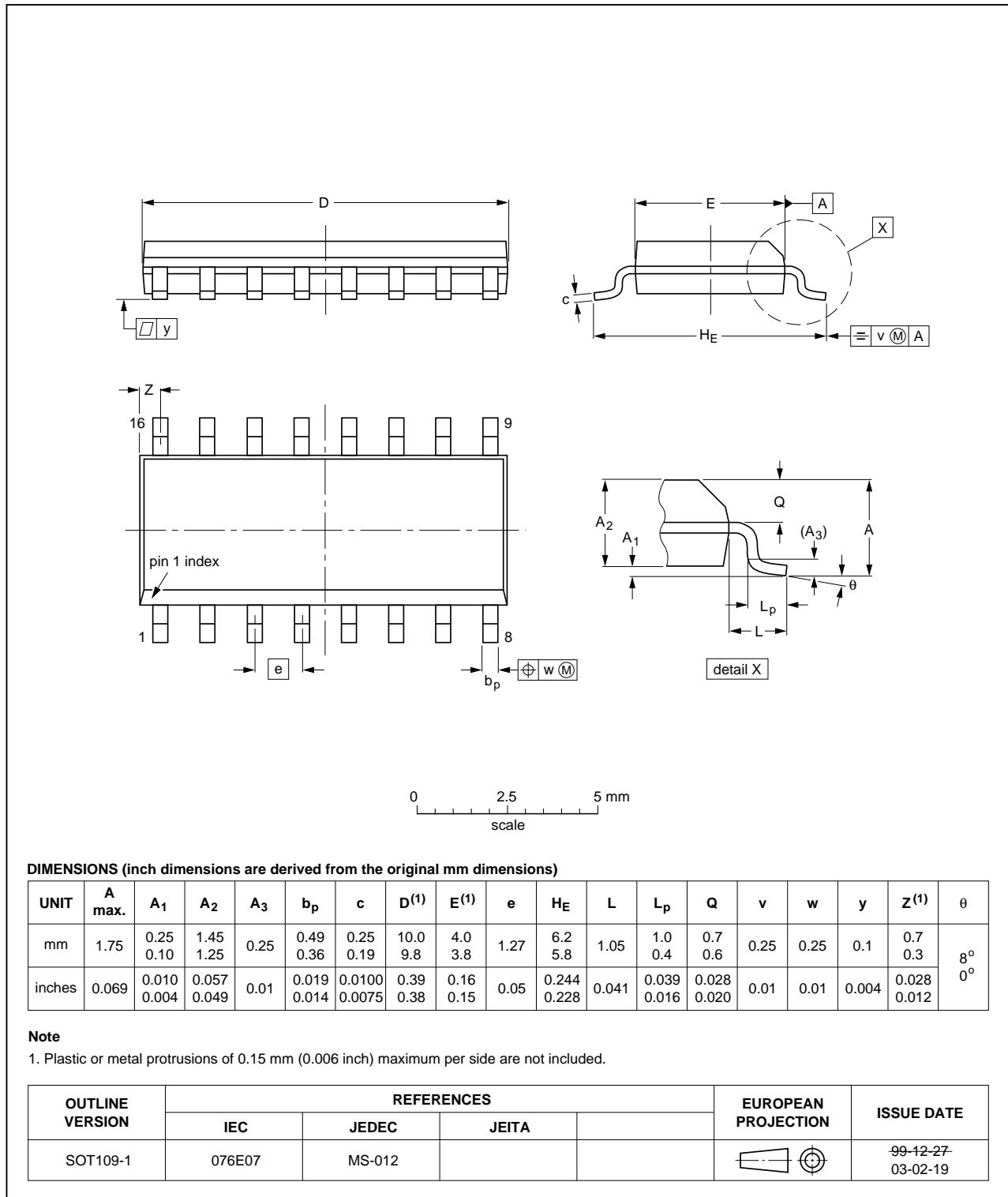


Fig 17. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

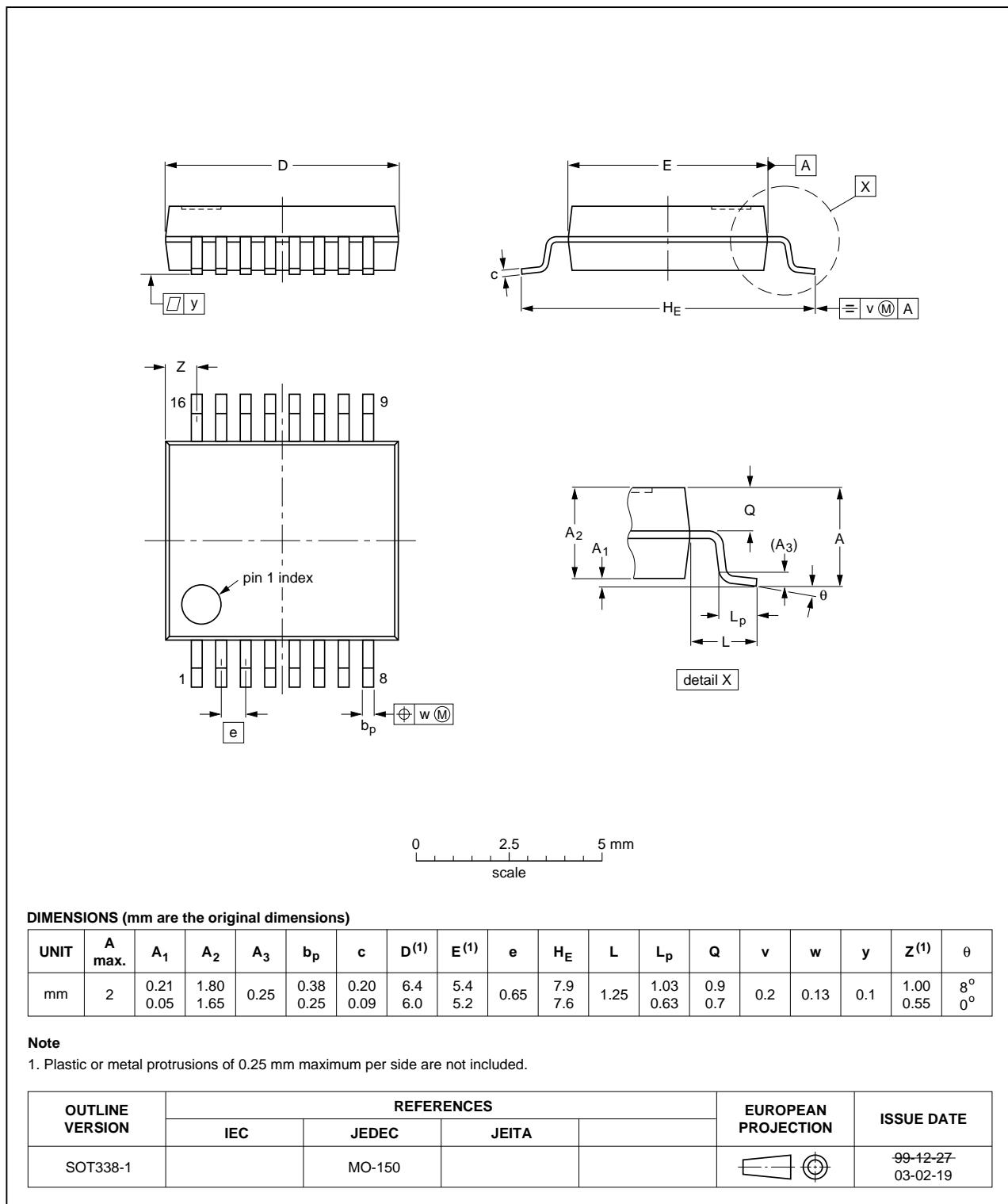


Fig 18. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

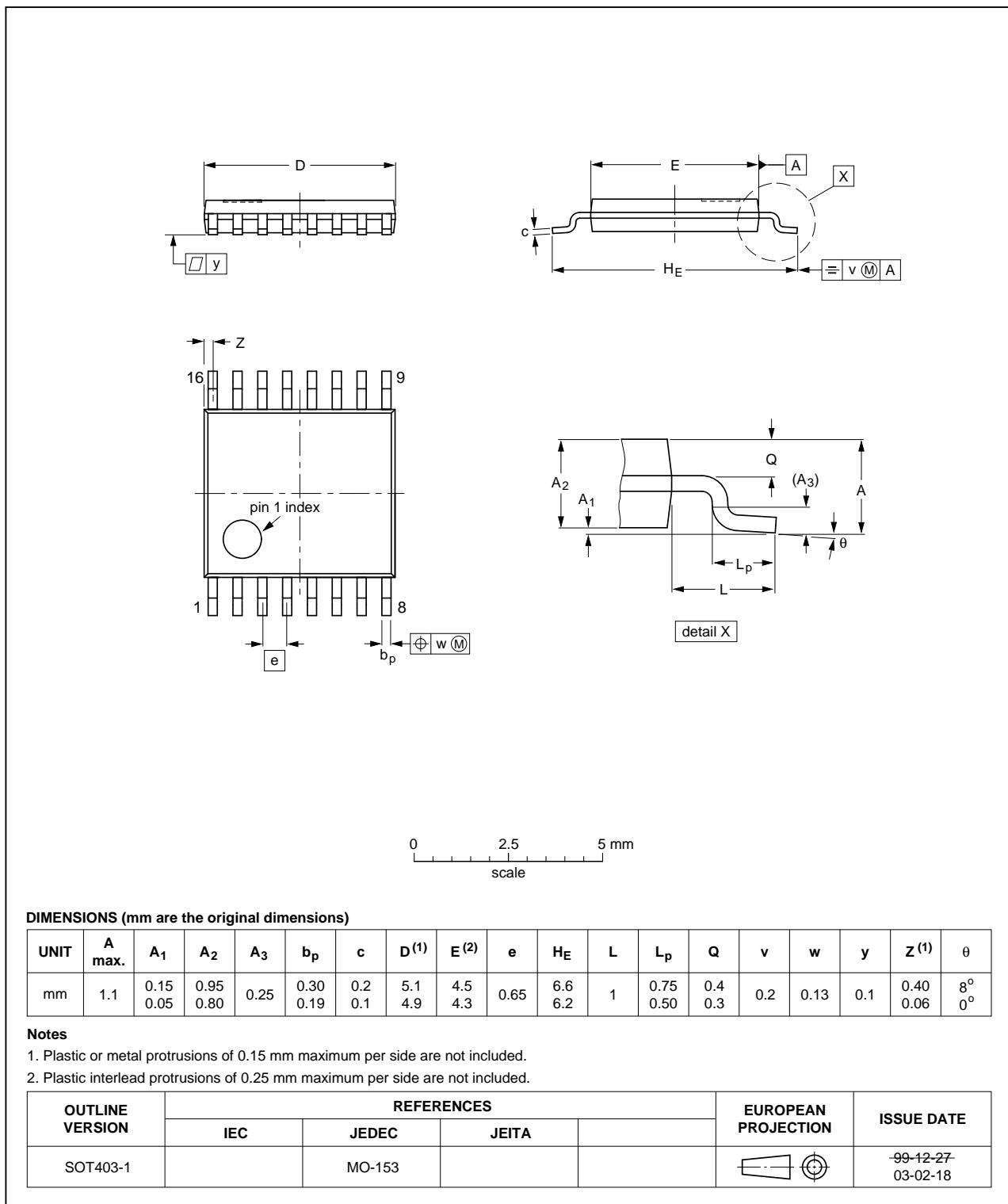


Fig 19. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

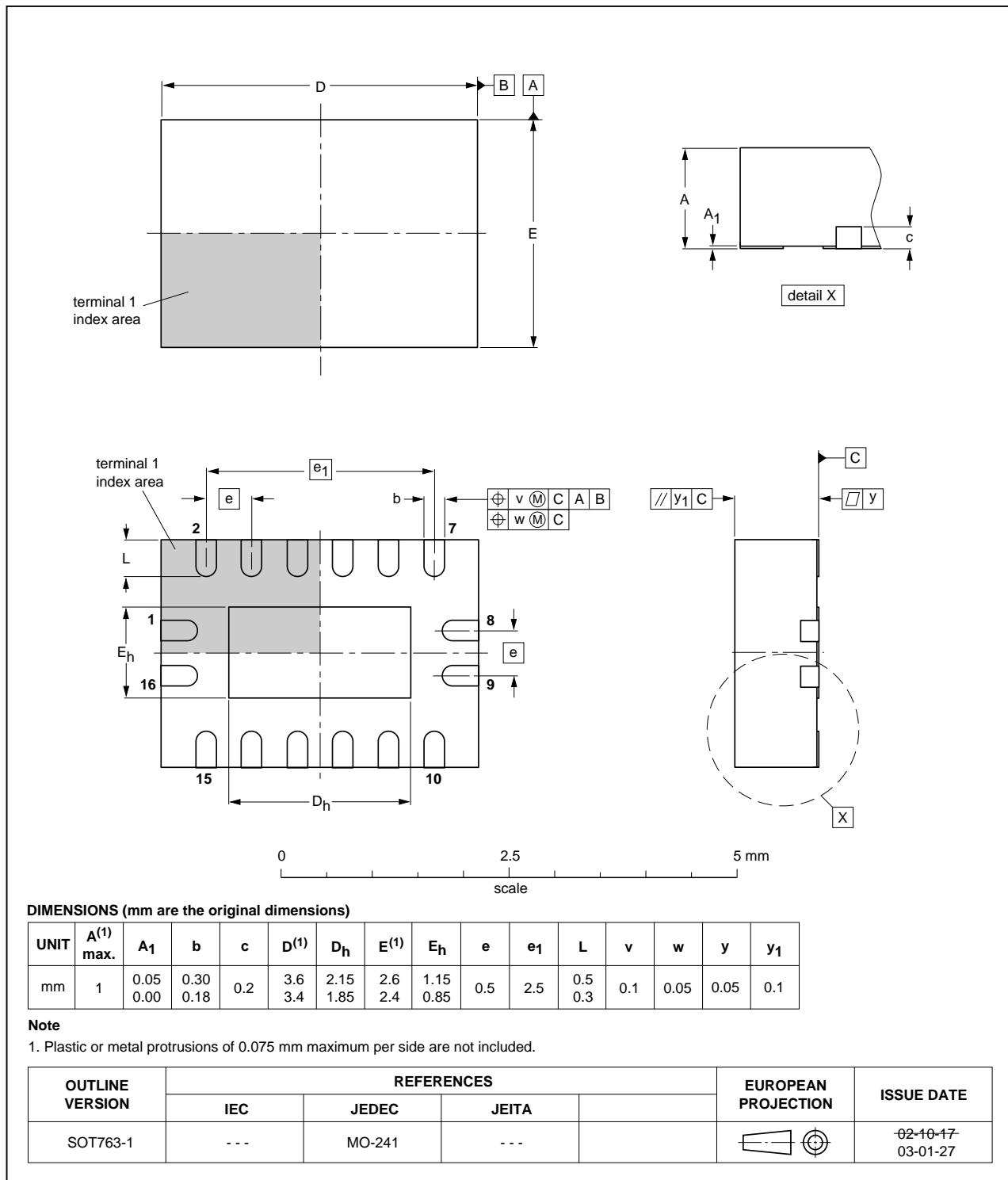


Fig 20. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 9. Abbreviations

| Acronym | Abbreviation |
|---------|------------------------------------------------|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MM | Machine Model |

15. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--------------------------------------------------------------------------|-----------------------|---------------|---------------------|
| 74HC_HCT123 v.8 | 20111216 | Product data sheet | - | 74HC_HCT123 v.7 |
| Modifications: | <ul style="list-style-type: none"> • Legal pages updated. | | | |
| 74HC_HCT123 v.7 | 20110825 | Product data sheet | - | 74HC_HCT123 v.6 |
| 74HC_HCT123 v.6 | 20110314 | Product data sheet | - | 74HC_HCT123 v.5 |
| 74HC_HCT123 v.5 | 20090713 | Product data sheet | - | 74HC_HCT123 v.4 |
| 74HC_HCT123 v.4 | 20060616 | Product data sheet | - | 74HC_HCT123 v.3 |
| 74HC_HCT123 v.3 | 20040511 | Product specification | - | 74HC_HCT123_CNV v.2 |
| 74HC_HCT123_CNV v.2 | 19980708 | Product specification | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

malfuction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

| | | |
|-----------|-----------------------------------------------|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Ordering information | 2 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 4 |
| 5.1 | Pinning | 4 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 5 |
| 7 | Limiting values | 5 |
| 8 | Recommended operating conditions | 6 |
| 9 | Static characteristics | 6 |
| 10 | Dynamic characteristics | 8 |
| 11 | Waveforms | 12 |
| 12 | Application information | 15 |
| 12.1 | Timing component connections | 15 |
| 12.2 | Power-up considerations | 15 |
| 12.3 | Power-down considerations | 16 |
| 13 | Package outline | 17 |
| 14 | Abbreviations | 22 |
| 15 | Revision history | 22 |
| 16 | Legal information | 23 |
| 16.1 | Data sheet status | 23 |
| 16.2 | Definitions..... | 23 |
| 16.3 | Disclaimers..... | 23 |
| 16.4 | Trademarks..... | 24 |
| 17 | Contact information | 24 |
| 18 | Contents | 25 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 16 December 2011

Document identifier: 74HC_HCT123