

SN5472, SN7472 AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

SDLS117 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave

The logical states of the J and K inputs must not be allowed to change when the clock pulse is in a high state.

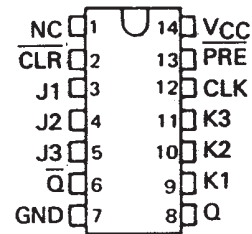
The SN5472, and the SN54H72 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7472 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

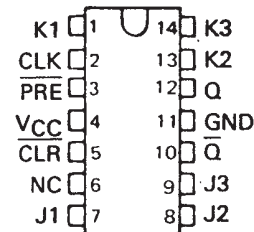
| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----------|---|---|---------------|---------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H^{\dagger} | H^{\dagger} |
| H | H | \square | L | L | Q_0 | \bar{Q}_0 |
| H | H | \square | H | L | H | L |
| H | H | \square | L | H | L | H |
| H | H | \square | H | H | TOGGLE | TOGGLE |

[†] This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN5472 . . . J PACKAGE
SN7472 . . . N PACKAGE
(TOP VIEW)

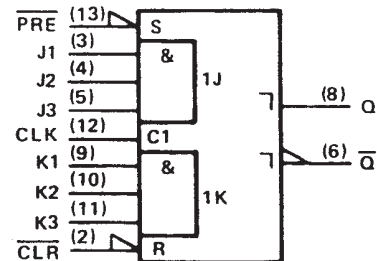


SN5472 . . . W PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

positive logic

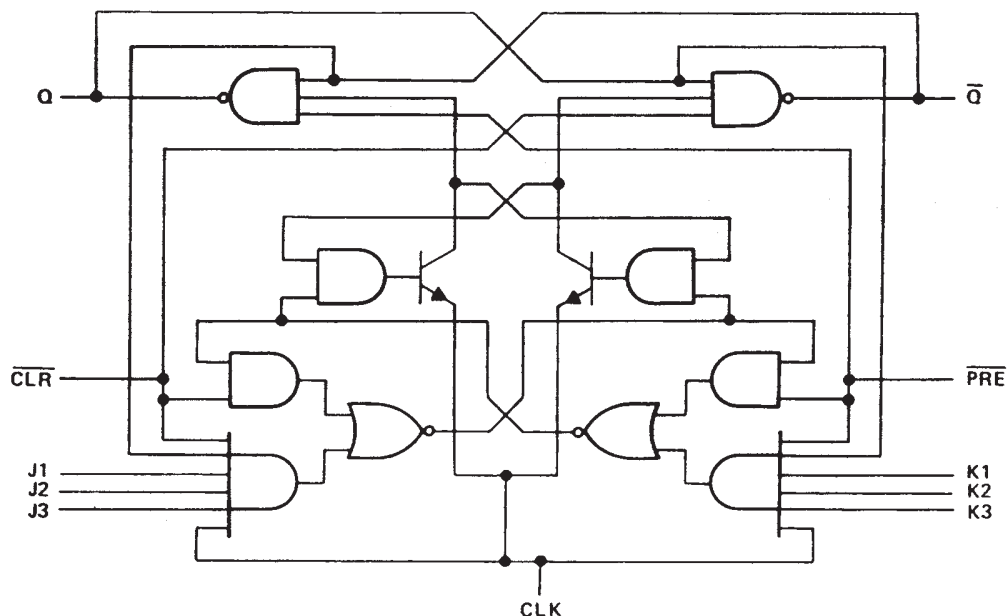
$$J = J1 \cdot J2 \cdot J3$$

$$K = K1 \cdot K2 \cdot K3$$

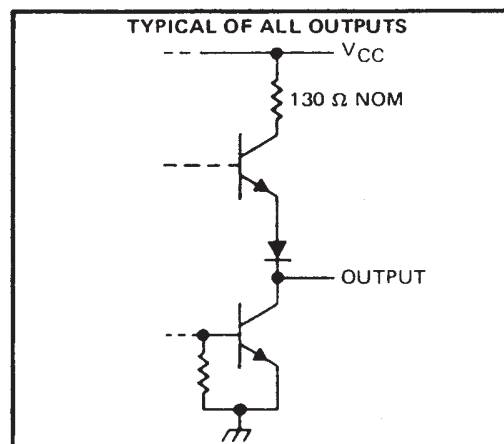
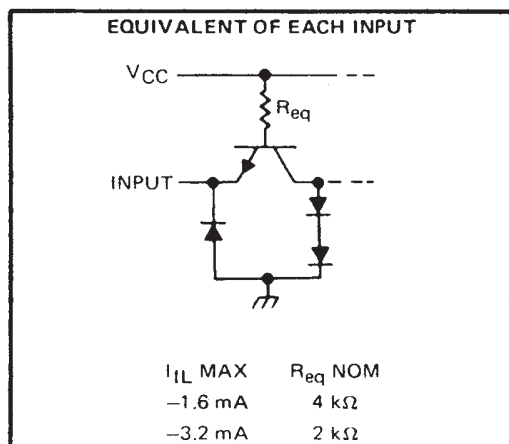
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logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---------------------------------------|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Operating free-air temperature: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN5472, SN7472

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

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recommended operating conditions

| | | SN5472 | | | SN7472 | | | UNIT |
|----------|----------------------------------|------------|-----|-------|--------|-----|-------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | – 0.4 | | | – 0.4 | mA |
| I_{OL} | Low-level output current | | | 16 | | | 16 | mA |
| t_w | Pulse duration | CLK high | 20 | | 20 | | | ns |
| | | CLK low | 47 | | 47 | | | |
| | | PRE or CLR | 25 | | 25 | | | |
| t_{su} | Input setup time before CLK ↑ | 0 | | | 0 | | | ns |
| t_h | Input hold time-data after CLK ↓ | 0 | | | 0 | | | ns |
| T_A | Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS † | | SN5472 | | | SN7472 | | | UNIT |
|-----------|-----------|---|--|--------|------|-------|--------|------|-------|---------------|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$ | | | | – 1.5 | | | – 1.5 | V |
| V_{OH} | | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$ | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V_{OL} | | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$ | | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I_I | | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | | 1 | | | 1 | mA |
| I_{IH} | J or K | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$ | | | | 40 | | | 40 | μA |
| | All other | | | | | 80 | | | 80 | |
| I_{IL} | J or K | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | | – 1.6 | | | – 1.6 | mA |
| | All other | | | | | – 3.2 | | | – 3.2 | |
| $I_{OS}§$ | | $V_{CC} = \text{MAX}$ | | – 20 | | – 57 | – 18 | | – 57 | mA |
| I_{CC} | | $V_{CC} = \text{MAX}, \text{ See Note 2}$ | | | 10 | 20 | | 10 | 20 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|---|-----|-----|-----|------|
| f _{max} | | | R _L = 400 Ω, C _L = 15 pF | 15 | 20 | | MHz |
| t _{PLH} | PRE or CLR | Q or Q̄ | | | 16 | 25 | ns |
| t _{PHL} | | | | | 25 | 40 | ns |
| t _{PLH} | CLK | Q or Q̄ | | | 16 | 25 | ns |
| t _{PHL} | | | | | 25 | 40 | ns |
| | | | | | | | |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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