

SN5472, SN7472 AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

SDS117 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave

The logical states of the J and K inputs must not be allowed to change when the clock pulse is in a high state.

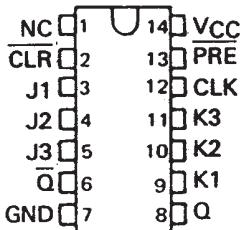
The SN5472, and the SN54H72 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7472 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

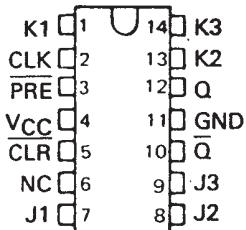
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	⊜	L	L	Q_0	\bar{Q}_0
H	H	⊜	H	L	H	L
H	H	⊜	L	H	L	H
H	H	⊜	H	H	TOGGLE	

[†]This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN5472 . . . J PACKAGE
SN7472 . . . N PACKAGE
(TOP VIEW)

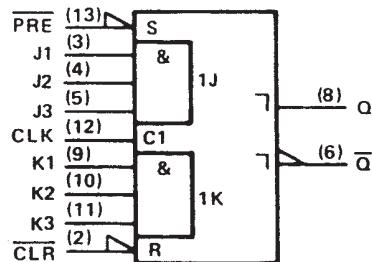


SN5472 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol[‡]



[‡]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

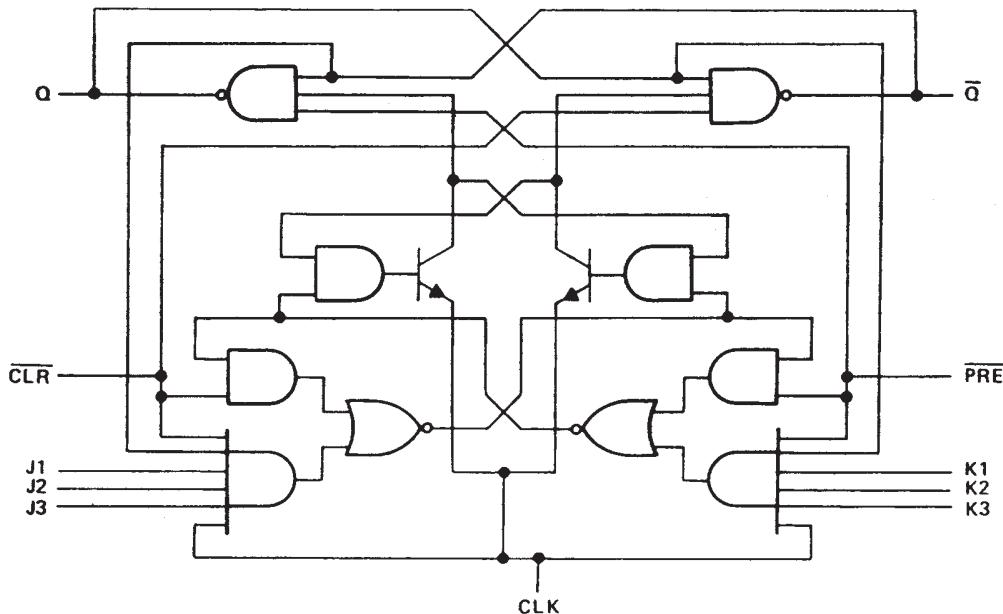
positive logic

$$\begin{aligned} J &= J_1 \cdot J_2 \cdot J_3 \\ K &= K_1 \cdot K_2 \cdot K_3 \end{aligned}$$

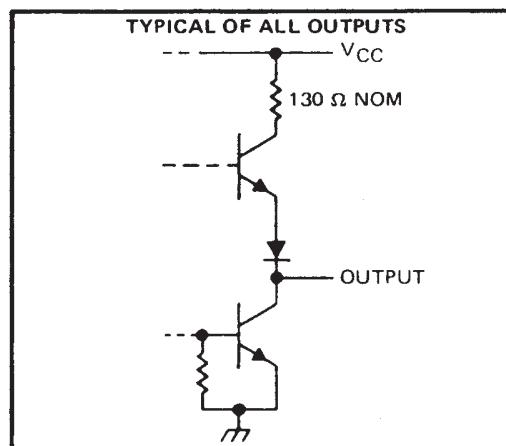
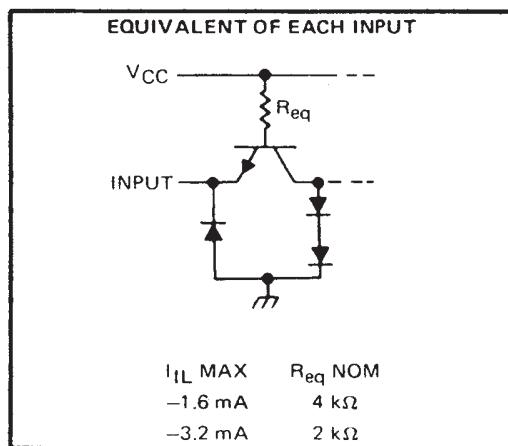
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logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

			SN5472			SN7472			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current				-0.4			-0.4	mA
I _{OL}	Low-level output current				16			16	mA
t _w	Pulse duration	CLK high	20			20			ns
		CLK low	47			47			
		PRE or CLR	25			25			
t _{su}	Input setup time before CLK ↑		0			0			ns
t _h	Input hold time-data after CLK ↓		0			0			ns
T _A	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			SN5472			SN7472			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA					-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA			2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA			0.2	0.4		0.2	0.4		V
I _I	V _{CC} = MAX, V _I = 5.5 V					1			1	mA
I _{IH}	J or K					40			40	μA
	All other	V _{CC} = MAX, V _I = 2.4 V				80			80	
I _{IL}	J or K					-1.6			-1.6	mA
	All other	V _{CC} = MAX, V _I = 0.4 V				-3.2			-3.2	
I _{OS\$}	V _{CC} = MAX			-20	-57	-18	-20	-57	-18	mA
I _{CC}	V _{CC} = MAX, See Note 2			10	20		10	20	10	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

\$ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			MIN	TYP	MAX	UNIT	
f _{max}			R _L = 400 Ω, C _L = 15 pF			15	20		MHz	
t _{PLH}	PRE or CLR	Q or \bar{Q}				16	25		ns	
t _{PHL}						25	40		ns	
t _{PLH}	CLK	Q or \bar{Q}				16	25		ns	
t _{PHL}						25	40		ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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