

## Features

- Buffered Inputs
- Asynchronous Parallel Load
- Typical  $f_{MAX} = 60\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs ..... 10 LSTTL Loads
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V}$  (Max),  $V_{IH} = 2\text{V}$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}, V_{OH}$

## Description

The Harris CD74HC597 and CD74HCT597 are high-speed silicon gate CMOS devices that are pin-compatible with the LSTTL 597 devices. Each device consists of an 8-flip-flop input register and an 8-bit parallel-in/serial-in, serial-out shift register. Each register is controlled by its own clock. A "low" on the parallel load input ( $\overline{PL}$ ) shifts parallel stored data asynchronously into the shift register. A "low" master input ( $\overline{MR}$ ) clears the shift register. Serial input data can also be synchronously shifted through the shift register when  $\overline{PL}$  is high.

## Ordering Information

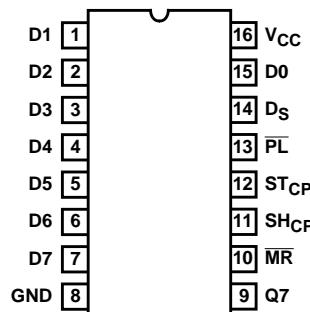
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC597E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT597E	-55 to 125	16 Ld PDIP	E16.3
CD74HC597M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT597M	-55 to 125	16 Ld SOIC	M16.15

### NOTES:

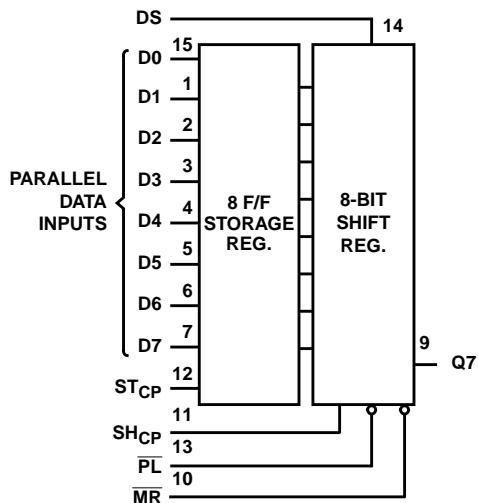
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

## Pinout

CD74HC597, CD74HCT597  
(PDIP, SOIC)  
TOP VIEW



### **Functional Diagram**



**FUNCTION TABLE**

<b>ST<sub>CP</sub></b>	<b>SH<sub>CP</sub></b>	<b>PL</b>	<b>MR</b>	<b>FUNCTION</b>
↑	X	X	X	Data Loaded to Input Flip-Flops
↑	X	L	H	Data Loaded from Inputs to Shift Register
No Clock Edge	X	L	H	Data Transferred from Input Flip-Flops to Shift Register
X	X	L	L	Invalid Logic, State of Shift Register Indeterminate when Signals Removed
X	X	H	L	Shift Register Cleared
X	↑	H	H	Shift Register Clocked Q <sub>n</sub> = Q <sub>n-1</sub> , Q <sub>0</sub> = D <sub>S</sub>

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High CP Level

**Absolute Maximum Ratings**

DC Supply Voltage, $V_{CC}$	.....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$ For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	.....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$ For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	.....	$\pm 20mA$
DC Drain Current, per Output, $I_O$ For $-0.5V < V_O < V_{CC} + 0.5V$	.....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$ For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	.....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$	.....	$\pm 50mA$

**Thermal Information**

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	90
SOIC Package	160
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

**Operating Conditions**

Temperature Range, $T_A$	.....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	.....	
HC Types	.....	2V to 6V
DC Input or Output Voltage, $V_I, V_O$	.....	0V to $V_{CC}$
Input Rise and Fall Time		
2V	.....	1000ns (Max)
4.5V	.....	500ns (Max)
6V	.....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## NOTE:

3.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**DC Electrical Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>													
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V	
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V	
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V	
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V	
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V	
			0.02	6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V	
			4	4.5	-	-	0.26	-	0.33	-	0.4	V	
			5.2	6	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$	

# CD74HC597, CD74HCT597

## DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

## HCT Input Loading Table

INPUT	UNIT LOADS
D <sub>S</sub>	0.2
D <sub>n</sub>	0.3
PL, MR	1.5
S <sub>TCP</sub> , S <sub>HCP</sub>	1.5

NOTE: Unit load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications Table, e.g., 360μA max. at 25°C.

## Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>HC TYPES</b>												
SH <sub>CP</sub> Frequency	f <sub>MAX</sub>	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz

# CD74HC597, CD74HCT597

## Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SH <sub>CP</sub> Pulse Width	t <sub>W</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
ST <sub>CP</sub> Pulse Width	t <sub>W</sub>	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
MR Pulse Width	t <sub>W</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
PL Pulse Width	t <sub>W</sub>	2	70	-	-	90	-	-	105	-	-	ns
		4.5	14	-	-	18	-	-	21	-	-	ns
		6	12	-	-	15	-	-	18	-	-	ns
ST <sub>CP</sub> to SH <sub>CP</sub> Setup Time	t <sub>SU</sub>	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns
D <sub>S</sub> to SH <sub>CP</sub> Setup Time D <sub>n</sub> to ST <sub>CP</sub> Setup Time	t <sub>SU</sub>	2	50	-	-	65	-	-	75	-	-	ns
		4.5	10	-	-	13	-	-	15	-	-	ns
		6	9	-	-	11	-	-	13	-	-	ns
ST <sub>CP</sub> to SH <sub>CP</sub> Setup Time Time	t <sub>H</sub>	2	0	-	-	0	-	-	0	-	-	ns
		4.5	0	-	-	0	-	-	0	-	-	ns
		6	0	-	-	0	-	-	0	-	-	ns
D <sub>S</sub> to SH <sub>CP</sub> Hold Time D <sub>n</sub> to ST <sub>CP</sub> Hold Time	t <sub>H</sub>	2	3	-	-	3	-	-	3	-	-	ns
		4.5	3	-	-	3	-	-	3	-	-	ns
		6	3	-	-	3	-	-	3	-	-	ns
MR to SH <sub>CP</sub> Removal Time	t <sub>REM</sub>	2	3	-	-	3	-	-	3	-	-	ns
		4.5	3	-	-	3	-	-	3	-	-	ns
		6	3	-	-	3	-	-	3	-	-	ns
<b>HCT TYPES</b>												
SH <sub>CP</sub> Frequency	f <sub>MAX</sub>	4.5	25	-	-	20	-	-	16	-	-	MHz
SH <sub>CP</sub> Pulse Width	t <sub>W</sub>	4.5	20	-	-	25	-	-	30	-	-	ns
ST <sub>CP</sub> Pulse Width	t <sub>W</sub>	4.5	13	-	-	16	-	-	20	-	-	ns
MR Pulse Width	t <sub>W</sub>	4.5	18	-	-	23	-	-	27	-	-	ns
PL Pulse Width	t <sub>W</sub>	4.5	16	-	-	20	-	-	24	-	-	ns
ST <sub>CP</sub> to SH <sub>CP</sub> Setup Time	t <sub>SU</sub>	4.5	24	-	-	30	-	-	36	-	-	ns

# CD74HC597, CD74HCT597

## Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
D <sub>S</sub> to SH <sub>CP</sub> Setup Time D <sub>n</sub> to ST <sub>CP</sub> Setup Time	t <sub>H</sub>	4.5	10	-	-	13	-	-	15	-	-	ns
ST <sub>CP</sub> to SH <sub>CP</sub> Hold Time	t <sub>H</sub>	4.5	0	-	-	0	-	-	0	-	-	ns
D <sub>S</sub> to SH <sub>CP</sub> Hold Time D <sub>n</sub> to ST <sub>CP</sub> Hold Time	t <sub>H</sub>	4.5	3	-	-	3	-	-	3	-	-	ns
MR to SH <sub>CP</sub> Removal Time	t <sub>REM</sub>	4.5	10	-	-	13	-	-	15	-	-	ns

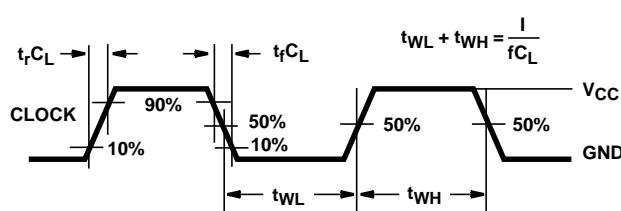
**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay SH <sub>CP</sub> to Q7	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	30	-	37	-	45	ns
PL to Q7	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	200	-	250	-	300	ns
			4.5	-	-	40	-	50	-	60	ns
		C <sub>L</sub> = 15pF	5	-	17	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	34	-	43	-	51	ns
ST <sub>CP</sub> to Q7	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	240	-	300	-	360	ns
			4.5	-	-	48	-	60	-	72	ns
		C <sub>L</sub> = 15pF	5	-	20	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	41	-	51	-	61	ns
MR to Q7	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	30	-	37	-	45	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>I</sub>	C <sub>L</sub> = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance, (Notes 4, 5)	C <sub>PD</sub>	-	5	-	13.5	-	-	-	-	-	pF
<b>HCT</b>											
Propagation Delay SH <sub>CP</sub> to Q7	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	38	-	48	-	57	ns
			C <sub>L</sub> = 15pF	5	-	16	-	-	-	-	ns
PL to Q7	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	48	-	60	-	72	ns
		C <sub>L</sub> = 15pF	5	-	20	-	-	-	-	-	ns
ST <sub>CP</sub> to Q7	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	56	-	70	-	84	ns
		C <sub>L</sub> = 15pF	5	-	23	-	-	-	-	-	ns

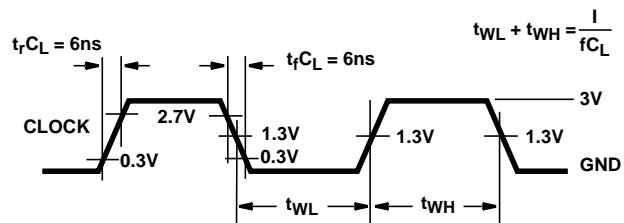
**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C to 85°C		-55°C to 125°C	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX
MR to Q7	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	44	-	55	-	66
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22
Input Capacitance	$C_I$	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10
Power Dissipation Capacitance, (Notes 4, 5)	$C_{PD}$	-	5	-	18.5	-	-	-	-	pF

## NOTES:

4.  $C_{PD}$  is used to determine the dynamic power consumption, per package.5.  $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$  where:  $f_i$  = Input Frequency,  $f_o$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.**Test Circuits and Waveforms**

NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

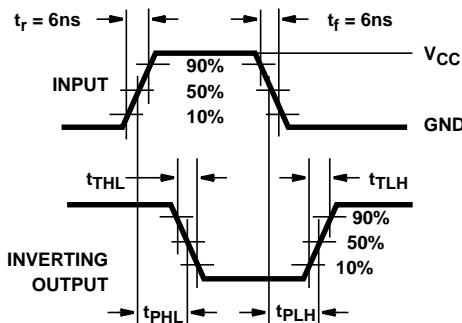


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

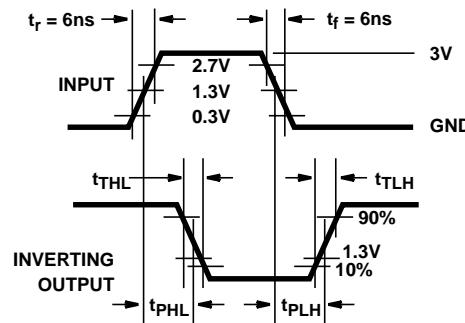
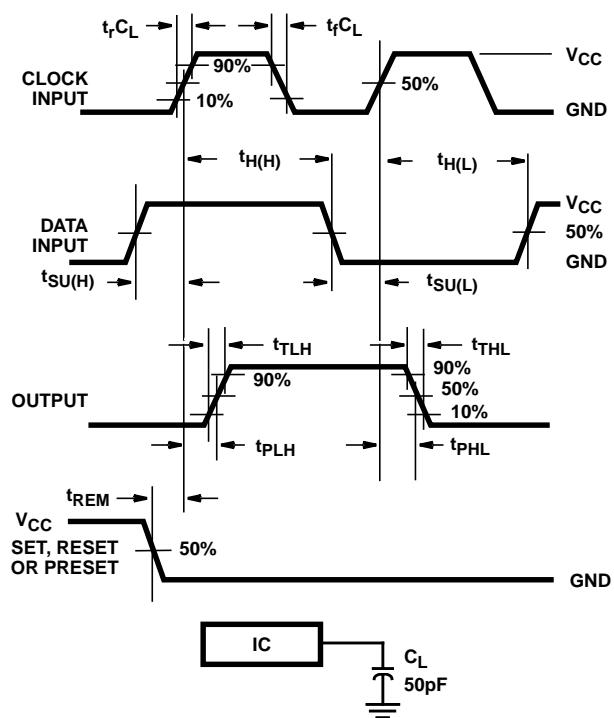
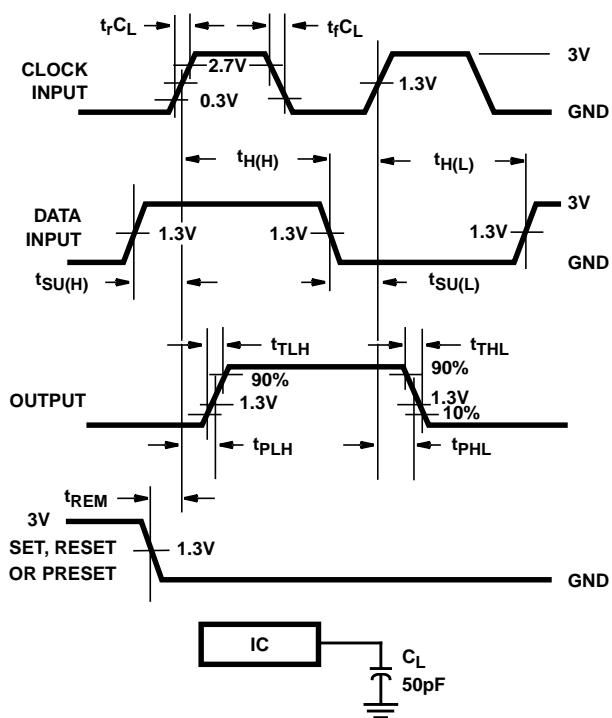


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

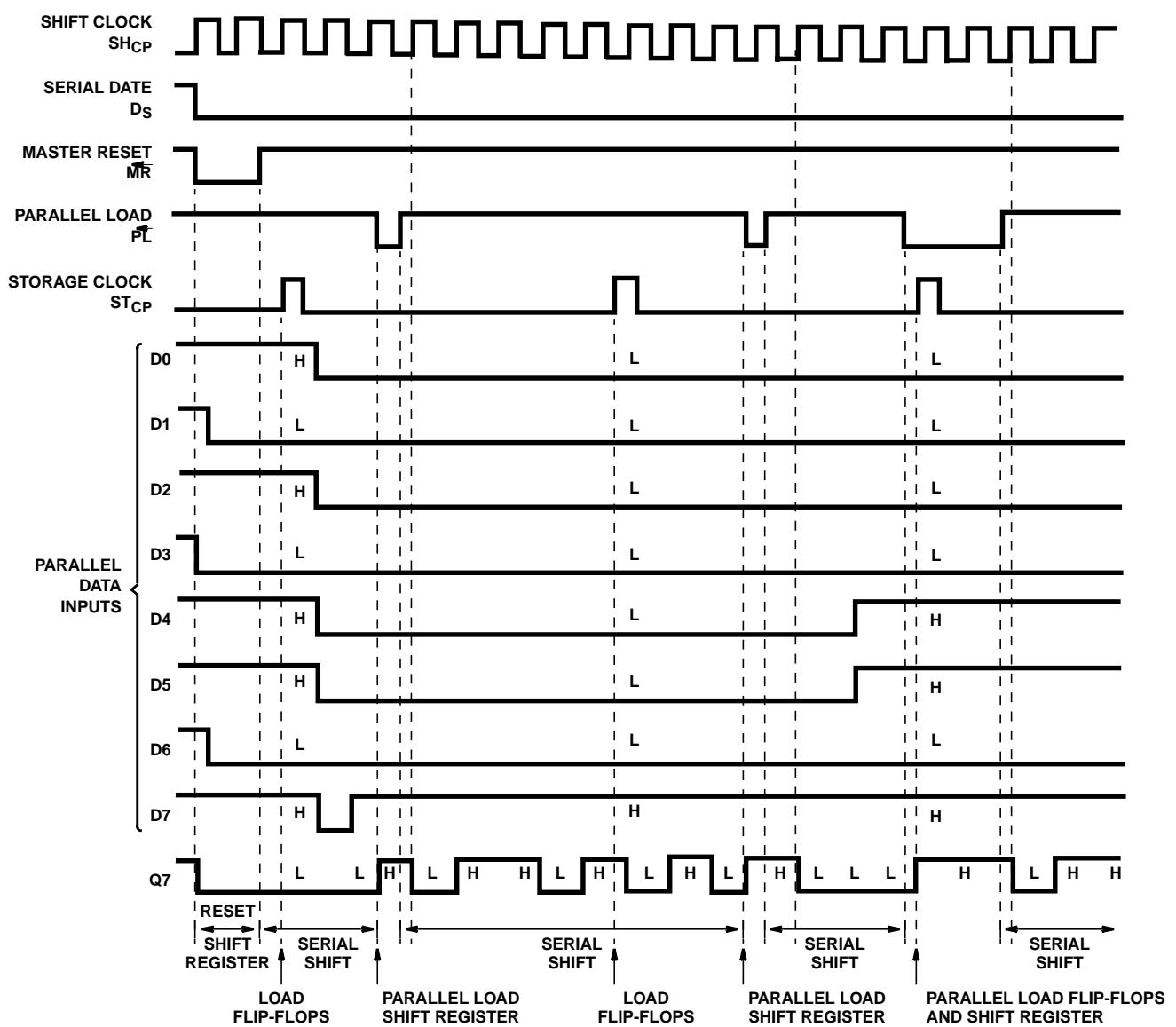
**Test Circuits and Waveforms (Continued)**



**FIGURE 5.** HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS



**FIGURE 6.** HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**Timing Diagram**

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