

**74AC573**

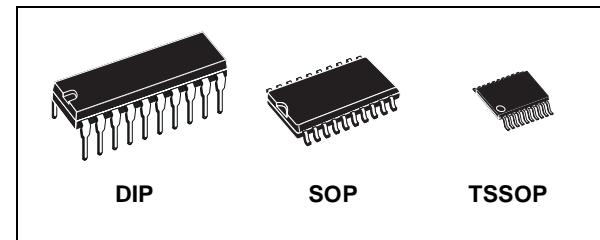
## OCTAL D-TYPE LATCH WITH 3 STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:  $t_{PD} = 4.5\text{ns}$  (TYP.) at  $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A}$ (MAX.) at  $T_A=25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (MIN.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OHI}| = I_{OL} = 24\text{mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 573
- IMPROVED LATCH-UP IMMUNITY

### DESCRIPTION

The 74AC573 is an advanced high-speed CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input (OE). While the LE inputs is held at a high level, the Q



### ORDER CODES

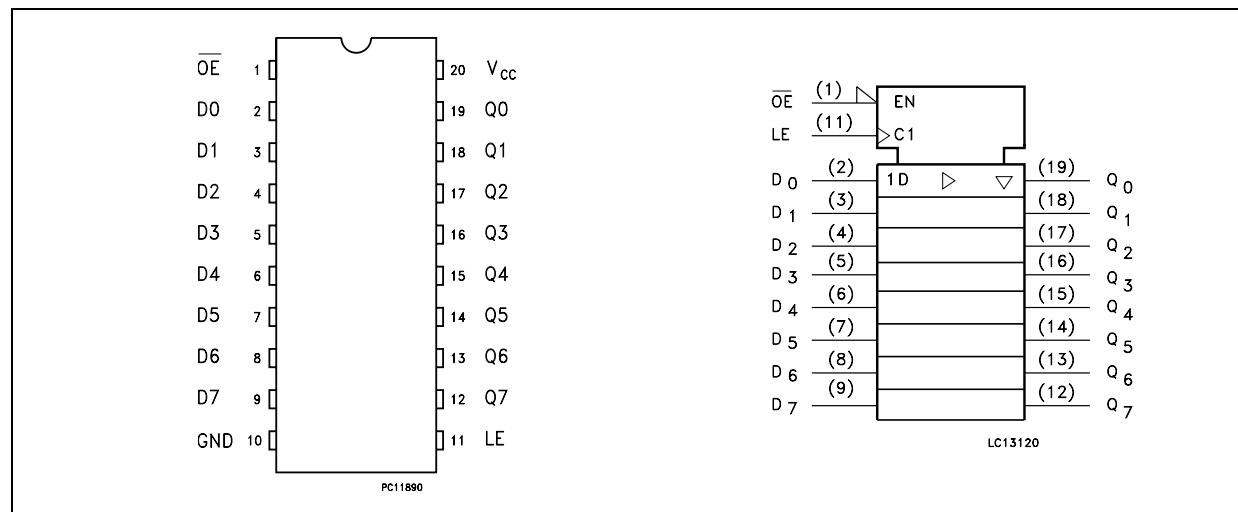
PACKAGE	TUBE	T & R
DIP	74AC573B	
SOP	74AC573M	74AC573MTR
TSSOP		74AC573TTR

outputs will follow the data input precisely.

When the LE is taken low, the Q outputs will be latched at the logic level of D input data. While the (OE) input is low, the 8 outputs will be in a normal logic state (high or low logic level); while OE is in high level, the outputs will be in a high impedance state.

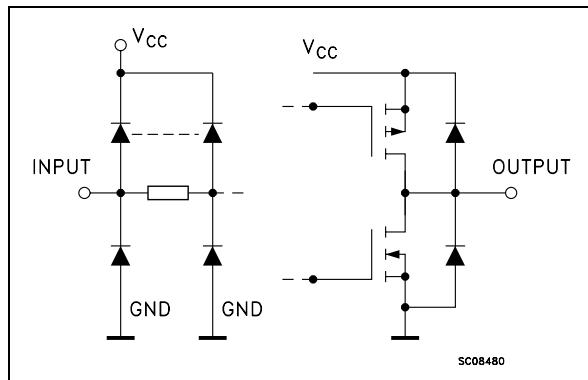
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# 74AC573

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	OE	Asynchronous Master Reset (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

## TRUTH TABLE

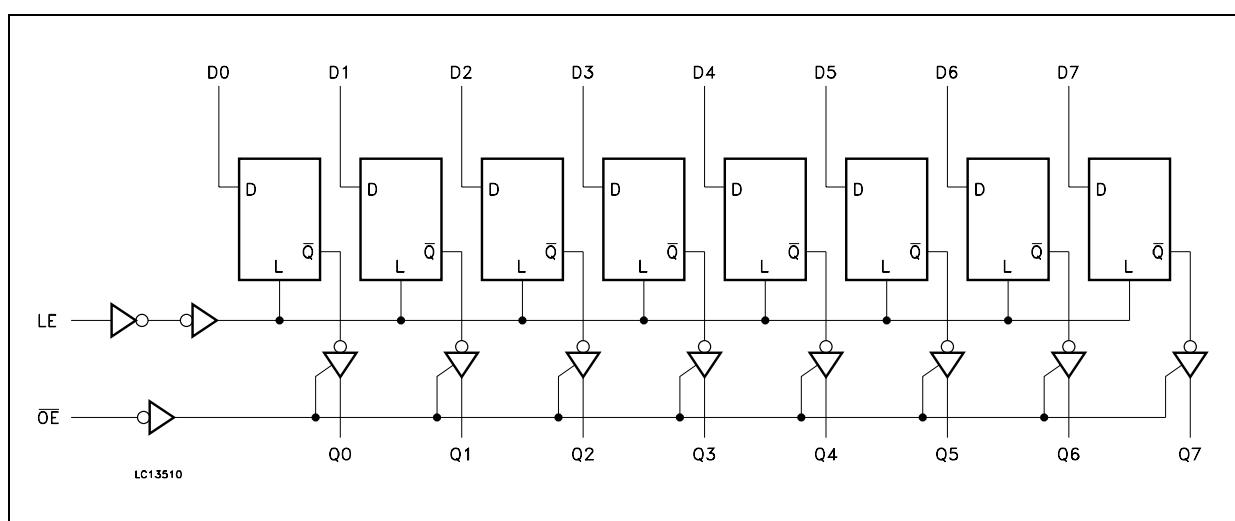
INPUTS			OUTPUT
OE	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE
L	H	L	L
L	H	H	H

X : Don't Care

Z : High Impedance

NOTE: Outputs are latched at the time when the input is taken LOW logic level

## LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

<b>Symbol</b>	<b>Parameter</b>	<b>Value</b>	<b>Unit</b>
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

<b>Symbol</b>	<b>Parameter</b>	<b>Value</b>	<b>Unit</b>
$V_{CC}$	Supply Voltage	2 to 6	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0, 4.5$ or $5.5V$ (note 1)	8	ns/V

1)  $V_{IN}$  from 30% to 70% of  $V_{CC}$

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	3.0	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V	2.1	1.5		2.1		2.1		V
		4.5		3.15	2.25		3.15		3.15		
		5.5		3.85	2.75		3.85		3.85		
V <sub>IL</sub>	Low Level Input Voltage	3.0	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V		1.5	0.9		0.9		0.9	V
		4.5			2.25	1.35		1.35		1.35	
		5.5			2.75	1.65		1.65		1.65	
V <sub>OH</sub>	High Level Output Voltage	3.0	I <sub>O</sub> =-50 μA	2.9	2.99		2.9		2.9		V
		4.5	I <sub>O</sub> =-50 μA	4.4	4.49		4.4		4.4		
		5.5	I <sub>O</sub> =-50 μA	5.4	5.49		5.4		5.4		
		3.0	I <sub>O</sub> =-12 mA	2.56			2.46		2.4		
		4.5	I <sub>O</sub> =-24 mA	3.86			3.76		3.7		
		5.5	I <sub>O</sub> =-24 mA	4.86			4.76		4.7		
V <sub>OL</sub>	Low Level Output Voltage	3.0	I <sub>O</sub> =50 μA		0.002	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	
		5.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	
		3.0	I <sub>O</sub> =12 mA			0.36		0.44		0.5	
		4.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
		5.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>OZ</sub>	High Impedance Output Leakege Current	5.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			± 0.5		± 2.5		± 5	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	5.5	V <sub>OLD</sub> = 1.65 V max					75		50	mA
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$ , Input  $t_r = t_f = 3\text{ns}$ )

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time LE to Q	3.3 <sup>(*)</sup>			6.0	13.0		15.0		16.5	ns
		5.0 <sup>(**)</sup>			4.5	9.5		11.0		12.5	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time D to Q	3.3 <sup>(*)</sup>			5.5	13.0		15.0		16.5	ns
		5.0 <sup>(**)</sup>			4.5	10.0		11.5		13	
$t_{PZL}$ $t_{PZH}$	Output Enable Time	3.3 <sup>(*)</sup>			6.5	11.0		12.5		13.5	ns
		5.0 <sup>(**)</sup>			5.0	9.0		10.0		11.5	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time	3.3 <sup>(*)</sup>			7.0	12.5		13.5		15.0	ns
		5.0 <sup>(**)</sup>			6.0	11.0		12.5		13.5	
$t_W$	CLOCK Pulse Width HIGH or LOW	3.3 <sup>(*)</sup>			1.5	4.0		4.5		4.5	ns
		5.0 <sup>(**)</sup>			1.5	3.5		4.0		4.0	
$t_S$	D to CK, HIGH or LOW	3.3 <sup>(*)</sup>			0.5	3.0		3.5		3.5	ns
		5.0 <sup>(**)</sup>			0	2.5		3.0		3.0	
$t_h$	Hold Time D to CK, HIGH or LOW	3.3 <sup>(*)</sup>			-0.5	3.0		3.5		3.5	ns
		5.0 <sup>(**)</sup>			0	2.5		3.0		3.0	

<sup>(\*)</sup> Voltage range is  $3.3\text{V} \pm 0.3\text{V}$ <sup>(\*\*)</sup> Voltage range is  $5.0\text{V} \pm 0.5\text{V}$ 

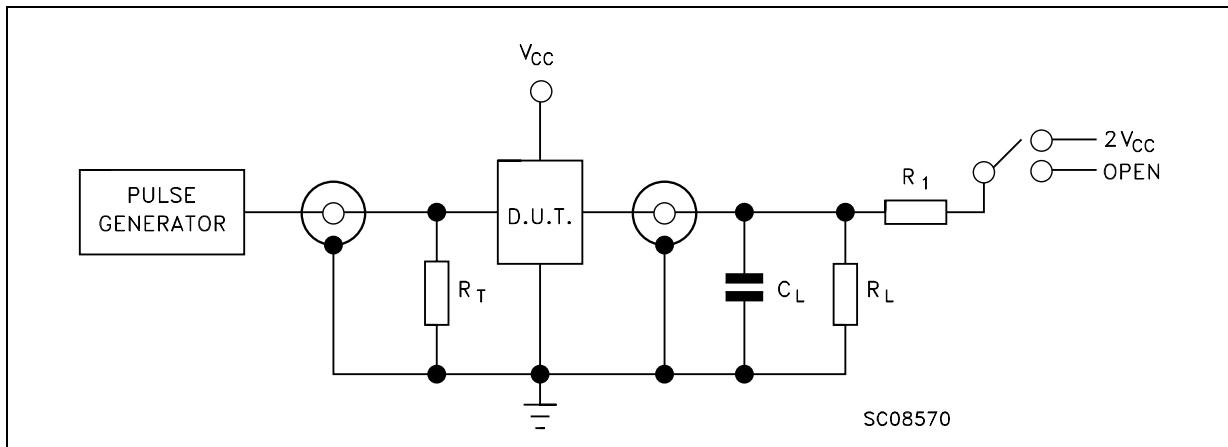
## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		
$C_{IN}$	Input Capacitance	5.0			4					pF	
$C_{OUT}$	Output Capacitance	5.0			8					pF	
$C_{PD}$	Power Dissipation Capacitance (note 1)	5.0	$f_{IN} = 10\text{MHz}$	20						pF	

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$  (per circuit)

# 74AC573

## TEST CIRCUIT



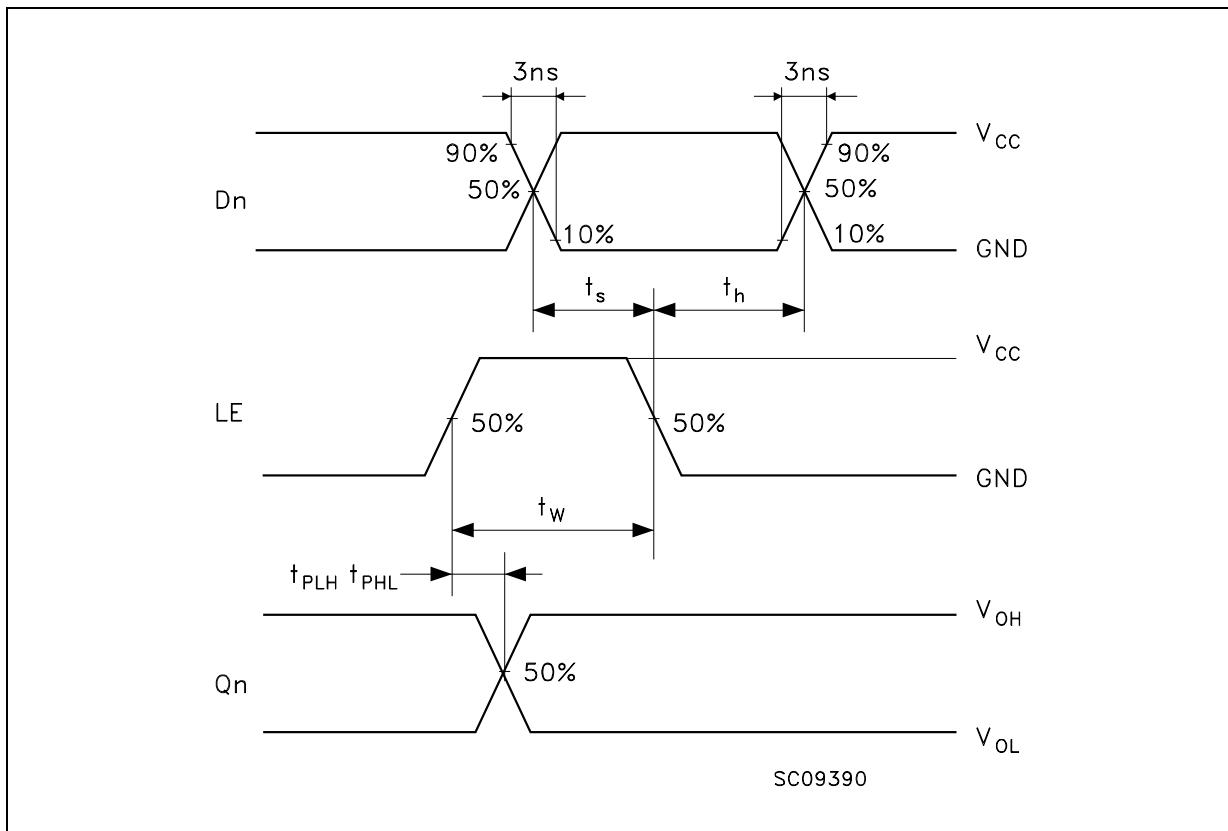
TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$2V_{CC}$
$t_{PZH}, t_{PHZ}$	Open

$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)

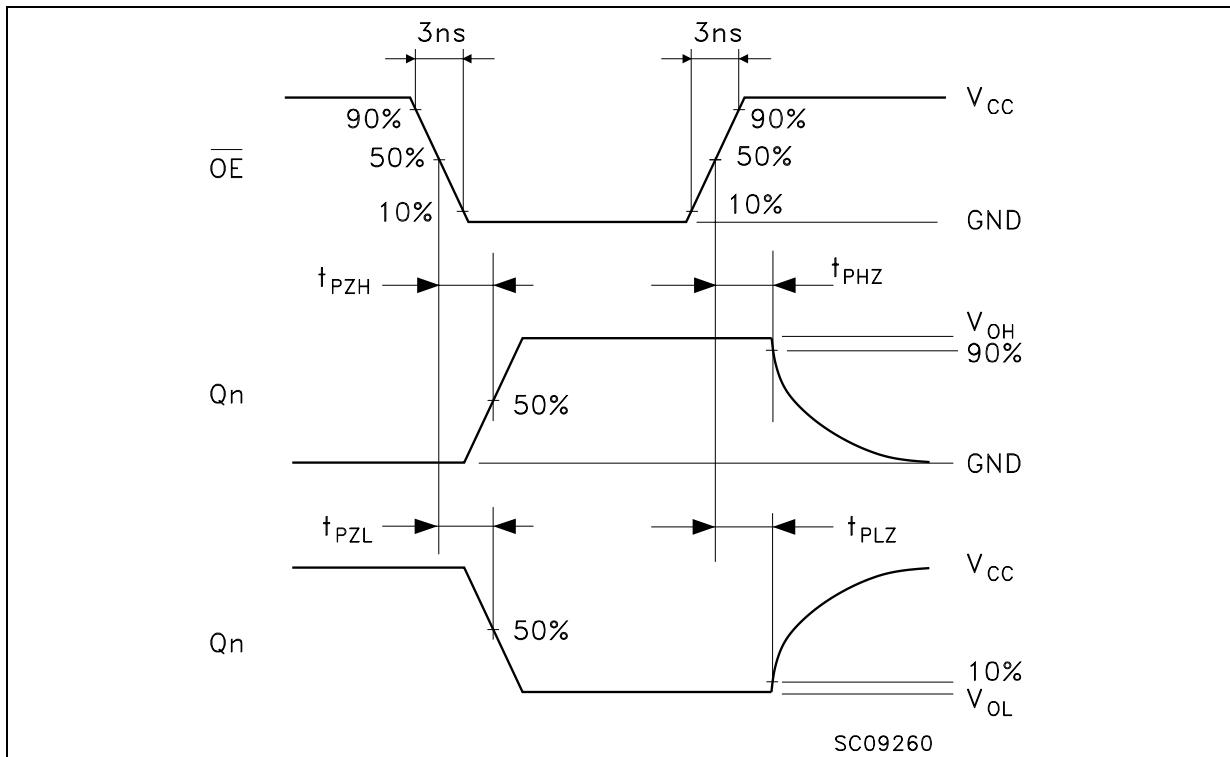
$R_L = R_1 = 500\Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

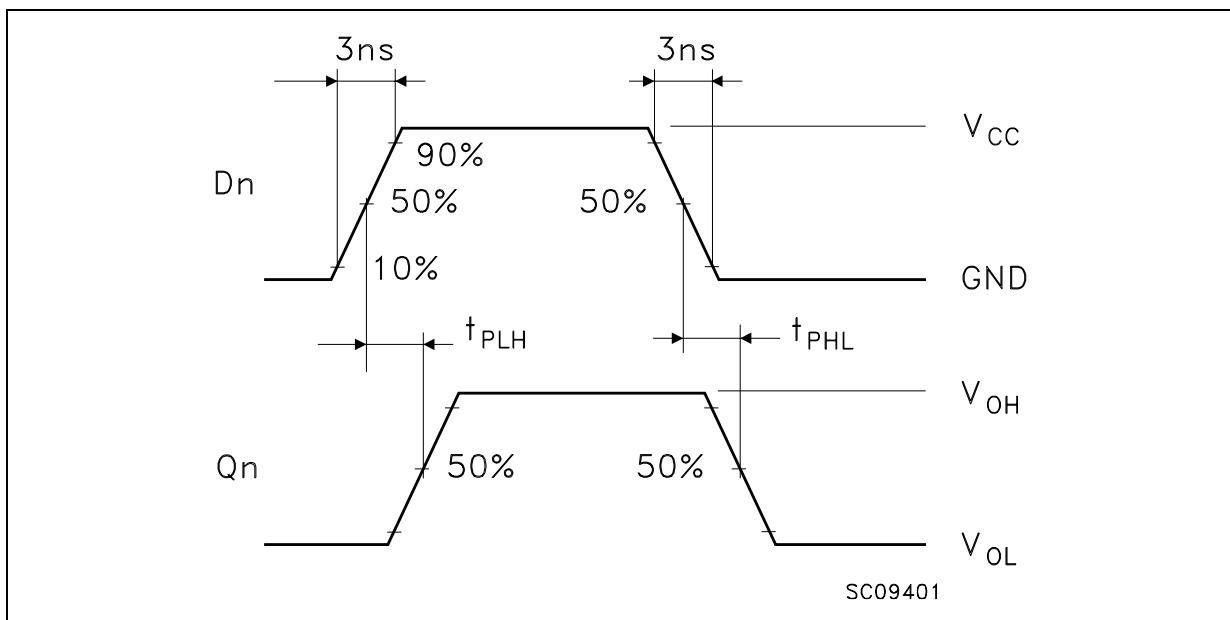
## WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES ( $f=1\text{MHz}$ ; 50% duty cycle)



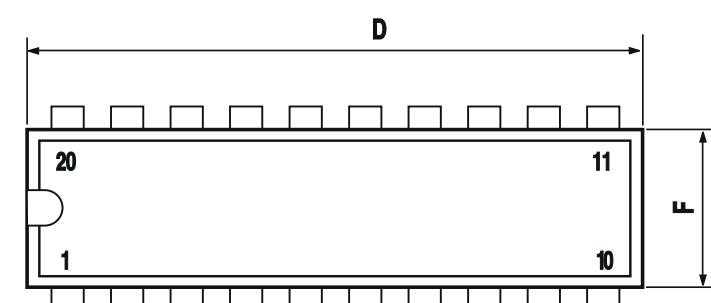
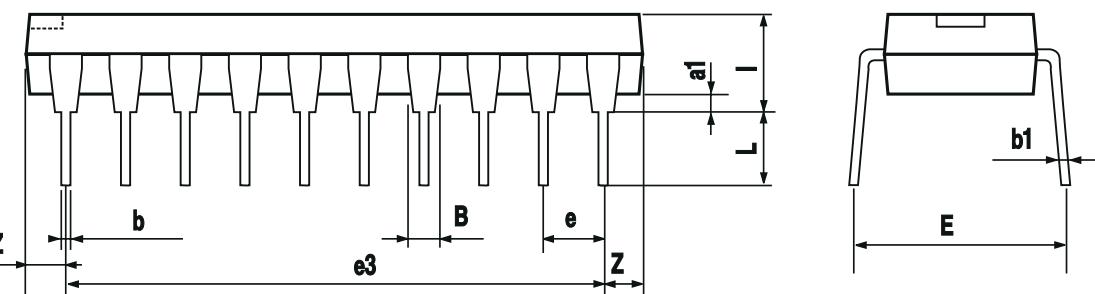
## WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)



## WAVEFORM 3: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)

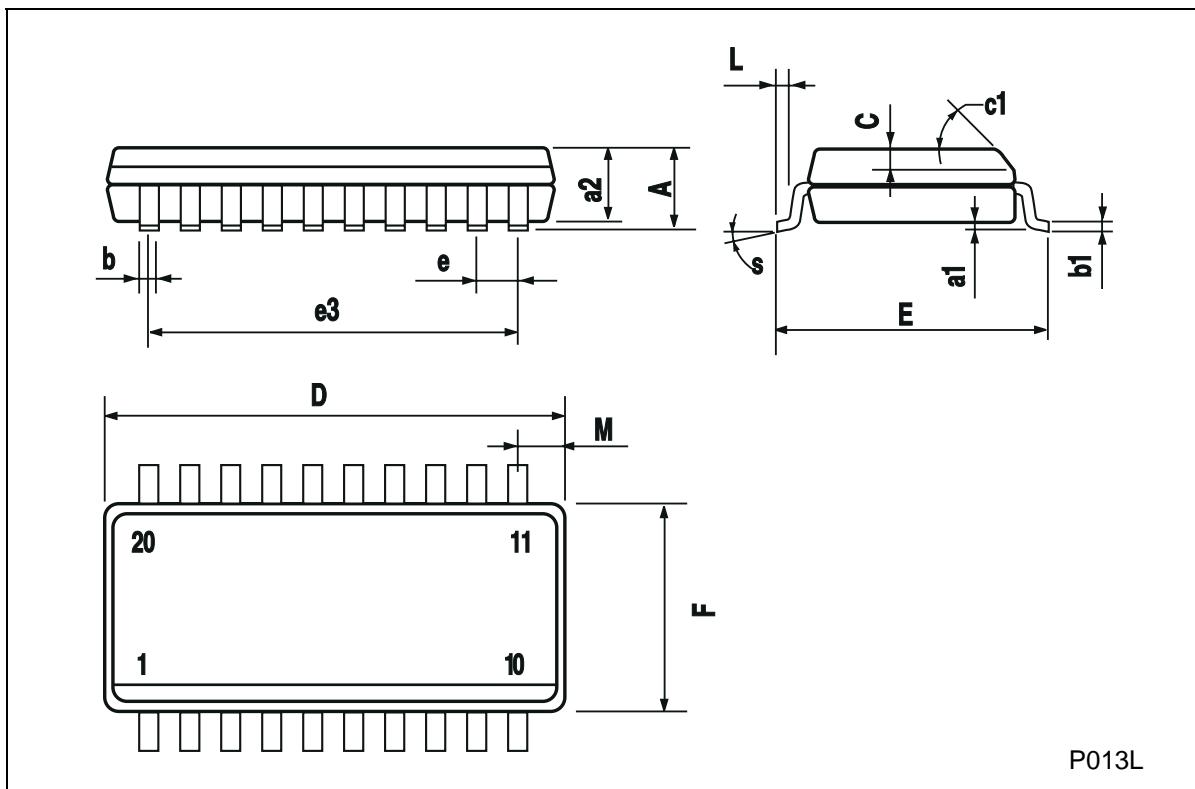


Plastic DIP-20 (0.25) MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



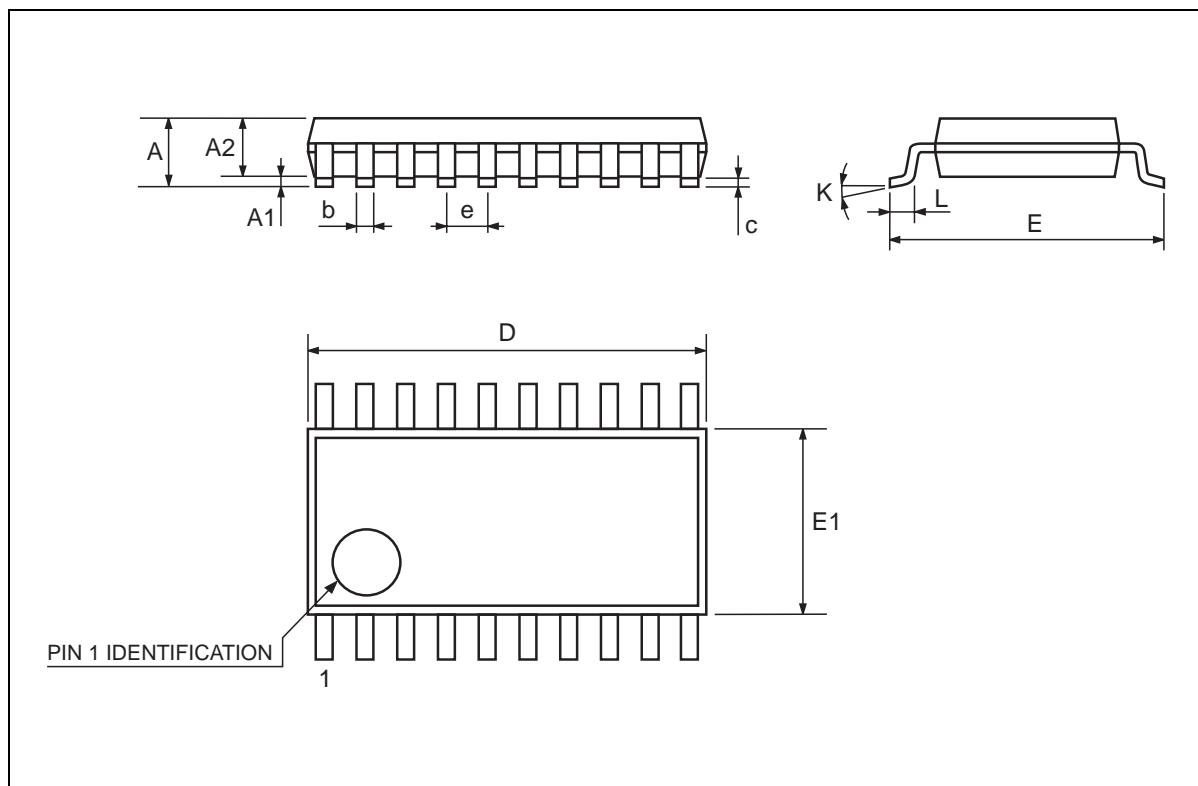
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SO-20 MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a <sub>1</sub>	0.10		0.20	0.004		0.007
a <sub>2</sub>			2.45			0.096
b	0.35		0.49	0.013		0.019
b <sub>1</sub>	0.23		0.32	0.009		0.012
C		0.50			0.020	
c <sub>1</sub>			45 (typ.)			
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e <sub>3</sub>		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S			8 (max.)			



## TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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