Data Sheet

SYNOPSYS®

DesignWare Cores

Hi-Speed USB On-The-Go Controller Subsystem

Overview

The DesignWare® Cores Hi-Speed USB On-The-Go (HS OTG) Controller Subsystem provides designers high-quality USB IP for the most demanding USB 2.0 peripherals. Based on Synopsys' success in building and deploying Hi-Speed USB 2.0 Host, Device and PHY designs in over 100 design wins, the DesignWare HS OTG Subsystem incorporates all Synopsys learning to date in Reuse Methodology, Constrained Random Verification, and USB PHY interoperability to deliver flexible, quality IP in Verilog source.

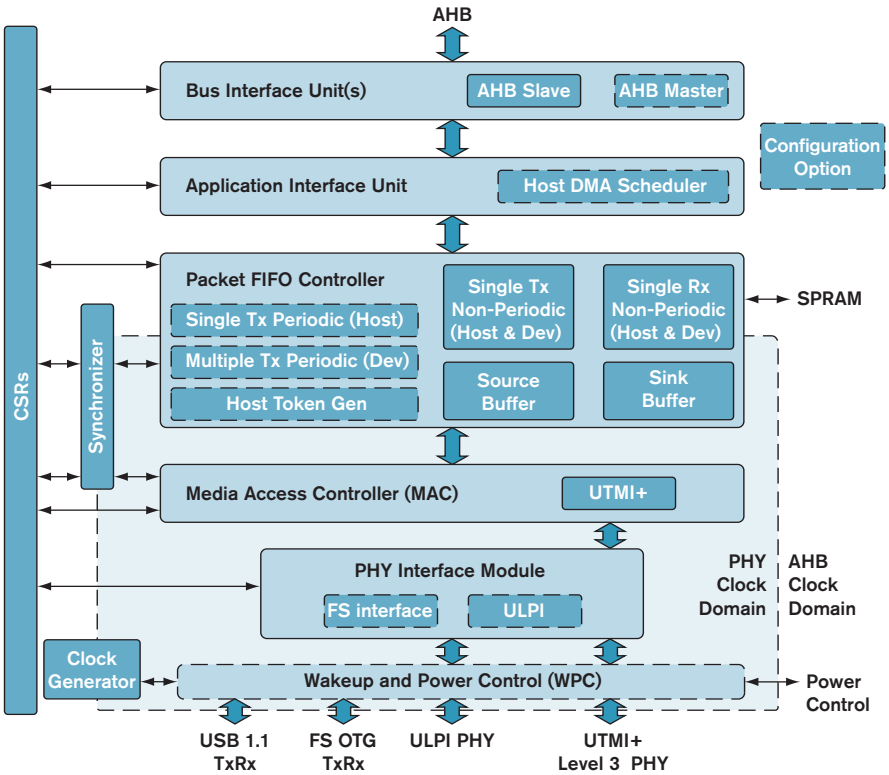
The DesignWare HS OTG Subsystem performs as a standard Hi-Speed, Dual-Role Device (DRD), operating as either a USB 2.0 Hi-Speed compliant peripheral, or Hi-Speed USB 2.0 host. For example, when HS OTG is implemented in a PDA, the PDA can synchronize with a PC. The PDA can also act as the host printing pictures and documents directly to a USB printer without the aid of a PC. Additional applications include mobile phones, MP3 players, digital cameras, set-top boxes, scanners and fax machines.

The DesignWare USB HS OTG Subsystem delivers a flexible, low gate count USB controller capable of OTG, host and device functions.

Features

- Hi-Speed OTG, Hi-Speed Host, and Hi-Speed Device core designed for low gate count, power sensitive products
- Software flexible for post-silicon configuration
- Testbench enables subsystem unit-testing in the target configuration option for shared FIFO memory to minimize RAM area.
- Slave only option to eliminate the need for DMA
- Option to include internal DMA
- Supports single port RAM to minimize area use
- Supports ULPI or UTMI+ Level 3 PHY
- Optional support for FS OTG or USB 1.1 TxRx

HS OTG v2.0 Architecture



Highlights

- Configuration options to maximize performance and minimize CPU interrupts
- Flexible parameters enable easy integration into low and high-latency systems
- Transfer or transaction-based processing of USB data based on system requirements
- Configurable data buffering options to fine-tune performance/area trade-offs
- Buffer and descriptor pre-fetching maximizes host throughput
- Firmware-selectable endpoint configurations enable post-silicon application changes and the flexibility of one-chip design for multiple applications
- Quality IP is tested through extensive Constrained Random Verification
- AMBA™ High-Performance Bus (AHB) interface enables rapid integration into ARM-based designs
- UTMI+ Level 3 enables rapid integration with compatible PHYs
- Hi-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) operation is compliant to the USB OTG Supplement
- Supports all OTG features, including Host Negotiation Protocol and Session Request Protocol
- Verilog source RTL

DesignWare HS OTG

Subsystem Architecture

The Synopsys DesignWare HS OTG Subsystem is built on the industry's most widely used and proven DesignWare USB 2.0 Device Controller. The subsystem includes the HS OTG Controller, Transaction Layer Interface, and Bus Interface Unit (BIU).

The Controller executes all USB and OTG commands in hardware. This module:

- Tracks endpoint information in the EP Info block
- Processes data to and from UTMI+ PHY in the parallel interface engines
- HNP an SAP features may be removed during configuration to save gate count.
- Manages downstream devices through the Root Hub
- Saves power by suspending and resuming controller operation in compliance with the USB specification

The Transaction Layer Interface (TLI) buffers data for the controller. The TLI includes:

- FIFO control logic for buffering data in and out of the subsystem and minimizing configuration, design, and verification time
- Control and Status registers for reconfiguring the subsystem through firmware for maximum flexibility

The optional DMA Controller provides AHB Master capability, including the following:

- Interfacing through descriptors for the software
- Reducing CPU interrupts
- Enhancing throughput on AHB
- Optional generic interface to a DMA controller for designers to use their own DMA

DesignWare HS OTG from the USB IP Industry Leader

Synopsys engineers built the DesignWare HS OTG Subsystem based on expertise gained in delivering Synopsys' robust USB 2.0 Host, Device, OTG, and PHY product lines. This extensive range and proficiency, along with world-class documentation, provides the definitive source for users to integrate high-performance, high-quality USB IP into their advanced designs.

About DesignWare Cores

Synopsys' DesignWare Cores provide system designers with silicon-proven, digital and analog connectivity intellectual property (IP) for some of the world's most recognized products including communications processors, routers, switches, game consoles, digital cameras, computers, and computer peripherals. The DesignWare Cores family includes industry-leading connectivity IP such as USB 1.1, 2.0, OTG and PHYs, PCI, PCI-X, PCI Express, PCI Express PHY, SATA and Ethernet IP standards. Provided as synthesizable RTL source code or in GDS format, these cores enable designers to create innovative, cost-effective systems-on-chip and embedded systems. Synopsys provides flexible licensing options for the DesignWare Cores. Each core can be licensed individually, on a fee-per-project basis, or users can opt for the Volume Purchase Agreement, which enables them to license all the cores in one simple agreement.

For more information on DesignWare IP, visit:
www.designware.com

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