



"Implementation and optimization of an ultra-low power vagus nerve sensing system for epileptic seizures detection"

Jaminon-De Roeck, Chen-Terry

ABSTRACT

Epilepsy is a neurological disorder that affects more than 50 million of people around the world. Among those people, two-thirds cannot be cured with medications. The need for finding a suitable non-invasive solution for those people, medications resistant, is a medical and vital stake to help them lead a more bearable daily-life by reducing the frequency and the intensity of the epilepsy crisis. To this aim, it is necessary to detect the epileptic seizures. The vagus nerve is of interest to this as it contains bio-markers associated with epileptic seizures. This work proposes a design and implementation of a system combining analog front-end and micro-controller in order to isolate the vagus nerve electroneurogram and detect those bio-markers. The design is made according to two figures of merit, the added noise and the total power consumption, in order to make the system suitable for a long-term medical implantation. This work succeeded in detecting those bio-markers and getting a power consumption of 1.623 mW, the same range of power consumption as already existing implantable medical devices like cochlear or muscle stimulator. The results obtained allow to consider the developed system as a suitable solution to epilepsy detection. Experiments on real subjects still need to be conducted as the efficiency of this design was tested only on signals generated in laboratory.

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École polytechnique de Louvain

Implementation and optimization of an ultra-low power vagus nerve sensing system for epileptic seizures detection

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Abstract

Epilepsy is a neurological disorder that affects more than 50 million of people around the world. Among those people, two-thirds cannot be cured with medications. The need for finding a suitable non-invasive solution for those people, medications resistant, is a medical and vital stake to help them lead a more bearable daily-life by reducing the frequency and the intensity of the epilepsy crisis. To this aim, it is necessary to detect the epileptic seizures. The vagus nerve is of interest to this as it contains bio-markers associated with epileptic seizures. This work proposes a design and implementation of a system combining analog front-end and micro-controller in order to isolate the vagus nerve electroneurogram and detect those bio-markers. The design is made according to two figures of merit, the added noise and the total power consumption, in order to make the system suitable for a long-term medical implantation. This work succeeded in detecting those bio-markers and getting a power consumption of 1.623 mW, the same range of power consumption as already existing implantable medical devices like cochlear or muscle stimulator. The results obtained allow to consider the developed system as a suitable solution to epilepsy detection. Experiments on real subjects still need to be conducted as the efficiency of this design was tested only on signals generated in laboratory.

Contents

List of abbreviations	vi
Introduction	1
1 Fundamentals and State of the art	4
1.1 Epilepsy overview	4
1.1.1 Symptoms	4
1.1.2 Causes	5
1.1.3 Refractory epilepsy	5
1.1.4 Available treatments	5
1.1.4.1 Medicine	5
1.1.4.2 Ketogenic diet	5
1.1.4.3 Surgery	6
1.1.4.4 Deep Brain Stimulation (DBS)	6
1.1.4.5 Vagus nerve stimulation (VNS)	6
1.2 VENG signal	6
1.3 Recording	7
1.3.1 Tripolar Cuff-electrodes	7
1.3.2 Ideal model	8
1.3.3 Cuff-imbalance	9
1.3.4 True tripole	11
1.3.5 Adaptive tripole	11
1.4 Introduction to the system architecture and implication of this work	12
1.4.1 System architecture and functionality	12
1.4.2 Position of this work	13
2 Analog front-end design and development	14
2.1 Input signals and specifications	15
2.2 Noise analysis	18
2.2.1 Noise of integrated IA	19
2.2.2 Analytical computation of the noise of the Sallen Key, AAF	20

2.2.3	Analytical computation of the noise of the discrete IA	23
2.2.4	Total input noise at input of discrete IA due to the discrete IA and the AAF	24
2.2.5	Evolution of the input referred noise with the partition of the gain	25
2.2.6	Simulation of the discrete IA noise with LTSpice and the MCP6241x op. amp. model	28
2.2.7	Selection of operational amplifier	31
2.2.8	Noise analysis with the selected operational amplifier	34
2.2.9	Final noise results for the AFE and comparison with the previous operation amplifier in term of noise and power consumption	35
2.3	Issue with the analog front-end frequency response	37
2.3.1	Issue of the frequency response	37
2.3.2	Solution to fix the overshoot	37
2.4	Analysis of the power consumption	41
2.4.1	Power of integrated IA	41
2.4.2	Power of discrete IA and AAF	41
2.4.3	Total power of the AFE	42
2.5	PCB design	43
2.6	Measures of the AFE	44
2.6.1	Tests of the frequency response and gains of the AFE	44
2.6.2	Measurement of the noise of the AFE	46
2.6.3	Measurement of the power consumption of the AFE	48
3	Digital back-End for the adaptive tripole	50
3.1	Functional overview of the digital back-End for adaptive tripole	50
3.2	Choice of MCU	51
3.3	Description of the embedded program operations	53
3.4	Choice of implementation for the embedded code	55
3.5	Working principle of the adaptive tripole embedded code	58
3.6	Characterization of the ADC channels	61
3.7	Time partition	63
3.8	Measurement of the power consumption of the MCU with the adaptive tripole embedded code	65
4	Test on the complete system, final results and position among other works	68
4.1	Measurement of the total noise of the system	68
4.2	Test of the complete system	70
4.2.1	Test with artefact	70

4.2.2	Test with ENG	74
4.3	Total power consumption	75
4.4	Comparison with other Works	78
4.5	Perspective	79
Conclusion		80
Bibliography		84
Appendix A: Information on the integrated IA		90
Appendix B: discrete IA equations		91
Appendix C: Verification of the noise density of the MCP6241 Op Amp LTspice model		94
Appendix D: AC-coupled analog front-end equation		96
Appendix E: Values of the component of the Discrete IA and AAF		98
Appendix F: Choice of the voltage and current references		99
Appendix G: detailed power consumption of the AFE and comparison with the previous and new discrete IA		101
Appendix H: PCB		103
Appendix I: analog adaptive tripole		105
Appendix J: code of the adpative tripole		106
Appendix K: histograms of the ADC noise for 12 bits of resolution		108
Appendix L: Tests on MCU to prove the functionality of the adaptive tripole embedded code and noises		110
Appendix M: SNR figures of the ENG signal		116

List of acronyms

AAF	Anti-Aliasing Filter
ADC	Analog to Digital Converter
AFE	Analog Front-End
CNS	Central Nervous System
DBS	Deep Brain Stimulation
DIA	Discrete Instrumental Amplifier
ENG	Electroneurogram
IIA	Integrate Instrumental Amplifier
MCU	Micro-Controller Unit
PCB	Printed Circuit Board
SNR	Signal to Noise Ratio
SIR	Signal to Interference Ratio
VENG	Vagus nerve Elctroneurogram
VNS	Vagus Nerve Stimulation

Introduction

Epilepsy is a neurological disorder characterized by disturbed electrical rhythms in the central nervous system (CNS) causing seizures [1]. The seizures are a period of unusual behavior with a wide variety of symptoms such as simple momentary loss of awareness or uncontrolled shaking movements. Epileptics crisis concern about 50 million people worldwide [4] and can touch everyone during their lifetime. While two-thirds of those people can be cured with anti-epileptic drugs, the rest need lifelong treatments to control their epilepsy [6]. In those one-third of patients that are drug resistant [6], a suitable solution is surgery but only 5-50 % are good candidates for it [28]. Alternative ways of fighting and reducing epilepsy for the rest of the people is to use stimulation of the brain as seizures are due to electrical rhythms disturbance. Two solutions stand out, the deep brain stimulation (DBS) and the vagus nerve simulation (VNS) [7]. The DBS is highly invasive as electrodes are directly and deeply inserted into the brain and then present a non-negligible risk for the patient [22]. The VNS uses hooked or cuff electrodes to stimulate the vagus nerve, a nerve directly connected to the brain, meaning that it is less invasive than the DBS. The VNS is then the one that is of interest in this work.

Stimulation of the vagus nerve can be regulated with an open loop that does not take the onset of the seizures into account or with a feedback-loop that stimulates only when seizures occur. The feedback loop requires to detect when the seizures occur and then to record the vagus nerve electroneurogram (VENS). To record the VENS, a new method [1] is highlighted that uses a true tripolar cuff-electrodes. The main issues are the recording of artefacts that are interfering signals and the low magnitude of VENS, around $7.1 \mu V_{rms}$ [8]. To get rid of those artefacts and to only keep the signal associated with the seizures [14][15], an adaptive tripole is used which is implemented on a micro-controller to minimize its size and power consumption in order to make it suitable for long term implant. This adaptive tripole uses a feedback loop to adapt gains to the imbalance. The imbalance is a word which refers to all non-idealities linked to the cuff and can be temporal showing the need of adaptive gains to cancel the artefact with the evolution of the imbalance. As the VENS is low in magnitude and the adaptive tripole is in digital space, the sensed signals by means of the true tripolar cuff-electrodes,

must be amplified before sampling it and the bandwidth restricted to the desired band to avoid high noise addition. This is done with an analogue conditioning chain.

The purpose of this work is to develop a suitable solution for long term implantation of a system which detects when bio-markers (neural signal) characteristic of the epilepsy occur in the vagus nerve. This solution is composed of an analog part used to amplify and restrict the bandwidth as well as a digital part that is implementing the adaptive tripole on a MCU. The development of this solution is composed of a characterization phase where features of the system are chosen in function of the needs and a designing phase which target at minimizing two figures of merit:

- Minimizing power consumption
- Minimizing noise

Those two phases are realized for both the analog conditioning chain and the digital adaptive tripole.

The contribution of this master thesis is divided in 5 chapters:

- **Chapter 1: Background and Fundamentals:** The fundamentals to understand how an epileptical crisis works and how to detect it are described. The way of working of the VNS, the true tripolar cuff electrodes and the adaptive tripole. At the end, the functionality of the system to be implemented and designed is explained as well as the different parts of the system and the targets of the design.
- **Chapter 2: Analog Front-End Design:** The analog part of the system is characterized and analysed with the aim to get a low power consumption while avoiding excessive noise. Once totally designed, a PCB will be done and a comparison between the simulations and experiments in laboratory is performed to ensure the good working.
- **Chapter 3: Digital Back-End for the adaptive tripole:** The functionality of the digital back-end is described (functional scheme) in terms of functions and then translated to the different modules (electrical scheme) of the MCU that should be used to accomplish these functions. The specifications of the MCU are then chosen in function of the needs for the implementation of the adaptive tripole. Finally, the coded is tested on different generated signals to ensure the good working of the implement and also characterizes in terms of noise added and power consumption.
- **Chapter 4** The analog and digital parts are brought together to characterize the full system. Then, the results are compared to other works on the same

implementation and to other biomedical implants to position epilepsy implant among other type of medical implants. Finally, some perspectives are give to help improving the system or to guide for other experiments.

- **Chapter 5:Conclusion:** The work is summarized with its results possible improvements and perspectives are given.

Chapter 1

Fundamentals and State of the art

This chapter aims at giving fundamentals to understand and to apprehend the epilepsy. It then gives the basics to record signals associated with epileptic seizures as well as the principles of the circuits used in this work. This includes their way of working, their advantages and their utilities in the case of seizures detection. Finally, it introduce the architecture of the system that will be designed in this work in a functional way as well as the context and the goals of this work.

1.1 Epilepsy overview

Epilepsy is a neurological disease that affects more than 50 million people worldwide [4]. In this first section, the epilepsy is over-viewed in terms of symptoms, causes and available treatments. The aim is to familiarize with the notions of epilepsy, seizures and medical treatments.

1.1.1 Symptoms

The epilepsy manifests through different symptoms occurring during seizures. The symptoms vary and depend on which region of the brain is the onset of the seizure and how the seizure spreads on the brain.

There are temporary symptoms such as disturbances of movements, confusions, convulsions and loss of awareness [3]. But also higher risk in some domains such as physical problems(bruising from injuries,), psychological problems, in fact people with epilepsy are more likely to develop depression or anxiety. Finally, higher rate of premature mortality is observable for people with epilepsy [3].

1.1.2 Causes

Up to 50 % of people diagnosed with epilepsy are idiopathic meaning that the causes are unknown [1].

For the other part, many different causes are known. It can be genetic with specific genes but in most cases genes are only partial reason of epilepsy [1]. Some genes make people more sensitive to environmental conditions that trigger seizures. It can be brain abnormalities such as tumors or strokes, head trauma, infectious disease as meningitis or encephalitis. It can finally be due to troubles during the development of the person such as prenatal injuries in case of poor nutrition, oxygen deficiencies, ... or congenital abnormalities associated to brain malformations [3].

1.1.3 Refractory epilepsy

About one third of people are drug resistant, meaning the crisis can not be cured and controlled with medication [7]. Despite the researches, scientific community still do not know why some patients suffer from refractory epilepsy.

There is then a need to find suitable solutions to lower the number of seizures. Combination of drugs or special diet achieve this need but are invasive in every day life. Alternatives exist, such as stimulation of the brain (deep brain stimulation), stimulation of the vagus nerve or removing brain area in cause of the seizures [7].

1.1.4 Available treatments

Different kinds of treatments exist to control seizures linked to epilepsy. A review of the different treatments available is good to see their way of working and limitations.

1.1.4.1 Medicine

A wide range of antiseizure drugs (ASD) exist. The aim of the drugs is to reduce seizure frequencies or cancel them. The drugs used are dependent on the patient according to the nature of epilepsy. The drugs have side effects on the patient. The most common are drowsiness, stomach upset and dizziness. As some types of epilepsy need a combination of drugs, therefore the number of side effects increase [19][20].

1.1.4.2 Ketogenic diet

As some patients are drugs resistant, alternatives are proposed to reduce the frequency of seizures. One way is by following a ketogenic diet [2]. It consists in lowering the sugar and protein intakes while increasing the amount of fat. If the

sugar intake is too low, the body starts to transform fat in sugar (ketoses). This reaction called ketosis, modifies the metabolism. This change affects the seizures frequencies and intensities.

1.1.4.3 Surgery

If the patient is drug resistant and that the seizures are identified to be caused by a brain lesion, surgery is suggested by doctors. It consists in removing the region causing the seizures only if the region is not in charge of speech, movements, memory and thinking. Surgery is the method with the highest success rate to remove seizures but has a lot of risks [20] [21].

1.1.4.4 Deep Brain Stimulation (DBS)

The DBS sends pulses to the brain via electrodes placed deeply in it. Those pulses are in fact mild electrical pulses and aim at controlling abnormal brain activities [19], [20]. The DBS is really efficient against seizures but is very invasive and risky as the electrodes are directly inserted deeply into the brain [22].

1.1.4.5 Vagus nerve stimulation (VNS)

In this case, the vagus nerve is stimulated instead of the brain [27]. In the same way electrical pulses are sent through electrodes placed on the vagus nerve that is a cranial nerved meaning it is directly connected to the brain [27]. It is less efficient than DBS but it is less invasive as the brain is not directly touched by the electrodes. The VNS is the one that is of interest in this work but only the part to detect the seizures in order to find when to stimulate the vagus nerve, is approached in this work.

1.2 VENG signal

The vagus nerve carries parasympathetic information and innervates multiple organs (Source [8]). As respiratory and cardiac changes are induced when a seizure occurs, the vagus nerve iss then found to be a good nerve to sense in order to detect those seizures (Source [8]). Moreover, the vagus nerve is directly connected to the brain where seizures are triggered. To detect the seizures, it is good to identify bio-markers associated. According to experiments realized in the work [8], those bio-markers take a triphasic shape as depicted on Figure 1.1.

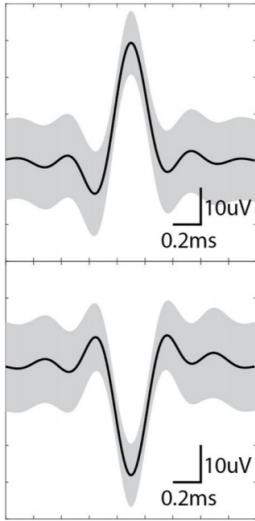


Figure 1.1: Triphasic shape of the biomarker in vagus nerve associated with seizures ([8])

In the VENG, those triphasic shape consists of high and low amplitude bursts synchronous to respiration and heartbeat respectively. The mean square amplitude and the peak amplitude depends on the use of hook or cuff electrode and the distance between the electrodes. In this work, the interest goes on the use of cuff-electrodes.

In average a spike duration is less than 1.5 ms. Its average mean square amplitude is $7.1 \pm 2.3 \mu\text{V}$ when using a tripolar cuff-electrodes with 2 mm space between electrodes ([8]). Its peak amplitude is different for the positive and negative spikes with $20.7 \pm 6.6 \mu\text{V}$ for the positive and $24.1 \pm 7.7 \mu\text{V}$ for the negative ([8]).

1.3 Recording

In this section, the different concepts associated with the recording of the signal are described. This includes the type of electrodes, the tripolar model, the linearization effect, the adaptive tripole and the imbalance.

1.3.1 Tripolar Cuff-electrodes

A tripolar cuff electrode is a cuff electrode composed of three electrodes that wrap around an organ in this case the vagus nerve as shown on Figure 1.2. As cuff-electrodes are stable and non invasive, they are suitable for long term implant [9],[10].

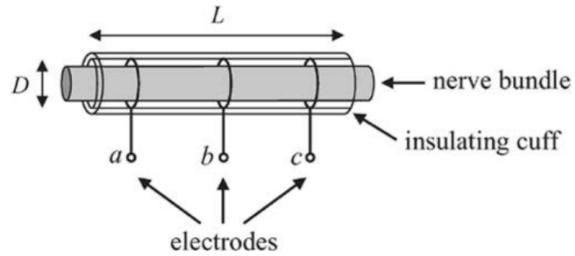


Figure 1.2: Tipolar cuff-electrodes surrounded nerve [61]

The amplitude of the signal sensed by the cuff electrodes is proved to decrease with inner radius of the cuff with a factor R^2 [23]. Plus the minimum size of the inner diameter of the cuff electrodes must be 20% larger than the organ diameter in order to avoid neuropathy [24]. Due to this, the sensed signal is very low and it is the main disadvantage of the use of cuff-electrodes. The tripolar design presented in [15] allows to tackle the problem of cuff imbalance as explained further.

1.3.2 Ideal model

The ENG signal propagates along the nerve with triphasic shape as seen previously. Inside the cuff, the tripolar cuff-electrodes senses a weighted sum of this triphasic potential. Figure 1.3 depicts that the amplitude of the ENG signal at the center electrode is higher than for the border ones [14].

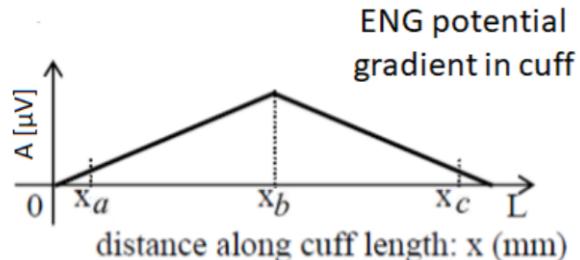


Figure 1.3: Schema of the amplitude of the ENG signal sensed by the tripole cuff-electrodes ([52], p_9)

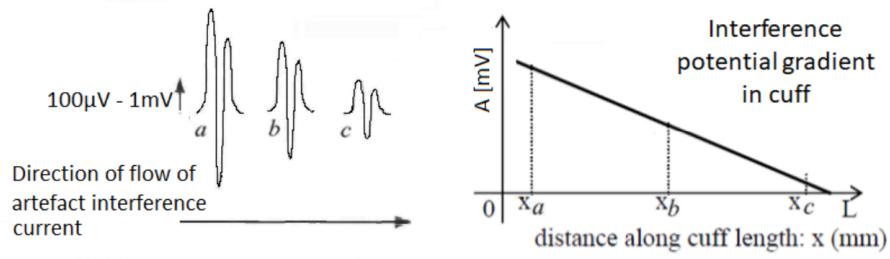


Figure 1.4: Linearization effect due to the tripolar cuff-electrodes. The signals on the left (Source [14]) represent the artefact signal measured at the three electrodes. The Figure on the right represent the linear potential gradient of the artefact signal in function of the distance along the cuff (Source [15]).

The Figure 1.4 highlights well why the tripolar cuff electrodes are used. In fact, the tripolar cuff-electrodes linearized the potential field inside the cuff. It is called linearization effect. This potential field is due to all external sources. Those sources can be cardiac, breath, muscular, ... for the main ones and are called artefacts. If the tripolar cuff-electrodes is considered as perfect without any mismatch between the three electrodes, with the same distances between each pair of consecutive electrodes and that the tissue of the nerve inside the cuff is perfectly homogeneous, the following relation take place if only the artefacts are considered (not the neural signal) [14][15]:

$$|V_a - V_b| = |V_b - V_c| \quad (1.1)$$

1.3.3 Cuff-imbalance

In reality, the sensed artefact voltage through the nerve does not perfectly follow the linearization due to non-idealities [15]. Those non-idealities are called cuff-imbalances. It is called imbalance as it is due to asymmetries inside the cuff. Asymmetries can be due to border effect, tissue growth or inflammation, asymmetry of the electrodes [26] and the orientation towards the dipole artefact source, [15]. Figure 1.5 depicted the effect of the imbalance on the evolution of the potential of the artefact sensed by the electrodes of tripolar cuff-electrodes. In this case the voltage between each pair of successive electrodes is not equal.

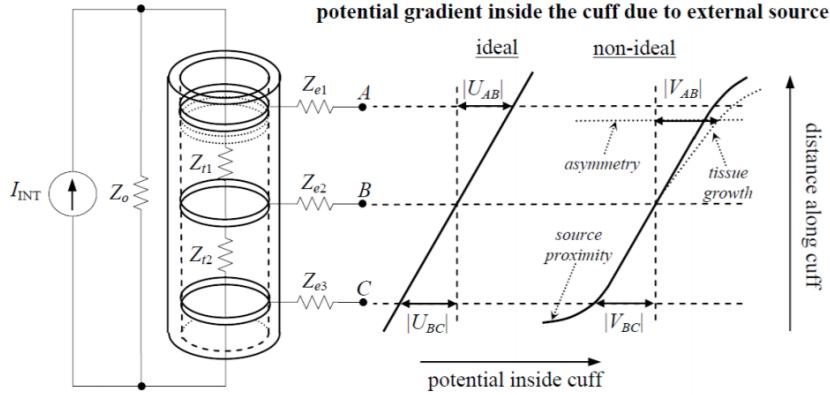


Figure 1.5: Ideal cuff linearization vs cuff linearization with imbalance[15]

To take consideration of these imbalances, a factor $Ximb$ is introduced in equation 1.1 that is not valid anymore in the case of imbalance. In fact, the impedance between each pair of successive electrodes is not the same. Defining Z_{t1} the impedance of the tissue inside the cuff between the pair A-B and Z_{t2} , the impedance if the tissue inside the cuff between the pair B-C (Source [15]), it results due to the imbalance that $Z_{t1}Z_{t2}$. The equation can be rewritten:

$$Ximb = \frac{Z_{t1} - Z_{t2}}{Z_t} \quad (1.2)$$

Where Z_t is the mean of the two values of impedance. Moreover, now, Z_{t1} and Z_{t2} can be expressed in function of $Ximb$ and Z_t , [15].

$$Z_t = \frac{Z_{t1} + Z_{t2}}{2} \quad (1.3)$$

$$Z_{t1} = \frac{(1 + Ximb)Z_t}{2} \quad (1.4)$$

$$Z_{t2} = \frac{(1 - Ximb)Z_t}{2} \quad (1.5)$$

Finally, the factor of imbalance $Ximb$ can be expressed by mean of the sense voltage by the different electrode of the tripolar cuff-electrode and the relation 1.1 can be rewritten, [15].

$$Ximb = \frac{|V_A - V_B| - |V_B - V_C|}{|V_A - V_B| + |V_B - V_C|} \quad (1.6)$$

$$(1 + Ximb)|V_A - V_B| = (1 - Ximb)|V_B - V_C| \quad (1.7)$$

1.3.4 True tripole

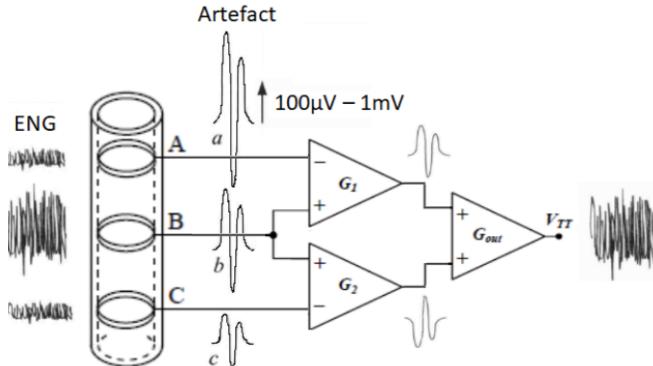


Figure 1.6: Analog implementation of the true tripole ([14], [15])

The need of only retrieving the ENG signal at the output when sensing the vagus nerve with tripolar cuff-electrode , brings on the use of tripole conditioning chain. The one used in this work, is the true tripole model. The true tripole implementation can be seen on Figure 1.6, it is composed of three amplifiers. At the first stage on two different canals, the border electrode sensed signals are subtracted to the middle electrode sensed signal and multiplied by a gain G1 or G2. The second stage outputs the difference between the two obtained signal of the first stage affected by a last gain G_{out} . As the result of this conditioning only an amplified version of the ENG signal should be acquired at the output ([14], [15]). The output is computed as follow:

$$V_{out} = G_{out}(G1(V_A - V_B) + G2(V_B - V_C)) \quad (1.8)$$

If the artefact was perfectly linearized both gain G1 and G2 should be equal to 1 and the output if only artefact was present would be $V_{out,if \text{ only } artefact} = 0[V]$. The true tripole has also the advantage to be very insensitive to impedances Z_{e1} , Z_{e2} and Z_{e3} (on Figure 1.5) that are the electrode-tissue contact impedance (Source [15])

1.3.5 Adaptive tripole

The adaptive tripole is an adaptation of the true tripole that takes the imbalance into account. In case of imbalance, the gains G1 and G2 should differ. They should be adapted to the imbalance. This is called "adaptive tripole". In this model G1 and G2 are variables that depend on X_{imb} , the cuff-imbalance. Those gains are

adapted with a feedback loop that compute the Ximb to follow its evolution with time (Source [14], [15]).

$$G1 = G0.(1 + Ximb) \quad (1.9)$$

$$G2 = G0.(1 - Ximb) \quad (1.10)$$

This model suits perfectly in the case of long time implant. In fact, the tissue encapsulated by the cuff-electrodes can grow with time or the electrodes can move or degrade.

1.4 Introduction to the system architecture and implication of this work

1.4.1 System architecture and functionality

The system developed in this work aims at implementing the vagus nerve electroneurogram sensing and at isolating it from the artefacts in order to detect the bio-markers linked to epileptic seizures. To this aim, the system combines an analog front-end (AFE) and a digital back-end. The AFE is used to amplify, to filter and to go from the tripolar sensing of the VENG signal to a differential one. The amplification is needed as the ENG signal is low in magnitude (μV range) [8]. After the AFE, the digital back-end takes over and do the job of the adaptive tripole. The main motivations of implementing the adaptive tripole on a micro-controller, are its small size and its low power consumption making it more suitable for long term implantation. Both have different functionalities and their respective functions are depicted on figure 1.7.

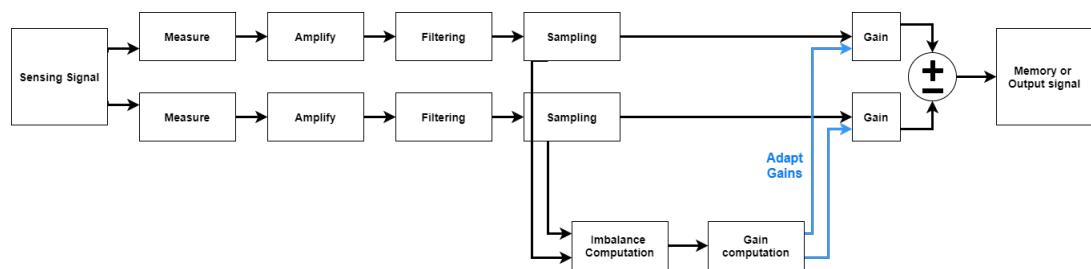


Figure 1.7: Functional scheme of the system for VENG sensing and isolating

First the signal is sensed by the tripolar cuff-electrodes. After, the AFE takes over and measures the signal coming from the tripolar cuff-electrodes. Once the signal is measured, the AFE amplifies and filters it. After the filtering, the digital back-end comes in action and first samples the filtered and amplified analog voltage.

Next, it processes the input samples with the adaptive tripole embedded code. It discards the artefacts and isolates the ENG signal. Finally, it outputs the results that is supposed to contain only the amplified ENG signal. Also, at each running of the adaptive tripole embedded code, the digital back-end compute the imbalance and adapt the gains subsequently.

1.4.2 Position of this work

This work follows up the previous work on the same subject of Louise Coppieters [52]. The aim of this previous work was to create a miniaturized system for epileptic seizures detecting with a digital implementation of the adaptive tripole.

This work continues the previous thesis with the target of optimizing the system according to two figures of merit namely a good SNR and a low power consumption. This is done by designing the AFE and the digital back-end separately. The design of the AFE concentrates on reducing the noise added and the power consumption while the digital back-end is mainly designed according to the power consumption.

Chapter 2

Analog front-end design and development

The first part of the system that is designed is the analog front-end. An analog conditioning chain is desired as the ENG signal sensed is in the order of μV . It must be amplified before being sampled by the ADC. The ADC uses a reference voltage of 1.5V (in this work as stated in the chapter 3) and the resolution of the ADC is 12 bits (see chapter 3). It means that the least significant bit is $366 \mu\text{V}$. There is also a need to reduce the bandwidth to the minimum possible in order to reduce the noise added. The gain and the bandwidth condition the analog front-end.

First it is good to have a look on the conditioning chain that will be used in this application. It is composed of three parts, a custom integrated differential instrumentation amplifier (Integrated IA) previously designed in the ECS group at UCLouvain, an instrumentation amplifier built using discrete components (discrete IA) and an anti-aliasing filter at the end before the sampling with the ADC of the MCU. This conditioning chain was the one used during a previous work on the same subject (Source [52]) and is depicted in figure 2.1. The goal of the integrated IA is to amplify the input signal with low power consumption. The goal of the discrete IA is to go from tripolar to differential signal before being processed by the adaptive tripole implemented in the digital back-end. The AAF is there to cut high frequencies to avoid aliasing before sampling the signals.

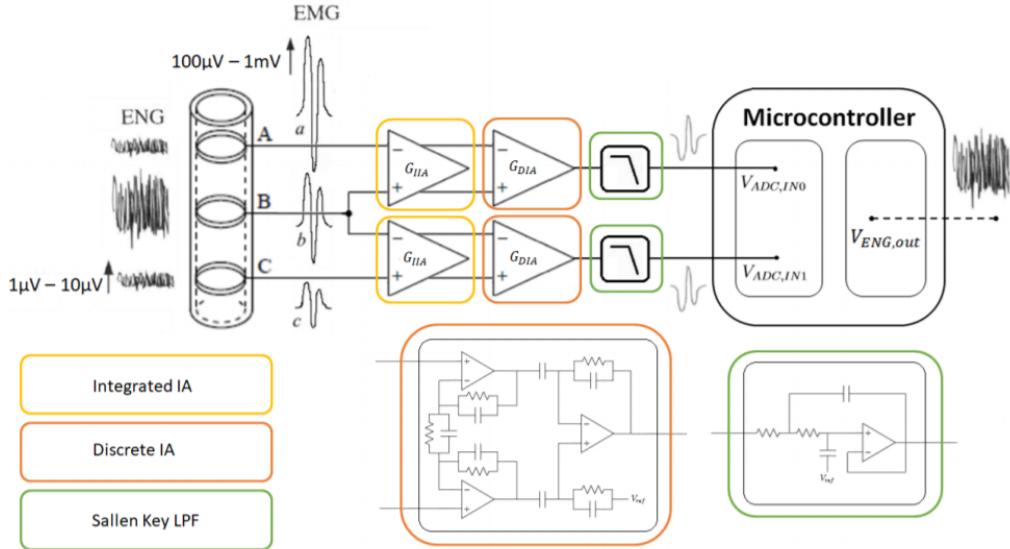


Figure 2.1: Schema of the analog conditioning chain, Picture from the TFE of Louise Coppieters de Gibson [52]

In the AFE, the noise can only be optimized on the discrete IA and the AAF parts as the Integrated IA is fixed (already developed by the ECS team). This is why only these parts will be analyzed in details and optimized.

In this chapter, the AFE is totally analyzed and designed. First, the noise is computed analytically and optimized according to the partition of the gains between the different stages of the AFE. Next, operational amplifiers are selected according to their noise density and power consumption. After, the power consumption is estimated. Once the design of the AFE is done, a PCB is created. Finally, tests and measurements are done on the PCB containing the AFE.

2.1 Input signals and specifications

Before choosing the specifications, the different input signals, neural (ENG) and artefacts, must be known in term of amplitude and bandwidth. The amplitude of the neural signal was already given in the previous chapter according to [8]. The Table 2.1 brings the other needed specifications according to two works found on the subject.

	Rahal [14]	Triantis [15]
ENG bandwidth [Hz]	800 - 10k	500 - 10k
ENG amplitude [μ V]	1 - 10	1 - 7
Artefact Bandwidth [Hz]	0 - 3 k	1 - 3 k
Artefact Amplitude [μ V]	100 - 1000	1000
Artefact Amplitude between two electrodes [μ V]	\	100

Table 2.1: Specifications of the ENG and Artefact

From these specifications, the needed gain can be chosen. The MCU is powered by 1.8 V and the ADC uses an internal voltage reference of 1.5 V (see Chapter 3). As the amplifiers used will be powered by 1.8 V, the DC voltage chosen for the dynamic of the signal at the input of the ADC, is 0.9 V. The maximum dynamic allowed is then 0.6V of amplitude for the amplified signal. The limiting factor when amplifying is the amplitude difference of the artefacts between two consecutive electrodes and due to the linearization effect. It is stated in Table 2.1 that this amplitude is $\approx 100 \mu$ V. To avoid saturation a safety coefficient of 25 % (totally arbitrary) is applied and it is decided to design the needed gain considering this safety coefficient then 125μ V will be considered. This leads to a desired total gain of:

$$G_{tot} = \frac{0.6V}{125\mu V} = 4800 \left[\frac{V}{V} \right] \quad (2.1)$$

The different specifications considered in this work for the conditioning chain are listed below. They will constraint all the design of the AFE.

- Bandwidth(BW)= [500 , 10 000] Hz
- Neural Signal = [500 , 10 000] Hz and average of $7.1 \pm 2.3\mu$ V and amplitude of $20.7 \pm 6.6\mu$ V (Source:[8])
- Amplitude at Input of MCU = [0.3,1.5] V (supplied by 1.8V)
- Total gain of the conditioning chain = 4.8×10^3 V/V

Concerning the choice of the ENG signal amplitude, it is not chosen in the Table 2.1 as a more recent work on the use of the cuff-electrode for sensing VENG ([8]) was found and giving new values (see chapter 1).

As the integrated IA that is already design by the ECS team of UCLouvain, is available in four different configurations that cannot be change, the choice of the configuration used in this work can already be done. The integrated IA being the first stage of amplification, it is good that the gain is high in order to cut the noise of the following stages. Then for this purpose the configuration with the higher gain was chosen, configuration 4, (see annexe A: Figure 4.3). The gain of this configuration is the highest available, 63.8 V/V but it has also the highest power consumption, $23.9 \mu\text{W}$ per channel. As it is an integrated IA the power consumption is however very small compared to other parts of this conditioning chain as it will be seen further. Then even if it would be better to have a lower power consumption, as it consumes only $23.9 \mu\text{W}$ per channel, it is not a big issue while the noise of this integrated IA is, as it is the first stage of amplification. The integrated IA is a fully differential gain stage and its equations can be found in appendix A.

Concerning the discrete IA and the AAF, the noise can be optimized by choosing the amplifiers and the partition of the gains among the different amplification stages . In fact, the discrete IA is composed of two amplification stages namely "input buffer" and "differential stage" as stated on figure 2.2. The discrete IA and the AAF are better illustrated on Figure 2.2, the circuit is the one used on the previous work on the same subject (Source [52]). The goal of the discrete IA is to go from a tripolar to differential. As the integrated IA already amplifies by 63.8 [V/V] the input signals, the discrete IA and the AAF still need to amplify by a factor $75.23 \approx 75$ as the total gain is 4.8×10^3 V/V as specified before.

The AAF being the last stage of the conditioning chain, it does not need to amplify the signal to avoid adding too much noise. It is then chosen to have a gain of 1.

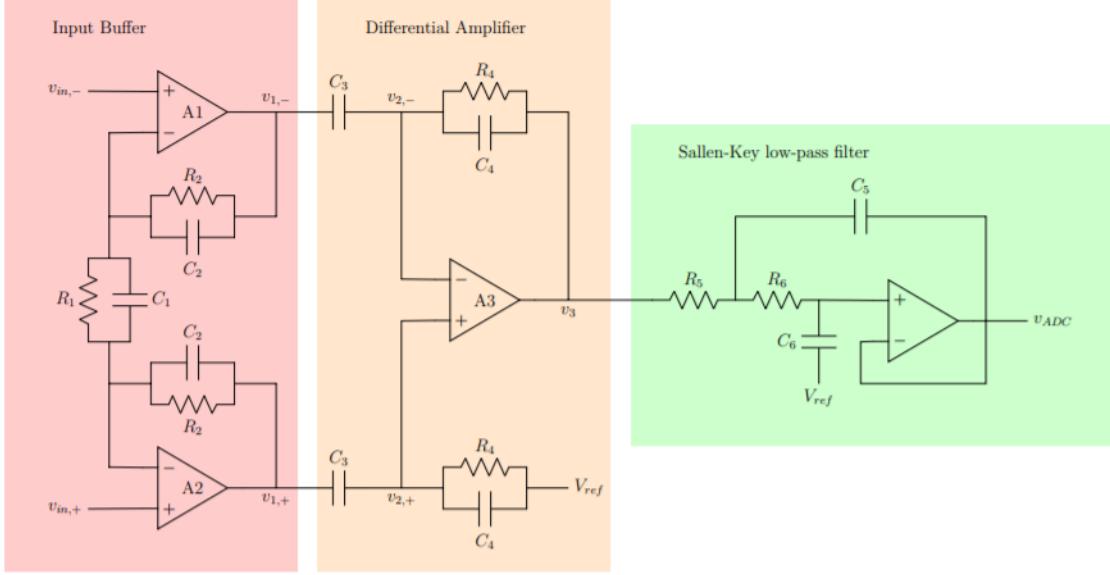


Figure 2.2: Discrete IA and AAF, picture come from [52]

The total gain of the conditioning chain is composed of the multiplication of the gains associated to the different parts and is expressed as follow:

$$G_{tot} = G_{IIA}G_{IB}G_{Diff}G_{AAF} \quad (2.2)$$

$$(2.3)$$

where the definitions of the notations are the following:

- $G_{Integrated-IA} = G_{IIA} = 63.8V/V$
- $G_{Discrete-IA} = G_{DIA} = G_{Input-Buffer}G_{Differential-Amplifier} = G_{IB}G_{Diff} = 75V/V$
- $G_{Sallen-Key} = G_{AAF} = 1V/V$

2.2 Noise analysis

In epilepsy detection, the neural signal is in the order of $7.1 \pm 2.3 \mu V_{rms}$ with peaks of $20.7 \pm 6.6 \mu V$ when sensed by tripolar cuff-electrodes spaced of 2 mm between each pair of electrodes [8]. As this signal is very low, care must be taken to avoid that the noise added by the analog conditioning chain is too great and

averts correct detection of the ENG signal.

The degrees of freedom to limit the noise are the partition of the gains of the different stages of the AFE and the choice of operational amplifiers used. When choosing these amplifiers, another criterion comes into consideration, it is the need of low power consumption in order to get a suitable system for long time implantation.

In this section the noise of the analog front-end will be first computed analytically in order to emphasize the effect of the degrees of freedom on the total input referred noise. Then simulation of the conditioning chain is made with LTspice and the current amplifier MCP624x [33] (used in the previous work [52]) to observe the impact of the gains on the input referred noise and confirm analytical results. After a choice of new amplifiers will be done to enhance the input referred noise compared to the amplifier MCP624x [33] that was used for all the circuit until now. The choice will be made in the aim of reducing the power consumption without increasing too much the input referred noise. Finally, the choice of new amplifiers will be confirmed with LtSpice simulations.

2.2.1 Noise of integrated IA

The noise added by the integrated IA/input gain stage with low power consumption, is computed by considering the thermal noise which has a noise density of $16.26 \frac{nV}{\sqrt{Hz}}$ and the Flicker noise (see Annexe A figure 4.10). The total noise is computed as follow with a considered bandwidth of 12.6 kHz, see section 2.2.2 "Analytical computation of the noise of the Sallen-Key, AAF":

$$E_{n,thermal} = e_{n,th} \sqrt{BW} \quad (2.4)$$

$$E_{n,flicker} = e_{n,f_0} \sqrt{f_0} \sqrt{\log(\frac{f_H}{f_L})} \quad (2.5)$$

$$E_{tot} = \sqrt{E_{n,thermal}^2 + E_{n,flicker}^2} \quad (2.6)$$

with the following meaning for the notations:

- f_0 is the frequency in the flicker zone where we take the value of the noise density for the flicker noise
- e_{n,f_0} the voltage noise density at f_0
- $f_l = \frac{1}{aperture-time}$ is the lower frequency on the noise density graph

- f_H is the corner frequency
- $e_{n,th}$ = voltage noise density in the thermal noise region

The noise values obtained are presented in the Table 2.2.

	Noise [μVrms]
$E_{n,flicker}$	1.4
$E_{n,thermal}$	1.984
E_{tot}	2.43

Table 2.2: Noise of the integrated IA

2.2.2 Analytical computation of the noise of the Sallen Key, AAF

The noise added by the AAF is computed analytically to see on what it depends. This filter is designed to have a cut off frequency of 10 000 Hz according to the desired bandwidth stated in the specifications of the ENG in section 2.1.

To simplify the design, it was chosen that the two capacitors have the same values and the same for the resistors. The choice of the values of the components, is conditioned by the need of the cut-off frequency according to $f_c = \frac{1}{2\pi RC}$. The value chose are the following:

	Cut-off frequency	R	C	Q (quality factor)
Value	10 kHz	16 k Ω	1 nF	0.5

Table 2.3: Design values of the AAF

and the transfer function is the following:

$$\frac{1}{s^2 R^2 C^2 + 2RCs + 1} \quad (2.7)$$

As the -3dB gain is obtained at 12.6 kHz, the bandwidth considered for the computation of the noise will be 12.6 kHz.

Voltage noise

The voltage noise associated with the operational amplifier is composed mainly of 2 parts, the flicker noise and the thermal noise. As the lower bound of the BW is low, 500 Hz, both are taken into consideration during the computation of the noise. The noise gain affecting the input voltage noise of the AAF:

- voltage noise gain factor $\frac{(j\omega RC+1)(j\omega RC+2)-1}{(j\omega RC+1)^2} \approx 1$ in the BW

As for the Integrated IA, the thermal, flicker and total noise are computed as follow:

$$e_{th} = e_{n,th} \sqrt{1.22 * BW} \text{ as it is second order filter} \quad (2.8)$$

$$e_{flick} = e_{n,f_0} \sqrt{f_0} \sqrt{\log\left(\frac{f_H}{f_L}\right)} \quad (2.9)$$

$$e_{tot} = \sqrt{e_{th}^2 + e_{flick}^2} \quad (2.10)$$

$$= \frac{e_n \sqrt{1.22BW + f_0 \log\left(\frac{f_H}{f_L}\right)}}{G_{IB}G_{Diff}G_{AAF}} \quad (2.11)$$

The notations are the same that were used to compute the noise of the integrate IA and to facilitate the analytical analysis with Matlab, f_0 was chosen at corner frequency such that $e_{n,f_0} = e_{n,th}$. The last expression for the total noise (equation 2.11) is referred at the input of the discrete IA. Meaning that the output noise of the AAF computed according to formula 2.8 - 2.10, is divided by the total gain of the dcrete IA. A last comment, the factor 1.22 comes from the considered equivalent noise bandwidth as a second order low pass filter is used.

Current noise

The operational amplifiers experiments also a noise associated with the current and is referred to a voltage through the gain that the current experiment to the output of the amplifier.

The noise gain factors of the current noise associated with the positive and negative inputs of the amplifier are the followings, i_n is the noise density:

- $i_{n,+}$ noise gain factor = $\frac{R}{(1+j\omega RC)^2} \approx 399$ in the BW
- $i_{n,-}$ noise gain factor = $R_{out,Op} = 15\Omega$ (source [33])

Then the voltage input referred noise due to those current noise density is expressed as follow:

$$e_{i,+} = \frac{i_{n,+}\sqrt{BW}399}{G_{IB}G_{Diff}G_{AAF}} \quad (2.12)$$

$$e_{i,-} = \frac{i_{n,-}\sqrt{BW}R_{out,Op}}{G_{IB}G_{Diff}G_{AAF}} \quad (2.13)$$

Resistor noise

Taking the conventions for the resistors number of the Figure 2.2:

- R_5 noise gain factor = $\frac{1}{(j\omega RC+1)^2} \approx 1$ in the BW
- R_6 noise gain factor = $\frac{1}{(j\omega RC+1)^2} \approx 1$ in the BW
- $e_{n,R_{rms}} = \sqrt{4k_B T R \Delta f}$

It leads to the following values for the noise of the resistors, noticing that R_5 is chosen to be equal to R_6 , see Table 2.3:

$$e_{n,R_{rms}} = 4k_B T R \Delta f = 1.62 \mu V_{RMS} \quad (2.14)$$

Capacitance noise

Always taking the convention of the Figure 2.2

- C_5 noise gain factor = $\frac{j\omega RC(j\omega RC+2)}{(j\omega RC+1)^2} \approx 0.08$ in the BW
- C_6 noise gain factor = $\frac{1}{(j\omega RC+1)} \approx 1$ in the BW
- $e_{n,C} = \sqrt{\frac{k_b T}{C}}$

It leads to the following values for the noise of the capacitors as C_5 equals to C_6 , see Table 2.3:

$$e_{n,C} = 2.03 \mu V_{RMS} \quad (2.15)$$

Total noise at input of discrete IA due to salien key

The BW being high and the total noise being the sum of the squared, all noises can be neglected in front of the voltage noise. In fact, even if the current noise depends also on the square root of the BW, the current noise density i_n is always much smaller than the voltage noise density of the amplifiers and the noise gain factors of the current noise are not sufficiently high to compensate.

$$e_{n,tot,AAF} = \frac{e_{n,AAF} \sqrt{1.22BW + f_0 \log(\frac{f_H}{f_L})}}{G_{Diff} G_{IB} G_{AAF}} \quad (2.16)$$

2.2.3 Analytical computation of the noise of the discrete IA

The design of the discrete IA / tripolar to differential stage, aims at reducing the noise added by it. To see which parameters influence the total noise added by it, an analytical computation of its total noise is done. As for the AAF as voltage noise of the amplifiers is much bigger than the noise associated with the current noise density and with the components will not be taken into account

More over, as the noise related to the components is independent of the noise of the amplifier, the apportionment of the gain between the 2 stages of the discrete IA can be found by minimising only the noise associated with the amplifiers. Then, an optimum can be found for the noise associated with the components considering fix gain and fix cut-off frequencies. Finally, the total noise will be the sum of both as follow because they are independent:

$$e_{n,tot,DIA} = \sqrt{e_{n,amplifier,DIA}^2 + e_{n,components,DIA}^2} \quad (2.17)$$

Voltage noise of the differential amplifier stage

Recalling that:

- f_0 is the frequency in the flicker zone where we take the noise density
- e_{n,f_0} the voltage noise density at f_0
- $f_l = \frac{1}{aperture-time}$ is the lower frequency on the noise density graph
- f_H is the corner frequency
- $e_{n,th}$ = voltage noise density of the amplifier in the thermal noise region

The noise associated with the differential amplifier stage of the discrete IA, referring to figure 2.2 can be computed as follow:

$$e_{th} = e_{n,th} \sqrt{1.22 * BW} \quad (2.18)$$

$$e_{flick} = e_{n,f_0} \sqrt{f_0} \sqrt{\log\left(\frac{f_H}{f_L}\right)} \quad (2.19)$$

$$e_{n,tot,Diff} = \sqrt{e_{th}^2 + e_{flick}^2} \quad (2.20)$$

$$= \frac{e_{n,A3} \sqrt{1.22BW + f_0 \log\left(\frac{f_H}{f_L}\right)} (1 + G_{Diff})}{G_{Diff} G_{IB}} \quad (2.21)$$

where $(1+G_{Diff})$ is the noise gain affecting the voltage noise of this amplifier. To facilitate the analytical analysis with Matlab, f_0 was chosen at corner frequency such that $e_{n,f_0} = e_{n,th}$.

Voltage noise of the input buffer stage

The noise for the two amplifiers of the input buffer stage is not the same as for the differential amplifier stage as the noise gain affecting the voltage noise is different and equal to $G_{IB}G_{Diff}$ in this case. It then gives the following input voltage noise at the input of the Discrete IA.

$$e_{th} = e_{n,th}\sqrt{1.22 * BW} \quad (2.22)$$

$$e_{flick} = e_{n,f_0}\sqrt{f_0}\sqrt{\log\left(\frac{f_H}{f_L}\right)} \quad (2.23)$$

$$e_{n,tot,IB} = \sqrt{e_{th}^2 + e_{flick}^2} \quad (2.24)$$

$$= \frac{e_{n,A1}\sqrt{1.22BW + f_0\log\left(\frac{f_H}{f_L}\right)}(G_{IB}G_{Diff})}{G_{Diff}G_{IB}} \quad (2.25)$$

To facilitate the analytical analysis with Matlab, f_0 was chosen at corner frequency such that $e_{n,f_0} = e_{n,th}$.

2.2.4 Total input noise at input of discrete IA due to the discrete IA and the AAF

As the noise associated with the different operational amplifiers are independent, the total noise computed easily by mean of the square root of the sum of the square of the different noise sources. Here the amplifiers A1 and A2 are considered to be the same for matching reasons. With the gain of the AAF already chosen to be one, only the partition between the two stages of amplification of the discrete IA plays a role in the total noise.

Voltage noise

$$e_{vn,tot}^2 = \left(2(e_{n,A1,A2,IB} \frac{\sqrt{1.22BW + f_{0,IB} \log(\frac{f_{H,IB}}{f_{L,IB}}) * G_{IB}G_{Diff}}}{G_{IB}G_{Diff}})^2 \right. \\ \left. + (e_{n,A3,Diff} \frac{\sqrt{1.22BW + f_{0,Diff} \log(\frac{f_{H,Diff}}{f_{L,Diff}}) * (1 + G_{Diff})}}{G_{IB}G_{Diff}})^2 \right. \\ \left. + (e_{n,AAF} \frac{\sqrt{1.22BW + f_{0,AAF} \log(\frac{f_{H,AAF}}{f_{L,AAF}})}}{G_{Diff}G_{IB}G_{AAF}})^2 \right)$$

This analytical formula highlights that the total noise referred at the input of the discrete IA, depends on the voltage noise density of the amplifiers and on the partition of the gain among the two stages of amplification of the discrete IA through the voltage noise gain.

2.2.5 Evolution of the input referred noise with the partition of the gain

In this section, the aim is to analyse the impact of the distribution of the gain using the analytical formula computed previously and a software like Matlab to simulate. The need to low input referred noise is important in this context as the sensed signal, ENG, is very low $\approx 7.1 \mu V_{rms}$.

To analyse the impact of the gain partition, we can first discard the part associated with the noise of the AAF because its gain is chosen to be 1 and whatever the distribution of the gain between the two stages of the discrete IA is, the noise associated with the AAF will be divided by 75, the total gain of the discrete IA, when taking the reference for the noise at the input of the discrete IA. The part of the AAF can be omitted when analytically computing because, the three noise sources are independent.

To analyse the noise, it is good to isolate the variables that impact it. From the formula of the total noise that was computed before, the variables on which it is possible to play are the voltage noise density of the amplifiers and the partition of the gains. Before simulating with Matlab, it was considered that the two amplifiers of the input buffer stage are the same for symmetry (matching) as it is a fully differential, and that the noise voltage density of the amplifier of the differential stage (referring to the convention taken on Figure 2.2) is the one of the amplifier

used for the input buffer stage (referring on the same Figure 2.2) multiplied by a factor \mathbf{X} meaning it is considered that the amplifier of the last stage might be different from the ones of the first stage. Leading to :

$$e_{n,A1,IB} = e_{n,A2,IB} = \mathbf{X}e_{n,A3,Diff} \quad (2.26)$$

$$e_{n,A1} = e_{n,A2} = \mathbf{X}e_{n,A3} \text{ Smaller notation for convenience} \quad (2.27)$$

Another thing, good to make, is to express the gain of the 2 stages of the discrete IA in function of only one stage (detailed computation of the discrete IA gains can be seen in Appendix B) :

$$G_{DIA} = G_{IB}G_{Diff} = 75 \quad (2.28)$$

$$G_{IB} = Y \quad (2.29)$$

$$\Rightarrow G_{Diff} = \frac{75}{G_{IB}} = \frac{75}{Y} \quad (2.30)$$

To facilitate the analyse, it was also chosen that the constant associated with the flicker noise (f_0 , f_H and f_l) are the same for all amplifiers.

It finally leads to the following expression:

$$e_{vn,tot} = e_{n,A1} \sqrt{1.22BW + f_{0,D} \log\left(\frac{f_{H,D}}{f_{L,D}}\right)} \sqrt{2 + \left(X \frac{(Y+75)}{75Y}\right)^2} \quad (2.31)$$

$$\propto \sqrt{2 + \left(X \frac{(Y+75)}{75Y}\right)^2} \quad (2.32)$$

$$\propto \sqrt{2 + X^2 \frac{(Y+75)^2}{(75Y)^2}} \quad (2.33)$$

$$(2.34)$$

This expression highlights well that to have the minimum input noise the multiplicative term must be as low as possible.

The simulation on Matlab was done assuming that the gain is constant over all the BW that is not the case in reality as the gain does depend on the frequency (see Appendix B). Then, the results are closer to reality if we consider only the part of the bandwidth in which the gain is maximal and equals to 75 . It is also considered that the cut-off frequencies remain the same for the different gain partition which is not true as the cut-off frequencies change with the values of the components that depend on the values of the gain desired on one stage.

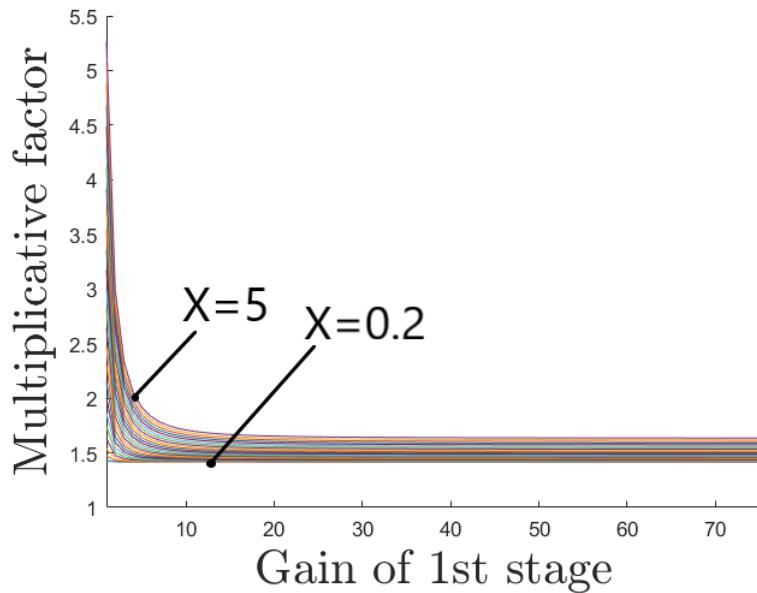


Figure 2.3: Multiplicative factor of noise density in function of the gain of the first stage: Full scale [1,75]

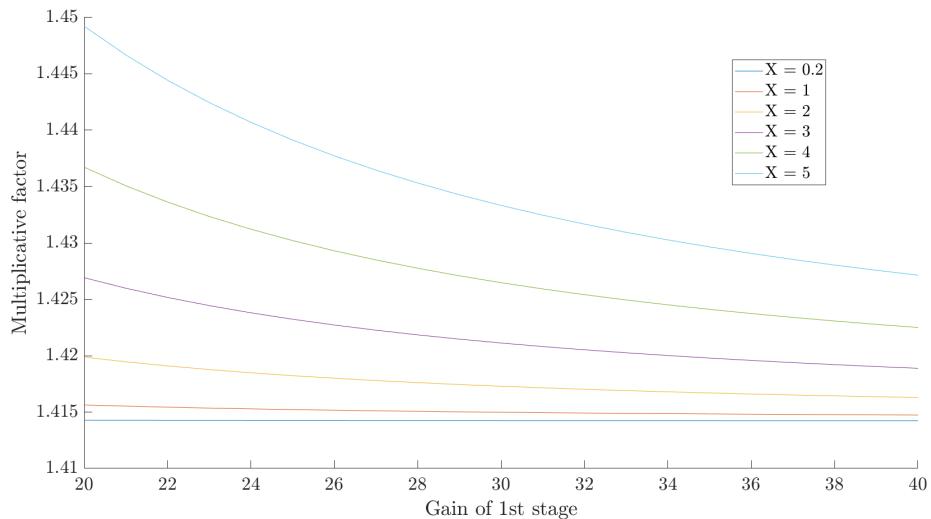


Figure 2.4: Multiplicative factor of noise density in function of the gain of the first stage: limited scale [20,40] for $X \in [0.2,1,2,3,4,5]$

This figure 2.3 represents the evolution of the multiplicative factor with the gain of the first stage of the discrete IA/tripolar to differential stage, for different values

of the voltage noise density of the amplifier used in the second stage of this discrete IA, $X \in [0.2, 5]$ with a step of 0.2 . As it can be seen, after a certain amount of gain for the first stage of the discrete IA, the noise reduction is not significant. Then it is good to not put all the gain on the first stage as the minimum GBWP needed to make so is also increasing. It is not desired because the goal is to have a suited devices for long term then a low power consumption is needed. The power consumption increase with the GBWP as a bigger current is needed to increase the GBWP. Concerning the voltage noise density of the second stage of the discrete IA, according to simulations the multiplicative factor does change that much with the factor X. On figure 2.4, going for $X = 0.2$ to $X = 5$ for a gain of 30, changes only the multiplicative factor from 1.41 to 1.43. This highlights that is the gain of the first stage of the discrete IA is correctly chosen, the change in voltage noise density between the amplifiers of the first stage and the one of the second stage, has not a big impact on the total input noise.

The limited scale version (figure 2.4) allows to see that above a gain of 30, the reduction of multiplicative factor is not significant. Then a good choice for the gain of the first stage would be around 30, allowing to have a good impact on the minimization of total input referred noise without requiring too high GBWP and the cost overhead in power.

2.2.6 Simulation of the discrete IA noise with LTSpice and the MCP6241x op. amp. model

To have a more accurate measurement of the input referred noise and confirm the analytical results of the previous section, simulations of the discrete IA was realised on LTspice. As the noise associated with the amplifiers is desired to be isolated from the noise of the components, the LTspice simulation will be run with components being noiseless. To be sure that the model used in LTspice represents well the noise due to the MCP6241 Op amp, simulation for the voltage noise density of this model has been realized and can be seen in Appendix C. The result is a perfect fit between the voltage noise density curve of the LTspice model and the one of the datasheet ([33]).

In this subsection, it is desired to check with LTspice simulations, the results obtained analytically concerning the distribution of the gain between the two stages of the discrete IA.

The target of the simulations is to establish the evolution of the noise referred at the input of this discrete IA with the partition of the gain (75 V/V) between the two stages of this discrete IA. During the simulations, all the operational amplifiers

are the same and are MCP6241x that has the following characteristics.

Specifications	GBWP	Input Voltage noise density	Input Current noise density
Values	550 [kHz]	45 [nV/ \sqrt{Hz}] at 1 kHz	0.6 [fA/ \sqrt{Hz}] at 1 kHz

Table 2.4: Characteristics of the MCP6241 Op-Amp from datasheet [33]

The fact that the GBWP is 550 kHz is a constraint compared to the analytical case. It leads to a maximum gain that can be achieved by one amplifier in closed loop.

$$G_{max} = \frac{GBWP}{BW} \quad \text{with } BW \approx 10 \text{ kHz for the neural signal} \quad (2.35)$$

$$= 55 \quad (2.36)$$

It leads also to a limitation for the minimum gain of one stage:

$$G_{min} = \frac{75}{G_{max}} \geq 1.364 \quad (2.37)$$

Leading to :

$$G_{per_stage} \in [1.37, 55] \quad (2.38)$$

It is then not needed to simulate for a gain above 55 for one stage of the discrete IA.

Care must be taken while changing the gain because some specifications of the amplification chain must be respected. These constraints are resumed in table below and come from [52] p_35.

Specifications	1st Cut-off frequency	2nd Cut-off frequency
1st Stage	$f_{1,IB} \in [10, 60]$	125 Hz ($f_{1,Diff}$)
2nd Stage	140 Hz ($f_{2,IB}$)	/

Table 2.5: Characteristics of the differential chain (choice of frequencies following the previous work [52])

The high cut-off frequencies are really important to ensure to get the desired gain in the bandwidth and to cut the low frequencies that are outside this BW. Concerning the low cut-off of the first stage, it comes from a zero in the transfer

function and can be variable (see Appendix B for details). However, it is preferable to have low cut off frequency as it allows to have a really good low frequencies attenuation but it can not be too low (in this case below 10 Hz) or it will require negative resistors which is not physical.

The constraints of Table 2.5 are related to the values of the components in the discrete IA. Taking the conventions of Figure 2.2 for the labels of the components, the following relations link the cut-off frequencies with the values of the components:

$$f_{1,IB} = \frac{2R_2 + R_1}{2\pi R_2 R_1 (2C_1 + C_2)} \quad (2.39)$$

$$f_{2,IB} = \frac{1}{2\pi R_2 C_2} \quad (2.40)$$

$$f_{1,Diff} = \frac{1}{2\pi R_4 C_4} \quad (2.41)$$

The gains of the different stages of the discrete IA are also dependent on the values of the components according to the following relations:

$$G_{IB} = \frac{2C_1 + C_2}{C_2} \text{ gain in the Bandwidth} \quad (2.42)$$

$$G_{Diff} = \frac{C_3}{C_4} \quad (2.43)$$

$$\Rightarrow C_3 = \frac{75}{G_{IBB}} C_4 \quad (2.44)$$

All the development of the equations of the discrete IA can be found in the appendix B.

Giving the equations of the cut-off frequencies and the gains, it was chosen to fix the values for R_2, R_4, C_2 and C_4 and to change the values of C_1 and C_3 to adapt the gains. The chosen values are the following :

Components	C_2	R_2	C_4	R_4
Values	0.47 nF	2.7 MΩ	1 nF	1 MΩ

Table 2.6: Characteristics of the differential chain

From these values, the fixed cut-off frequencies and the wanted gains, R_1 can be deduced according to equation 2.39 to keep this frequency constant when simulating. After choosing to keep the values of these components constant, a matlab routine was created to find the values of the rest of the components needed for simulation to keep the cut-off frequencies constant and to get desired gain. The result of the total input referred noise in function of the gain of the first stage of the discrete IA, is depicted on Figure 2.5.

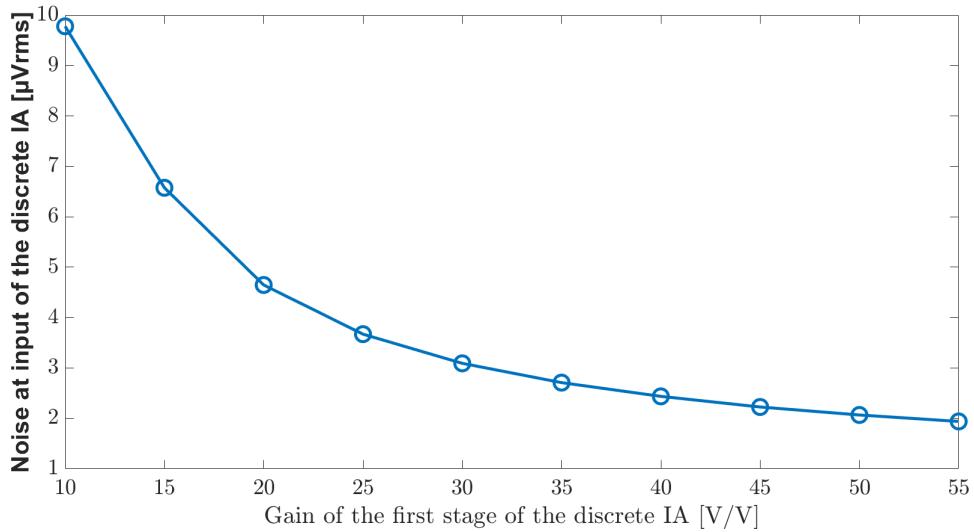


Figure 2.5: Noise at the input of the discrete IA in function of the gain of the first stage

The simulation was performed until 55 for the first stage gain according to the GBWP constraint of the amplifier. The lower frequency of the first stage $f_{1,IB}$ was fixed to 30 Hz.

The Figure 2.5 shows the same dynamic than the figures 2.3 and 2.4 that depict the total noise at input of discrete IA obtained by analytical computation and Matlab (the multiplicative factor of this constant noise) . It confirms then the choice of taking a gain around 30 for the first stage of the discrete IA because above this gain, the total noise decrease is not significantly high to pay the price of higher GBWP need and the cost overhead in power consumption associated. The noise at the input of the discrete IA is around $3\mu V_{rms}$ with a gain of 30 and around $2\mu V_{rms}$ for a gain of 55. AS the noise of this discrete IA is already low in front of the one of the integrated IA that should be around $155\mu V_{rms}$ ($2.43\mu V_{rms} * 63.8$ (gain of the IIA)) at the input of the discrete IA, the small difference is insignificant in the total noise.

2.2.7 Selection of operational amplifier

Using the results obtained previously, it was decided to track a gain of 30 for the first stage of the discrete IA in order to minimise the noise associated with the amplifiers. This choice leads to a gain of 2.5 for the second stage as the total gain must be 75 and the gain of the AAF is 1.

Considering that the choice of the amplifiers is made in the order to get low power consumption but with a constraint on the GBWP and on the slew rate to avoid distorted signal. The minimum slew rate is obtained from $SR = 2\pi f V_{peak-to-peak}$ where $V_{peak-to-peak}$ is the peak to peak voltage of the output AC signal of the current stage. This formula assumed that the signal is a sinusoidal, this might not be the case in the context of ENG signal that has a triphasic shape as stated in chapter 2. This peak to peak voltage is maximum 0.48 V at the output of the first stage of the discrete IA and maximum 1.2V at the output of the second stage and the output of the AAF as the gain of the AAF is 1. It is maximum 1.2 v peak to peak as the total gain of the AFE was chosen to output at maximum an AC voltage with 0.6 V of amplitude around a DC point 0.9 V, meaning that it lies in [0.3,1.5] V

These constraints are summarized in the table 2.7:

	Input Buffer	Differential Amplifier	AAF
GBWP (min.) [kHz]	300	25	10
SR (min.) [V/ μ s]	0.03	0.0754	0.0754

Table 2.7: Constraints on amplifiers

The research of new operational amplifier that suits well for the application was done according to these constraints, keeping in mind that it is desired to reduce the power consumption and to avoid excessive noise.

	MCP6241x [33] (current Op. Amp.)	TSV62xA [33]	NCS20094 [36]	TSZ121 [34]	TLV9042 [31]
Typical					
Power consumption @ 1.8 V [μ W]	90	52.2	36	50.4	18
GBWP [kHz]	550	420	350	400	350
SR [V/ μ s]	0.3	0.19	0.15	0.17	0.2
Input noise					
voltage density [nV/sqrt(Hz)] @ 1 kHz	45	77	40	60	66
Offset Voltage [μ V] @ 25°C	5000	800	500	5	600

Searching through different suppliers, the Op Amplifiers depicted in the Table 2.2.7 (just above) are the ones that suit the most for the application.

First the TLV9042 [31] is chosen for the first stage of the discrete IA. It offers sufficient GBWP and SR. It has the lower power consumption among all making it more suitable for long term implant and its noise density is not much higher than the current Op Amp MCP6241x [33].

Concerning the second stage of the discrete IA (the differential pair referring to table 2.7), all op. amplifiers respond to the GBWP constraint but the SR needed is higher than for the first stage as the full gain is applied. The choice was made to also take the TLV9042 [31].

Finally as the constraint on the SR is the same for the AAF than for the second stage but the GBWP needed for the AAF is lower. The same amplifier than for the second stage was chosen for the AAF.

2.2.8 Noise analysis with the selected operational amplifier

In the same way than for the MCP6241 the noise of the TLV9042 will be computed analytically in order to compare them. The noise of the amplifier is composed of two different parts, the flicker and the thermal noise. The flicker noise is considered as the bandwidth starts at 140 Hz which is below the corner frequency.

The noise is computed on the basis of the basis of equations (2.4) , (2.5) and (2.6) where :

- BW = 12.6 kHz
- $f_0 = 10$ Hz
- $f_L = 0.1$ Hz
- $f_H = 1$ kHz
- $e_n = 66 \left[\frac{nV}{\sqrt{Hz}} \right] @ 1kHz$

The values of the flicker and the thermal noise are:

- $e_{flicker} = 1.68 \mu V_{RMS}$
- $e_{thermal} = 8.05 \mu V_{RMS}$

Resulting in a total noise for the TLV9042 in the bandwidth of :

$$\begin{aligned} e_{n,TLV9042} &= \sqrt{e_{flicker}^2 + e_{thermal}^2} \\ &= 8.22 \mu V_{RMS} \end{aligned}$$

2.2.9 Final noise results for the AFE and comparison with the previous operation amplifier in term of noise and power consumption

To see the benefit of taking this new op amp compared to the one of the previous work [52], a comparison is made in terms of noise added and power consumption.

The final results are summarize in the Table 2.8. This table contains the total noise at input of the integrated IA/ inpu gain stage for one channel of the conditioning chain and the power consumption of one channel for the discrete IA/tripolar to differential stage and AAF. The noise of the MCU that will discuss in the dedicated section in chapter 3 and is resumed in Table 3.2, is already inserted in this Table

	Previously (using MCP6142)	Now : TLV9042
Power consumption of the discrete IA and AAF [μW]	360	72
Noise of the Sallen Key [μVrms]	0.0012	0.0018
Noise of Discrete IA [μVrms]	0.13	0.1823
Noise of the Integrated IA [μVrms]	2.43	2.43
Total Noise @ input of the Integrated IA [μVrms]	2.433	2.437

Table 2.8: Final noise and power consumption results for one channel of the AFE

From the Table 2.8, it is first seen that the total noise is dominated by the noise of the integrated IA.

The choice of new amplifiers affect clearly the noise associated with the discrete IA but as this noise is one order below the noise of the integrated IA, the increase in total noise is only 0.16% compare to the use of the previous Op Amp..

In term of power consumption, using new amplifiers shows really good result compared to the previous work ([52]). There is a factor 5 in power consumption between the use of the previous op amp. and the use of the newly chosen.

2.3 Issue with the analog front-end frequency response

2.3.1 Issue of the frequency response

When simulating the frequency response of the discrete IA and the AAF, the bode diagram of Figure 2.6 was obtained. An overshoot in the bandwidth of the neural signal can be observed. It is not desired as the gain is chosen to avoid saturation of the amplifiers. There is also the fact that the noise increases with the gain that is not desired to avoid loosing SNR.

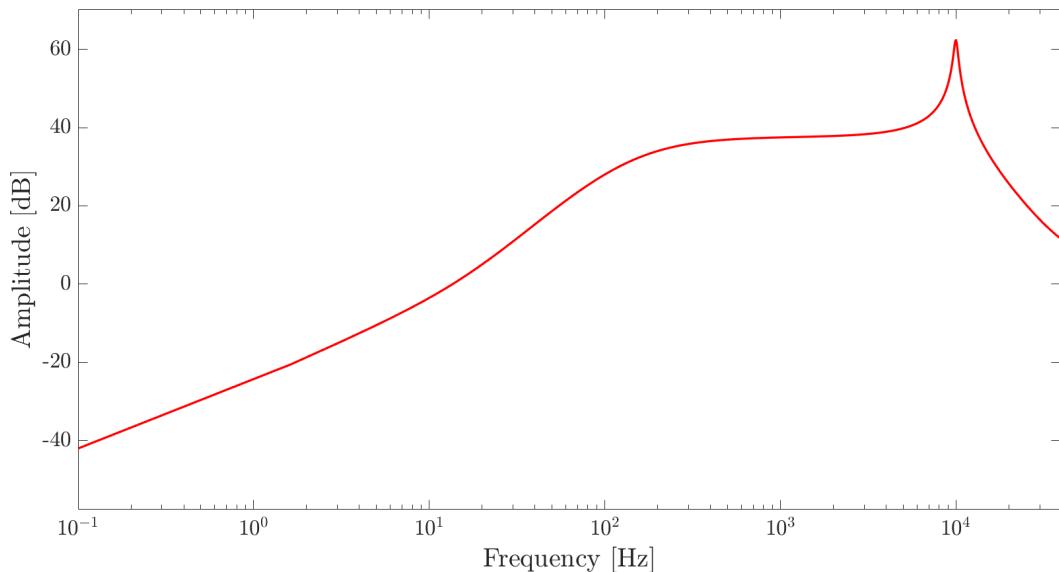


Figure 2.6: Bode Diagram of the discrete IA and AAF obtained with LTspice

The simulation of the bode diagram was done considering the output impedance of the integrated IA. To model this output impedance, the voltage sources were connected in series with resistors, R_I , of $150\text{ k}\Omega$. The gain of the first stage of discrete IA was 30 and the one of the second stage 2.5

2.3.2 Solution to fix the overshoot

A solution to fix this overshoot, is to use the circuit of the Figure 2.7 and proposed by [39].

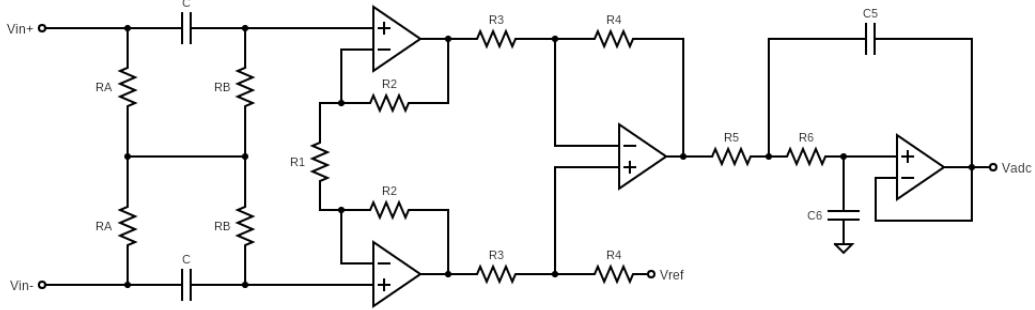


Figure 2.7: Proposed circuit for the discrete IA (Source [39])

Before simulating the Bode diagram with this proposed circuit, the components must be chosen according to the desired gains and the cut-off frequencies. The gain chosen are the same that for the current discrete IA. The gain of the new circuit depends on the values of the resistors R1 to R4 as follow:

$$G_{DIA} = \frac{2R2 + R1}{R1} \frac{R4}{R3} \quad (2.45)$$

This gain does not depend on frequency as in the previous solution as not capacitors are present (complete equation of this circuit can be found in Appendix D).

As no capacitors are present in this new discrete IA, it is needed to have another circuit before to cut the low frequencies. The circuit of the Figure 2.8 was proposed in the same paper (Source [39]). It is called "AC coupled front-end".

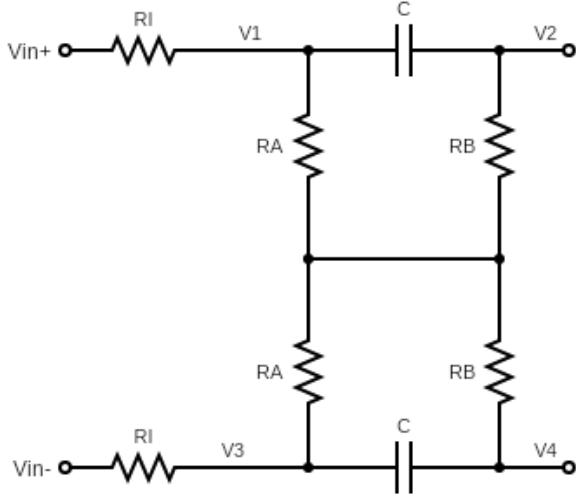


Figure 2.8: AC coupled Front End with serial resistance of the Integrated IA (Source [39])

This AC coupled front-end as it contains capacitors and resistors, presents poles and zeros. To design the values of the capacitors and resistors of this AC coupled front-end, it is necessary to know how the transfer function and the pole and zero look like. Complete equations can be found in Appendix D.

$$\omega_p = \frac{(R1 + RI)}{C(R2R1 + R2RI + R1RI)} \quad (2.46)$$

$$\omega_z = \frac{(R1 + RI)}{CR2R1} \quad (2.47)$$

The pole and zero depend on the output impedance, RI, of the integrated IA. To avoid the influence of RI, it is needed to have R1 and R2 much bigger than RI. It leads to the following approximations of the transfer function, pole and zero:

$$H(\omega) = \frac{j\omega CR2}{1 + j\omega R2} \quad (2.48)$$

$$\omega_p = \omega_z = \frac{1}{CR2} \quad (2.49)$$

Having this simplification means that the cut-off frequency can be only decided according to the values of C and R2. It also implies that the gain of the AC couple front-end in the BW will be unitary as needed. The chosen values of components

can be found in the Appendix E in table 4.4 where the names of the components takes the conventions of the figure 2.7.

With the design done, the proposed circuit can now be simulated to compare its bode diagram to the one of the previous circuit. The result is shown on Figure 2.10. Compared to the previous circuit frequency response on Figure 2.6, the frequency response of the proposed circuit is perfectly flat in the bandwidth as desired.

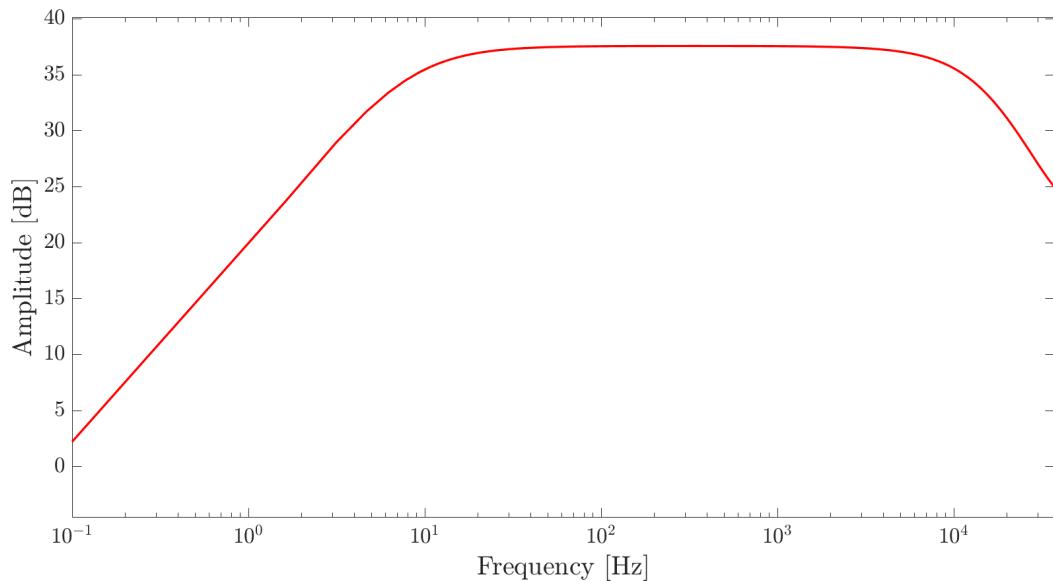


Figure 2.9: Bode diagram of Proposed solution

Figure 2.10: Comparison between the bode plot of the previous solution and the proposed solution

The Table 2.9 proposes a comparison the two circuits in terms of power consumption, noise added and BW. The lower limit for the BW is smaller in the case of the proposed circuit but even with a bigger bandwidth the total resulting noise is 4.3 times smaller due to the absence of overshoot. The power consumption is also 3% less due to the absence of feedback capacitance.

	Previous Solution	Proposed Solution
Power consumption,avg [μW]	74.8	72.56
Input Referred Noise due to the discrete IA and AAF @input of Integrated IA [μVrms]	0.54	0.126
BW [Hz]	[160, 12.5k]	[35, 12.5k]
Overshoot in BW	48.2 dB @ 9.9 kHz	\

Table 2.9: Simulation with LTspice and Comparison of the previous and the proposed circuits for the Discrete IA.

2.4 Analysis of the power consumption

In this section, a computation of the power consumption based on datasheets and simulation is proposed for the AFE. The goal is to have an estimation of the power consumed before realising measurements.

2.4.1 Power of integrated IA

The power consumption of the integrated IA/input gain stage is given in the Table 4.3 (appendix A) for different configurations. The fourth one is chosen in this work and its power consumption is $23.9 \mu\text{W}$ per channel. Two channels are used in this work resulting in $2*23.9\mu\text{W}$ of power consumption. To that, $5.1 \mu\text{W}$ must be added for the power consumption of the chip of the Integrated IA. The total power consumption is then $52.9\mu\text{W}$

2.4.2 Power of discrete IA and AAF

The power of the discrete IA and AAF was obtained by simulating the circuit with LTspice. The discrete IA and AAF were simulated considering the two channels used for amplifying the three signals obtained with the tripolar cuff-electrodes. The obtained values were $109 \mu\text{W}$ for the discrete IA and $36.9 \mu\text{W}$ for the AAF. By looking at the power consumption of the used operational amplifier (TLV9042) in datasheet ([31]) that is $18 \mu\text{W}$ per amplifier, the same result can be obtained. In

fact the discrete IA is composed of three amplifier and the AAF of one giving a power consumption of $72\mu\text{W}$ multiplied by two for the two channel. The computed total power consumption is $144 \mu\text{W}$ and the one obtained by simulation is $145.9 \mu\text{W}$. The results are really closed.

2.4.3 Total power of the AFE

To the power consumption of the integrate IA, discrete IA and AAF, the power consumed by the different voltage and current sources must be added. Using data-sheets, the consumption of those references can be estimated. Concerning the choice of the current and voltage references (such as LDO), the explanations of the choices can be found in Appendix F.

Power consumption of the current references

The LMD334DT ([41])which is the chip used for the reference current, has only for consumption of $1\mu\text{A}$ which is the current pumped up by the integrated IA. Then, the total power consumption as two LMD334DT's are needed by the integrated IA, is $2 * 1\mu\text{A} * 1.8V = 3.6\mu\text{W}$.

Power consumption of the 1.2V LDO

According to the datasheet ([40]), the ground current of the LDO chosen is $\approx 280 \mu\text{A}$ with the load current of approximately $1 \mu\text{A}$ that is the current consumed approximately by the output of this LDO. The ground current is defined as the difference between the input current and the output current that includes the quiescent current. The quiescent current is the current to supply internal parts of the circuit.

Final power consumption results

The pie chart of figure 2.11 of the power consumption of the AFE with the new solution for the discrete IA, shows that the LDO is the main contributor of the power consumption with 71.3 % of the consumption. It is followed by the discrete IA with only 15.4%. The total power consumption is **706.4 μW** . A detailed table can be found in Appendix G that compares the AFE with previous discrete IA and with the new discrete IA in terms of power consumption. A better choice of LDO such as the "TPS7A0512PDBZR" ([44]) could have been done. This LDO consumes only $10.8 \mu\text{W}$ instead of 504 for the current LDO.

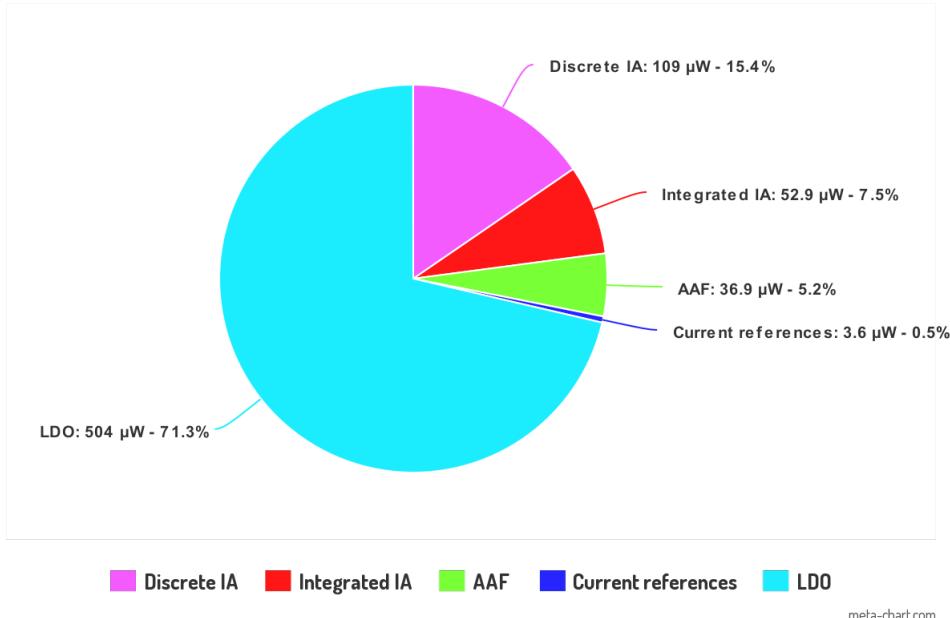


Figure 2.11: Pie chart of the power consumption for the proposed solution for AFE (made with Meta chart [42])

2.5 PCB design

Now that the analog front end is designed, a solution must be now found to test the circuit in real condition and to associate it with the MCU that will be used for the digitally implemented adaptive tripole. To facilitate the association of the circuit with the MCU, it was decided to use a PCB that will be plugged on the MCU. The design of the PCB was made with the software Eagle. Before ordering the PCB, it is of good practice to ensure the circuit is functional with the input impedance of the ADC. To test its functionality, it was decided to make simulations with LTspice. The system must be functional in the BW of the neural signal between 500 Hz and 10 kHz as stated in chapter 2. The amplifier used for the LTspice simulation is the TLV9042 and its LTspice model which was found [43].

The simulation was done considering the output as being the ADC of the MCU. The input impedance of the ADC is composed of a resistor and a capacitor in series (Source [45], [46]). According to the datasheet of the MCU used in this work ([50]), the Apollo3 from Ambiq (see chapter 4), the input impedance is composed of a resistance of $720\text{ k}\Omega$ for the ADC channel 0 ($3600\text{ M}\Omega$ for the seven other channels) and 4 pF of input capacitance. Also as the integrated IA as no model

available for simulation with LTspice, it was considered as a sinusoidal sources of 0.4V DC component with a resistor "R1" in series of 150 kΩ that is the output impedance of the integrated IA. The simulations were done for multiple frequencies both for an ENG signal or artefacts at the inputs and were also done with the two possible values of impedance of the ADC. The system worked correctly during all the simulations.

The simulations results can be found in the Appendix G as well as all the pictures of the PCB and the schematics of it obtained with the eagle software.

2.6 Measures of the AFE

Now that the PCB is done, it is good to check that the required characteristics when designing the analog front-end are respected or at least closed to the desired ones.

The first thing was to ensure that all the voltage and current reference were correct before to realize deeper tests on the PCB containing the AFE. As it is the case on the ordered PCB, the next tests are done.

The first thing to test is the functionality of the system in term of frequency response. Then the two figures of merit that were the targets of the design of the AFE that is the power consumption and the noise.

2.6.1 Tests of the frequency response and gains of the AFE

First, the functionality of the AFE is checked. The way to check the functionality is to check that the gain and the bandwidth are as desired. The frequency response test was only done on the discrete IA and AAF as the integrated IA was already developed by the ECS team of UCLouvain.

The set up to test the gains, is the one on the Figure 2.12. The waveform generator was used to give two different inputs to the discrete IA, one of higher amplitude than the other. The choice was made to have one with 20 mVpp and the other one with 10 mVp but both with a DC offset of 0.4V which is the one imposed by the integrated IA.

To get the Bode diagram, the input signals were applied for different frequencies between 1 Hz and 20 kHz.

As it is a differential amplifier the output depends on the difference between the two input signals and the gain was computed as follow:

$$Gain = 20 \log\left(\frac{V_{out}}{V_{in1} - V_{in2}}\right) \quad (2.50)$$

Of course the measures of the gain were realised for both channels of the discrete IA but as these got the same results only the results of the first canal are shown. The output of the AFE was measured with an oscilloscope, the TBS2104 [47].

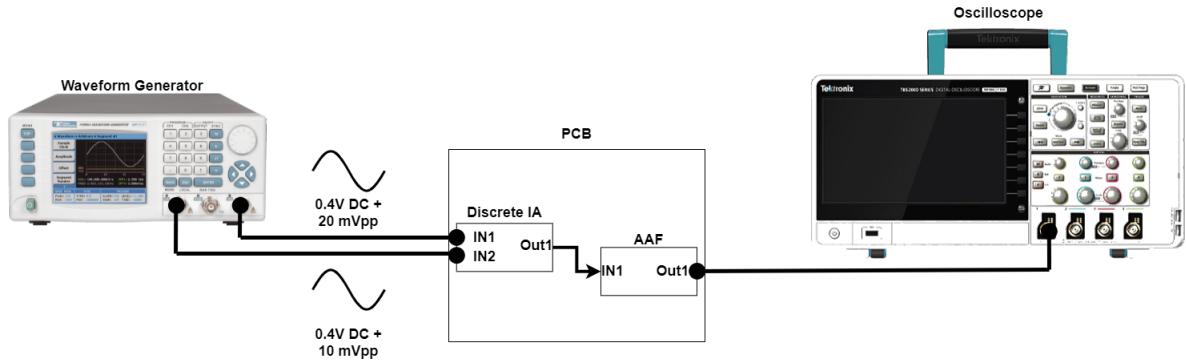


Figure 2.12: Set-up for the test of the frequency response of the discrete IA and AAF on PCB

The Figure 2.13 depicts the fact that the bode diagram obtained while measuring the output of the AAF (Blue dots) is closed to the one obtained when simulating with LTspice (Red Line). Two differences can be highlighted. First, the maximal gain of the real discrete IA is a little bit higher, 76 against 75 for the designed gain. A way to change this is to replace the R2 on the Figure 2.7 by a smaller one. For the moment, it is $15\text{ k}\Omega$ and replacing it with $14\text{ k}\Omega$ should give the proper gain as the gain associated with R3 is $\frac{2R_2+R_1}{R_1}$. Secondly, the roll-off at the high cur-off frequency, is higher in the real case which is nice as it cut faster the frequencies out of the bandwidth.

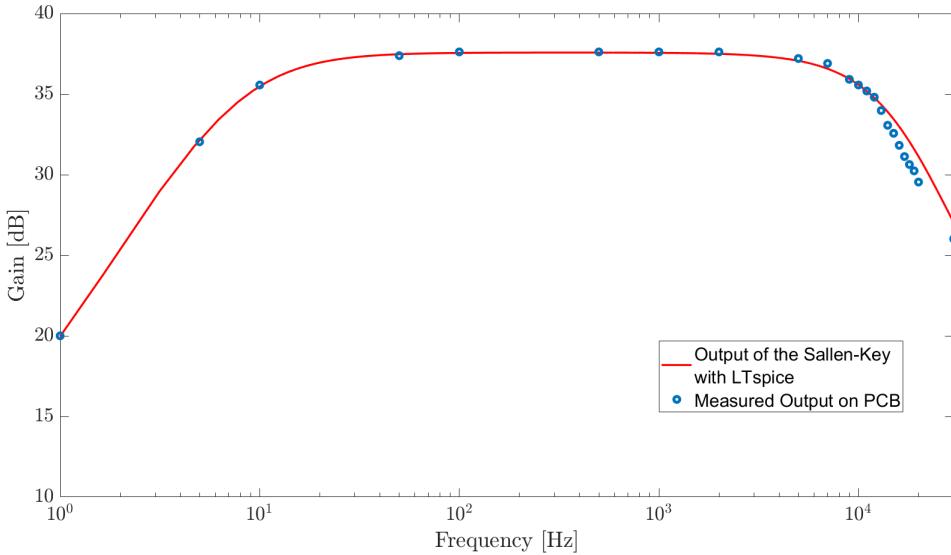


Figure 2.13: Measured Bode Diagram of the analogue front-end (PCB)

2.6.2 Measurement of the noise of the AFE

Now that it is sure the AFE works correctly, it is now important to check at the figure of merits. Here the noise of the AFE will be analyzed and compared to the computed noise to see if they are any notifiable differences.

To measure the noise, it is necessary to apply a short circuit between all input pins of the AFE and to impose a common voltage. This voltage was chosen to be the ground. The Figure 2.14 shows the set-up used to measure the output noise of the AFE. The noise was measure with an oscilloscope (TBS2104 [47]) and for only one channel of two of the AFE.

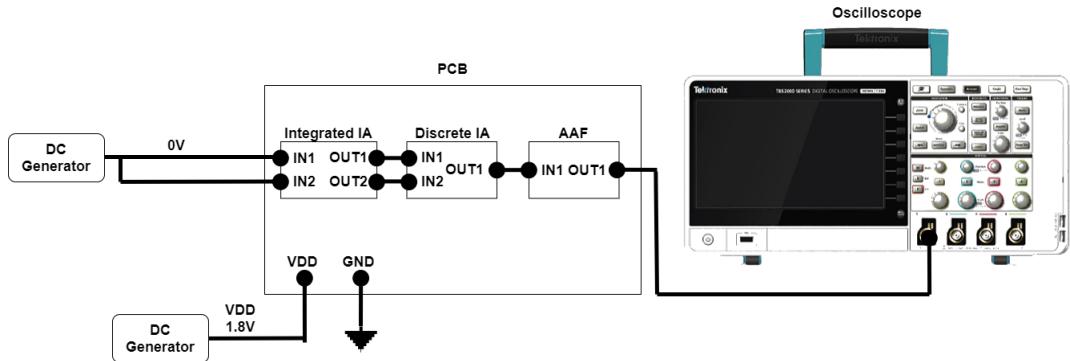


Figure 2.14: Set-up to measure output noise of the AFE

The sampling frequency of the oscilloscope was 625 kHz. On Figure 2.15 is represented the one-sided psd obtained from the samples of then noise. When the one-sided psd is integrated until 12.6 kHz (cut-off frequency of the AAF), it gives a total noise of 11.5 mV_{rms} and when bringing to the input of the integrated IA, it gives $\approx 2.4 \mu\text{V}_{rms}$ comparing with the $2.433 \mu\text{V}_{rms}$ obtained by simulating the noise of the discrete IA with LTspice and adding the analytically computed noise of the integrated IA. This slightly difference could come from the considered bandwidth when computing the noise of the integrated IA as this is the main source of noise and that the computed noise of the discrete IA is possibly more accurate as it was obtained with LTspice.

Concerning the one-sided psd, in the log-log scale it is closed to a straight line until around 10 kHz meaning that dominant noise is flicker noise. After 10 kHz, the one sided-psd reaches a plateau meaning that thermal noise is dominant.

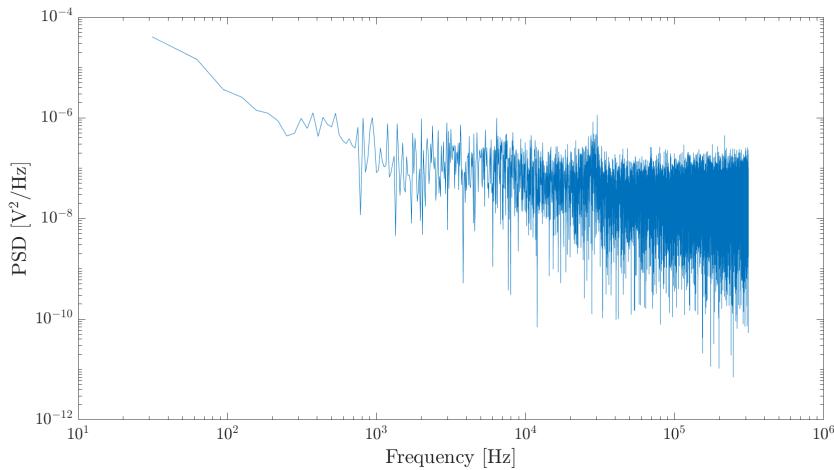


Figure 2.15: One sided psd of the measured noise of the AFE

2.6.3 Measurement of the power consumption of the AFE

To measure the power consumption of the AFE, the set-up depicted by Figure 2.16 is used. The SMU , K2450 [48], is supplying the power pins of the PCB containing the AFE, with 1.8 V is applied that is the voltage applied but the MCU when PCB is plugged on it. The current is then displayed by the SMU. Also, the input pins that are normally used for the input ENG signal and the artefacts, were connected to GND.

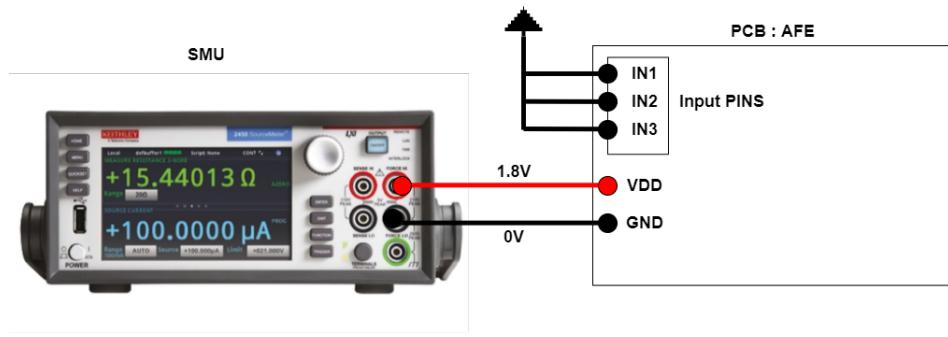


Figure 2.16: Set-up to measure the power consumption of the AFE

The power consumption was first tested without the integrated IA to ensure no short circuits are present in the discrete IA/tripolar to differential stage and AAF parts. The obtained current was $344 \mu\text{A}$. This results is coherent as the discrete IA, AAF and current references consumes $83 \mu\text{A}$ leaving $261 \mu\text{A}$ for the LDO. According to the datasheet [40], the LDO consumes approximately $270 \mu\text{A}$ with no

load at the output.

Next, it was tested on the full AFE with the integrated IA as no short circuits were found. The obtained value for the current is $387.6 \mu\text{A}$ giving a power consumption of **$697.7 \mu\text{W}$** . The computed power consumption in section "Power analysis" was of $706.4 \mu\text{W}$, the measured power consumption represents a decrease of 1.37 %. This is surely due to the estimation of the current consumption by the LDO as the graphic used to find this value (in the datasheet of the LDO [40]) is not quite accurate. However, the result is really close to the computed one.

Chapter 3

Digital back-End for the adaptive tripole

After the amplification and filtering of the AFE, the next step is to compensate the imbalance and to remove the artefacts, this is the role of the adaptive tripole implemented on the MCU.

In this chapter is proposed an implementation and an optimization with regards to the power consumption, of the adaptive tripole on a micro-controller. The purpose of this implementation is to obtain a functional adaptive tripole that can be used for an implant of small size.

The following points are also developed in this chapter. A characterization of the ADC in term of noise. A choice of specifications for the embedded code and an explanation of its implementation. Testings of the functionality of the embedded code on the MCU. A measurement of the power consumption of the running embedded code.

3.1 Functional overview of the digital back-End for adaptive tripole

Before trying to implement the system on the MCU, it is of good practice to try to define functionally what the system must do.

The Figure 3.1 highlights the different operations that the system must perform.

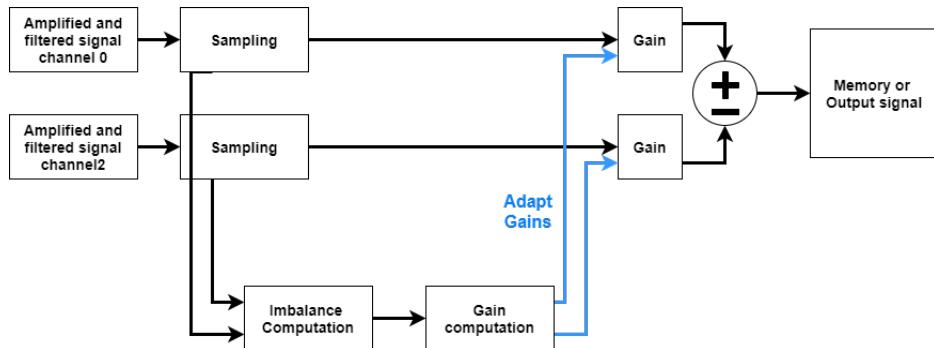


Figure 3.1: Functional Scheme of the digital back-end

After having been amplified and filtered by the AFE, the the digital back-end takes over. The first step of the digital back-end is to sample the signal as it will be processed in digital form.

After the sampling, it differentiates the two samples taken from two different channels to cancel the artefact and only retrieve the amplified ENG at the output of the system. Meanwhile, it also computed the imbalance and adapt the gains in function of it in order to compensate it.

3.2 Choice of MCU

The choice of the MCU is a crucial step in order to minimize the power consumption. To choose which MCU suited the most, it was necessary to look at the power consumption for the same task between all the different MCU meaning the benchmarks.

Different MCU could be chosen and their characteristics are resumed in the Table 3.2. All the datasheets can be found on the link in the bibliography [53], [55], [56], [57], [58]

MCU	STM32 (actual)	MCU005 (epeas)	Apollo	Apollo2	Apollo3	Apollo4
CPU	Cortex M0 - 32bit	\	Cortex M4F- 32bit	Cortex M4F- 32bit	-Cortex M4F- 32bit	Cortex M4F- 32bit
Max Frequency (CPU) [MHz]	32	\	24	48	-48	-96
ADC	12 bits (1.14MS/s)	12 bits (1.14MS/s)	10 bits (0.8 MS/s)	14 bits (2.67 MS/s)	14 bits (2.67 MS/s)	12 bits (2.8 MS/s)
Active Power Consumption @ 1.8 V (CoreMark executing from flash) [μ W/MHz]	388	53	91.8	43.2	32.76	\
Memory (Flash) [kB]	192	\	512	1 000	1 000	2000 (MRAM)
Memory (RAM)[kB]	20	\	64	256	384	1800

The first MCU on the left on the Table 3.2 is the MCU that was used in the previous master thesis [52]. In this Table, the "\ " means that no data was available. As the choice of the MCU is conditioned by its power consumption, it is decided to use the Apollo3 Blue. Comparing to the MCU STM32 that was used in the previous master thesis ([52]), it offers a factor 12 in power reduction when comparing their power consumption for a CoreMark operation.

Two other great enhancements can be find compared to the STM32. First, the maximum CPU frequency (excluding the TurboSPOT mode) is 50% bigger meaning that the processing tasks could be done faster and might lead to further power consumption reduction as the deep sleep could be activated more often. Secondly, the resolution of the ADC can now reach 14 bits and can sample at least twice faster than the previous MCU. In fact, it means that the conversion time is reduced. The use of 14 bits could reduce the quantization noise by 4. This noise reduction could be of interest if the quantization noise take an important part of the total noise remembering that the ENG signal is in the range of $7.1 \mu V_{rms}$ [8].

3.3 Description of the embedded program operations

One input buffer to contain the samples

With the MCU chosen, a precise description of what this MCU will do adn which modules of the MCU are useful, is necessary before trying an implementation. For this purpose a scheme is proposed on Figure 3.2. On this scheme, the different tasks done by the MCU are expressed in the proper order they are realized. First, two ADC channels sample the output of the AFE. The samples are transferred to an input buffer by the DMA. Once the DMA has transferred all the samples, it triggers a DMA complete interrupt. To know when to trigger this interrupt, a counter is initialized with the amount of samples to transfer. Each time a sample is transferred by the DMA, this counter is decreased by one until reaching 0 and launching the interrupt. This step is implemented by the MCU itseld when using DMA with ADC as stated in the datasheet of the Appolo3 blue [54]. After that the DMA complete interrupt occurred, the CPU wakes-up and the input Buffer with the samples is read and formatted. In fact the samples at the output of the ADC have a special format on 32-bit in which there is the bits for the samples, bits to say what is the canal of ADC used and bits to say the number of sample used to average the output sample if the output sample is obtained through averaging (more information in the datasheet [54] p_754). Next, the CPU operates the adaptive tripole and cuff-imbalance computation and finally outputs the result in

an output buffer or through UART. Also, once the input buffer is completely read and formatted, all the ADC and DMA interrupts are cleared, the DMA for the ADC is reconfigured and the first sample of the ADC is triggered to restart the sampling.

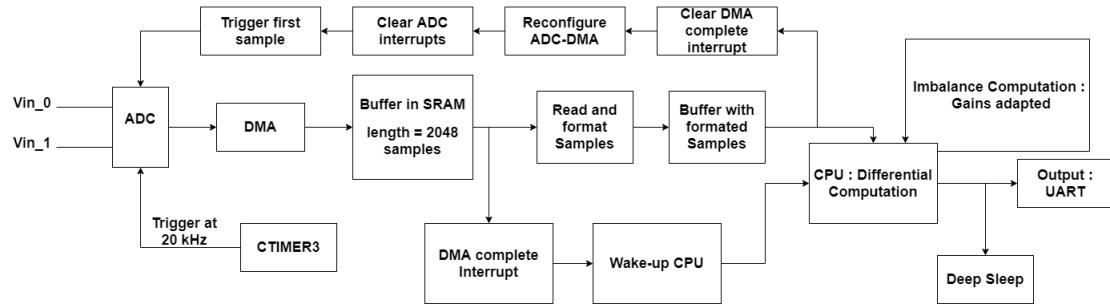


Figure 3.2: Processing of the MCU with one input buffer

Issue with the use of only one input buffer for the samples

A problem encountered with the use of only one input buffer, is the time needed to read and format the input samples before re-configuring the ADC-DMA and re-triggering the ADC for sampling. The measured time between the DMA complete interrupt rising and the restart of the sampling by the ADC, is then conditioned by the time to read and format the input samples that is 11.6 ms as stated in the Figure 3.6. To show how problematic it is, recall that the ENG signal can go up to 10 kHz. If the ENG signal is for example at 10 kHz, this means its period is 100 μ s and that 116 period of the ENG signal are lost between the two sampling periods.

Solution using two input buffers for the samples

To counteract this problem, a solution was to used two input buffers and to alternate their usage. Figure 3.3 show the principle of the use of two input buffers instead of one. This time a boolean variable "Buff" is used. In one case, the input buffer 1 is chosen to be the target of the DMA for the transfer of ADC samples in the other it is the input buffer number two. When the DMA complete interrupt is raised up, the boolean variable is changed and the ADC-DMA is reprogrammed to target the other buffer. As the DMA is reconfigured and the ADC first sample triggered before reading and formatting the sample of the currently used input buffer, the time associated with this task is not lost between two sampling periods. Now the time between the raise of the DMA complete interrupt and the re-triggering of the ADC is only $\approx 40 \mu$ s (measured). If the same case of an ENG signal of 10 kHz is taken, this means that only 0.4 period of the ENG signal are lost instead of 116.

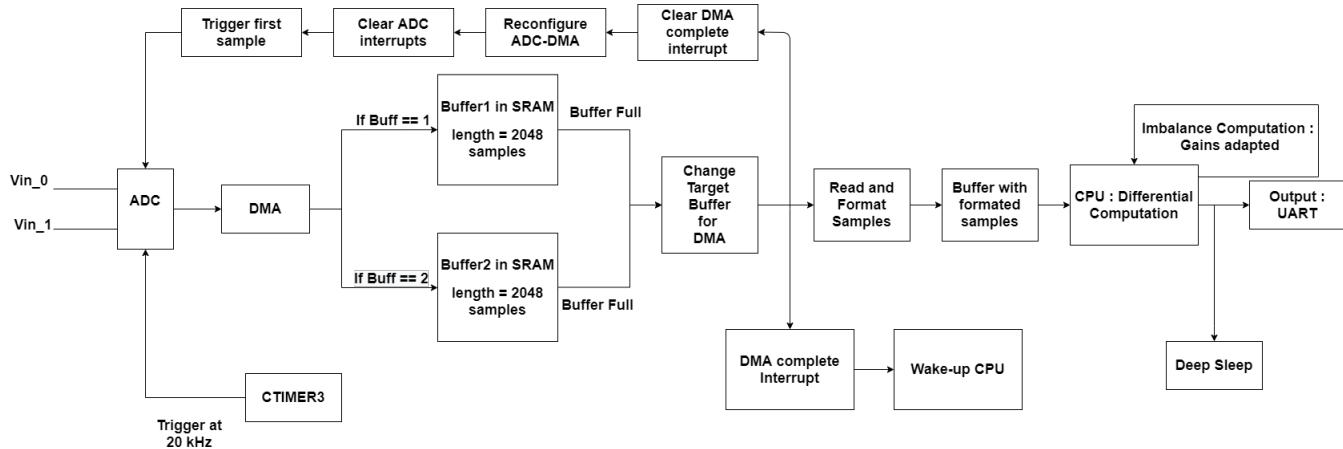


Figure 3.3: Processing of the MCU with two input buffers

3.4 Choice of implementation for the embedded code

Now that the MCU is chosen and that the functionality of the program as well as which modules of the MCU must be used to implement the task of the code, are known, it is good to decide before starting the implementation what are the desired specifications.

Choice and justification of the choices

The first point to decide on, is the specifications of the ADC. The sampling frequency must be chosen according to the bandwidth of the ENG to respect the Nyquist theorem. As the ENG signal can go up to 10 kHz, the sampling frequency is chosen to 20 kHz. If on tests on real signal, it should appear that aliasing is encountered, increasing the sampling frequency is still possible but at the cost of increasing the power consumption. The next point is the voltage reference used by the ADC to sample the input signals; As the MCU is powered by a 1.8V and that the choice of internal voltage reference for the ADC on the Apollo3 is only 1.5 V or 2.0V, only the 1.5 V can be used in this case as the supplied voltage is 1.8V. Another specification is the choice of the resolution. With the Apollo3 blue, it can go from 8 to 14 bits. Increasing the number of bits increase also the power consumption but decreasing the number of bits increase the quantization noise. There is a trade-off to take into account. The choice of the resolution will be investigated further in the section "Characterization of the ADC". To finish

the choices linked to the ADC, the choice of the power mode. The ADC has different power modes but only the "Low Power Mode 0" can be used in this context (see datasheet [54] p_759). In fact, the two other power modes power off the ADC between samples but at the cost of latency for calibration between samples. As the minimum latency is $70 \mu\text{s}$ and that the sampling frequency is 20 kHz meaning one sample each $50 \mu\text{s}$, none of the two other power modes can be used.

The next point to decide is the clock frequency of the CPU. The choice of the clock can be made between 24 and 48 MHz. Increasing the clock frequency means increasing the computation speed leading to less time to compute the cuff-imbalance and maximizing the time in deep sleep. The counterpart is increasing the instantaneous power when computing the cuff imbalance. The choice will be made by testing the code for the two frequencies and choosing the best one in term of mean power consumption.

The sampling of the ADC is triggered by the CTIMER3, the clock of the CTIMER3 must be then sufficient to generate a triggered at 20kHz. It was then chosen to be equal to 3MHz and to trigger the ADC each 150 periods.

A next crucial choice for the power consumption is the choice of the quantity of SRAM to be used. This will depend on the number of samples that are desired to be stocked before computing the imbalance, adapting the gains and outputting the resulted signal after processing by the adaptive tripole. It was decided to follow the choice of the previous master thesis [52] and to stock 2048 samples in an input buffer before doing the processing task. Furthermore, as stated before, two inputs buffers will be used to avoid loss of period of the ENG signal. As each sample is 32 bits long meaning 4 bytes, the minimum memory needed per buffer, is $4*2048$ bytes equal to $\approx 8 \text{ kB}$. Two buffers must be used to contain the samples after the ADC, another for the samples read and transformed in the correct format (also 32bit) and an output buffer that is half the size of the input ones (one input computed from two samples). This leads to a minimum of 28 kB (3 times 8kB plus 4 kB) needed. To these 28 kB more memory must be added as a lot of inner variables exist. It was chosen to use 64 kB of SRAM on the 384 kB available because 32 kB might be too few.

The CPU sleep mode between two computation of the output, must also be chosen. The CPU can be placed in deep sleep as the time to wake-up from deep sleep to running is of $15 \mu\text{s}$ (see datasheet [54] p_806). It is much less than the time needed to full-fill the input buffer.

After it is good to decide after how many times the gain for the cuff-imbalance will be updated. Those gains need to be updated as the imbalance change with time. At first those gains will be updated every 32 cycles pursuing the choice of the previous master thesis [52]. It could be possible to update less as the imbalance might change slowly.

The last thing to decide is related with the imbalance compensation. To make the imbalance compensation, it is necessary to retrieve the mean of the samples (see equation 3.3). As the mean of the two ADC could diverge if their dynamic is a little bit different, it is nice to get one mean for each channel of ADC used. Moreover, those means could evolve with the time as it is a system for long time implant. To take this possibility, the means of the different ADC channels are computed and changed after a certain number of period of the system. The choice is conditioned to the fact that the evolution with time might be small then it is not necessary to adapt often those means. It is then decided to adapt those means after 100 full periods of the running program (ADC sampling + cuff compensation).

Summary of the choices of implementation

The specifications can be resumed as follow:

- 1.5 V internal voltage ref ADC
- 20 kHz sampling frequency
- 2 input pins for the ADC (2 ADC channels)
- Low Power Mode 0 for the ADC
- clock of the CTIMER3 module at 3 MHz
- 24 or 48 MCU clock frequency
- CPU in deep sleep between each imbalance computation
- 64 kB of SRAM
- 2048 samples in the input buffers
- update of the gains every 32 cycles
- update of the ADC means every 100 cycles

3.5 Working principle of the adaptive tripole embedded code

In this section, the working of the embedded code for the adaptive tripole is explained.

When the DMA complete interrupt is triggered and wakes-up the CPU, the CPU processes on the input samples to compute the output and adapt the gains of the adaptive tripole. The Figure 3.4 shows an overview of what the CPU does when waking-up.

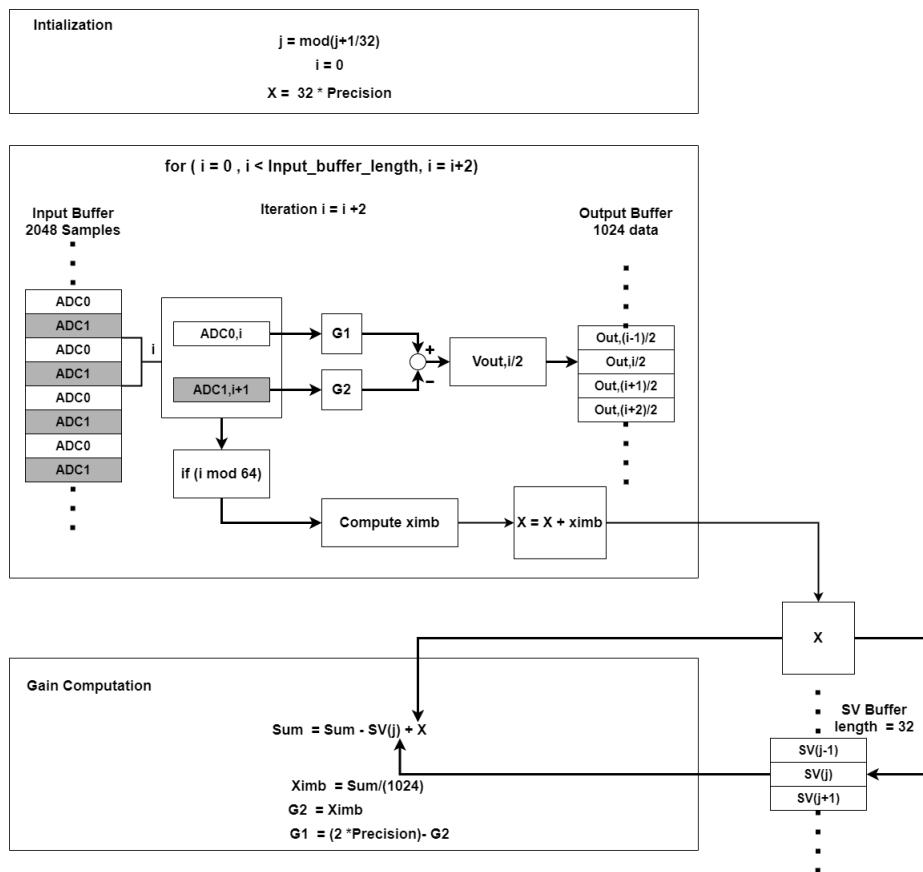


Figure 3.4: Scheme of the adaptive tripole embedded code

Initialization

At the start, there is an initialization phase. At each call of the function, the index j is incremented by 1 and index i reset to 0. The index i is used in the for loop and incremented by 2 at each iteration of the for loop until i is equal to the input

buffer length (here equals to 2048 samples). The index j only increase at each period of the process (Sampling phase + DMA + Processing task). This j is the index of the Storage Vector, " SV Buffer", which is of size 32. The storage vector keeps the previous value of the cuff-imbalance factor "X" that was computed 32 periods ago (32 as it was chosen to update the gains every 32 periods). Once j attains 31, it is reset to 0. Finally, the variable X that will contain the sum of the imbalance computed is initialize to 32*Precision as the input buffer is of size 2048 and the ximb is computed "mod 64" or every 64 samples meaning $\frac{2048}{64} = 32$ times during a period. The variable precision is due to the use of integers variables and used to choose the number of decimals wanted. In this case, "Precision" was decided to be equal to 1000 meaning 3 decimals are kept. If the imbalance is 0 then ximb is equal to 0 and the gains should be equal to 1*Precision. As the SV buffer contains the previous X and the "Sum" is initially 1024*Precision, if the imbalance does not change SV(j) (previous X for same index j) is equal also to 32*Precision and then cancel the X leading to sum equals to 1024*Precision giving the gains of 1*Precision as divided by 1024.

For Loop

The for loop iterates to take all the samples of the input buffer. At each iteration, the output is computed over two new input samples. Each input samples is affected by a different gain that allows to compensate the imbalance and the artefacts. As the inputs of the ADC's have an offset due to the AFE (0.9V), it must first be retrieve before computing the output as only the AC part is of interest to detect the ENG and cancel the artefact. This is done by taking the means of the ADC's. The means are computed separately for the two ADC channels in order to take into consideration the differences in their sampling dynamics. The means are computed by averaging the input samples of the two channels over 10 times a full input Buffer meaning 10*1024 samples for each channel as the input buffer is of size 2048 (samples) and composed of half samples from one channel and half of the other.

$$Mean_{ADC0} = \frac{\sum_{index=1}^{10} \sum_{l=0}^{l=1023} (V_{ADC0,l} * precision)}{10 * 1024 * Precision} \quad (3.1)$$

$$Mean_{ADC1} = \frac{\sum_{index=1}^{10} \sum_{l=0}^{l=1023} (V_{ADC1,l} * Precision)}{10 * 1024 * Precision} \quad (3.2)$$

With the computed means, the output values can be computed as follow:

$$V_{out,i} = \frac{G1 * (V_{ADC0,i} - Mean_{ADC0}) - (G2) * (V_{ADC1,i+1} - Mean_{ADC1})}{Precision} \quad (3.3)$$

The $ximb$, imbalance factor, is computed every time i is a multiple of 64 meaning 32 times during the full for loop as the input buffer size is 2048. Using the equation 1.6 of the electrode voltage to compute $ximb$, it is easily translated to the use of the ADC's values. The means still need to be retrieve before the computation:

$$ximb = \frac{|V_{ADC0} - Mean_{ADC0}| - |V_{ADC1} - Mean_{ADC1}|}{|V_{ADC0} - Mean_{ADC0}| + |V_{ADC1} - Mean_{ADC1}|} * Precision \quad (3.4)$$

The absolute value is taken to only consider the amplitude of the signal and not the sign.

Gain Computation

The imbalance value is averaged over 1024 $ximb$, imbalance factor, computations. The "1024" is due to the fact that the $ximb$ is computed 32 times in the for loop and that they are summed up to give "X" and the fact that the "Sum" is composed of 32 iteration of the code as j goes from 1 to 31 before being reset to 0, $32*32 = 1024$ (as stated before the gains are updated every 32 periods). The average over 1024 values is done to have an accurate value for the imbalance. The "Sum" add at each iteration the new value of "X" and subtract the previous value of "X" for the index j in the SV Buffer. The new value replaces the previous in the SV Buffer for the next time. The imbalance is then computed as :

$$X_{imb} = \frac{Sum}{1024} \quad (3.5)$$

From this X_{imb} , the gains are computed for the adaptive tripole :

$$G2 = X_{imb} \quad (3.6)$$

$$G1 = (2 * Precision) - G2 \quad (3.7)$$

Range of Values

The table 3.1 resumed the range of the different variables and index used in the code as well as the size of the different Buffers used.

	Name	Size	Type	Min. Value	Max. Value
Buffers	Input Buffer	2048	uint_32t	0	4095
	Output Buffer	1024	uint32_t	0	4095
	SV Buffer	32	uint32_t	0	64000
Variables	G1	1	uint16_t	0	2000
	G2	1	uint16_t	0	2000
	ximb	1	long	-1000	1000
	Sum	1	uint32_t	0	2 048 000
	Ximb	1	uint16_t	0	2000
Index	i	1	uint_16t	0	4094
	j	1	uint_16t	0	31

Table 3.1: Name, Types and Range of values of the Buffers, Variables and index used in the adaptive tripole code

3.6 Characterization of the ADC channels

In this characterization the aim is to decide which resolution will be used for the ADC's. The metric to decide is the quantity of noise added by the different resolutions.

The Table 3.2 is obtained by applying a DC signal on the ADC and recording the samples. Once the samples are recorded over a sufficient amount of time, the standard deviation as well as the single sided psd are computed with matlab.

		ADC 16	ADC 32
Noise [LSB]	8 Bits	1.52	1.48
	10 Bits	3.38	3.12
	12 Bits	9.61	9.49
	14 Bits	27.6	27.2
Noise at Input of the Integrated IA [μV_{rms}]	8 Bits	1.83	1.81
	10 Bits	1.035	0.955
	12 Bits	0.735	0.726
	14 Bits	0.528	0.52

Table 3.2: Noise fo the ADC 16 and ADC32 channels in LSB and referred at the input of the integrated IA in μV_{rms}

As it can be seen on Table 3.2, going from 8 to 14 bits divides the input referred noise by a factor 3.5. Comparing to the integrated IA,input gain stage of the AFE, noise which is equal to $2.4 \mu V_{rms}$ as found in the test of the AFE in chapter 2, and the noise associated with the discrete IA,tripolar to differential stage of the AFE, and referred to the input of the integrated IA (Table 2.9), of $0.126 \mu V_{rms}$, the total input referred noise goes from $3.02 \mu V_{rms}$ for 8 bits to $2.46 \mu V_{rms}$ for 14 bits. Knowing that the ENG signal which is desired to be detected is approximately $7.1 \mu V_{rms}$ (Source [8]), it is better to keep higher number of bits.

To avoid too much cost overhead in power consumption while keeping a lower value for input referred noise, the choice was made to keep 12 bits for ADC. In fact the total input referred noise for 12 bits is $2.51 \mu V_{rms}$ and $2.46 \mu V_{rms}$ for 14 bits which is only an increase of 2 % of the total noise.

A last comment can be made, the noise between the different resolution, does not follow the quantization noise = $\frac{LSB}{\sqrt{12}}$ which should be divided by 4 for each increase of two bits of resolution. This means that there is also a residual noise in the ADC which is added to the quantization noise.

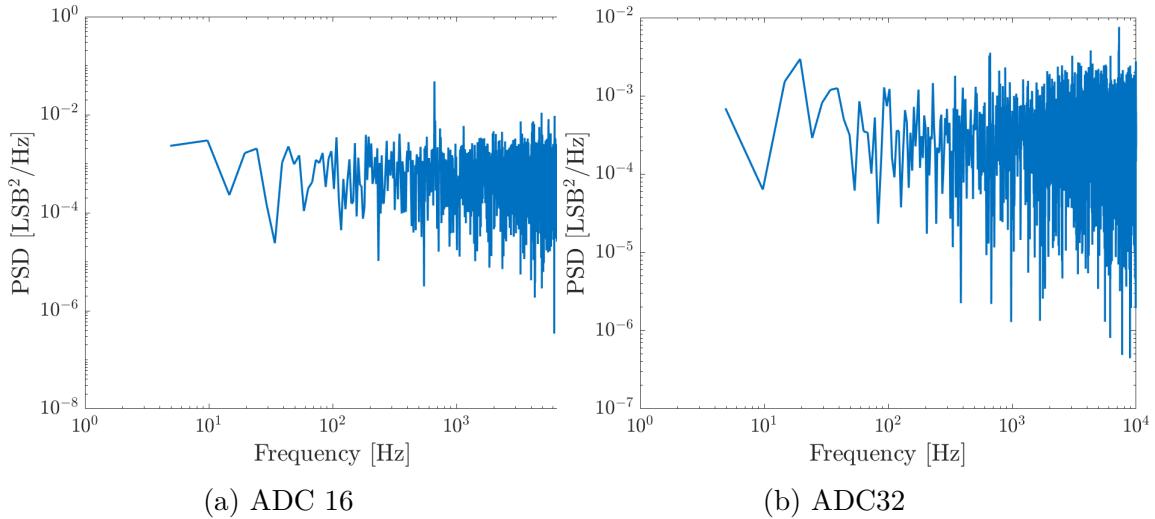


Figure 3.5: Single sided FFT of the ADC noise using 12-Bits ADC for a constant signal applied of 0.9 V

The single sided psd being in log-log scale highlights well that the ADC noise is mainly due to thermal noise. In fact, as the thermal noise is exponential, it translates in a plateau in the log-log plane. The noise density of the two ADC channels is of same magnitude for the plateau confirming the results of the Table 3.2 that the noise of the two channels are closed to each other. Histograms showing the distribution of the samples around the mean for 12-bits of resolution, can be seen in Appendix J.

Finally the resolution chosen for the ADC's is 12 bits. If in further tests, the SNR of the ENG signal is too low, it is still possible to change for 14 bits of resolution.

3.7 Time partition

In this section, the time partition of the different task done by the MCU is shown on figure 3.6.

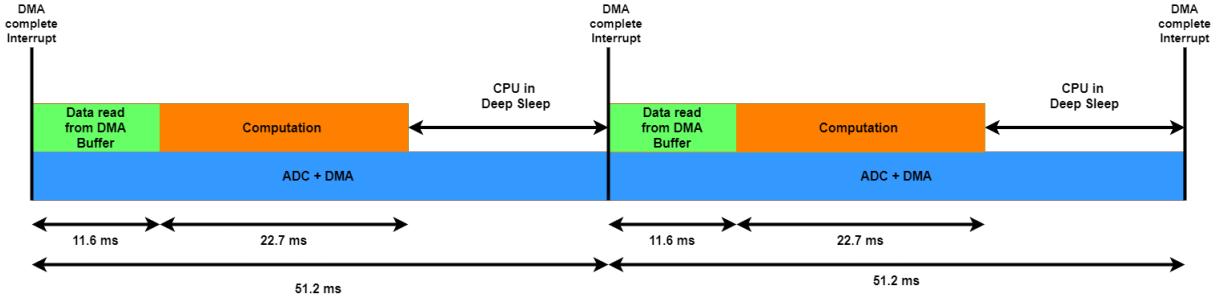


Figure 3.6: Distribution of the time between the different steps during running of the Cuff-Imbalance code on the MCU

The time is cycled by DMA completed interrupt that occurs when 2048 samples are transferred by the DMA from the ADC to one of the input buffers. The time between two "DMA completed" interrupts is ≈ 51.2 ms. It comes from the sampling rate which is of 20 kHz and the size of the input buffer which contains the samples. The size of the input buffer was chose to be 2048 sample. With 20 kHz of sampling rate, 1 samples is taken every $t_{sampling} = \frac{1}{f_{sampling}} = \frac{1}{20[kHz]} = 5 * 10^{-5}[s]$. As two ADC canals are used, 2 samples are taken every $5 * 10^{-5}$ seconds, leading to $\frac{2048}{2} * 5 * 10^{-5}[s] = 51.2ms$ to completely fill the input buffer. The DMA transferred of the last two samples take the time left to reach ≈ 51.2 ms.

The spending time for the Data read (green) and the computation of the output (orange) are found by using the IDE Keil μ Vision that allows to put stop points during debugging. By placing correctly the stop points between crucial steps in the code, it allows to clearly compute the time of each task.

When the "DMA completed" interrupt, the samples are read from their 32-bits formats and placed into a structure containing the number of the slot from which the sample comes and the value of the sample in "unsigned long" format. As shown on Figure 3.6, it takes 11.6 ms.

The last step is the "computation" step which computed the output from the samples of the ADC with the adaptive tripole and computed the cuff-imbalance to adapt the gains of the adaptive tripole. It was calculated to take 22.7 ms.

During the reading and the processing task, the CPU is running at 48 MHz. After the processing task during the sampling by the ADC and while waiting for the next "DMA completed" interrupt, it is in deep sleep allowing to spare power while continuing of sampling and transferring the samples with the DMA.

3.8 Measurement of the power consumption of the MCU with the adaptive tripole embedded code

The tests of the functionality of the code for ENG signal and artefact signals, can be found in Appendix L as the same tests will be realized on the full system and presented in the chapter 4. The tests realized on the MCU only were successful and proved its functionality. As the code is proved to be functional, it is time to measure its power consumption that is one of the figure of merit of this work.

The Figure 3.7 shows the power consumption of the running MCU for three different cases. The left column represents the consumption obtained in the previous master thesis [52] while the two others, the consumption obtained in this work for 48 MHz and 24 MHz frequencies for the clock of the CPU.

The power consumption is distributed among different tasks running on the CPU. The baseline task is the deep sleep, the CPU used in this work show a much lower consumption in deep sleep than in the previous work, $4.95 \mu\text{W}$ against $670 \mu\text{W}$. The DMA and ADC sampling at 20 kHz add $1300 \mu\text{W}$ to the case of only deepsleep for the previous work and $840 \mu\text{W}$ or $733 \mu\text{W}$ for respectively the 48 MHz and 24 MHz cases.

Finally, the blue portion associated with the periodic computation of the imbalance is much bigger for the previous Master thesis than for this work.

The total power consumption obtained for the best case at 24 MHz is **925 μW** against $2585 \mu\text{W}$ for the previous work representing 2.8 between them.

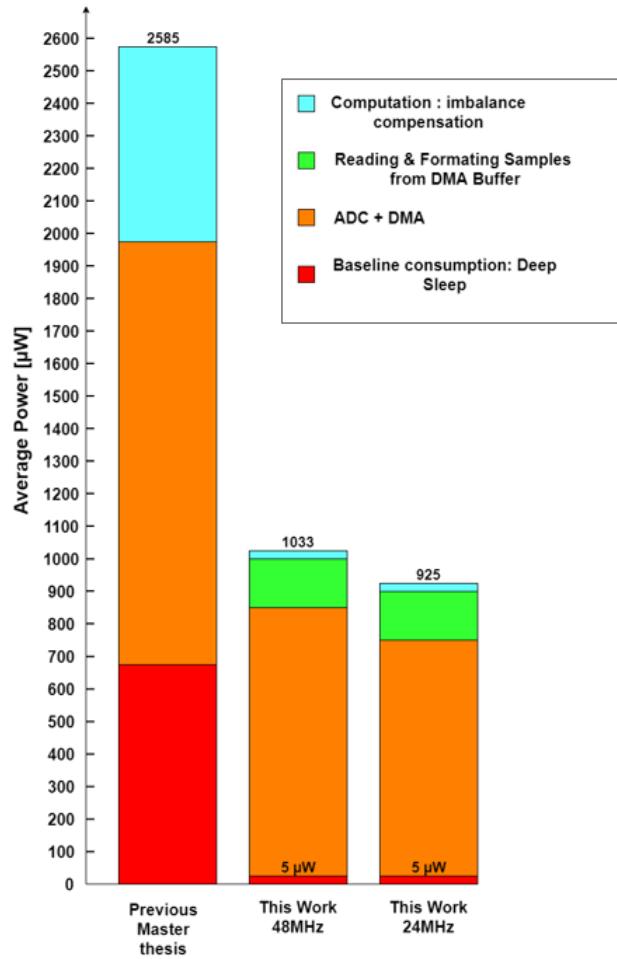


Figure 3.7: Power consumed by the different steps of the code for cuff-imbalance for this work with 48 MHz and 24 MHz and the previous work [52]

The Table 3.3 shows how changing the CPU clock frequency from 48 MHz to 24 MHz, impacts the power consumption.

Going from the top of the table, the deep sleep consumption does not change which is normal as the CPU is not active. Adding the ADC and DMA step shows a difference in power consumption of $106 \mu\text{W}$ from $839.05 \mu\text{W}$ to $733.05 \mu\text{W}$ added to the baseline power consumption of the deep sleep. The lecture step costs $14 \mu\text{W}$ more for the 24 Mhz case and the computation of the imbalance reduces the consumption of $16 \mu\text{W}$, from $39 \mu\text{W}$ to $23 \mu\text{W}$.

The total saving associated with the use of 24 MHz clock for the CPU instead of 48 MHz is then $108 \mu\text{W}$ representing 10,45 %.

Power consumption @ 1.8 V	48 MHz	24 MHz
Deep Sleep [μW]	4.95	4.95
+ ADC/DMA [μW]	844	738
+ Lecture Data [μW]	994	902
+ Computation imbalance	1033	925
= Total [μW]		

Table 3.3: Comparison of power consumption for the same code running on the Apollo3 for 24–48 MHz of CPU clock frequency.

Chapter 4

Test on the complete system, final results and position among other works

After the design of the AFE and the digital back-end separately, the full system must be tested. In this final chapter, the full system (AFE + digital back-end) is tested on artefact and ENG signals to ensure the functionality of both parts together. The full noise added by the system is also computed just after sampling and after the processing task (adaptive tripole) to expose the imprecision/noise due to the computed means and non fixed gains of the adaptive tripole. The power consumption of the full system is also computed. Finally, the work is compared to other works.

4.1 Measurement of the total noise of the system

Two experiments were realized to compute the noise at different steps of the full system. The first one aimed at finding what is the noise of one channel of the ADC when sampling the output of the AFE with its inputs to the ground. This means what is the total noise added on the samples after amplification and sampling. It results that the total noise on one channel is 38.42 LSB's knowing that already 32 LSB's ($2.4 \mu V_{rms}$) come from the amplification chain (AFE). This means that 21 LSB's should come from the sampling dynamic of the ADC. This result is not in accord with the result obtained from ADC characterization in chapter 3. The noise added by the ADC channel is supposed to be of 9.61 LSB's meaning 2.2 times less. A cause of this could be the use of a breadboard and long cables to connect all the input pins to the ground. If the noise added by the ADC was perfect, the total noise after sampling on one channel should be equal to 33.4 LSB's. The total

noise measured is then 1.15 times bigger. Figure 4.1.a shows the distribution of the noise around the mean with histogram. This histogram seems like a Gauss curve supposing that the main noise contribution is thermal. The figure 4.1.b confirms this, showing that the one-sided psd looks like a plateau with only a small part at the beginning that could be due to flicker noise.

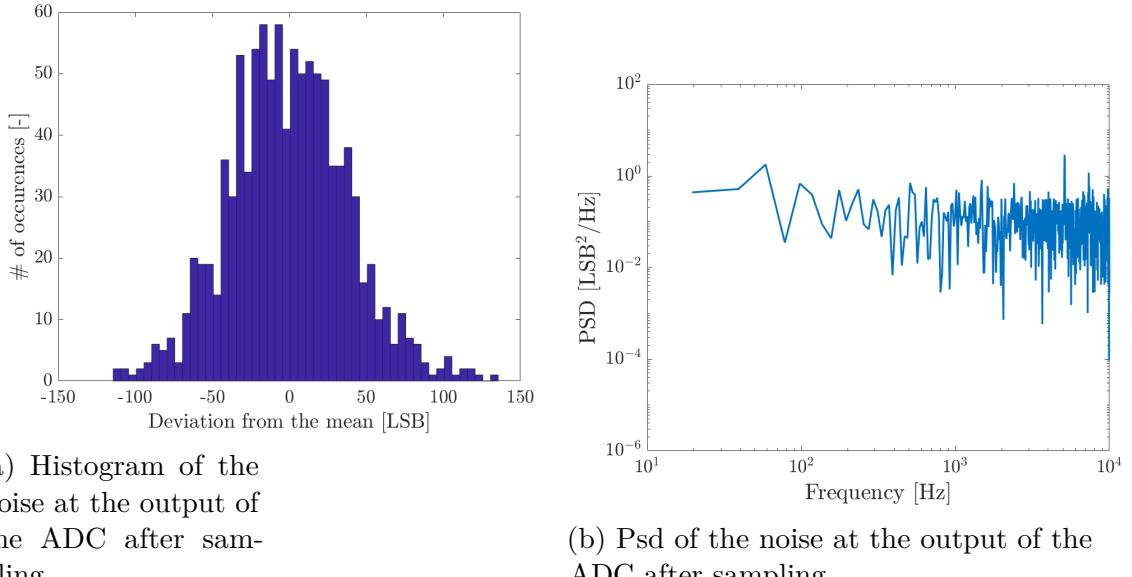


Figure 4.1: Noise figures at the output of the ADC 16 channel with AFE connected

The second experiment aims at measuring the total noise at the output of the digital back-end. This second experiment was still made with inputs of the AFE connected to the ground. The total noise measured is 69.45 LSB's. Using the measure of the experiment one, 38.42 LSB's, and multiplying by square root of two because of the noise addition of two independent channels, it should be 54.33 LSB's. Considering these 54.33 LSB's and the 69.45 LSB's obtained at the output in this second experiment, there is still a difference. This could come from the adaptive tripole and the gains evolving with time. In fact as the noise is present when sampling, the gain amplifies the difference between the two channels if they are not totally adapted for the imbalance and it could result in an increase of this difference. Also, the means of each ADC channel is computed and as noise is present from one time to another, the means can be adapted differently. This implies that the variance of the distribution of the mean is increased by the noise. Figures 4.2 can be compared to the ones of the first experiment. It can be seen on the graph that the one-sided psd have the same magnitude for the plateau as for the first test. Considering the histograms, in the second experiment, the maximum

values reached for samples is 200 LSB's while it is only around 120 LSB's for the first experiment. It highlights well that the processing with the adaptive tripole adds noise.

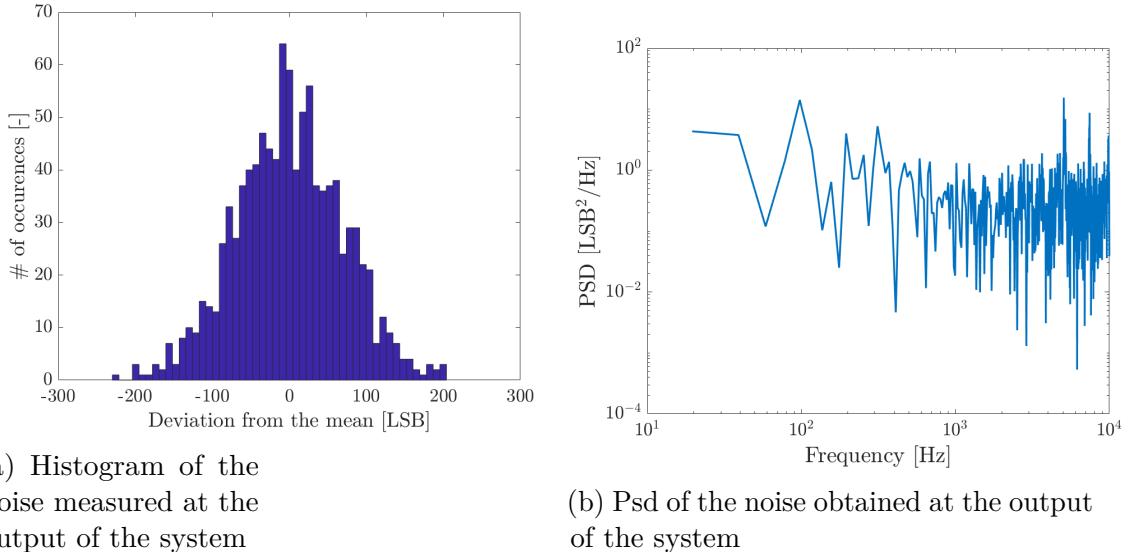


Figure 4.2: Noise figures at the output of the full system

Finally from the noise measurement an estimation of the reachable SNR can be computed. The total noise at the output is ≈ 70 LSB's or 25.6 mV_{rms} and the ENG signal is $7.1 \mu\text{V}_{rms}$ at the input of the integrated IA or 64.4 mV_{rms} after amplification and processing by the adaptive tripole. It should give an SNR of around 8 dB. As part of the noise is due to the adaption of the gains and the computation of the means, the total noise could be higher sometimes.

4.2 Test of the complete system

The last tests are performed on the full system when the AFE and the digital back-end are assembled. The tests are realized for the ENG and artefact.

4.2.1 Test with artefact

The artefact was tested applying different signals with different amplitudes to the three input pins of the AFE. The signal generated with the waveform generator is a sinusoidal at 100 Hz and with 10 mV of amplitude. According to the linearization effect the amplitude of the signal applied to the other pins was smaller. A decrease

of $89.3 \mu\text{V}$ of amplitude was made to simulate the linearization effect meaning that the input pin 2 was $89.3 \mu\text{V}$ smaller in magnitude than input pin 1. To simulate an imbalance, the amplitude difference between input 2 and 3 should be different than between input pin 1 and 2 as the linearization effect is not ideal in case of imbalance. The difference between input pin 2 and input pin 3 was then chosen to be $\frac{1}{4}$ of the difference between input pin 1 and input pin 2 meaning $22.325 \mu\text{V}$. This choice of amplitude difference was done according to Table 2.1 that reveals the maximum amplitude between the voltage sensed by two consecutive electrodes of the tripolar cuff-electrodes, is $100 \mu\text{V}$. This choice of imbalance is well exaggerated to test the robustness of the adaptive tripole. The set-up used it illustrated on figure 4.3.

To test the effectiveness of the adaptive tripole on artefact rejection, two experiments are made, one with the gains non-adapting to imbalance, then fixed to 1000, and one with the gains being adapted.

The aim of the system combining the AFE and the digital beck-end, is to cancel the presence of the artefact and to output an amplified version of the ENG signal. On the set-up of the Figure 4.3, the input signals of the two ADC channels are different in term of amplitude, 866 mVpp for the ADC0/ADC16 (because the gpio pin16 is used for the input of this ADC) channel and 216 mVpp for the ADC1/ADC32 channel. This difference in magnitude comes from the difference of amplitude at the input pins. The difference of $89.3 \mu\text{W}$ between input pin 1 and input pin 2 is amplified by 4800 V/V , the total gain of the AFE giving 433 mV of amplitude for the AC signal or 866 mVpp . The difference of amplitude between input pin 2 and input pin 3 being 4 times smaller the output of this channel as an magnitude 4 times smaller then 216 mVpp .

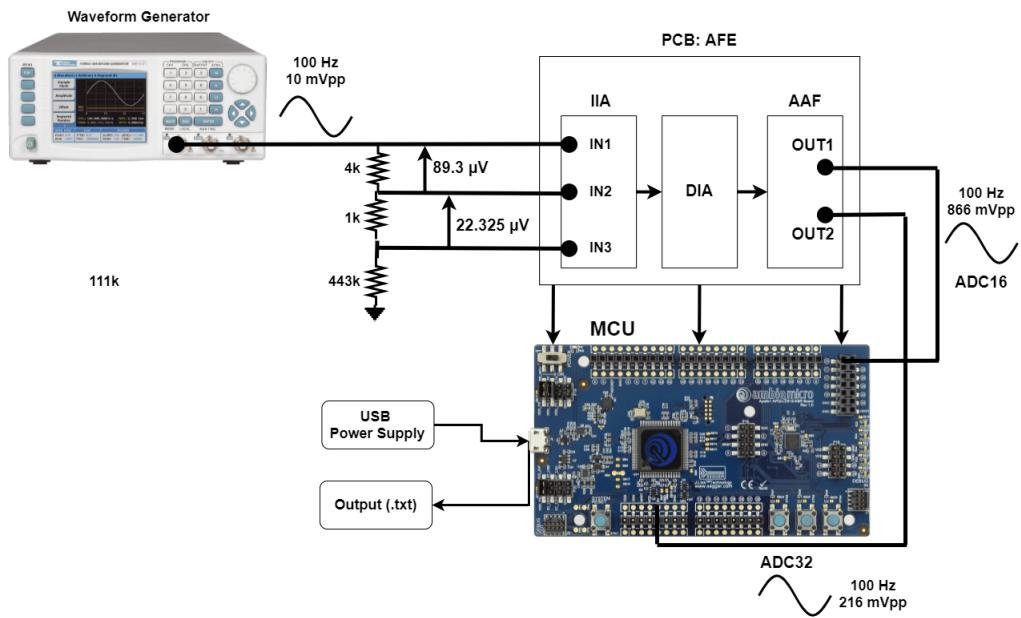


Figure 4.3: Set-up used to test the efficiency of the adaptive tripole on artefact

On the Figure 4.4, the gain are not adapted (adaptive tripole off) meaning that no importance is given to the signal from the ADC0 or the ADC1, both gains are equal. The result is the apparition of a reduced artefact at the output of the MCU but it still present.

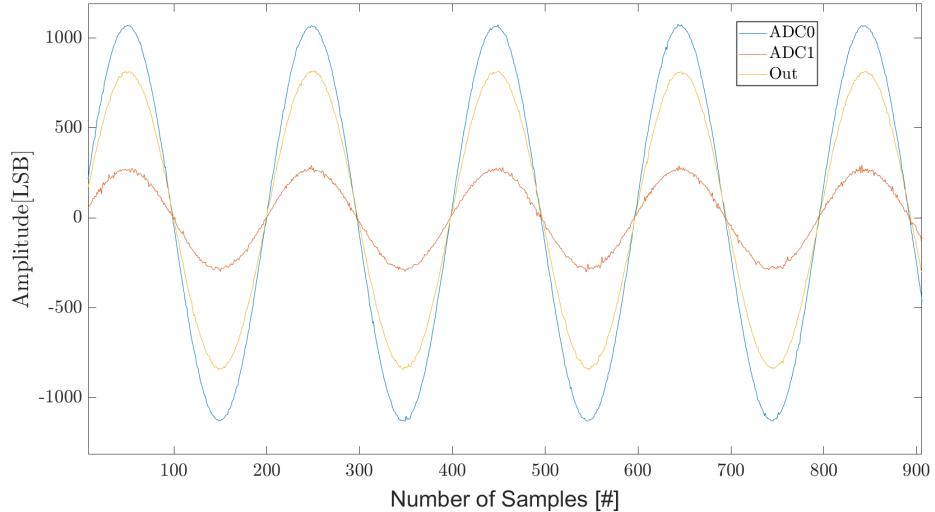


Figure 4.4: Output of the MCU for an artefact applied without adaptive gains

On Figure 4.5, this time the adaptive tripole is activated. The output is closed to 0, this means that the artefact is perfectly rejected and the gains are well adapted. The final gains are 400 for the ADC0 and 1600 for the ADC1 (due to the use of Precision factor of 1000) corresponding to the expected gains as one signal has times the amplitude of the other (imbalance of $\frac{1}{4}$).

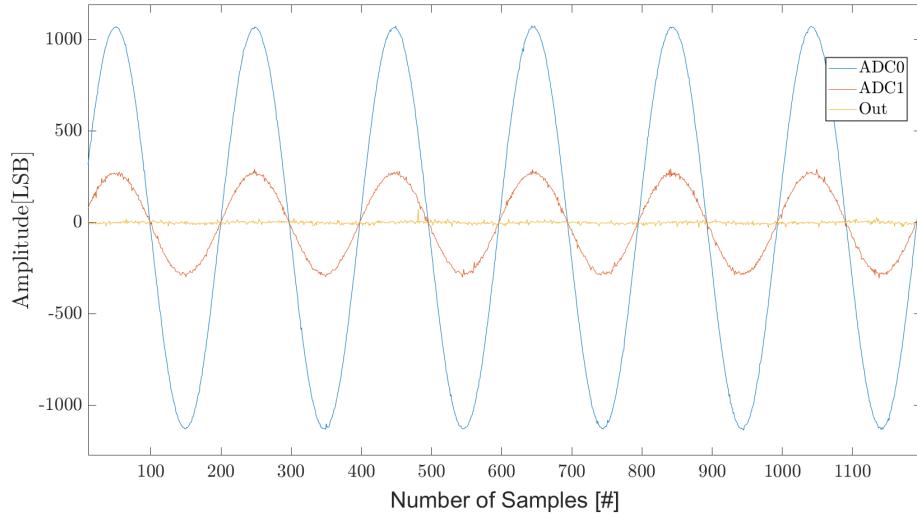


Figure 4.5: Output of the MCU with artefact applied and with adaptive gains

A zoomed output after cancellation of the artefact by the adaptive tripole is shown on Figure 4.6. The artefact is removed and no oscillation can be seen at the output. The peaks on the graph are due to noise. This noise is measured to be equal to 73 LSB's that is around the total measured noise in the previous section "Measurement of the total noise of the system" and was of 69.45 LSB's

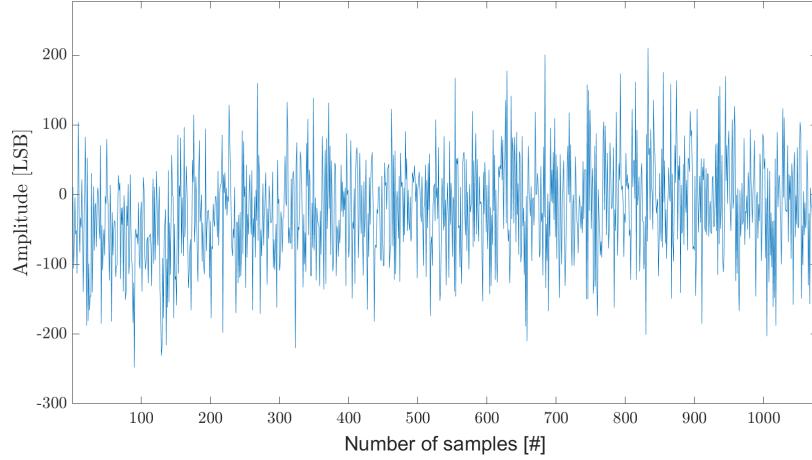


Figure 4.6: Output of the full system for artefact at its input

The Figure 4.7 shows the single-sided psd of the noise obtained at the output after artefact rejection by the adaptive tripole. The form of this psd, is the same as the one obtained in section "Measurement of the total noise of the system" and depicted on figure 4.2b. It begins with a noise that decreases linearly due to the flicker noise and then a plateau corresponding to thermal noise.

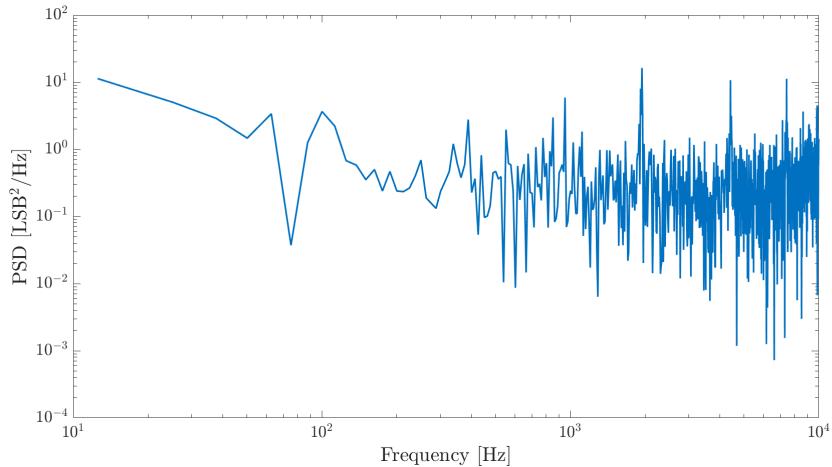


Figure 4.7: Psd of the output of the full system for artefact at its input

4.2.2 Test with ENG

The aim is to see if the ENG signal can be recognized at the output despite the noise added by the system. The same set-up as for the test with artefact,

figure 4.3, is used but this time, the experiment was made by connecting the two border input pins of the AFE to the ground because of the weighted sum of the tripolar cuff-electrodes when sensing the ENG signal, see Figure 1.3 leading to the approximation that border pins can be grounded. The center pin (input pin 2) is connected to a sinusoidal with $10 \mu\text{V}$ of amplitude as the ENG is supposed to be $7.1 \mu\text{V}_{rms}$ in average. In fact, it is impossible to generate triphasic shapes (shape of the ENG signal as seen in Chapter 1) with the available material, the generated signal to simulate the ENG was then chosen to be a sinusoidal of $10 \mu\text{V}$ of amplitude and 200 Hz of frequency. This gives the same rms value as for the ENG.

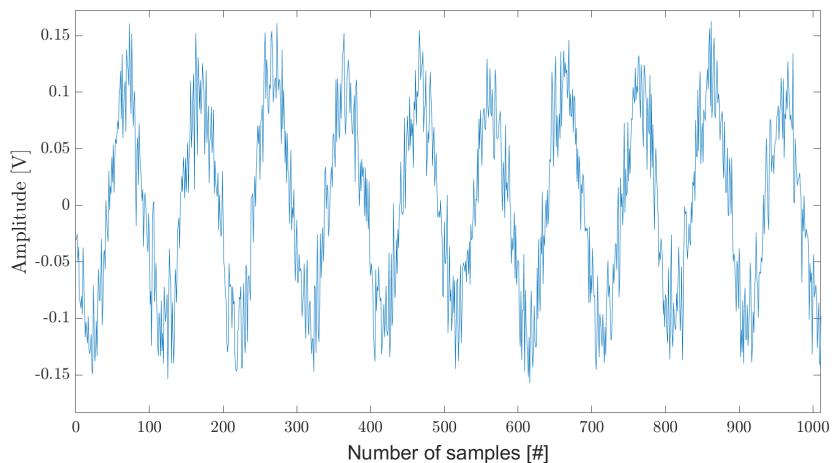


Figure 4.8: Outputted ENG signal after amplification and processing by the adaptive tripole

By using the "snr module" of Matlab, the obtained value for the SNR is 8.35 dB with a resolution for the ADC of 12 bits. This result confirms the expected SNR computed in the section 4.1. The SNR obtained using 14 bits, is 9.23 dB. The increase of SNR is good when using higher resolution but at the cost of more power consumption and as the obtained SNR with 12 bits of resolution is already good, it is not necessary. It is then better to privilege this resolution and to get a lower power consumption as it is more suitable for long term implants. SNR graphs can be viewed in Appendix K.

4.3 Total power consumption

The total power consumption of the AFE and MCU is resumed on the Figure 4.9. The detailed power consumption of the AFE part is explained in the chapter

2. This $1623 \mu\text{W}$, achieved by this work at 24 MHz, can be compared to the $3800 \mu\text{W}$ achieved in the previous work ([52]). It is a division of the total power consumption by a factor 2.34. In the figure is also depicted the result that could be achieved if the more adapted LDO was chosen as explained in section 2.4.3 of the chapter 2. Recalling that the LDO is the main source of power consumption in the AFE designed in this work. It could be possible to achieve $1132 \mu\text{W}$ meaning a reduction of 31% of the power consumption compared to result obtained for 24 MHz in this work.

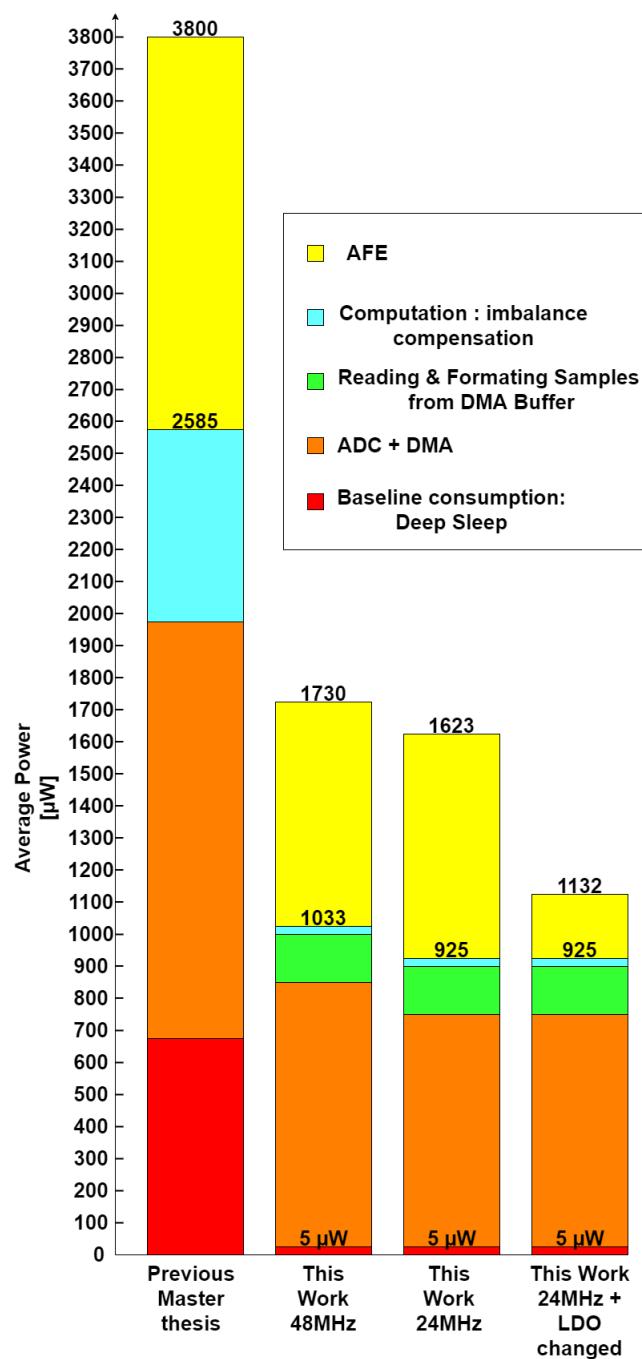


Figure 4.9: Total Power consumption for different frequencies of CPU, with a better LDO and of the previous work ([52])

4.4 Comparison with other Works

The Table 4.1 compares the results obtained to similar works. The comparison is done according to the two figures of merit, the noise and the power consumption.

	Triantis [15]	Shon [62]	WineRS-8 [63]	Previous master thesis [52]	This work
Stimulation	No	Yes	Yes	No	No
Recording	Yes	Yes	Yes	Yes	Yes
Simulations	Yes	Yes	No	Yes	Yes
Tested on real subjects (animals)	Yes	Yes	Yes	No	No
Sampling frequency [kHz]	20-25	10	25	20	20
SNR [dB]	5.02 (SIR)	5.46	2.12	4 (SIR)	>8
Power consumption [mW]	5	18.48	18.9	3.8	1.623
Year	2005	2018	2018	2020	2021

Table 4.1: Comparison with other works for peripheral nerve sensing

All the works in Table 4.1 are works that designed peripheral nerve sensing devices. The comparison between the results obtained in this work and the others, is done on some criteria.

Power Consumption

In terms of power consumption, the only work that could be compared is the Triantis on ([15]) as the other also stimulate the nerve. As the sampling rate is between 20-25 kHz for [15] and 20 kHz for this work and knowing that the sampling rate directly influenced the power consumption, it is reasonable to compare the power consumption of this work to the one obtained in this master thesis. Compared

to Triantis [15], the proposed design of this work consumes 67.54 % less. If the currently used LDO could be changed for the "TPS7A0512PDBZR" [44], it would go to 77.36%. To have more scale of power in order to locate the results of this work, the Table 4.2 resumed the power consumption of different implantable medical devices that can be found on the market (Source [64]). It can be seen that in the case where the LDO is changed, the proposed design does better than two of the medical implants in this list, the cochlear and the muscle stimulator.

Implant device	Power consumption [μW]
Cochlear	5 160
Muscle stimulator	1 300
Drug pump	400
Neuro-stimulator	50
Pacemaker	8

Table 4.2: Power consumption of different implantable medical devices (Source [64])

Noise

The metric used to see if the signal can be detected properly is the SNR. This work achieved an SNR of 8.35 dB with 12 bits of resolution for the ADC. Compared to the other work, this result is really good. In fact, the second best SNR is achieved by [62] and is equal to 5.46 dB that is almost 3 dB less. Concerning the result of [15], this work obtained 5.02 dB but it is the SIR that also take into account the interference of other signals. Also the previous master thesis [52] achieved a SIR of 4 dB while this work a SNR of 8.35 dB.

4.5 Perspective

LDO : As already stated before, the use of another LDO will lead to a decrease of power consumption.

Voltage reference of the discrete IA : As the inner voltage reference of the ADC is 1.5V, using a voltage reference of 0.75V instead 0.9V for the discrete IA will allow to have a bigger margin for amplification. The dynamic range would increase from [0.3,1.5] V at input of the ADC to [0,1.5] V. Further amplification

with the discrete is nonetheless not a good idea as it will also result in more power consumption and more amplification of the noise due to the integrate IA that is the main source of noise.

Amplification : As the SNR obtained is really good, it would be possible to amplify less the signal in order to select an amplifier with less GBWP and therefore consumes less power.

Test of the system on ENG and artefact : To finally test the efficiency of the system, it would be nice to test on ENG and artefact superposed to see if the ENG found at the output is still as good as when only ENG is applied and see if the SNR is still 8.35 dB.

Using float instead of integers : In general, the arithmetic with integers is faster than with floats allowing to make the adaptive tripole processing faster and then going more in deep sleep and saving power. But it might be possible to reduce power by using float instead of integers in this work. In fact, the MCU has a floating point unit allowing to make calculations faster with floats. From this point, it might then be possible that using float allows to finish faster the adaptive tripole processing task as the used of integers is associated with divisions and multiplications to keep decimals. As these multiplications and divisions are done in a for loop iterating on the size of the input buffer, it might be possible that the gain in speed associated with the use of arithmetic with integers, is less than the time loss due to the high number of multiplications and divisions associated also with the use of integers and that are not present with the use of floats. It would be then interesting to test the embedded code for adaptive tripole with floats instead of integers and to see which version take less time allowing to go faster in deep sleep and saving power. The power consumption of the running embedded code must be computed in both case as the use of floating point unit might also lead to an increase of power consumption.

Conclusion

Epilepsy is a disorder that affects more than 50 million people worldwide [6]. Everybody can be touched by epilepsy during their life. Most used treatments are drugs but about one-third of patients are drugs resistant leading to the need of a suitable solution to reduce the seizures frequencies and intensities. This is the aim of solutions such as surgery, ketogenic diet, DBS and VNS [19],[20]. The first three are functional solutions but either present high risks or are very constraining. A last solution is the VNS that is a better solution for long time treatments. As VNS stimulates the vagus nerve when seizures onset is detected. An important part of the VNS, is to correctly find when the seizures occurred. It appears that bio-markers associated with epileptic seizures pass through the vagus nerve with a triphasic shape [8].The main issue is the parasitic signals known as artefacts. Those have a higher amplitude in mV than the ENG signal in μ V [14] [15].

The use of tripolar cuff-electrodes allows to have a linearization effect on the artefacts and combined with a tripolar model, the ENG signal can be isolated from those artefacts [14] [15]. In an ideal world, only the ENG signal is sensed and the electrodes are perfectly matched and distances between each consecutive pairs are equal meaning the nerve impedance between each is also equal. But in reality, there are parasitics signal and mismatch of the electrodes. Those non-idealities are called imbalance. To take those imbalances into account, an adaptive tripole is used (Source [14], [15]).

This work proposes the implantation and design of a system to detect the bio-markers associated with epileptic seizures. The design of this system has for targets two figures of merit that are high SNR to correctly identify the bio-markers and low power consumption to make the system suitable for long term implant. The system is composed of an analog front-end for amplification, filtering and going from tripolar to differential signal, and a digital back-end implementing the adaptive tripole as it offers the possibility of low power consumption and miniaturized device.

The design of these two parts was realized through this work in different chapters.

In Chapter 2, the AFE is designed to have a small amount of added noise and a low power consumption. It was computed that the total gain that must be applied to the VENG signal is 4800 [V/V]. From this total gain, the configuration of the integrated IA was chosen to have a gain of 63.8 [V/V] and the rest of the gain was left to the discrete IA. The design began by investing on how the partition of the gain among the different stages of amplification of the discrete IA, affects the total noise. It was then decided to give to the first stage of the discrete IA a gain of 30 among the 75 required and the rest to the second stage as the trade-off between noise reduction and power consumption due to the need of higher GBWP was not favorable. Next, according to the partition of the gain, suitable operational amplifiers were selected. A PCB was next designed to carry the AFE. Finally, the AFE was tested in laboratory to ensure the functionality of it. The total power consumption of the AFE, achieved is $698 \mu\text{W}$ resulted from a bad choice of LDO. If the LDO could be changed for the "TPS7A0512PDBZR" [44], the total power consumption would be $207 \mu\text{W}$. The total input referred noise added by the AFE is $2.4 \mu\text{V}_{rms}$.

The third chapter was focusing on the implantation of the adaptive tripole on the MCU. Firstly, a choice of MCU was with q target of low power consumption. Then, specifications of the adaptive tripole, sampling frequency, sleep mode and CPU frequency were realized. The ADC sampling frequency was chosen at 20 kHz to avoid aliasing as the ENG signal is proved to go up to 10 kHz. The adaptive tripole was then implemented and tested in laboratory. Once functional, the power consumption of the embedded code was measured for different configurations of the MCU and the lowest power consumption achieved is $925 \mu\text{W}$.

The Chapter 4 was focusing on measuring the functionality of AFE and digital back-end together and measuring the SNR. It appears that the bio-markers are correctly identified at the output of the system. The SNR achieved is 8.35 dB in the case of 12-bits resolution for the ADC. To conclude some perspectives for further improvements such as the use of floats instead of integers, lowering the total gain to achieve lower power consumption the SNR is good,... or experiments that could be realized were given.

The results obtained according to these two figures of merit, are resumed:

- Total power consumption of 1.623 mW or 1.132 if the LDO is changed
- SNR of 8.35 dB

The power consumption is in the range of other medical implants and even lower than the cochlear or muscle stimulator.

The SNR achieved is very high compared to works on similar nerve detection that were around 5 dB at the best.

This work is concluded by the proven efficiency of the system with generated signals. The power consumption and SNR achieved are both good. It opens the opportunity of further investigations were this system will be tested on real subjects. It also allows to consider the implementation developed to record other nerves with medical interests.

Bibliography

- [1] World Health Organization, accessed January 25 2021, <https://www.who.int/news-room/fact-sheets/detail/epilepsy>
- [2] Mayo Clinic. Epilepsy, accessed 25 May 2021, <https://www.mayoclinic.org/diseases-conditions/epilepsy/diagnosis-treatment/drc-20350098>
- [3] Mayo Clinic. Epilepsy, accessed 25 May 2021, <https://www.mayoclinic.org/diseases-conditions/epilepsy/symptoms-causes/syc-20350093>.
- [4] Dr. Henri RUBINSTEIN. Chiffres clés et prévalence de l'épilepsie, 05/08/2018 (accessed May 5, 2021). <https://www.carenity.com/infos-maladie/epilepsie/chiffres-cles-et-prevalence-381>
- [5] Association of Neurological Surgeons American. Epilepsy, accessed May 6, 2021. <https://www.aans.org/en/Patients/ Neurosurgical-Conditions-and-Treatments/Epilepsy>.
- [6] Patrick Kwan and Martin J. Brodie. Early identification of refractory epilepsy. New England Journal of Medicine, 342(5):314–319, 2000. PMID: 10660394.
- [7] WebMD. Help When Epilepsy Treatment Doesn't Work, (accessed May 6, 2021). <https://www.webmd.com/epilepsy/refractory-epilepsy?prop16=vb4t&tex=vb4t>.
- [8] Lars Stumpf, Hugo Smets, Simone Vespa, Joaquin Cury, Pascal Doguet, Jean Delbeke, Emmanuel Hermans, Christian Sevcencu, Thomas N. Nielsen, Antoine Nonclercq, and Riem El Tahry. Recording of spontaneous vagus nerve activity during pentylenetetrazole-induced seizures in rats. Journal of Neuroscience Methods, 343:108832, 2020.
- [9] J. J. Struijk, M. Thomsen, J. O. Larsen, and T. Sinkjaer. Cuff electrodes for long-term recording of natural sensory information. IEEE Engineering in Medicine and Biology Magazine, 18(3):91–98, 1999.

- [10] W. M. Grill and J. T. Mortimer. Stability of the input-output properties of chronically implanted multiple contact nerve cuff stimulating electrodes. *IEEE Transactions on Rehabilitation Engineering*, 6(4):364–373, 1998.
- [11] La rédaction de Doctissimo. Qu'est-ce que l'épilepsie ?, accessed May 5, 2021, https://www.doctissimo.fr/html/dossiers/epilepsie/sa_3687_epilepsie_definition.htm.
- [12] Bauer B, Tang F, Hartz AMS. Drug-resistant epilepsy: Multiple hypotheses, few answers. *Frontiers in Neurology*, July 2017.
- [13] Kenneth D. Laxer, Eugen Trinka, Lawrence J. Hirsch, Fernando Cendes, John Langfitt, Norman Delanty, Trevor Resnick, and Selim R. Benbadis. The consequences of refractory epilepsy and its treatment. *Epilepsy Behavior*, 37:59 – 70, 2014.
- [14] Mouhamed Saleh Rahal. Optimisation of nerve cuff electrode recordings for functional electrical stimulation applications. July 2001.
- [15] Iasonas F.Triantis. An adaptive amplifier for cuff imbalance and interference reduction in nerve signal recording. (6), 6 2005.
- [16] B.N.Harding M.V.Squier S.M. Sisodiya, W.-R. Lin and M. Thom. Drug resistance in epilepsy: expression of drug resistance proteins in common causes of refractory epilepsy. *Med Biol Eng Comput*, pages 22–31, 2002.
- [17] Magdalena R. Epilepsy, active and impaired functions of the nervous system, July 2014 accessed May 5, 2021, <https://www.slideshare.net/MagdalenaReszke/epi-37166883>.
- [18] Robert H. Howland. Vagus nerve stimulation. *Current behavioral neuroscience reports*, 1,2:64–73, 10 2014.
- [19] Ligue francophone belge contre l'épilepsie. Traitement, accessed May 5, 2021, <https://ligueepilepsie.be/+-Traitement--+.html>.
- [20] National Institute of Neurological Disorders and Stroke. The Epilepsies and Seizures: Hope Through Research, June 2020. <https://www.ninds.nih.gov/Disorders/Patient-Caregiver-Education/Hope-Through-Research/Epilepsies-and-Seizures-Hope-Through#top>
- [21] Stella Manta. Effets neurophysiologiques de la stimulation du nerf vague : Implication dans le traitement de la dépression résistante et optimisation des paramètres de stimulation. *International Journal of Neural Systems* Vol. 23, No. 6, 1 2012.

- [22] American Association of Neurological Surgeons. Deep Brain Stimulation, accessed July 2020. <https://www.aans.org/en/Patients/Neurosurgical-Conditions-and-Treatments/Deep-Brain-Stimulation>
- [23] J.J. Struijk. The extracellular potential of a myelinated nerve fiber in an unbounded medium and in nerve cuff models. Biophysical Journal, 72(6):2457 – 2469, 1997
- [24] Joaquin Hoffer. Techniques to Study Spinal-Cord, Peripheral Nerve, and Muscle Activity in Freely Moving Animals, volume 21, pages 65–145. 02 2008.
- [25] Andreas Demosthenous Iasonas F.Triantisa. Electrophysiological responses from vagus nerve stimulation in rats. Medical engineering and physics, 30, 6 2008.
- [26] N. Donaldson M. Rahal, J. Taylor. The effect of nerve cuff geometry on interference reduction: a study by computer modeling. IEEE Transactions on Biomedical Engineering, 30, 1 2000.
- [27] Mayo Clinic, "Vagus nerve stimulation", accessed 26 May 2021 ,<https://www.mayoclinic.org/tests-procedures/vagus-nerve-stimulation/about/pac-20384565>
- [28] Ryvlin P, Rheims S. Epilepsy surgery: eligibility criteria and presurgical evaluation. Dialogues Clin Neurosci. 2008;10(1):91-103. doi:10.31887/DCNS.2008.10.1/pryvlin
- [29] "Op Amp Noise Analysis", Simon Brandle , accessed January 27 2021, http://www.simonbramble.co.uk/techarticles/op_amp_noise/op_amp_noise.htm
- [30] NI, Noise Analysis Using Analog Devices Operational Amplifiers in Multisim, accessed January 31 2021. <https://knowledge.ni.com/KnowledgeArticleDetails?id=kA03q000000YGtZCAW&l=fr-BE>
- [31] Texas Instrument,'Datasheet TLV904x Micro-power', accessed January 25 2021 https://www.ti.com/lit/ds/symlink/tlv9042.pdf?ts=1619358442528&ref_url=https%253A%252F%252Fwww.mouser.be%252F
- [32] ST,'Datasheet TSV6191, TSV6191A, TSV6192, TSV6192A', accessed January 25 2021 https://www.st.com/content/st_com/en/products/amplifiers-and-comparators/operational-amplifiers-op-amps/precision-op-amps-lt50-mhz/low-power-op-amps-lt1-ma/tsv6191.html

- [33] Microship, 'Datasheet MCP6241', accessed January 25 2021 <https://www.microchip.com/downloads/en/DeviceDoc/21882d.pdf>
- [34] ST, 'Datasheet TSZ121 ', accessed January 25 2021 <https://www.st.com/en/amplifiers-and-comparators/tsz121.html>
- [35] ST, 'Datasheet TSV62x, TSV62xA ', accessed January 25 2021 <https://www.st.com/resource/en/datasheet/tv624.pdf>
- [36] ON Semiconductor, 'NCS20094: Operational Amplifier ', accessed January 25 2021 <https://www.onsemi.com/products/amplifiers-comparators/operational-amplifiers-op-amps/ncs20094>
- [37] Microship, 'Spice Models MCP6241, accessed 25 January 2021, <https://www.microchip.com/doclisting/TechDoc.aspx?type=Spice>
- [38] Texas Instrument Inc., "Op-Amp Noise Calculation and Measurement", accessed 13 February 2021, <https://picture.iczhiku.com/resource/eetop/SIkHEFiIIDH1SccB.pdf>
- [39] Research Gate, "AC-Coupled Front-End for Biopotential MeasurementsEnrique Mario Spinelli , Student Member, IEEE, Ramon Pallàs-Areny, Fellow, IEEE, and Miguel Angel Mayosky, Senior Member, IEEE", accessed 28 February 2021, https://www.researchgate.net/publication/10826990_AC-Coupled_Front-End_for_Biopotential_Measurements
- [40] Mouser, "MAX8518EUB+T", accessed 26 January 2021, <https://www.mouser.be/datasheet/2/256/MAX8516-1514578.pdf>
- [41] Mouser, "LM334DT", accessed 26 January 2021, <https://www.mouser.be/datasheet/2/389/cd00000458-1795286.pdf>
- [42] Meta chart, accessed 26 May 2021, <https://www.meta-chart.com/pie#/data>
- [43] Texas Instrument, "TLV9042 : Design development", accessed 20 January 2021, <https://www.ti.com/product/TLV9042#design-development>
- [44] Texas Instrument, "TPS7A05 ", accessed 15 May 2021, https://www.ti.com/lit/ds/symlink/tps7a05.pdf?HQS=dis-mous-null-mousermode-dsf-pf-null-wwe&ts=1623233199595&ref_url=https%253A%252F%252Fwww.mouser.co.il%252F

- [45] Planet Analog, "ADC Guide, Part 13: Input Impedance" , accessed 26 February 2021, <https://www.planetanalog.com/adc-guide-part-13-input-impedance/>
- [46] Texas Instrument, "ADC Source Impedance", accessed 26 February 2021, <https://www.ti.com/lit/an/spna061/spna061.pdf>
- [47] Tektronix, " Digital Storage Oscilloscope: TBS2000 Series Datasheet", <https://www.tek.com/datasheet/digital-storage-oscilloscope>
- [48] Keithley, "2450 SourceMeter SMU Instrument Datasheet" , accesed 1 May 2021 ,https://download.tek.com/datasheet/2450-Datasheet_1KW-60904-0.pdf
- [49] "Datasheet apollo 2", fujitsu, accessed January 26 2021 https://www.fujitsu.com/uk/imagesgig5/Apollo2_Blue MCU Data_Sheet_rev0p8.pdf
- [50] "Datasheet apollo 3", fujitsu, accessed January 26 2021 https://www.fujitsu.com/uk/imagesgig5/Apollo2_Blue MCU Data_Sheet_rev0p8.pdf
- [51] Microchip. MCP621/1S/2/3/4/5/9 20 MHz, 200 μ V Op Amps with mCal, accessed October 15 2020. <https://www.microchip.com/wwwproducts/en/MCP624>
- [52] Coppieters de Gibson, Louise. Ultra-low-power miniaturized vagus nerve sensing platform for treating refractory epilepsy. Ecole polytechnique de Louvain, Université catholique de Louvain, 2020. Prom. : Bol, David. <http://hdl.handle.net/2078.1/thesis:26649>
- [53] Ambiq, Apollo 3 Blue, accessed January 26 2021, <https://ambiq.com/apollo3-blue/>
- [54] Ambiq, Apollo 3 Blue datasheet, accessed January 26 2021, <https://ambiq.com/wp-content/uploads/2020/10/Apollo3-Blue-MCU-Datasheet.pdf>
- [55] Ambiq, Apollo 2 Blue, accessed January 26 2021, <https://ambiq.com/apollo2-blue/>
- [56] Ambiq, Apollo Blue, accessed January 26 2021, <https://ambiq.com/apollo/>
- [57] Ambiq, Apollo 4 Blue, accessed January 26 2021, Ambiq, Apollo 3 Blue, accessed January 26 2021, <https://ambiq.com/apollo4-blue/>
- [58] STMicroelectronics, Ultra-low-power STM32L0x3 advanced Arm®-based 32-bit MCUs , accessed January 25 2021 , <https://www.st.com/en/microcontrollers-microprocessors/stm32l073rz.html#overview>

- [59] Cure Epilepsy, accessed May 19 2021, <https://www.cureepilepsy.org/for-patients/what-is-and-what-causes-epilepsy/>
- [60] <https://www.mayoclinic.org/diseases-conditions/epilepsy/symptoms-causes/syc-20350093>:text=Brain%20conditions%20that%20cause%20damage,viral%20encephalit
- [61] Andreas Demosthenous, John Taylor, Iasonas Triantis, Robert Rieger, and N. Donaldson. Design of an adaptive interference reduction system for nerve-cuff electrode recording. Circuits and Systems I: Regular Papers, IEEE Transactions on, 51:629 – 639, 05 2004.
- [62] Ahnsei Shon, Jun-Uk Chu, Jiuk Jung, Hyungmin Kim, and Inchan Youn. An implantable wireless neural interface system for simultaneous recording and stimulation of peripheral nerve with a single cuff electrode. Sensors, 18(1), 2018.
- [63] Koripalli M.K. Jia Y. et al. Lee, B. An implantable peripheral nerve recording and stimulation system for experiments on freely moving animal subjects. Sci Rep, 8, 2018.
- [64] Meriam Gay Bautista, Eryk Dutkiewicz, and Michael Heimlich. Subthreshold energy harvesters circuits for biomedical implants applications. In BODYNETS, 2015.

Appendix A: Information on the integrated IA

Equations of the integrated IA

$$V_{out,+} = \frac{1}{2}G_{IIA}(V_{in,+} - V_{in,-}) + V_{offset}$$
$$V_{out,-} = -\frac{1}{2}G_{IIA}(V_{in,+} - V_{in,-}) + V_{offset}$$

Voltage Noise density

This Figure shows the voltage noise density of the integrated IA and comes from the previous work [52].

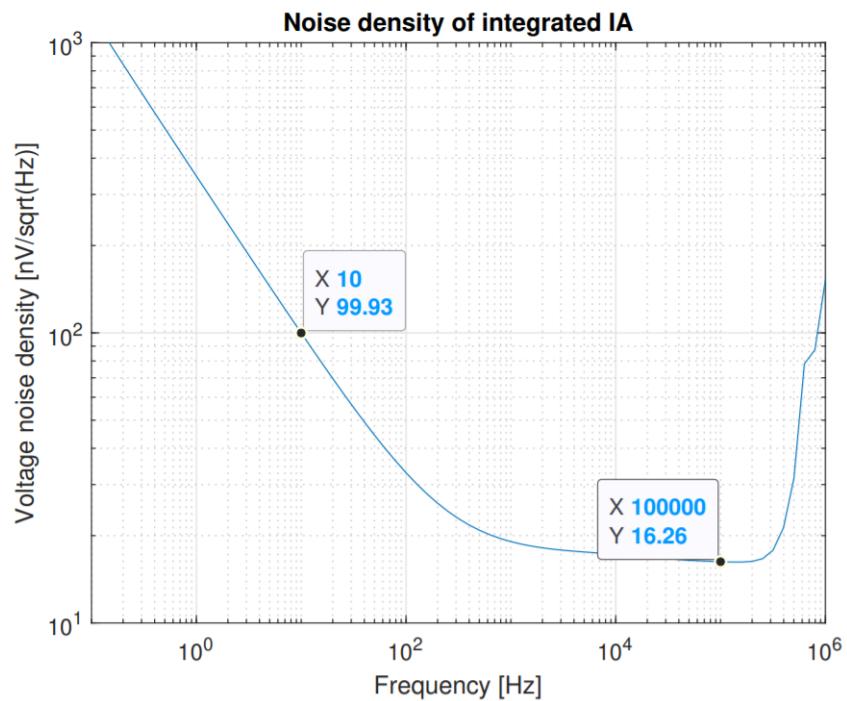


Figure 4.10: Voltage noise density of the Integrated IA from [52]

Configurations

Available configurations of the Integrated IA

	C1	C2	C3	C4
Power [μW]	0.631	1.31	5.41	23.9
Noise [μV_{rms}]	1.36	0.67	0.36	0.23
Gain [V/V]	48.9	32.6	44.3	63.8
Max BW [kHz]	29.3	82.1	185.6	279.5

Table 4.3: Configurations for the Integrated IA, information taken from [52]

Appendix B: discrete IA equations

Total transfer function

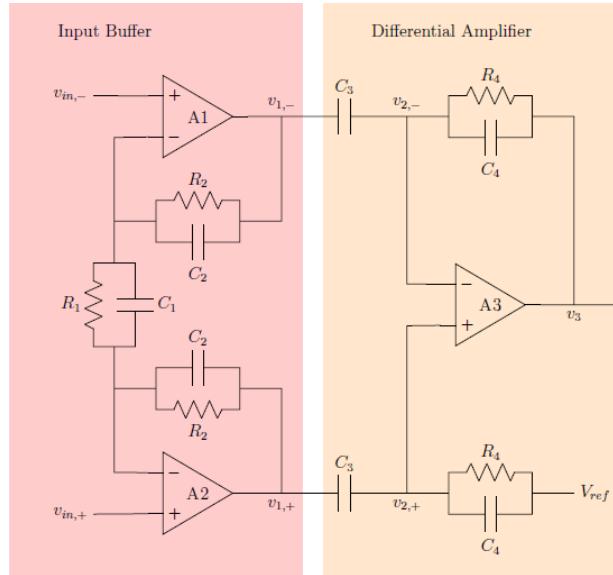


Figure 4.11: Discrete IA (figure from [52])

The transfer function of the discrete IA is obtained through different steps. First, $v_{1,-}$ and $v_{1,+}$ are computed in function of $v_{in,-}$ and $v_{in,+}$.

$$v_{1,-} = \frac{Z_2}{Z_1}(v_{in,-} - v_{in,+}) + v_{in,-}$$

$$v_{1,+} = \frac{Z_2}{Z_1}(v_{in,+} - v_{in,-}) + v_{in,+}$$

Then, $v_{2,-}$ and $v_{2,+}$ are expressed in function of $v_{1,-}$, $v_{1,+}$, v_3 and V_{ref} .

$$v_{2,-} = \frac{Z_4}{Z_3 + Z_4} v_{1,-} + \frac{Z_3}{Z_3 + Z_4} v_3$$

$$v_{2,+} = \frac{Z_4}{Z_3 + Z_4} v_{1,+} + \frac{Z_3}{Z_3 + Z_4} V_{ref}$$

If the gain of the operation amplifiers is ideal $v_{2,-} = v_{2,+}$. It allows to express v_3 in function of $v_{in,-}$, $v_{in,+}$ and V_{ref} .

$$v_3 = \frac{2Z_2 + Z_1}{Z_1} \frac{Z_4}{Z_3} (v_{in,+} - v_{in,-}) + V_{ref}$$

In this last equation that is the total transfer function of the discrete IA, the first term is the gain associate with the input buffer and the second one with the differential stage.

Gains and cut-off frequencies of the input buffer

The gain of the input buffer can be further developed to highlight the different cut-off frequencies. The gain is developed as follow:

$$\frac{2Z_2 + Z_1}{Z_1} = \frac{2R_2 + R_1}{R_2} \frac{j\omega(2C_1 + C_2)R_2 \frac{R_1}{2R_2 + R_1} + 1}{j\omega R_2 C_2 + 1}$$

The following cut-off frequencies are deduced :

- High cut-off frequency: $\frac{1}{2\pi R_2 C_2}$
- Low cut-off frequency: $\frac{2R_2 + R_1}{2\pi(2C_1 + C_2)R_2 R_1}$

The gain can be approximate in two cases, below the cut-off frequencies and in the BW above the cut-off frequencies:

- Low frequency AC gain: $\frac{2R_2 + R_1}{R_1}$
- AC gain in BW: $\frac{2C_1 + C_2}{C_2}$

Gain and cut-off frequency of the differential stage

In the same way as the input buffer stage, the gain of this stage can be developed:

$$\frac{Z_4}{Z_3} = \frac{j\omega C_3 R_4}{j\omega R_4 C_4 + 1}$$

From this, the gain in the BW (above the cut-off frequency) and the cut-off frequency can be deduced:

Cut-off frequency: $\frac{1}{2\pi R_2 C_2}$

AC gain in BW: $\frac{C_3}{C_4}$

Appendix C: Verification of the noise density of the MCP6241 Op Amp LTspice model

As the aim is to measure the noise, it is first good to see if the model of the amplifier used in the LTspice simulation has the same input noise voltage density than in the datasheet of the op. amp..

To compare both, the model of the MCP6241x was used in LTspice, this model was found [37]. The circuit used in LTspice to measure was a voltage follower as stated by the measurement procedure in [38].

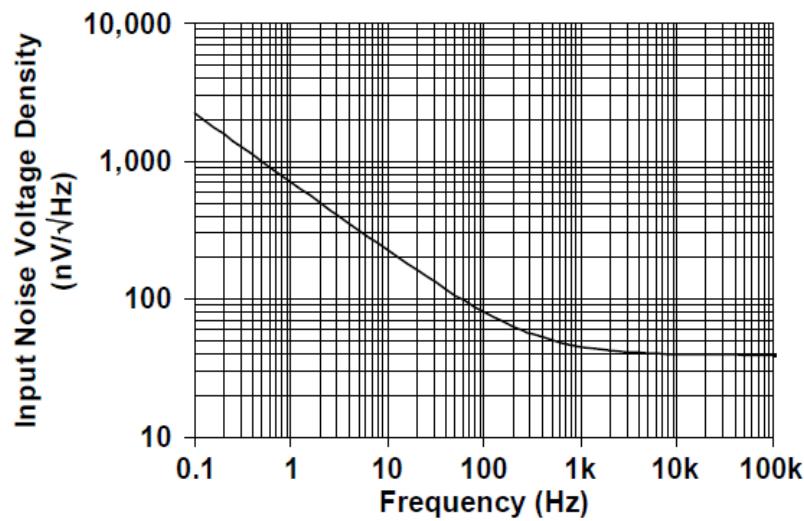


Figure 4.12: Input Voltage Noise density, in the datasheet [33]

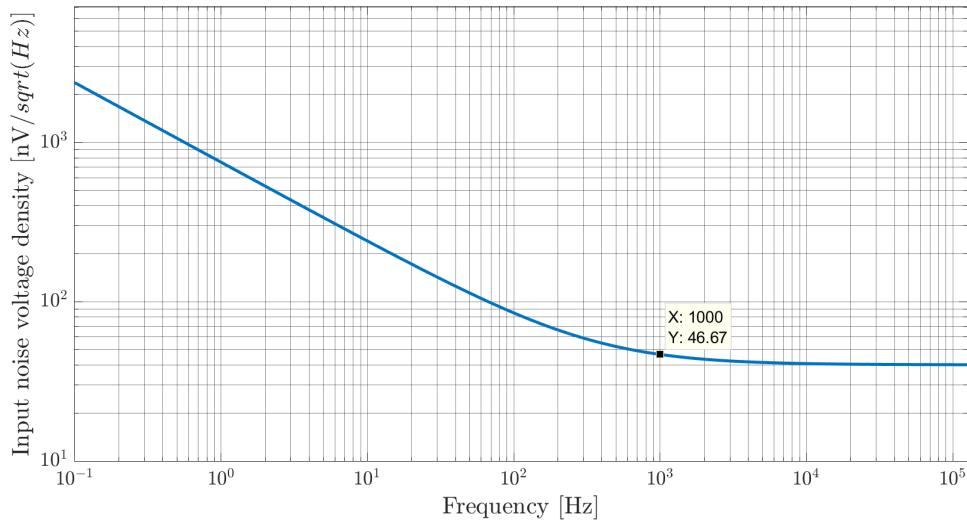


Figure 4.13: Comparison of Measured and Simulated with LTspice of the input voltage noise density of the MCP6241x

The simulated input voltage noise density is very close to the measured noise density found in the datasheet of the amplifier. The noise density of the model used in LTspice at 1 kHz is $46.67 \text{ nV}/\sqrt{\text{Hz}}$ compared to 45 in the datasheet. At 0.1 Hz, the density also seems to be the same than in the datasheet, around $2000 \text{ nV}/\sqrt{\text{Hz}}$. Then simulations can be done without expecting too much error on the total input referred noise.

Appendix D: AC-coupled analog front-end equation

Ac coupled front-end to cute the frequency of the newly used discrete IA, circuit proposed by [39].

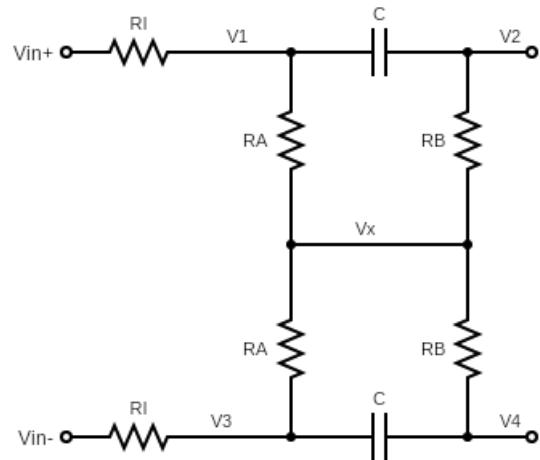


Figure 4.14: AC coupled front-end (Source [39])

$$\frac{V2 - V4}{V1 - V3} = \frac{R2}{R2 + Z_C} \text{ sum of current on node V2 and V4} \quad (4.1)$$

$$\frac{V2 - V4}{V_{in+} - V_{in-}} = \frac{R2R1}{Z_C(R1 + RI) + (R2R1 + R2RI + R1RI)} \text{ sum of current on node V1 and V3} \quad (4.2)$$

$$\frac{V2 - V4}{V_{in+} - V_{in-}} = H(\omega) = \frac{j\omega CR2R1}{1 + j\omega \frac{C(R2R1 + R2RI + R1RI)}{(R1 + RI)}} \quad (4.3)$$

$$\omega_p = \frac{(R1 + RI)}{C(R2R1 + R2RI + R1RI)} \quad (4.4)$$

$$\omega_Z = \frac{(R1 + RI)}{CR2R1} \quad (4.5)$$

Appendix E: Values of the component of the Discrete IA and AAF

Component	Values	Unit
RA	10	[MΩ]
RB	20	[MΩ]
C	1	[nF]
R1	1	[kΩ]
R2	15	[kΩ]
R3	3	[MΩ]
C3	1	[μF]
R4	7.5	[MΩ]
R5	40	[kΩ]
C5	0.1	[nF]
R6	40	[kΩ]
C6	0.1	[nF]

Table 4.4: Values of the components used in the AFE

Appendix F: Choice of the voltage and current references

The integrated IA and the Discrete IA use voltage and current reference. The Integrated IA need a voltage reference of 0.6 V and two current references of 1 μ A. The Discrete IA use a voltage reference of 0.9 V as DC component for the output signal before the sampling by the ADC in order to allow AC part to superposed on it.

Voltage References

0.9 V for Discrete IA

It was chosen to only use a voltage divider for the voltage reference of 0.9 V. The choice of resistance values must be done to avoid high power consumption and consequently 100 m Ω was chosen leading to $\frac{1.8^2[V]}{200M[\Omega]} = 16.2nW$. The use of capacitance of 200 nF in parallel with the second resistor is used to filter low frequency components.

Issue with 0.9 V reference voltage

The voltage reference being DC and the circuit used for the discrete IA using AC current because the input signals are AC, the voltage reference was not stable and deviated from the 0.9 with an AC dynamics. The DC point was no more 0.9 V. To counteract that a capacitor of 1 μ F is placed in series with the two resistors R3 on the Figure 2.7. It allows to cut the DC component. After the placing of those capacitor the reference voltage was perfectly stable.

0.6 V reference voltage

To obtain this voltage reference necessary for the integrated IA, an LDO that output 1.2 V was used (LDO used [40]). The LDO offer the advantage to have good load and line regulation compared to a simple voltage divider. From this stable voltage reference a voltage divider with two resistors of $10\text{ M}\Omega$ and a capacitor of 200 nF in parallel, is used to obtain the 0.6 V reference for the integrated IA.

Current Reference

The integrated IA needs two current references of $1\text{ }\mu\text{A}$. Attention must be taken to the turn on voltage needed (the difference between V^+ and V^- on Figure 4.15) of the current reference. The LM334DT ([41]) suits perfectly. To obtain the $1\text{ }\mu\text{A}$, a resistance of R_{set} of $68\text{k}\Omega$ is needed. The configuration of the current reference with the $68\text{ k}\Omega$ is depicted on Figure 4.15 where V_i^- is connected to the input of the Integrated IA.

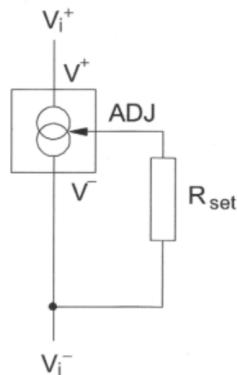


Figure 4.15: Configuration to obtain an output current of $1\mu\text{A}$ with the LM334DT (Source [41])

Appendix G: detailed power consumption of the AFE and comparison with the previous and new discrete IA

The Table 4.5 resumed the power consumption of the different sources in the AFE for the previous circuit of the discrete IA and for the proposed circuit for the discrete IA. There is only a decrease of 0.2 % of the total power consumption for the new discrete IA. This decrease is due to the absence of overshoot in the bandwidth of the new solution. As an overshoot means an higher gain more current is needed.

	Power Consumption New Solution [μW]	Power consumption Previous Solution [μW]
Integrated IA	52.9	52.9
Discrete IA Simulated with Spice	109	110.7
AAF only (Sallen-Key)	36.9	36.9
LDO	504	504
Current References	3.6	3.6
Total Power Consumption	706.4	708.1

Table 4.5: Detailed Power consumption Current Solution vs Previous Solution

Appendix H: PCB

In this section, the pictures associated with the design of the PCB can be found. Figure 4.16 is a schematic of the PCB used for the design of the PCB with the software Eagle.

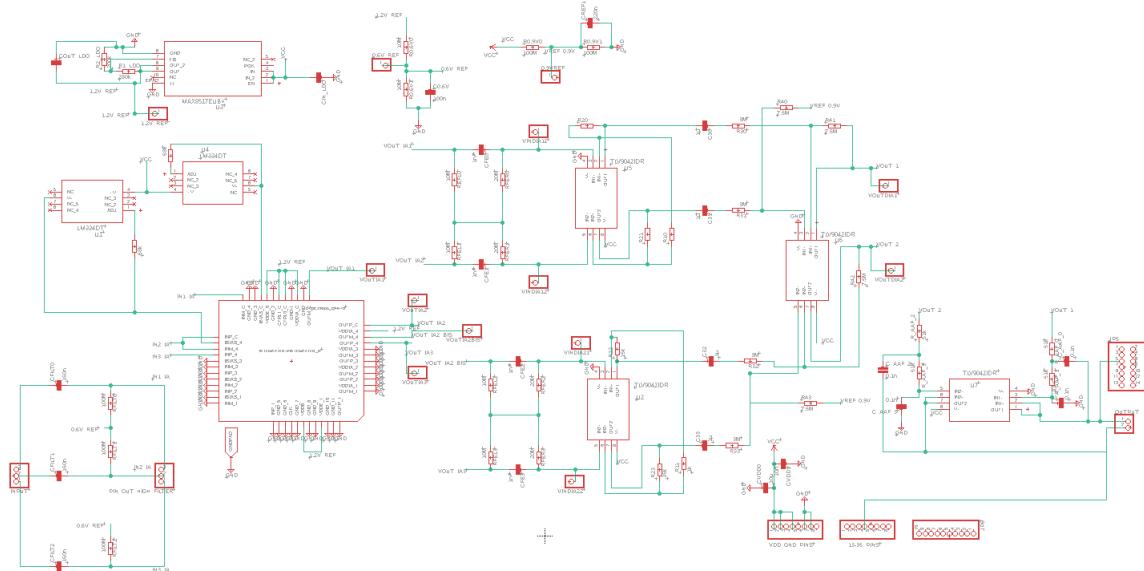


Figure 4.16: Schematic of the PCB in Eagle software

Figure 4.17 is the PCB itself as designed.

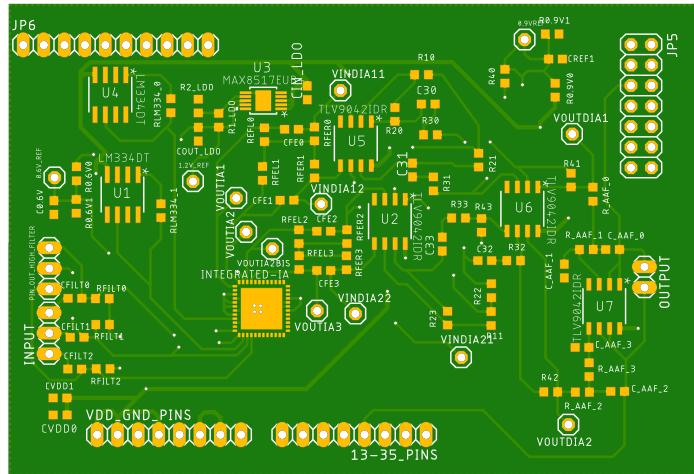


Figure 4.17: Picture of the PCB

Figure 4.18 depicts the output signal at the output of the anti aliasing filter for an input signal of 9 kHz. The sinusoidal input signal was of an amplitude of 0.007 V and has a DC component of 0.4V. The gain of the conditioning chain was chosen to be of 75 and at the output the amplitude is 0.53 V corresponding to a gain of 75.71. It shows that the output signal which will be sampled is sufficiently clean to be properly sampled by the ADC of the MCU. This simulation is done with $720\text{k}\Omega$ input resistance of the ADC but simulations with $3600\text{M}\Omega$ were also done and obtaining the same results. Also, other frequencies for the input signal were tested and leading to the same results.

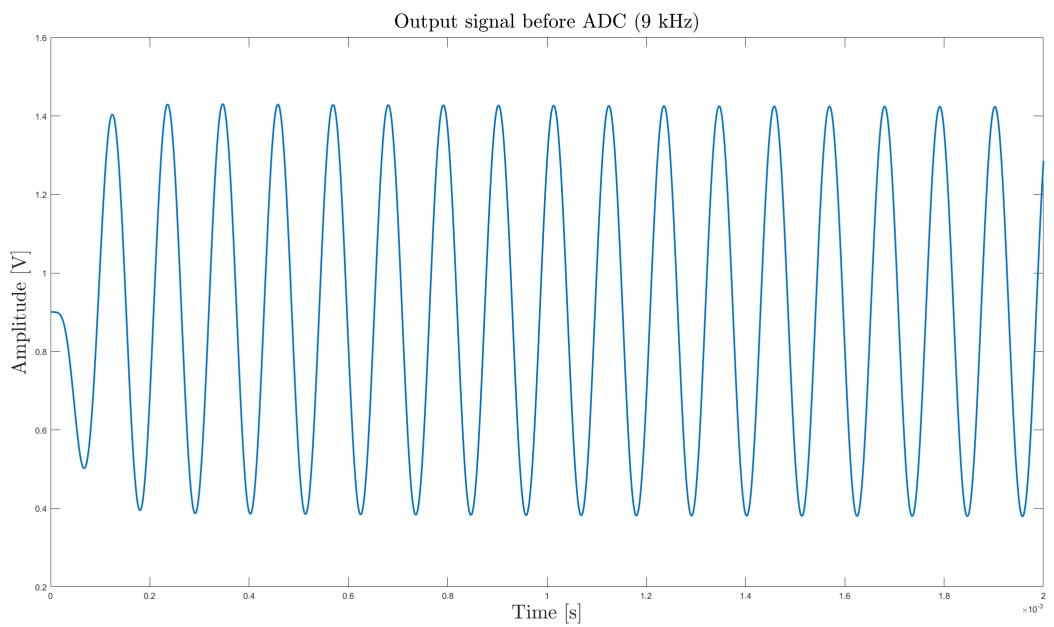


Figure 4.18: Output of the AAF for an input ENG signal of 9 kHz

Appendix I: analog adaptive tripole

Analog implementation of the adaptive tripole [14] [15]. A digital version of this adaptive tripole is implemented in this work. The gains are adapted by a feedback voltage V_{fb}

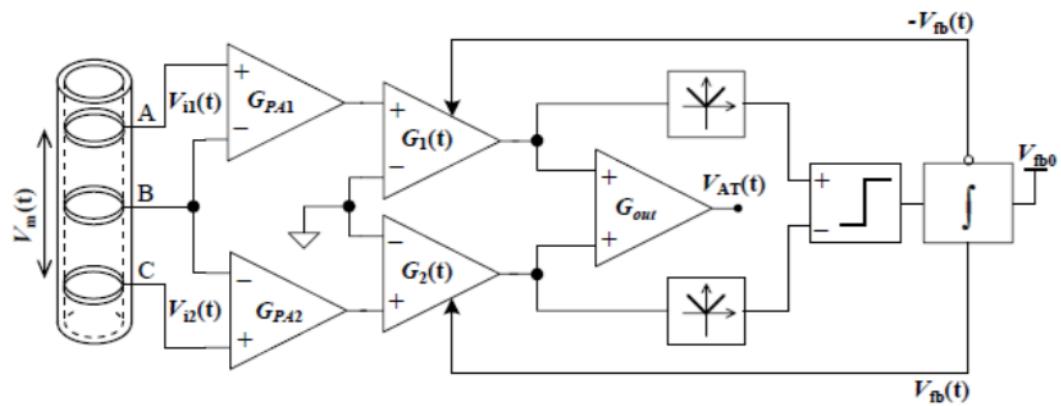


Figure 4.19: adaptive tripole [14],[15]

Appendix J: code of the adpative tripole

```

1 void adaptive_tripole( int Number){ // cuff imbalance compensation
2
3     uint32_t index = 0;
4     long X = SV_BUF_SIZE*Precision; // initialize X
5     if (DEMI == 0){
6         for( index = 0; index < ADC_SAMPLE_BUF_SIZE; index = index+2){
7             if(index%64 == 0){ //(ADC_SAMPLE_BUF_SIZE)/SV_BUF_SIZE
8                 Centered1 = abs((( SampleBuffer [index] . ui32Sample) - (mean_16)
9 )) ;
10                Centered2 = abs((( SampleBuffer [index+1]. ui32Sample) - (
11 mean_32)));
12                Diff = (Centered1 - Centered2);
13                Plus = (Centered1 + Centered2);
14                X = X + (Diff*Precision)/(Plus);
15            }
16            L1= G1*(( SampleBuffer [index] . ui32Sample)-mean_16);
17            L2 = G2*(( SampleBuffer [index+1]. ui32Sample)-mean_32);
18            L3 = (L1-L2)/Precision ;
19            L4 = L3;
20            OutputBuffer [ index /2] = L4 ;
21        }
22    } else {
23        for( index = 0; index < ADC_SAMPLE_BUF_SIZE; index = index+2){
24            if(index%64 == 0){ //(ADC_SAMPLE_BUF_SIZE)/SV_BUF_SIZE
25                Centered1 = abs((( SampleBuffer2 [index] . ui32Sample) - (
26 mean_16)));
27                Centered2 = abs((( SampleBuffer2 [index+1]. ui32Sample) - (
28 mean_32)));
29                Diff = (Centered1 - Centered2);
30                Plus = (Centered1 + Centered2);
31                X = X + (Diff*Precision)/(Plus);
32            }
33            L1= G1*(( SampleBuffer2 [index] . ui32Sample)-mean_16);

```

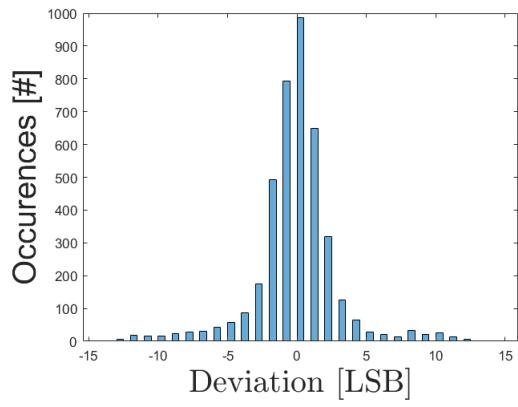
```

32     L2 = G2*(( SampleBuffer2 [ index+1].ui32Sample)-mean_32) ;
33     L3 = (L1-L2)/Precision ;
34     L4 = L3;
35     OutputBuffer [ index /2] = L4 ;
36 }
37 }
38 Sum = Sum - SVBuffer [ Storage_Vector_Index ] + X;
39 SVBuffer [ Storage_Vector_Index ] = X ;
40 Ximb = Sum/(1024); // compute cuff imbalance
41 G2 = Ximb; // update Gains
42 G1 = (2*Precision) - G2;
43
44 if (Storage_Vector_Index<(SV_BUF_SIZE-1)){ //update storage vector
45   index
46   Storage_Vector_Index = Storage_Vector_Index + 1;}
47 else{
48   Storage_Vector_Index = 0;}

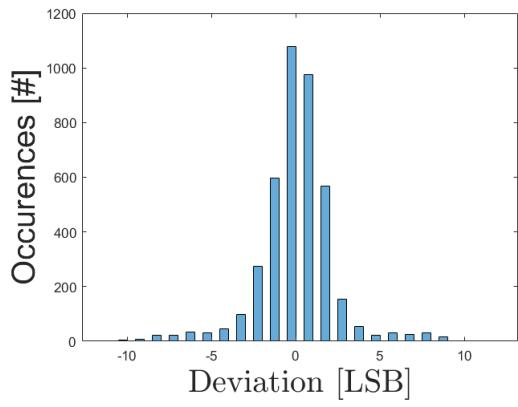
```

Appendix K: histograms of the ADC noise for 12 bits of resolution

The histograms shows that the noise takes a Gaussian distribution. From table 3.2 and the histograms, it can be seen that the two ADC's used for sampling the input signal have the same metric and that there differences are small. When sampling a DC voltage of 0.9V, the ADC 16 was a little bit more accurate giving a mean of the samples closer to 0.9V (0.892V) than the ADC32 (0.887V) but the ADC 32 seems to be less impacted by the thermal noise. It is well highlighted on the histograms. On the ADC 16 histogram, the deviation goes to -13 LSB and 12 LSB while for the ADC32, it only goes to -11 and 9 LSB. The accuracy of the ADC was computed by taking the mean of the ADC samples for 4096 samples. It gives that the ADC 16 had a mean of 2470 LSB or 0.9045 V and the ADC 32 a mean of 2476 LSB or 0.9067 V. It is not significant as it is only 0.25 % of difference. The difference of means is not a big issue as the embedded code compute the means of the two channels separately before subtracting it.



(a) ADC 16



(b) ADC32

Figure 4.20: Histograms of the deviation of the ADC noise using 12-Bits ADC for a constant signal applied of 0.9 V

Appendix L: Test with ENG signal with the PCB

Test with ENG signal with the PCB

The next step to test the functionality of the code is on ENG signal. Unlike the artefact, this one must not be rejected and must be retrieve at the output of the MCU. Recalling that the ENG signal is affected by a weighted sum as sensed by the tripolar cuff-electrodes (see Figure 1.3 in chapter 1), it means that most of the signal is only on the central electrode and it can be considered that no signal is on the other electrodes (border electrodes to ground). When being amplify by the AFE, the two outputs obtained through the two channels of the AFE have the sames dynamics in term of amplitude of the AC signal but with a phase shift of 180° between them. To simulate that with only the MCU, it would be required to generate two signals with a phase shift of 180° which was not possible with the available material. As the experiment of the ENG was already done on only the PCB and that it gives the correct output with a phase shift of 180° between the two outputs, it was decided to test the code on ENG signal by using the outputs of the PCB for an ENG input. The scheme of Figure 4.22 shows the set-up used to test the code of the MCU against an ENG input

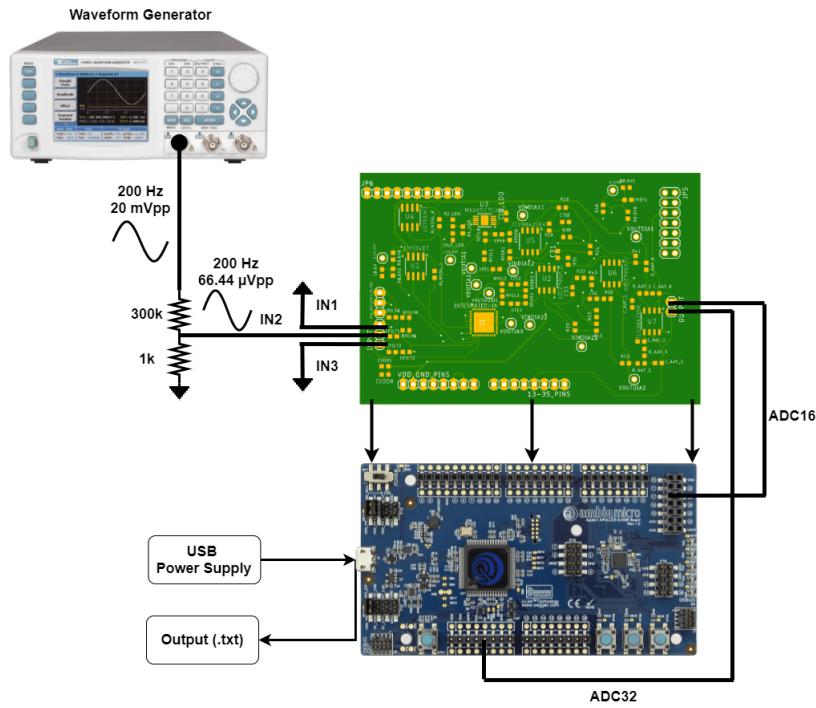


Figure 4.21: Set-up to test the functionality of the Full system on ENG signal

The signal used on pin 2 of the PCB was generated by signal from a waveform generator at 20 mVpp and at 200 Hz that is in the range of the ENG possible frequencies. The 20mVpp signal was divided by 301 k Ω giving 66,44 μ Vpp (a test on signal with the amplitude 20 μ V and 7.1 μ V_{rms} of the ENG signal as stated in the fundamental chapter will be realized in the chapter 4). These 66.44 μ Vpp were amplified by the gain of the Integrated IA and the gain of the Discrete IA leading to 320 mVpp at the input of the ADC channels. As the code in the MCU compute the output by subtracting the two inputs of the ADC affected by the proper adaptive tripole gain and recalling that those gains are equal in the case where no artefact is present and that the two inputs signals are phase shifted by 180 °, the output is then the double of the amplitude of one input signal. It leads to a signal of 640 mVpp at the output of the MCU. the Figure 4.22 shows the signal obtained at the output of the MCU and that has the correct amplitude.

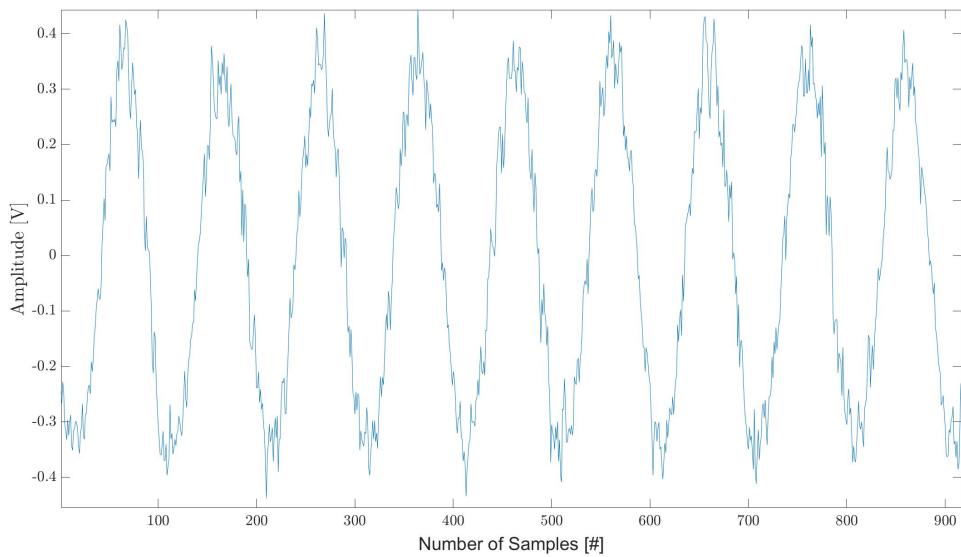


Figure 4.22: Output of the MCU for an ENG signal Input on the PCB

Test with artefact

The aim of this digital adaptive tripole is to cancel the presence of the artefact and to only output the amplified ENG signal.

To test the artefact rejection of the adaptive tripole code, the set-up of the Figure 4.23 is used. The input signals of the two ADC channels are different in term of amplitude, 800 mVpp for the ADC0 canal and 200 mVpp for the ADC1 canal, but with the same frequency of 100 Hz.

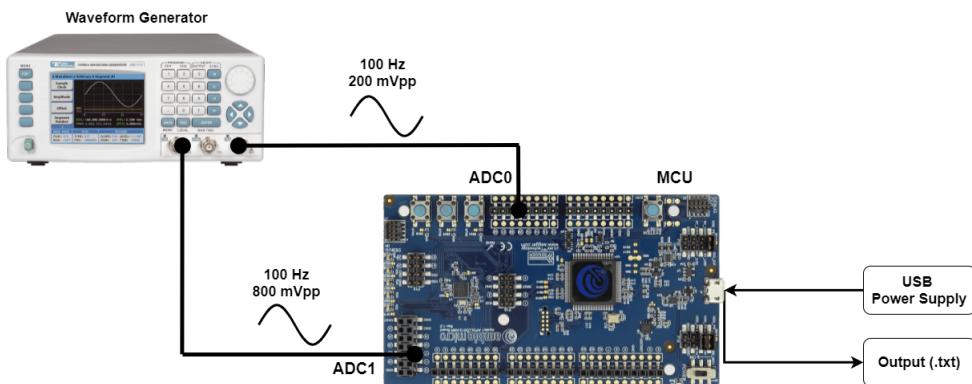


Figure 4.23: Set-up for the test of artefact rejection with implementation of adaptive tripole on Apollo3

On the Figure 4.24, the gain are not adapted (adaptive tripole off) meaning that no importance is given to the signal from the ADC0 or the ADC1, both gains are equal. The result is the apparition of a reduced artefact at the output of the MCU but it still present.

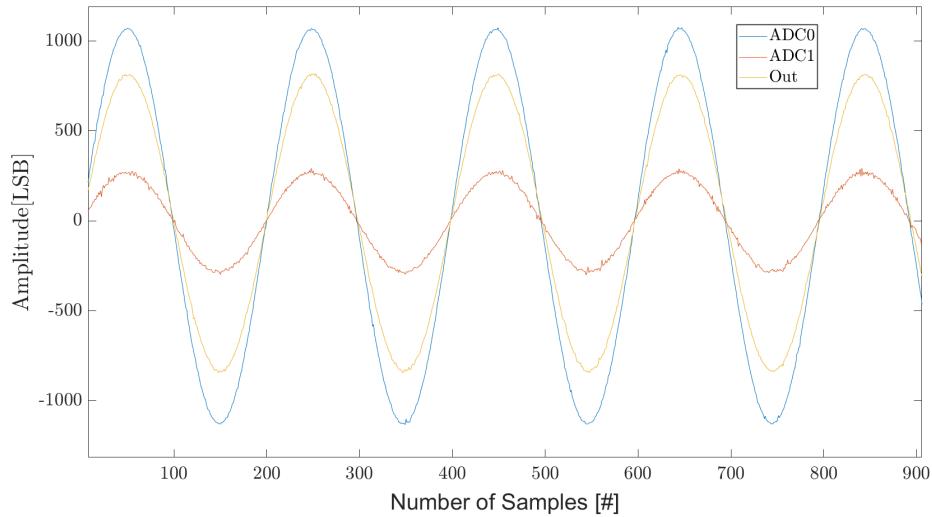


Figure 4.24: Output of the MCU for an artefact applied without adaptive gains

On Figure 4.25, this time the adaptive tripole is activated. The output is closed to 0, this means that the artefact is perfectly rejected and the gains are well adapted. The final gains are 625 for the ADC0 and 1375 for the ADC1 (due to the use of Precision factor of 1000).

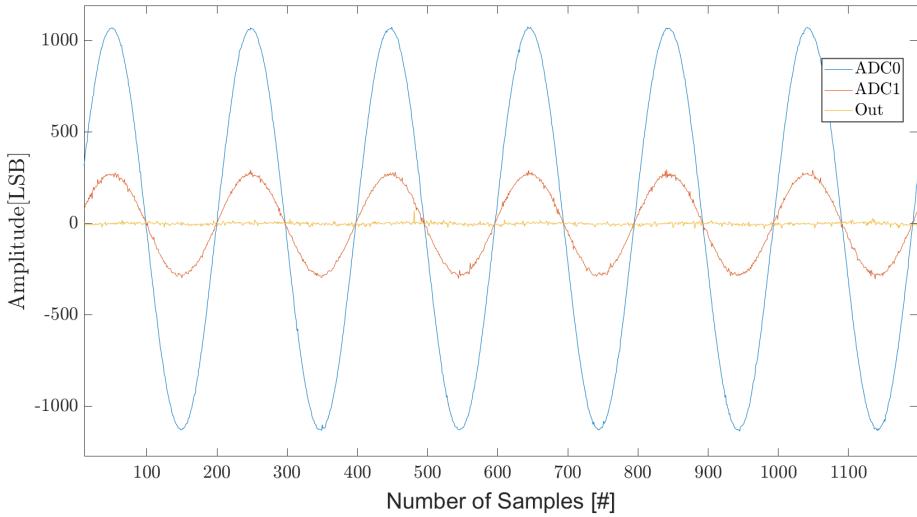


Figure 4.25: Output of the MCU with artefact applied and with adaptive gains

Figure 4.26 is a zoom on the output of the MCU for the test on the Figure 4.25. As it can be seen the output is not perfectly 0 but oscillate a little bit at the frequency of the input signals. It could be due to the adaptation of the gains as these oscillate around their perfect values due to small difference of time between the sampling of the two ADC channels . In fact, the sampling and conversion is done channel per channel in series and take 28 cycles with the resolution of 12 bits meaning $0.585 \mu\text{s}$ with a CPU clock frequency of 48 MHz. This might lead to residual noise on the samples. There is also the noise on each ADC channel due to the quantization. In case of 12 bits resolution, it is 9.61 LSB's for channel 0 or ADC with input pin 16 and 9.49 LSB's for channel 1 or ADC with input pin 32 (see Table 3.2). As these two noises are independent the total resulting noise is the square root of the sum of the squares leading to 4.69 LSB's.

The total resulting noise of this output signal on Figure 4.26 is 7.42 LSb's with already 4.69 LSB's from the dynamic of the two different canals used for the ADC.

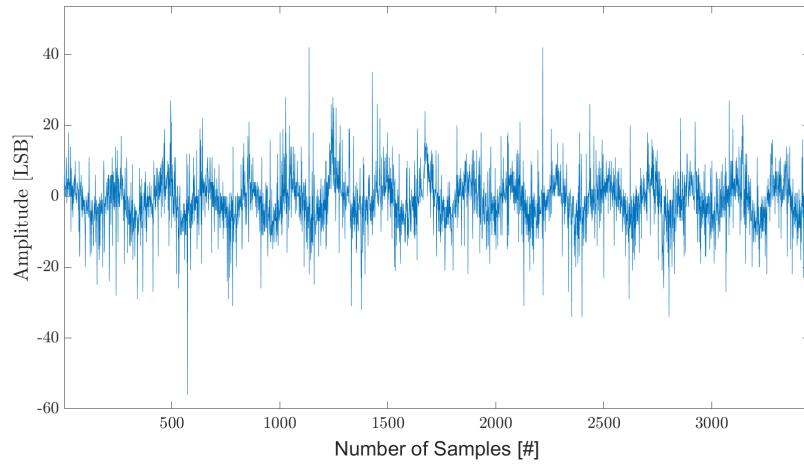


Figure 4.26: Output of the adaptive tripole for artefact at input

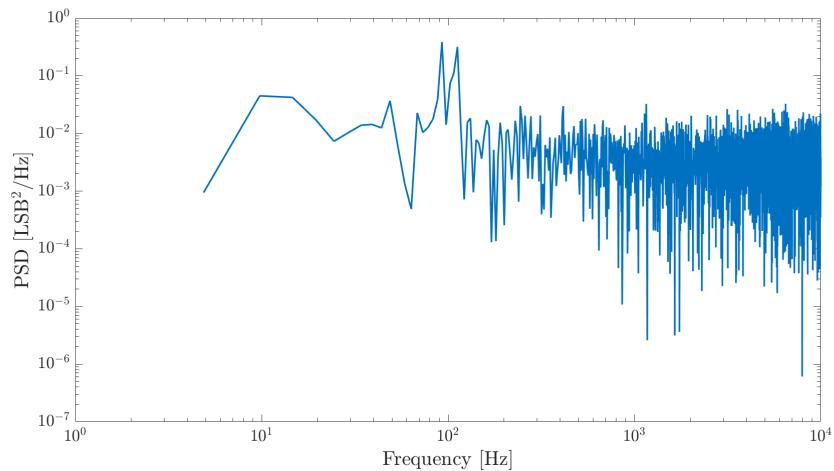


Figure 4.27: Noise of the output of the adaptive tripole for artefact at input

On the one sided psd, there seems to be a linear decrease of the psd at the beginning that could be due to flicker noise. At the end the main contribution must be thermal noise as the psd is flat.

Appendix M: SNR figures of the ENG signal

The Figures 4.28 and 4.29 depict the power of the fundamental, harmonics and noise obtained at the output of the system for an ENG signal applied at the input. It results that the SNR is higher with more bits of resolution for the ADC.

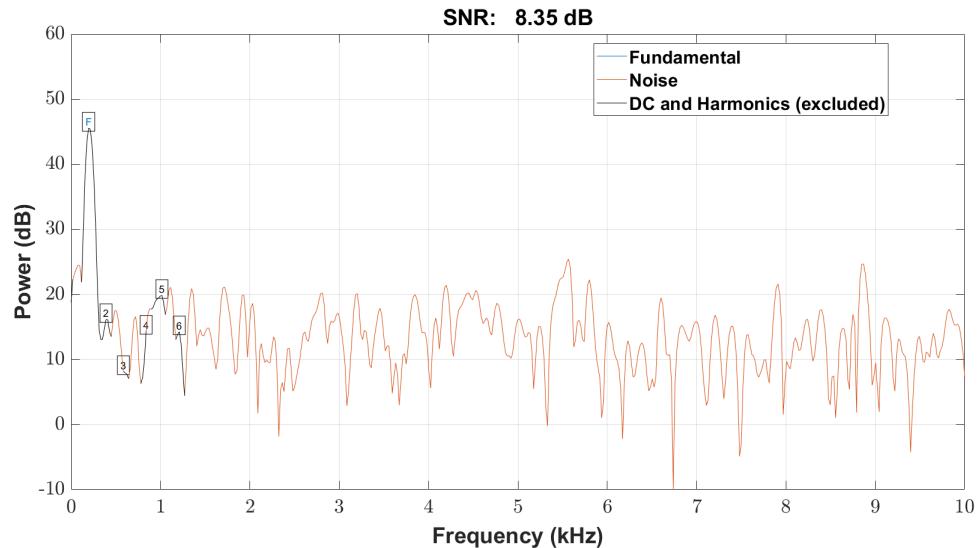


Figure 4.28: SNR figure obtained with "snr" module of Matlab of the output of the system for ENG signal applied with 12-bits of resolution for the ADC

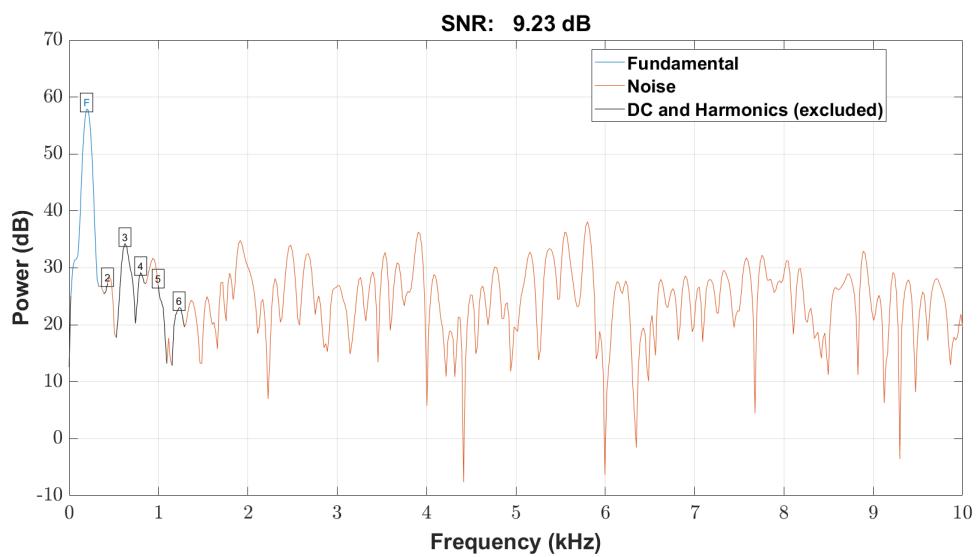


Figure 4.29: SNR figure obtained with "snr" module of Matlab of the output of the systeme for ENG signal applied with 12-bits of resolution for the ADC

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