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Bilgisayar Mimarisi

Projesi

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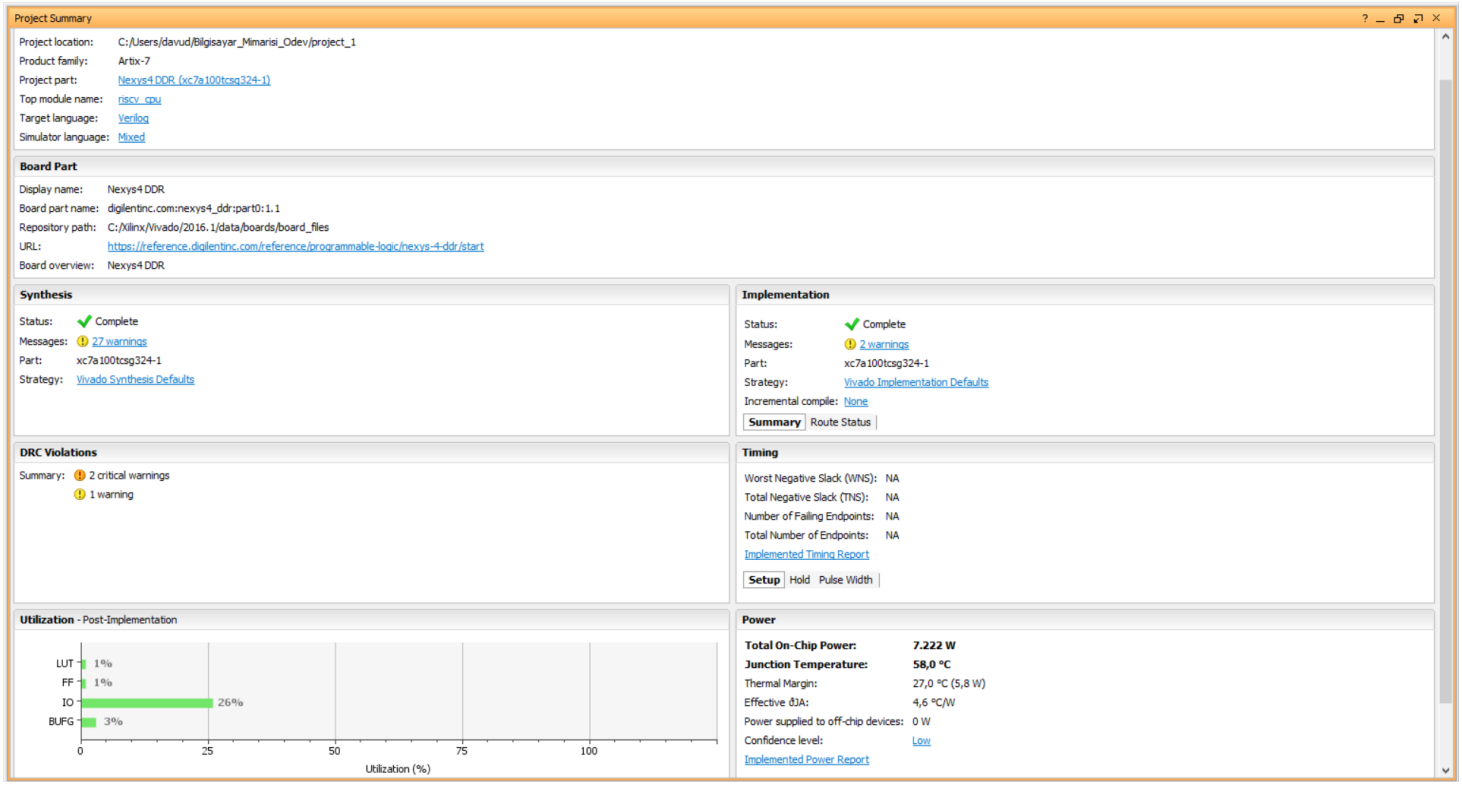
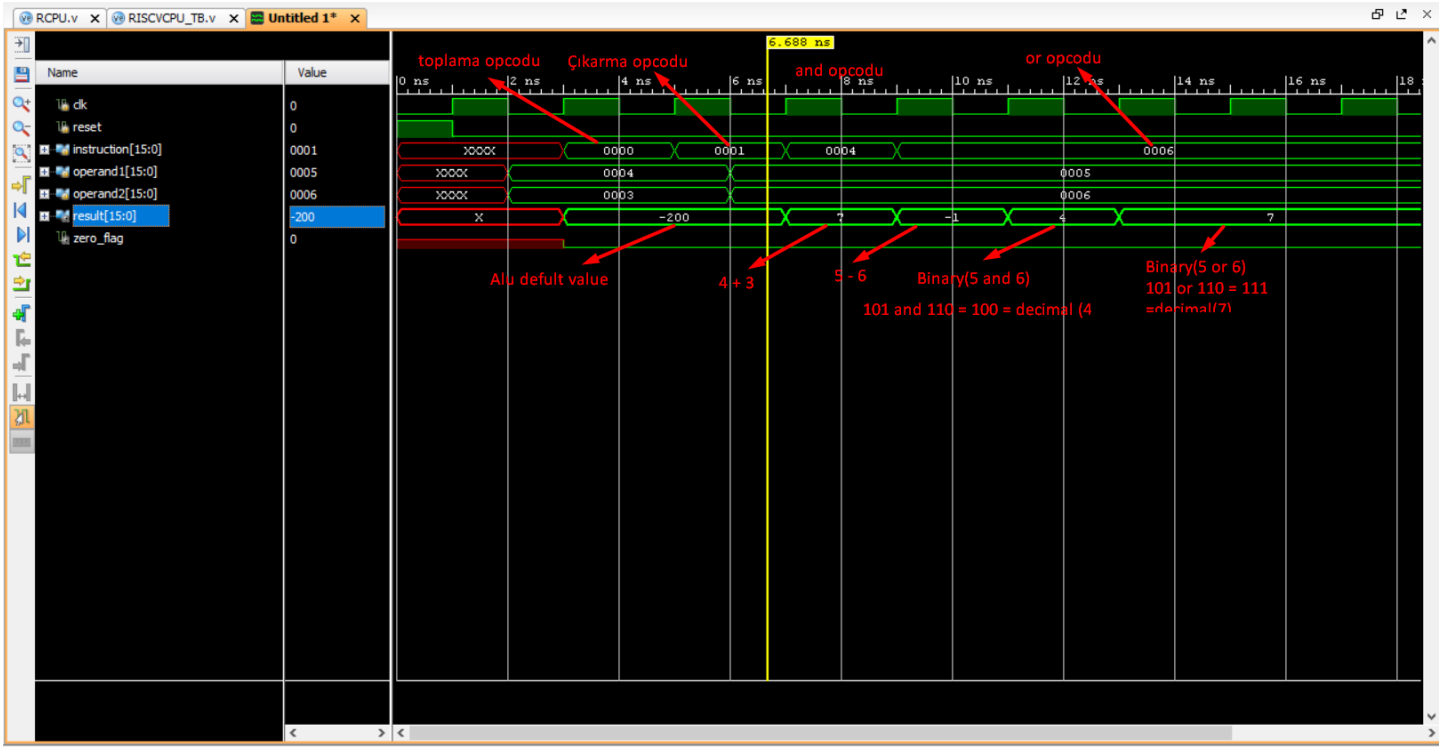
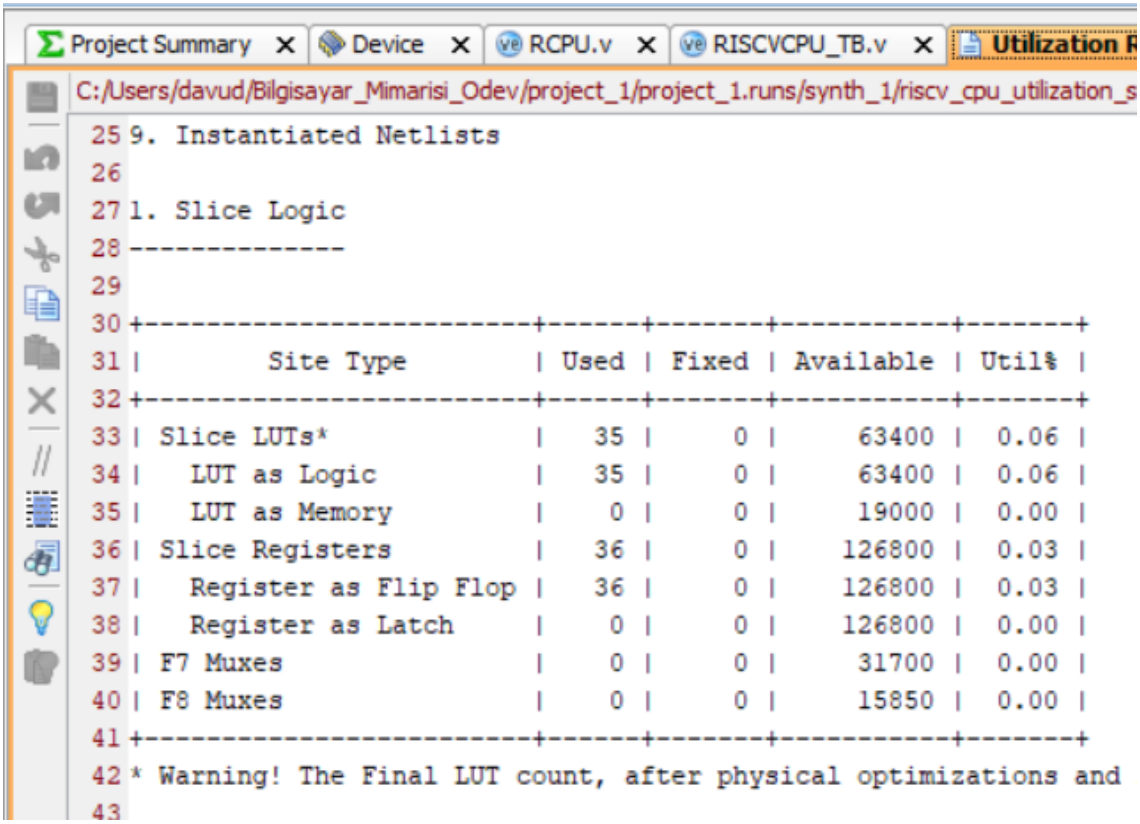
Bu projede ALU parçasını yapabildim test benchden instruction ve operandları göndererek istenilen sonuç alınmaktadır. Opcodu gelen instructionın soldan 3 biti yaptım instruction(3:0). Opcodu kullanarak programım farklı aritmetik işlemler gerçekleştirmektedir (add,sub,and,or) ve bu işlemin sonucunu alu_resulta yüklemektedir son olarak tüm işlem bittikten sonra output olarak result vermektedir. Ancak bu işlemin opcode ve operand geldikten 1 nabız sonra gerçekleşmektedir bu problemi ne yazıkki çözemedim.





Bu fotoğrafda görüldüğü üzere tasarlamış olduğum alu verilen operandlar ve instructionlara göre sonuç vermektedir ve sonuçlar bir posedge (nabız) gecikmesine rağmen doğrudur.

Utilization Design Information:



1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
36	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	135	0.00
RAMB36/FIFO*	0	0	135	0.00
RAMB18	0	0	270	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and ther

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	240	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	54	0	210	25.71
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
IBUFDS_GTE2	0	0	4	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	24	0.00
MMCME2_ADV	0	0	6	0.00
PLLE2_ADV	0	0	6	0.00
BUFMRCE	0	0	12	0.00
BUFHCE	0	0	96	0.00
BUFR	0	0	24	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
PCIE_2_1	0	0	1	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
IBUF	37	IO
FDRE	36	Flop & Latch
LUT6	19	LUT
OBUF	17	IO
LUT3	15	LUT
CARRY4	4	CarryLogic
LUT1	1	LUT
BUFG	1	Clock

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used