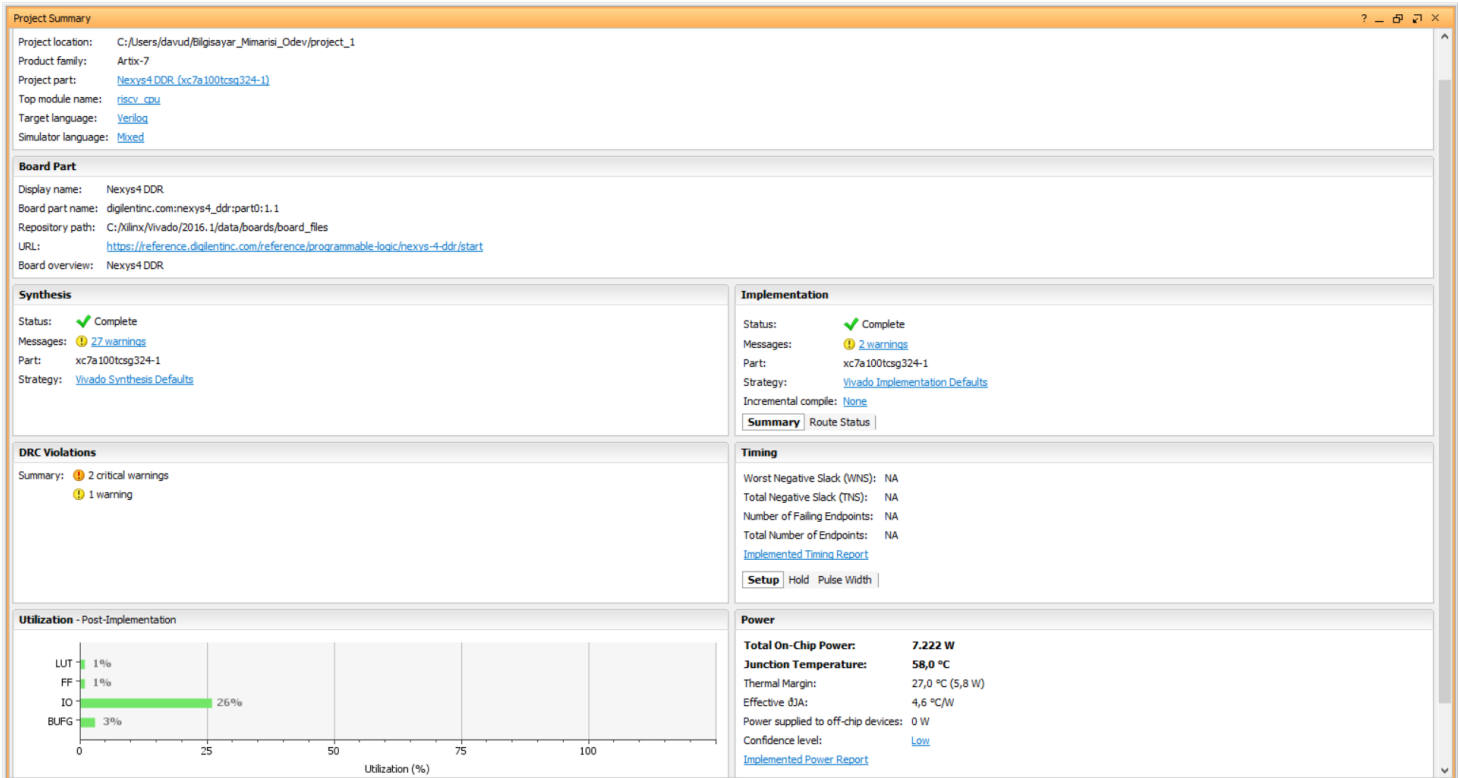


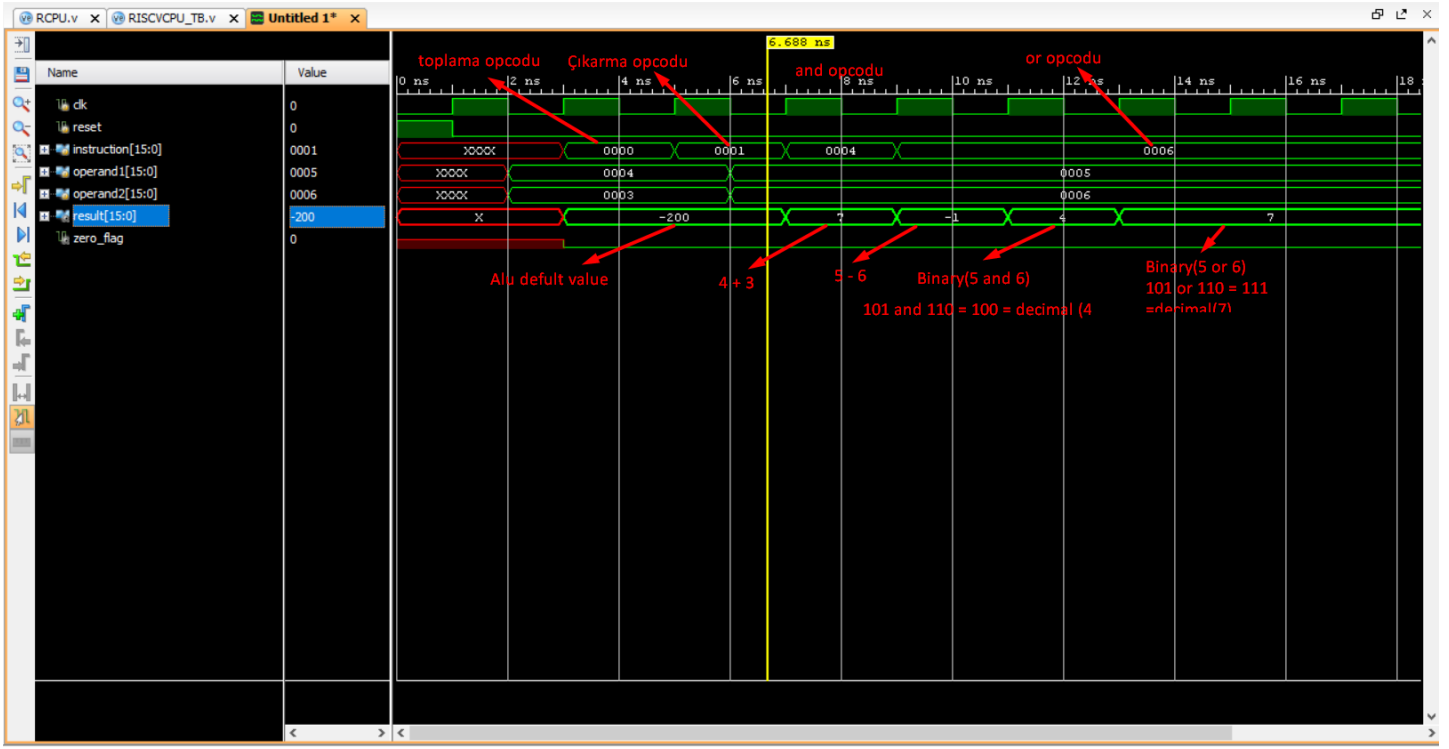
Bilgisayar Mimarisi

Projesi

Davud Kalayal 1030510042

Bu projede ALU parçasını yapabildim test benchden instruction ve operandları göndererek istenilen sonuç alınmaktadır. Opcode gelen instructionın soldan 3 biti yaptım instruction(3:0). Opcode kullanarak programım farklı aritmetik işlemler gerçekleştirmektedir (add,sub,and,or) ve bu işlemin sonucunu alu_resulta yüklemektedir son olarak tüm işlem bittikten sonra output olarak result vermektedir. Ancak bu işlemin opcode ve operand geldikten 1 nabız sonra gerçekleşmektedir bu problemi ne yazıkki çözemedim.





Bu fotoğrafta görüldüğü üzere tasarladığım alu verilen operandlar ve instructionlara göre sonuç vermektedir ve sonuçlar bir posedge (nabız) gecikmesine rağmen doğrudur.

Utilization Design Information:

Project Summary x Device x RCPV.v x RISCVCPU_TB.v x Utilization R

C:/Users/davud/Bilgisayar_Mimarisi_Odev/project_1/project_1.runs/synth_1/riscv_cpu_utilization_s

25 9. Instantiated Netlists

26

27 1. Slice Logic

28 -----

29

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	35	0	63400	0.06
LUT as Logic	35	0	63400	0.06
LUT as Memory	0	0	19000	0.00
Slice Registers	36	0	126800	0.03
Register as Flip Flop	36	0	126800	0.03
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

41 +-----+

42 * Warning! The Final LUT count, after physical optimizations and

43

44

45 1.1 Summary of Registers by Type

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47

48	+-----+-----+-----+-----+				
49	Total	Clock Enable	Synchronous	Asynchronous	
50	+-----+-----+-----+-----+				
51	0	-	-	-	
52	0	-	-	Set	
53	0	-	-	Reset	
54	0	-	Set	-	
55	0	-	Reset	-	
56	0	Yes	-	-	
57	0	Yes	-	Set	
58	0	Yes	-	Reset	
59	0	Yes	Set	-	
60	36	Yes	Reset	-	
61	+-----+-----+-----+-----+				

62

63

63

64 2. Memory

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66

67	+-----+-----+-----+-----+-----+					
68	Site Type	Used	Fixed	Available	Util%	
69	+-----+-----+-----+-----+-----+					
70	Block RAM Tile	0	0	135	0.00	
71	RAMB36/FIFO*	0	0	135	0.00	
72	RAMB18	0	0	270	0.00	
73	+-----+-----+-----+-----+-----+					

74 * Note: Each Block RAM Tile only has one FIFO logic available and the

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76

77 3. DSP

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79

80	+-----+-----+-----+-----+				
81	Site Type	Used	Fixed	Available	Util%
82	+-----+-----+-----+-----+				
83	DSPs	0	0	240	0.00
84	+-----+-----+-----+-----+				

85

87 4. IO and GT Specific

88 -----

89

90	+-----+-----+-----+-----+					
91	Site Type	Used	Fixed	Available	Util%	
92	+-----+-----+-----+-----+					
93	Bonded IOB	54	0	210	25.71	
94	Bonded IPADs	0	0	2	0.00	
95	PHY_CONTROL	0	0	6	0.00	
96	PHASER_REF	0	0	6	0.00	
97	OUT_FIFO	0	0	24	0.00	
98	IN_FIFO	0	0	24	0.00	
99	IDELAYCTRL	0	0	6	0.00	
100	IBUFDS	0	0	202	0.00	
101	PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00	
102	PHASER_IN/PHASER_IN_PHY	0	0	24	0.00	
103	IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00	
104	IBUFDS_GTE2	0	0	4	0.00	
105	ILOGIC	0	0	210	0.00	
106	OLOGIC	0	0	210	0.00	
107	+-----+-----+-----+-----+					

108

110 5. Clocking

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113	+-----+-----+-----+-----+					
114	Site Type	Used	Fixed	Available	Util%	
115	+-----+-----+-----+-----+					
116	BUFGCTRL	1	0	32	3.13	
117	BUFIO	0	0	24	0.00	
118	MMCME2_ADV	0	0	6	0.00	
119	PLLE2_ADV	0	0	6	0.00	
120	BUFMRCE	0	0	12	0.00	
121	BUFHCE	0	0	96	0.00	
122	BUFR	0	0	24	0.00	
123	+-----+-----+-----+-----+					

124

125

126 6. Specific Feature

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129	+-----+-----+-----+-----+					
130	Site Type	Used	Fixed	Available	Util%	
131	+-----+-----+-----+-----+					
132	BSCANE2	0	0	4	0.00	
133	CAPTUREE2	0	0	1	0.00	
134	DNA_PORT	0	0	1	0.00	
135	EFUSE_USR	0	0	1	0.00	
136	FRAME_ECCE2	0	0	1	0.00	
137	ICAPE2	0	0	2	0.00	
138	PCIE_2_1	0	0	1	0.00	
139	STARTUPE2	0	0	1	0.00	
140	XADC	0	0	1	0.00	
141	+-----+-----+-----+-----+					

142

144 7. Primitives

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147	+-----+-----+-----+		
148	Ref Name	Used	Functional Category
149	+-----+-----+-----+		
150	IBUF	37	IO
151	FDRE	36	Flop & Latch
152	LUT6	19	LUT
153	OBUF	17	IO
154	LUT3	15	LUT
155	CARRY4	4	CarryLogic
156	LUT1	1	LUT
157	BUFG	1	Clock
158	+-----+-----+-----+		

159

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161 8. Black Boxes

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164	+-----+-----+	
165	Ref Name	Used
166	+-----+-----+	

167

168

169 9. Instantiated Netlists

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171

172	+-----+-----+	
173	Ref Name	Used
174	+-----+-----+	

175