Class: cos 10004
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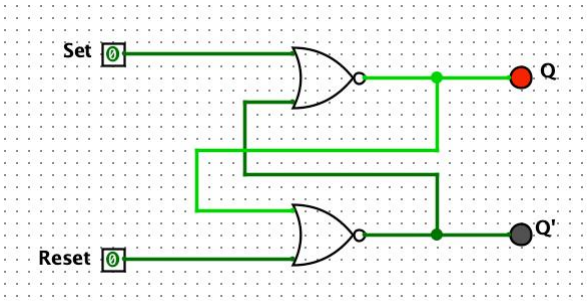
1->5



Set	Reset	Q	Q’
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0

7/ When we take Set as 1it will take the Q as 0 and the Reset at the same time is 0 then results in Q’ as 1(which means that it simply reset the other).
8/ When both of Set and Reset are 1, the situation will not defined by circuit.
The reason for that is the output of Q and Q’ keep changing between 0 and 1, racing fast. So it affects the digital circuit design.

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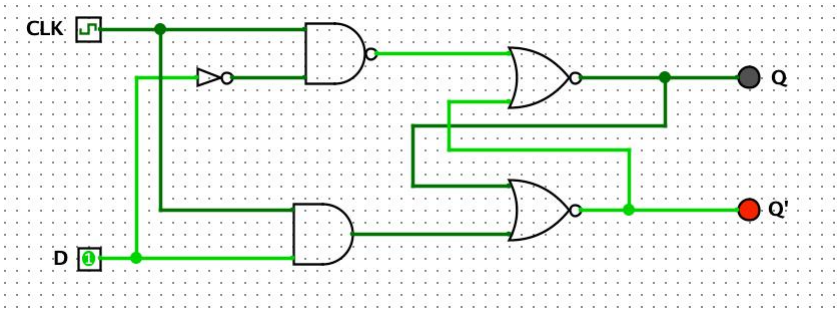

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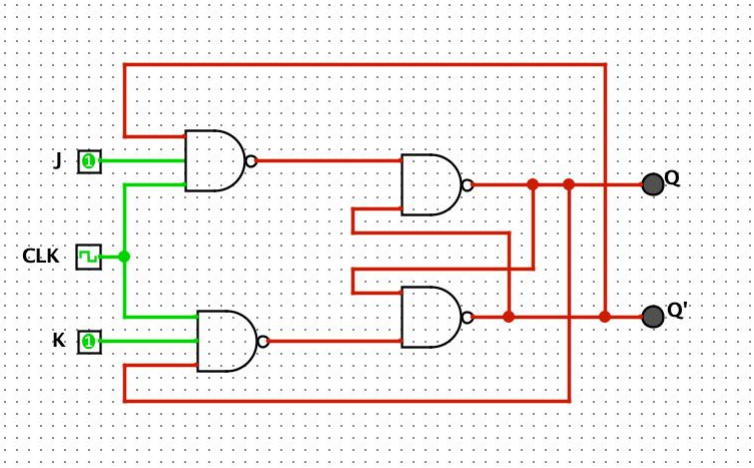
Clock	Data	Q	Q’
0	0	0	1
0	1	0	1
1	1	0	0
1	0	0	1

11/ D flip flops are commonly used in shift register, computer registers. This flip flop only contain a single input. When the clock presented in the circuit becomes active Q is changed or updated to be the same as D. The R and S input is generated by the external DATA input.
12/ Clock control the state of the signal given to the circuit. When the signal emitted by the clock is high, the input get active but when the signal emitted by the clock gets low, the output state of the circuit will not be affected because the signal given to the input is low.
13/ Because D flip flop keeps the data is synchronized, also makes non-standard counters and serial to parallel conversions can be done without extra pins.

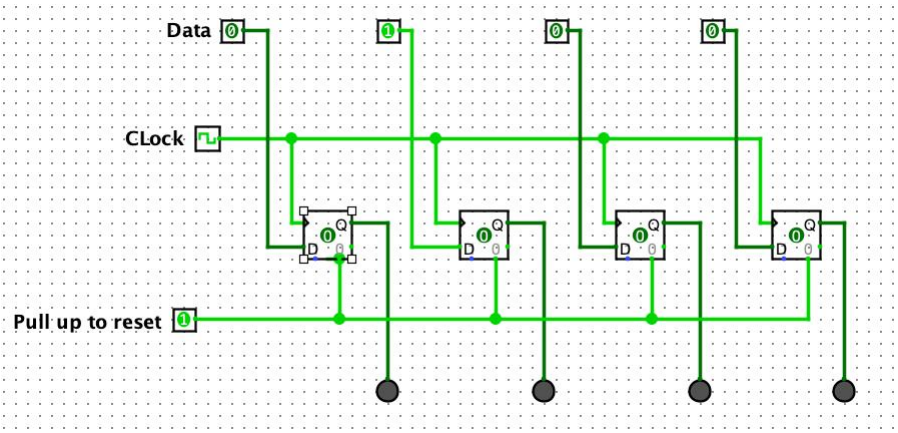
14,15/ JK flip flop



J	K	Q (When clocked)	Q' (when clocked)
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0

16/ Disconnect the wire of NAND gate and the out put Q and Q'
17/ Replace the input K with the connection of J and the second NAND gate

18-21/



22/

Ox	Input Binary	Output Binary
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
A	1010	1010
B	1011	1011
C	1100	1100
D	1101	1101
E	1110	1110
F	1111	1111