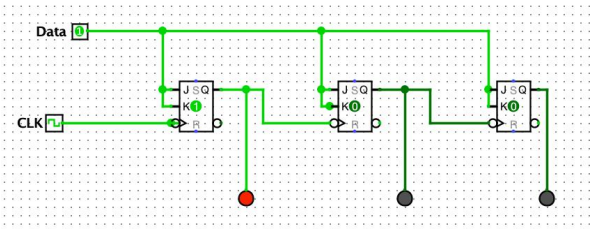
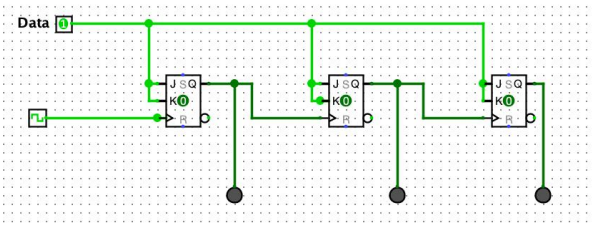
Student's ID: 104209393
Name: Ai Vi Tran

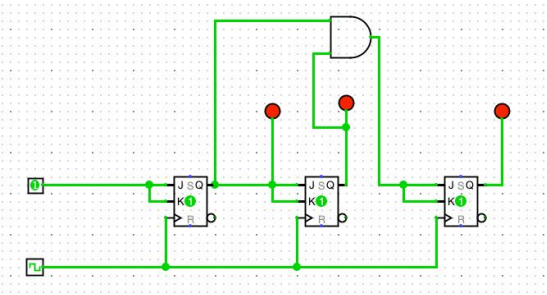


#The trigger: Falling edge = increment (Count up)



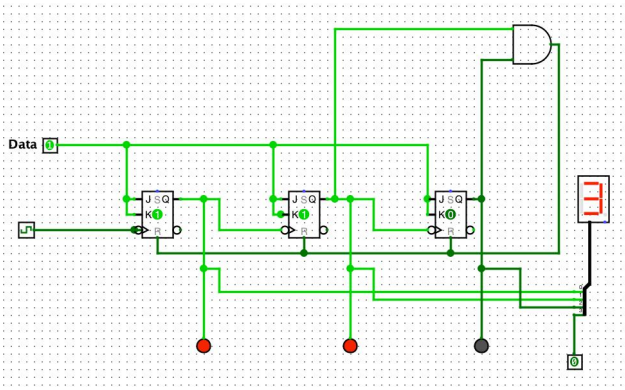
#Trigger: Rising edge = decrement (Count down)

7/



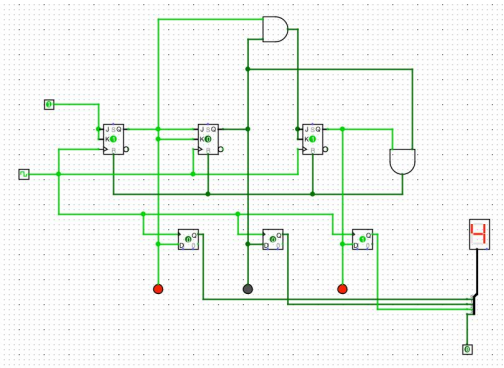
#Synchronous(the common clock) counter
Use D flip flop to create a buffer zone (complicated but more stable and predictable counter)

9/



#illegal state because of the AND gate
MOD 6 clock(return 0 when the value is 6)

10/



10.2/ If we take the value of the first outputs and remain them in the second JK flip flops, all of them will not be changed in state to the next clock pulse(keep stabilized and required a little moment of time to occur what state it should be.