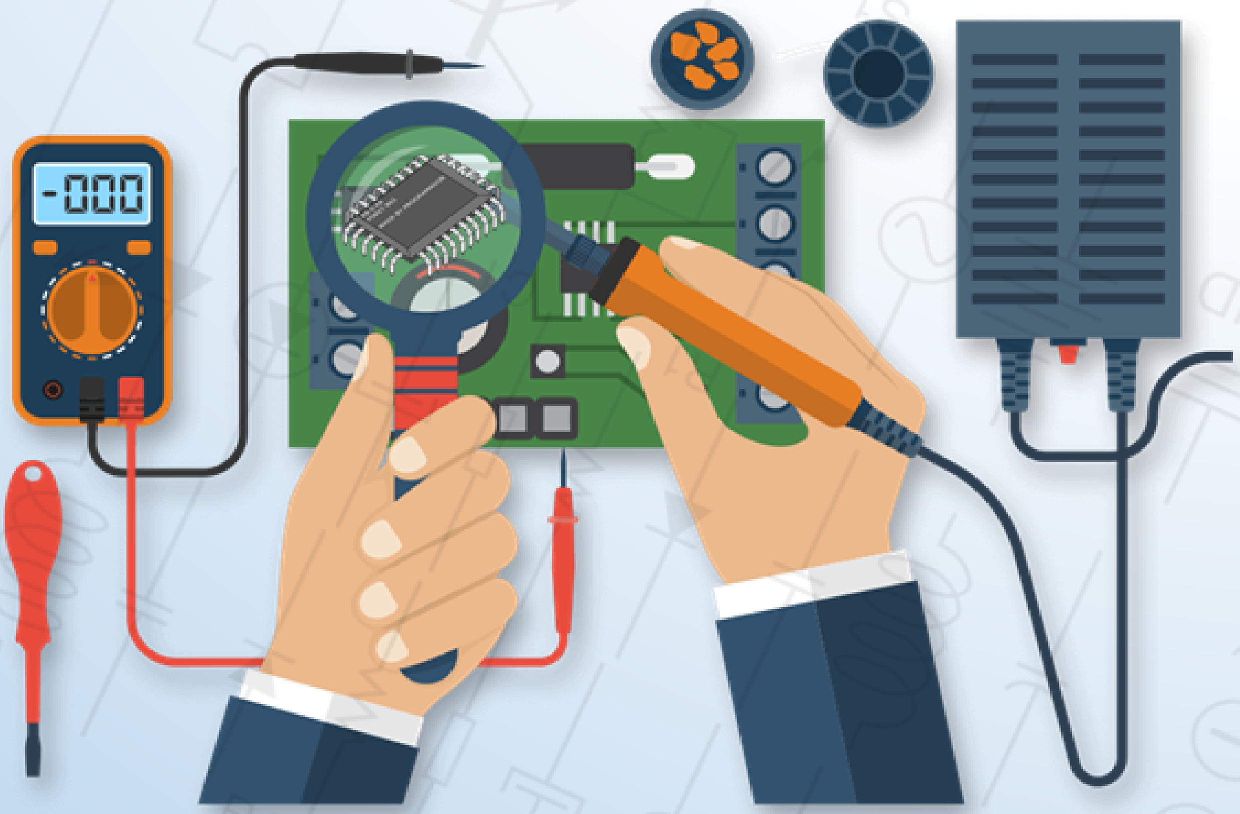
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
COMPUTER ENGINEERING

Electronic Device Component



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Contents

CHAPTER 1

Bipolar Junction Transistor

1 Introduction

In the diode tutorials we saw that simple diodes are made up from two pieces of semiconductor material to form a simple pn-junction and we also learnt about their properties and characteristics.

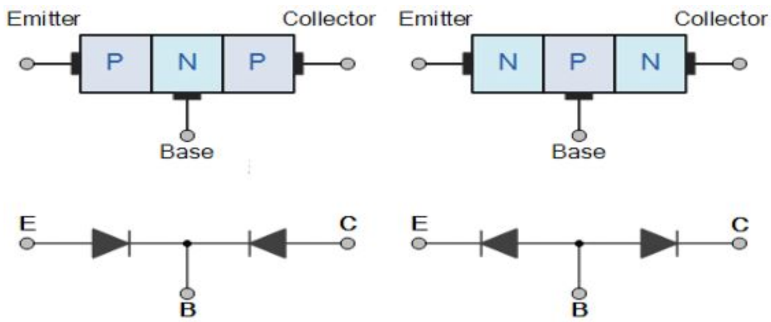

Figure 1.1: Bipolar transistor construction

If two individual signal diodes are joined together back-to-back, this will form a two PN-junctions connected together in series which would share a common Positive, (P) or Negative, (N) terminal. The fusion of these two diodes produces a three layer, two junction, three terminal device forming the basis of a Bipolar Junction Transistor (BJT), which is shown in the figure above.

Considering the symbol of the transistor in the schematic, the direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

The transistor is ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- Active region: The transistor operates as an amplifier and $I_C = \beta I_B$
- Saturation: The transistor is "Fully-ON" operating as a switch and $I_C = I_{Sat}$
- Cut-off: The transistor is "Fully-OFF" operating as a switch and $I_C = 0$

2 BJT simulation circuit

Implement the following circuit in PSPICE. The new component used is **QBreakN NPN**, which can be found in the Favorites list. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$

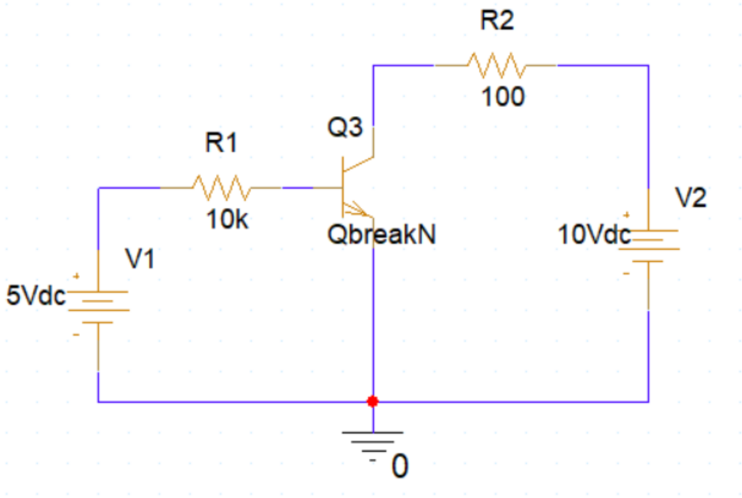

Figure 1.2: Simple connection with transistor

For a bias point simulation profile, the following results are expected:

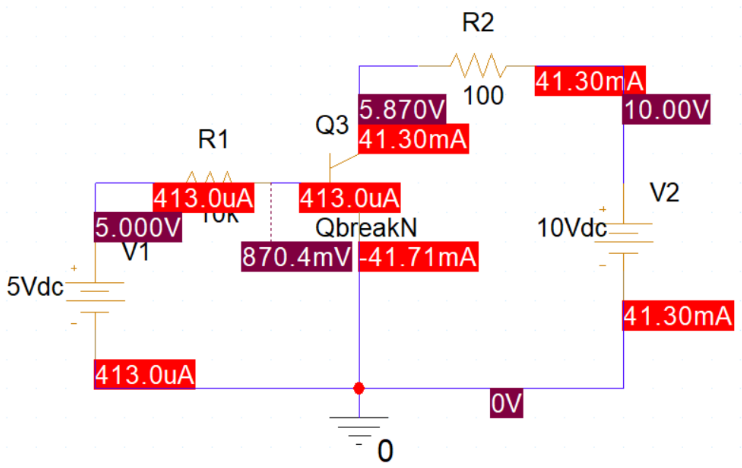

Figure 1.3: Bias profile simulation results

It is assumed that $V_{BE} = 0.7V$, the simulation results in PSPice are explained as follows:

- According to the Ohm Low, $I_B = (V_{BB} - V_{BE})/R1$ = (5V - 0.7V)/10k = 0.43mA
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta * I_B$ = 43mA
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C * R2$ = 10V - 43mA * 100Ohm = 5.7V

Since $V_{CE} > V_{CE(Sat)}$, the transistor is working in the linear mode, to confirm our assumption. Moreover, the theory calculation is very close to the PSpice simulations.

3 Exercise and Report

3.1 BJT in Saturation Mode

Change the value of **R1 to 1k** and run the simulation again. Capture the simulation results and explain the values of I_B, I_C, V_{CE}. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$ and $V_{BE} = 0.7V$.

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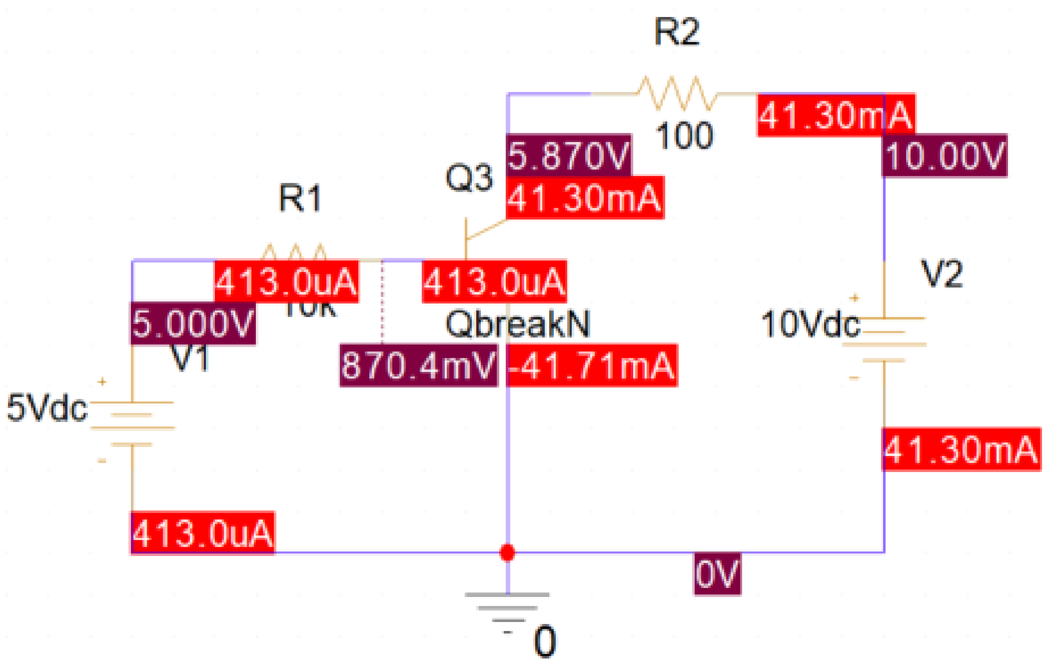

The results in PSpice are explained as follows:

According to the Ohm Law:

$I_B = \dfrac{V_1 - V_{BE}}{R_1} = \dfrac{5V - 0.7V}{1k} = 4.3$ (mA)

Let the transistor be in linear (or active) mode: $I_C = \beta.I_B = 0.43$ (A)

Testing: $V_{CE} = V_2 - I_C.R_2 = 10V - 0.43.100 = -33$ (V)

Because $V_{CE} < 0$, the transitor is saturated. We have now:

$I_C = \dfrac{V_2 - V_{CE(Sat)}}{R_2} = \dfrac{10 - 0.65}{100} = 93.5$ (A)

3.2 DC Sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC-Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:

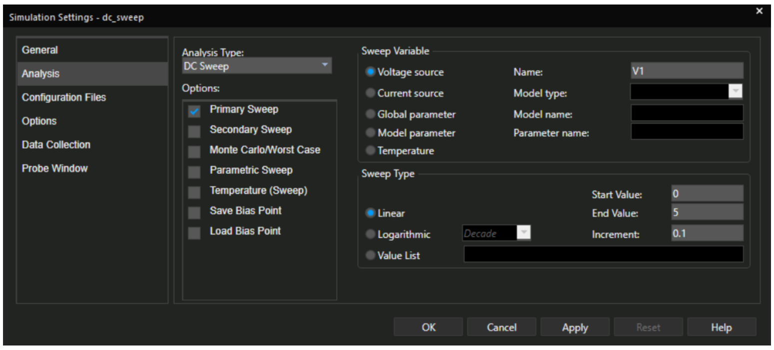

Figure 1.4: DC-Sweep profile for simulation

Run the simulation and trace for the current I_C according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.

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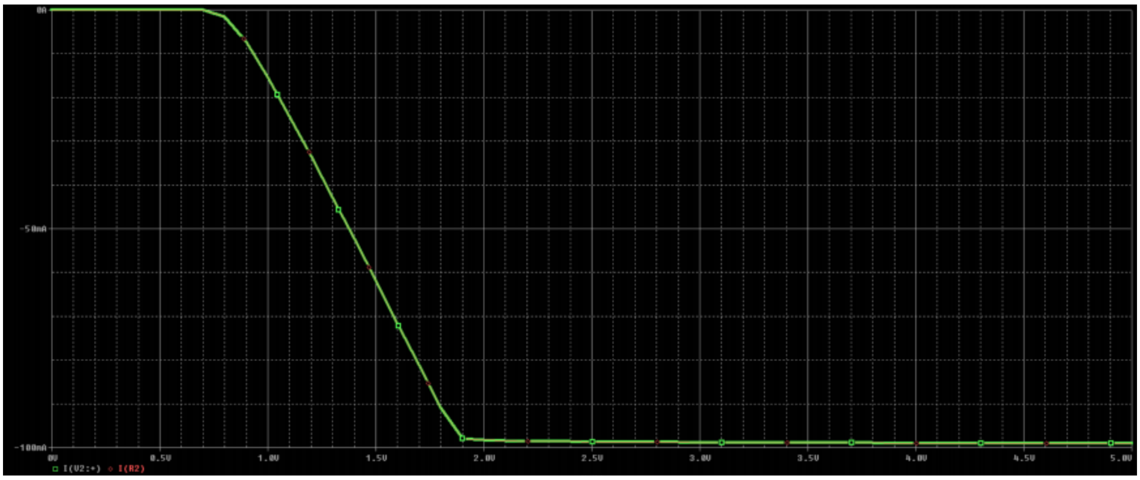

When the transistor becomes saturation, the value of V1 is 1.9 V.

Meanwhile: $I_B = \dfrac{I_C}{\beta} = \dfrac{97.889}{100} = 0.98$ (mA)

$I_{C(saturated)}$ is 97.89 (mA)

3.3 BJT used as a Switch

For a given BJT circuit, determine R1 and R2 to have IC saturated at 50mA. In this saturation mode, $V_{CE(Sat)}$ is 30mV. Assume that $V_{BE} = 0.7$V and the current gain $\beta = 100$.

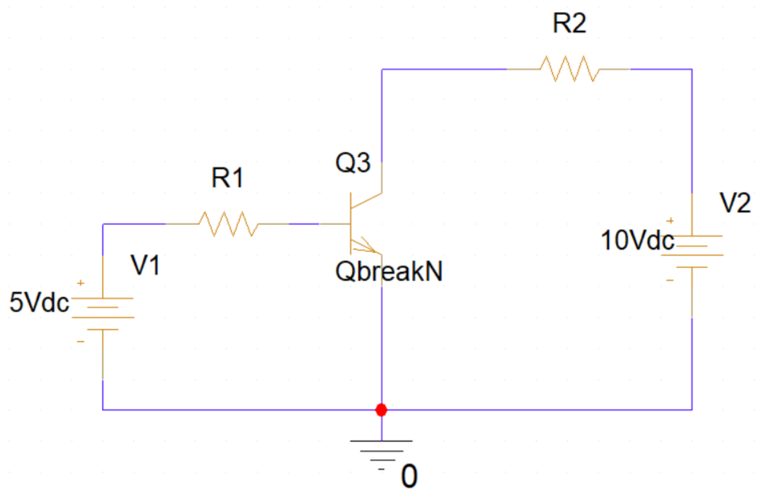

Figure 1.5: BJT used as switch in saturation mode

Present your solution to determine R1 and R2. Perform the simulation in PSpice to confirm the results. Capture the screen in PSpice and present in the report.

I_C saturated at 50 mA $\Rightarrow I_C = 50$ (mA)

$I_C \leq \beta . I_B \Rightarrow I_B \geq 0.5$ (mA)

$$I_B = \frac{V_1 - 0.7}{R_1} = \frac{5 - 0.7}{R_1} \geq 0.5 \Rightarrow R_1 \leq 8.6k \text{ (Ohm)}$$
$$I_C = \frac{V_2 - V_{CE}}{R_2} = \frac{10 - 0.03}{R_2} = 50 \Rightarrow R_2 \geq 199.4 \text{ (Ohm)}$$

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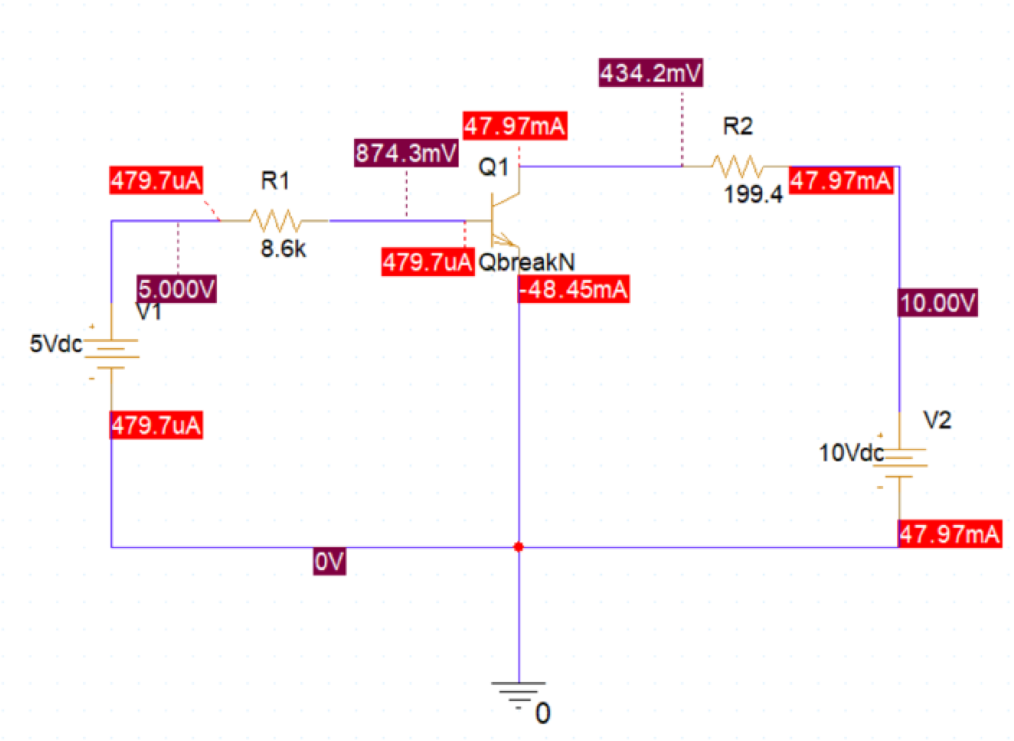

3.4 Drive a device with an NPN BJT

This exercise has a $5V$ logic output (the V_{ter} in Figure 1.6) that can source up to $10mA$ of current without a severe voltage drop and stand a maximum current of $20mA$. If the logic terminal sources a current larger than $20mA$, it would be damaged. Or, if it sources a current larger than $10mA$, the V_{ter} voltage will drop to less than $4V$. We should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of 5 ohms (the LOAD in Figure 1.6) and requires a current of at least $300mA$ and not exceeding $500mA$ to function normally. Given that we have an NPN transistor with the current gain β equals 100, the maximum I_C current is $400mA$, and the barrier potential at the BE junction is $V_{BE} = 0.7V$, select a resistor available in the market to replace the resistor R_B revealed in Figure 1.6. to make the circuit function well. After that, perform a simulation to double-check your selection.

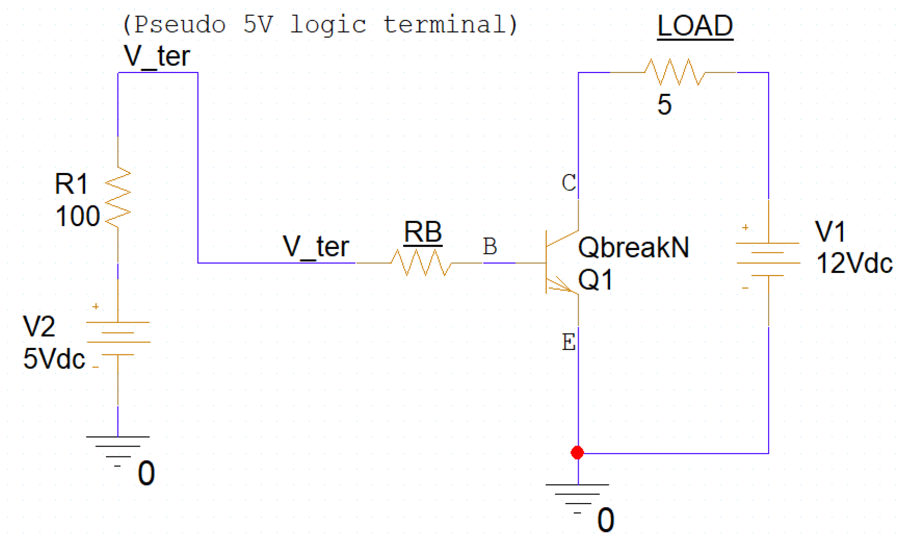

Figure 1.6: Select a resistor available in the market for R_B

3.4.1 Theory calculations

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the limits of loads and the transistor:
300 mA < I_C < 400 mA
3 mA < I_B < 4 mA

When $I_B(min) = 3$ mA:
$$R_B(max) = \frac{V_{ter} - 0.7}{I_B} - R_1 = \frac{5-0.7}{3.10^{-3}} - 100 = 1333.33 \text{ (Ohm)}$$
When $I_B(max) = 4$ mA:
$$R_B(min) = \frac{V_{ter} - 0.7}{I_B} - R_1 = \frac{5-0.7}{4 \cdot 10^{-3}} - 100 = 975 \text{ (Ohm)}$$

Therefore: 975 (Ohm) < R_B < 1333.33 (Ohm)
R_B(selected) = 1000 (Ohm)

3.4.2 Simulation

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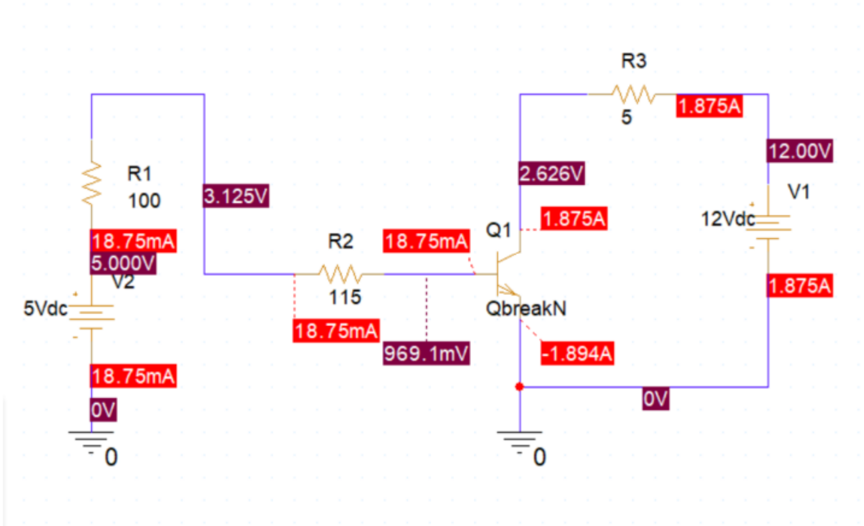
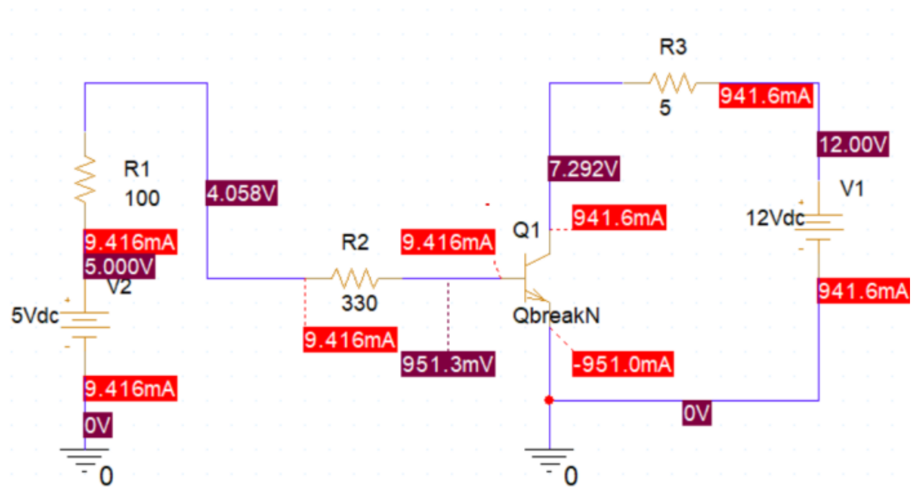
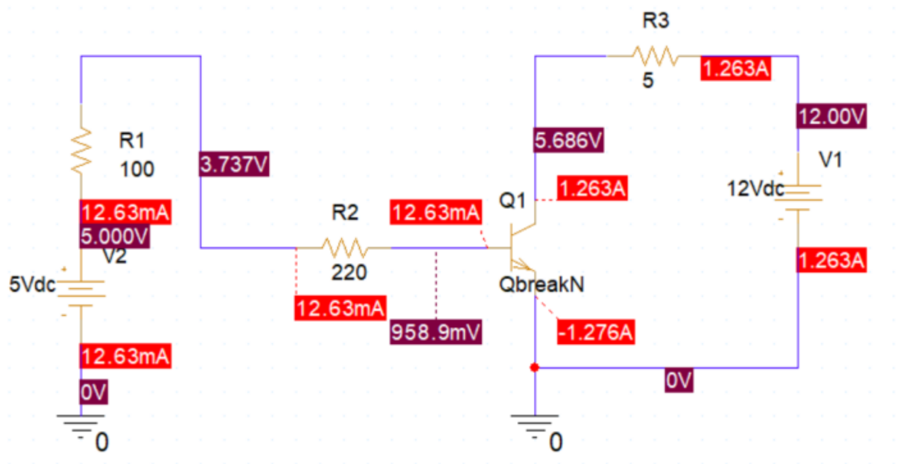
$R_B(min) : R_B = 975$ **Ohm**



$R_B(max) : R_B = 1333.33$ **Ohm**



$R_B(selected) : R_B = 1000$ **Ohm**



3.4.3 Compare

		Theory			PSpice		
	$R_B(\Omega)$	$V_{BE}(V)$	I_B (mA)	I_C (mA)	V_{BE} (V)	I_B (mA)	I_C (mA)
$R_B(min)$	975	0.7	4	400	0.93	3.79	378.8
$R_B(max)$	1333.33	0.7	3	300	0.92	2.8	284.6
$R_B(selected)$	1000	0.7	3.91	390.91	0.93	3.70	370.3

3.5 Simple bias configuration

The circuit given in Figure 1.7 is known as a simple kind of NPN bias configuration. First, students simulate the circuit with two values of RC, respectively 10 Ohms and 1k Ohms. Then, give your statement on the change of the current I_E and explain the phenomena.

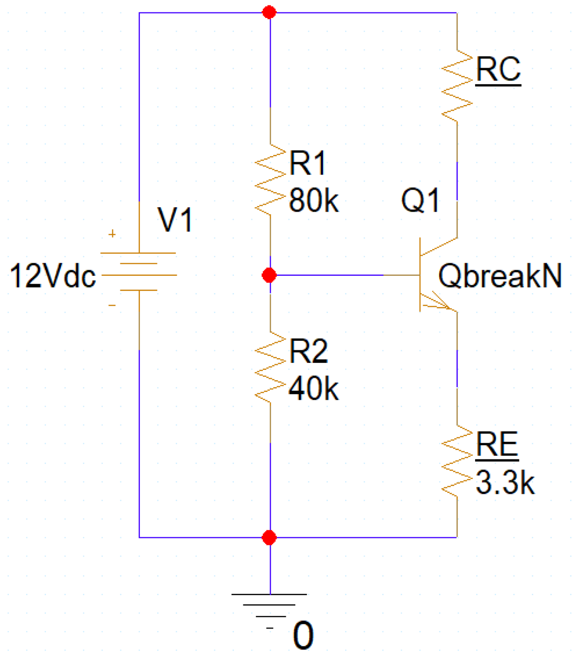


Figure 1.7: Simple bias configuration

3.5.1 Simulation

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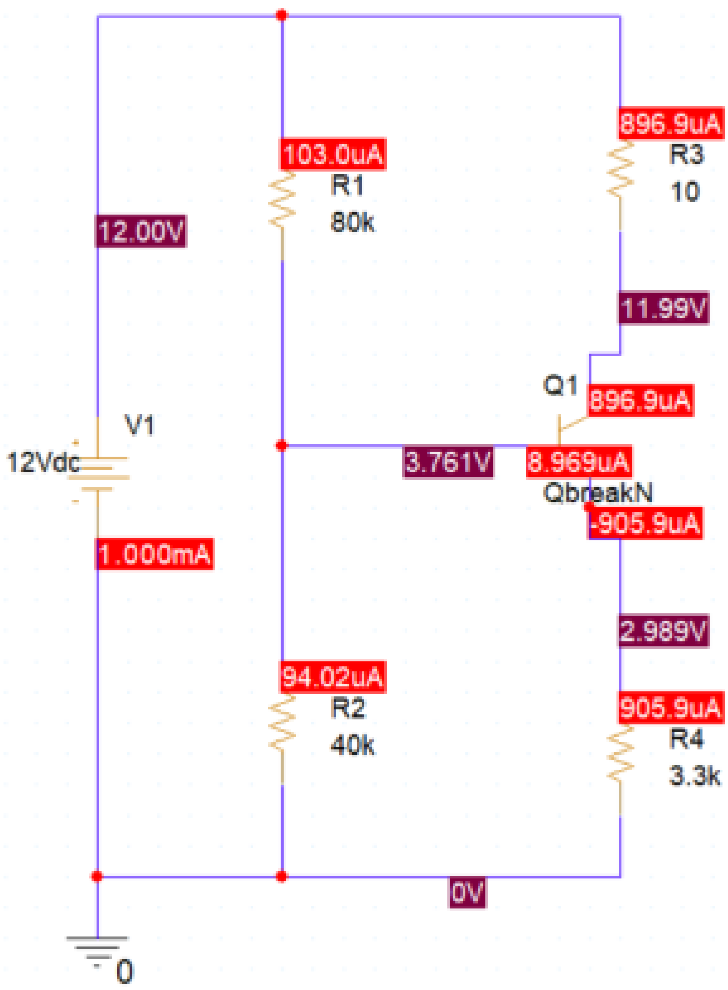
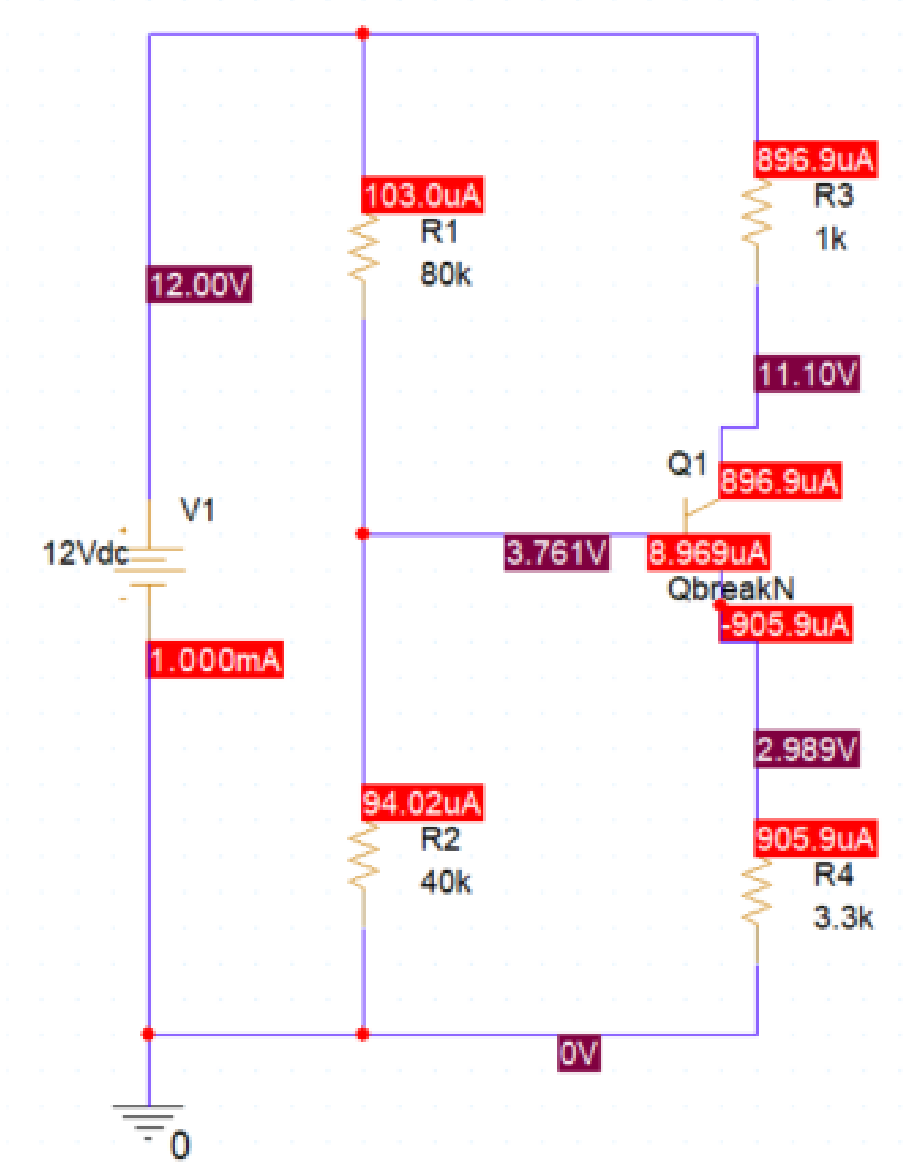
Step 1: Simulate the circuit with R_C = 10 Ohms.


896.9uA
R3
10
103.0uA
R1
80k
12.00V
11.99V
Q1
896.9uA
V1
12Vdc
3.761V
8.969uA
QbreakN
-905.9uA
1.000mA
2.989V
94.02uA
R2
40k
905.9uA
R4
3.3k
0V
0

Step 2: Simulate the circuit with R_C = 1k Ohms.



3.5.2 Circuit analysis

Conduct some theoretical calculation to explain for the phenomena you have observed from the simulation.

From the simulation results, we can see that the value of I_c remains the same whether R_c is 10 Ohm or 1k Ohm.

We calculate I_C with the default $\beta = 100$:

$V_{BE} = 0.7$ (V); $I_E = I_C + I_B$ and $I_C = \beta I_B$
$\Rightarrow I_E = (\beta + 1).I_B$

$R_{TH} = \dfrac{R_1.R_2}{R_1 + R_2} = \dfrac{80k.40k}{80k + 40k} = \dfrac{80k}{3} = 26.6667k(\text{Ohm})$

$V_{TH} = \dfrac{R_2}{R_1 + R_2}.V_1 = \dfrac{40k}{40k + 80k}.12 = 4\ (\text{V})$

We have: $V_{TH} = I_B.R_{TH} + V_{BE} + I_E.R_E = I_B.\dfrac{80}{3} + 0.7 + (\beta + 1).I_B.3.3k = 4(v)$

$\Rightarrow I_B = 9.17\ (\mu\text{A})$

$I_E = (\beta + 1).I_B = (100 + 1).9.1675 = 925.92\ (\mu\text{A})$

$\Rightarrow I_C$ does not depend on the value of R_c.

3.6 PNP Circuit

Figure 1.8 shows a very typical PNP transistor circuit. Calculate I_B, I_E, and I_C then simulate the circuit to double-check your calculation. Assume the current gain $\beta = 100$.

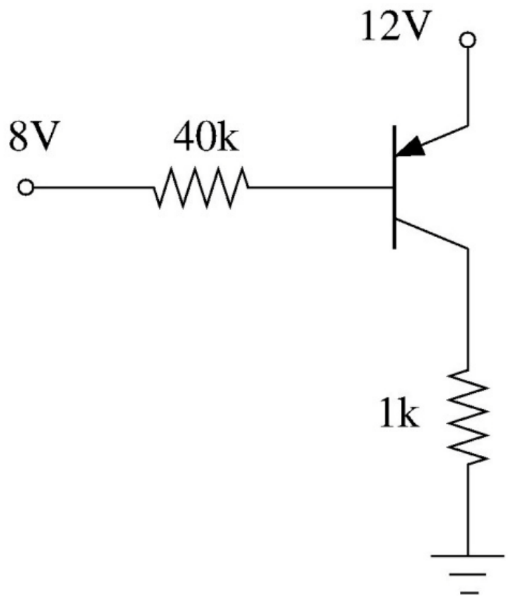


Figure 1.8: A PNP Circuit

3.6.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

$V_{EB} = 0.7$ (V)
$8 + V_{EB} + I_B.40k = 12(V)$
So $I_B = \dfrac{12 - 8 - V_{EB}}{40} = 0.0825$ (mA)
$I_C = \beta I_B = 100.0.0825 = 8$ (mA)
$I_E = I_C + I_B = 8.25 + 0.0825 = 8.33$ (mA)

3.6.2 Simulation

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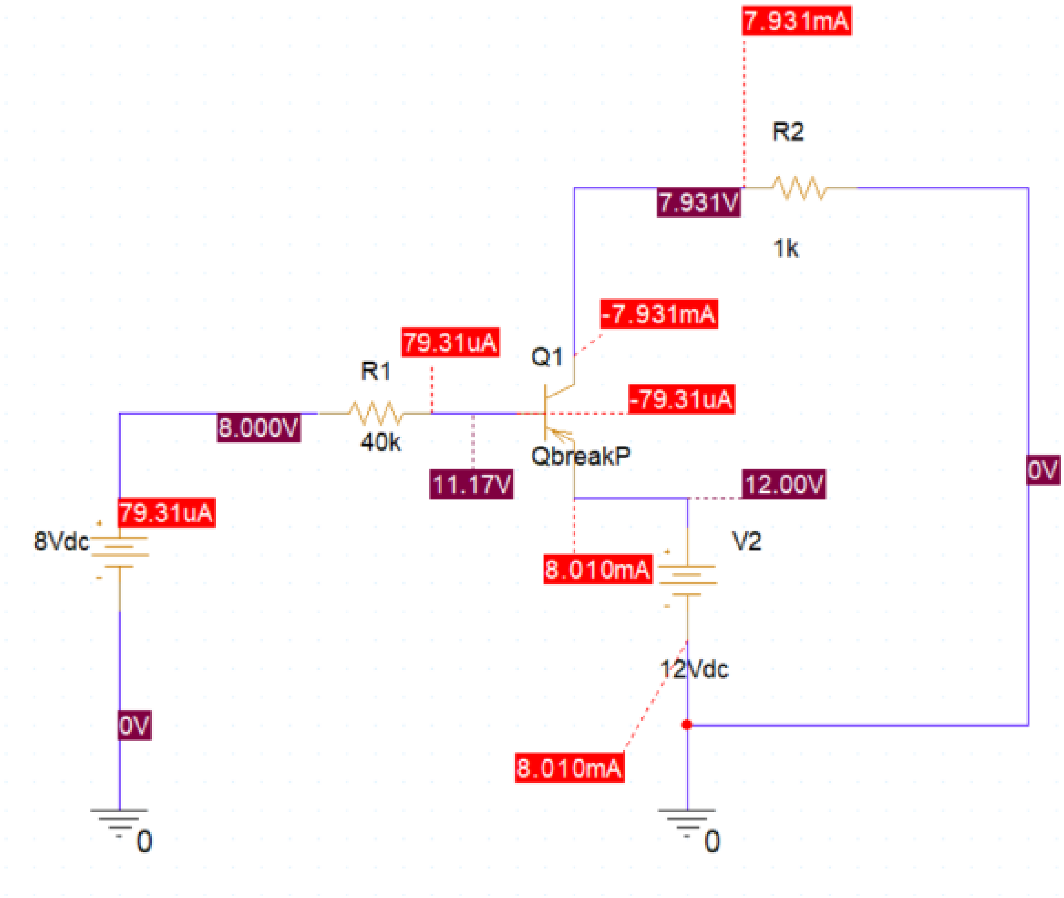

3.6.3 Comparison

I_B (In theory) = 0.08 mA .... I_B (simulation) = 0.079 mA ....

I_C (In theory) = 8.25 mA .... I_C (simulation) = 7.93 mA ....

I_E (In theory) = 8.33 mA .... I_E (simulation) = 8.01 mA ....

3.7 Circuit with NPN and PNP bipolar junction transistors

Give the circuit in Figure 1.9. Calculate the Voltage at all nodes and the current in all branches. Assume the current gain of both transistors is the same at $\beta = 100$. Then perform a simulation and compare the result with the theoretical calculation.

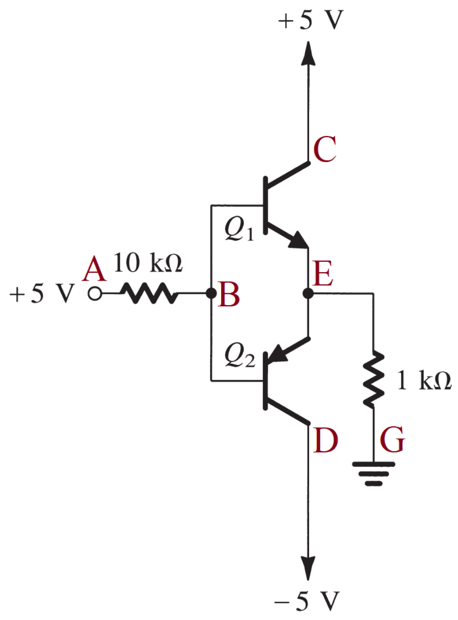

Figure 1.9: Circuit with NPN and PNP bipolar junction transistors

3.7.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

$V_{BE} = V_B - V_E = 0.7V > 0$ so V_E is smaller than V_B , the transistor Q_2 is cut-off.
According to Ohm Law, we have:
I_{BE}= I_{AB} $I_B.10k + 0.7 + I_E.1k = 5(V)$
$I_E = (\beta + 1).I_B \Rightarrow I_B.10k + 0.7 + I_B.101k = 5(V) \Rightarrow I_B = 38.7(\mu\text{A})$
$I_C = 3.87(\text{mA})$
$I_{EG} = I_B + I_C = 3.91(\text{mA})$
$V_E = I_{EG} \cdot 1k = 3.91 \cdot 1k = 3.91(\text{V})$
$V_B = 5 - I_B \cdot 10 = 5 - 38.7 \cdot 10^{-3} \cdot 10 = 4.61(\text{V})$

3.7.2 Simulation

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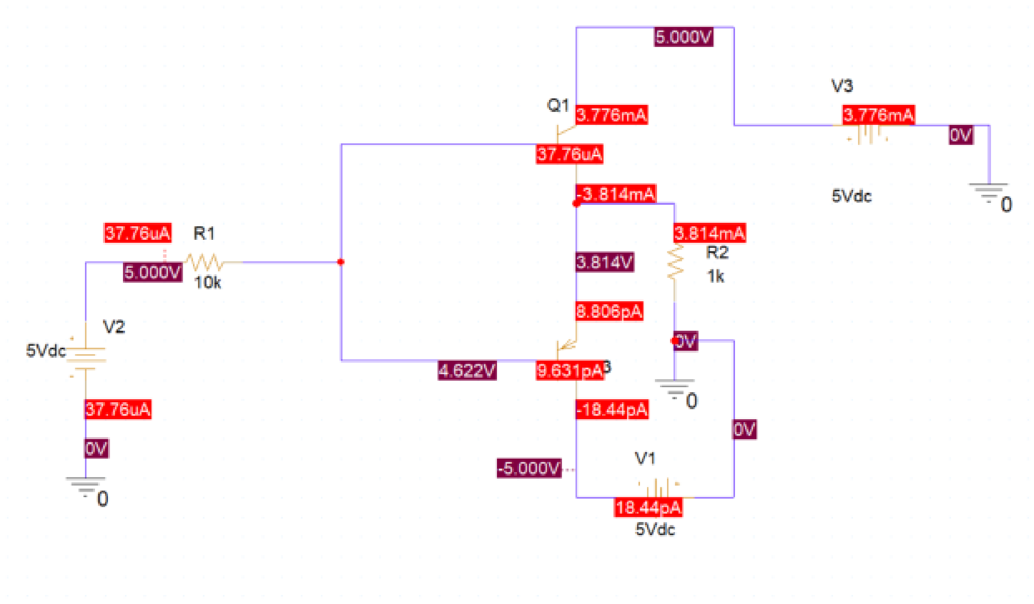

3.7.3 Comparison

	Theory Calculation					PSpice Simulation				
	I_B	I_C	I_{EG}	V_E	V_B	I_B	I_C	I_{EG}	V_E	V_B
	38.7μA	3.87mA	3.91mA	3.91V	4.61V	37.76μA	3.78mA	3.81mA	3.81V	4.62V