AS-0.3200 Project work – Battery stack monitor board design documentation

Table of Contents

Introduction

Abbreviations

ADC – analog to digital converter

BOM – bill of materials

ESD – electrostatic discharge

KCL – Kirchhoff's current law

LPF – low-pass filter

Communication

Communication to MCU

Communication to upper monitor

Communication to lower monitor

Battery interface

Connectors

All connectors have screw terminals. This allows a defined power connection sequence. Screw terminals are also resistant against vibration and shock, which is important consideration in an automotive environment.

The end goal is to integrate monitor board with balancer board, so connectors are 5.00 mm pitched with current carrying capacity of 10 A.

Every battery has their own connection. Batteries are connected in series on board, but this connection should not be used as only connection between batteries.

Note: Should this connection be removed to enforce good connection outside board?

Note 2: Does this connection serve as a redundant path to guard against breakage? @see LTC6803 datasheet p. 30

Monitoring

Measuring voltage

LTC6803-3 has 12-bit sigma-delta ADC. ADC outputs 12-bit code with an offset of 0x200 (512 decimal). Input voltage can be calculated as: $U_{\text{in}} = (D_{\text{out}} - 512) * 1{,}5\,\text{mV}$ [LTC6803 datasheet p. 14]

Passive discharging is turned off by default when cells are read. However, there exists a self-test mode where cell discharging switches are left on. [LTC6803 datasheet p. 14]

Filtering and anti-aliasing

Electrical connection to ADC has a RC low-pass filter shown in illustration [] to reject noise coupling into measurement. A 7.5 V zener diode gives overvoltage and limited reverse polarity protection for the measurement cell.

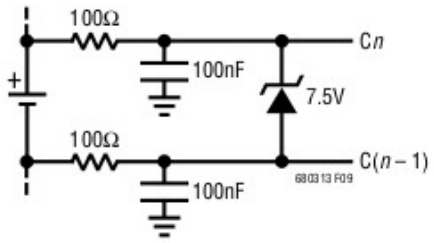

Illustration 1: LPF + protection zener

Series resistance introduces an 1 mV DC measurement error to ADC. On the other hand, LPF offers 30 DB noise rejection and ESD-protection with zener. Since 1 mV is smaller than LSB of ADC, this error is negligible. [LTC6803 datasheet p. 27]

On the other hand, ground connection of capacitor creates hazardous voltage differentials on board. In case where capacitor gets shorted grounded, up to 50 V (topmost cell, while charging) could be imposed on filtering resistor. This could be a catastrophic failure, as

$$P = U^2 * R \Rightarrow P = 25\,\mathrm{W}$$

While current of 0.5 A is not too much, if the resistor fails as short entire battery stack gets shorted.

As a mitigation measure LPF of 10k ohms and 3.3 uF could be used. 10 k series resistance limits current to 5 mA, and power dissipated is 250 mW. Capacitor that can handle at least 75 V (50% margin) is notably larger (at least 1206) and more expensive. DC error of such a circuit is smaller at 0.5 mV. [LTC6803 datasheet p. 27]

Design choice: Which component values to use? Or omit LPF altogether?

Open connection detection

Done in software, see details @ LTC6803 datasheet p 28.

<TODO>

Passive balancing

Current paths

LTC6803 has internal mosfets that can be used for modest passive balancing. Internal mosfets are connected directly into lower cell. LPF's series resistance would raise the voltage at ADC. Illustration [] clarifies issue. Discharge current should be returned to input connector of battery rather than to ADC input pin to avoid rising voltage at lower ADC over spec.

This is done by using external transistor which can direct most of the current back to connector input.

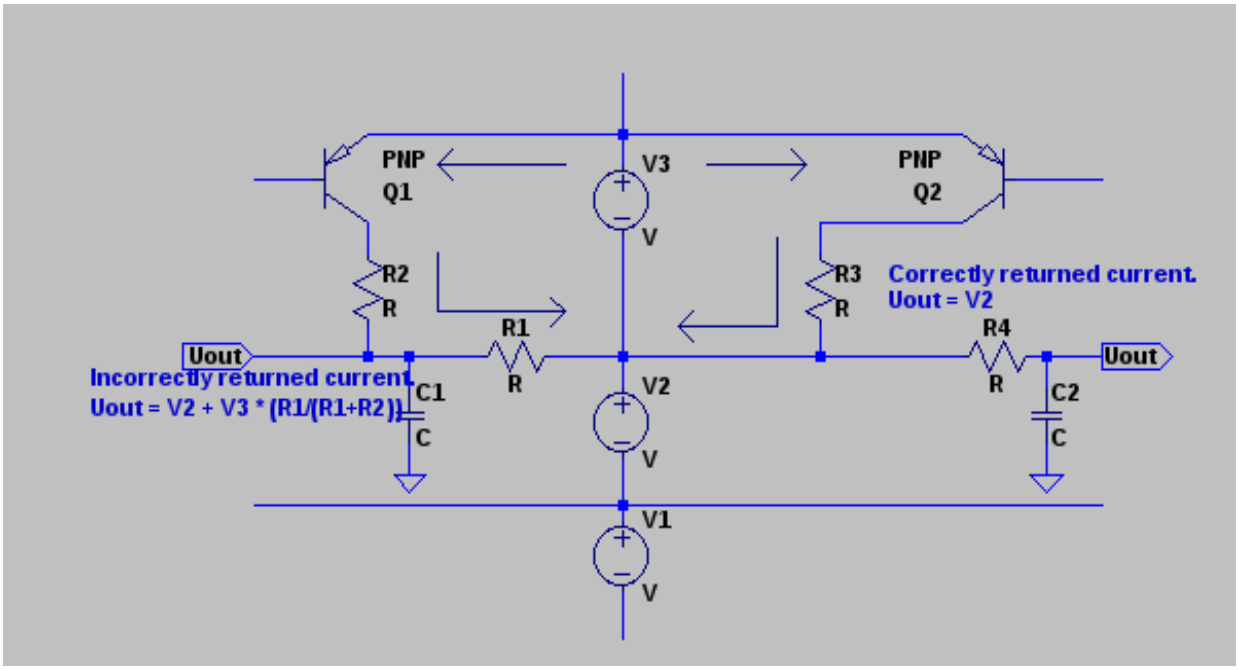

Illustration 2: Always, always, always consider KCL.

Transistor selection

Datasheet of LTC6803 suggests using Si2351DS PMOS with a protection zener from gate to source. Using a PNP transistor avoids the need for a separate protection zener, since zener of LPF couples the voltage of lower cell to next cell in series, and this voltage gets coupled into base of transistor through emitter-base junction.

Voltage and current ratings should be comparable to Si2352DS: -20 Vce and 3 A of collector

current. Design guidelines of project call for SOT-323 / SC-70 package, with pin order of BCE.

ZUMT718 is a decent match with Vce of -20 V, Ic of 1 A (3 A pulsed). It also has required package and it is readily available.

ZUMT718 has Hfe of at least 300 at collector current of 100 mA. The base resistor can be have 100 * resistance of shunt resistor while still keeping transistor in saturated condition.

NOTE: PLEASE check the reasoning above.

Power considerations

Since passive balancing can only turn excess charge into heat, heat management must be considered. Since we're already using external transistor to return bulk of current back to connectors, power dissipation at LTC6803 is negligible.

Most of the power is dissipated in shunt resistors. Since actual balancing is going to be implemented at a separate circuit, these resistors do not need to be scaled for useful powers. A 100 ohm 0805 resistor with power handling capacity of ¼ W is selected to simplify the BOM.

Approximately 40 mA can be pulled from battery through this resistor.

Note: This current could be used for a indicator led “Battery full”.

Minimizing leakage

Every mosfet has an property of drain-source leakage current. Internal mosfets of LTC6803 are surely not an exception. While leakage current of a mosfet would not usually be a problem, any leakage is amplified by external PNP transistor.

LTC6803 has internal pull-up mosfets which connects the base of transistor to potential of upper cell. This will keep transistor strictly in cut off region, limiting leakage to it's own leakage current.

Note: Make sure these pull-ups are on.

Protection against short to LPF ground

Lithium-ion batteries have ability of discharging at rather extreme currents, possibly causing fire or explosion. In case where PNP-transistor's base gets shorted to ground transistor will act as diode through emitter to base. Semiconductors have a habit of failing as short circuits unless internal connections of chip burn out.

This scenario is mitigated by laying base resistor before LPF's via to ground. In case of a short the resistors will limit the current through transistor and zener diodes will provide a path to ground for other cells. Resistors of LPF's will limit the current through these connections to approximately 7 mA, which is survivable.

While circuit itself might get destroyed in short, batteries themselves should survive this fault.

In conclusion

This section is summed up by Illustration []. LPF section with protection zener is shown. Passive discharge section shows the layout of LPF's ground via. Discharge current path is shown. This illustration assumes that LPF with 10 k ohm has been chosen.

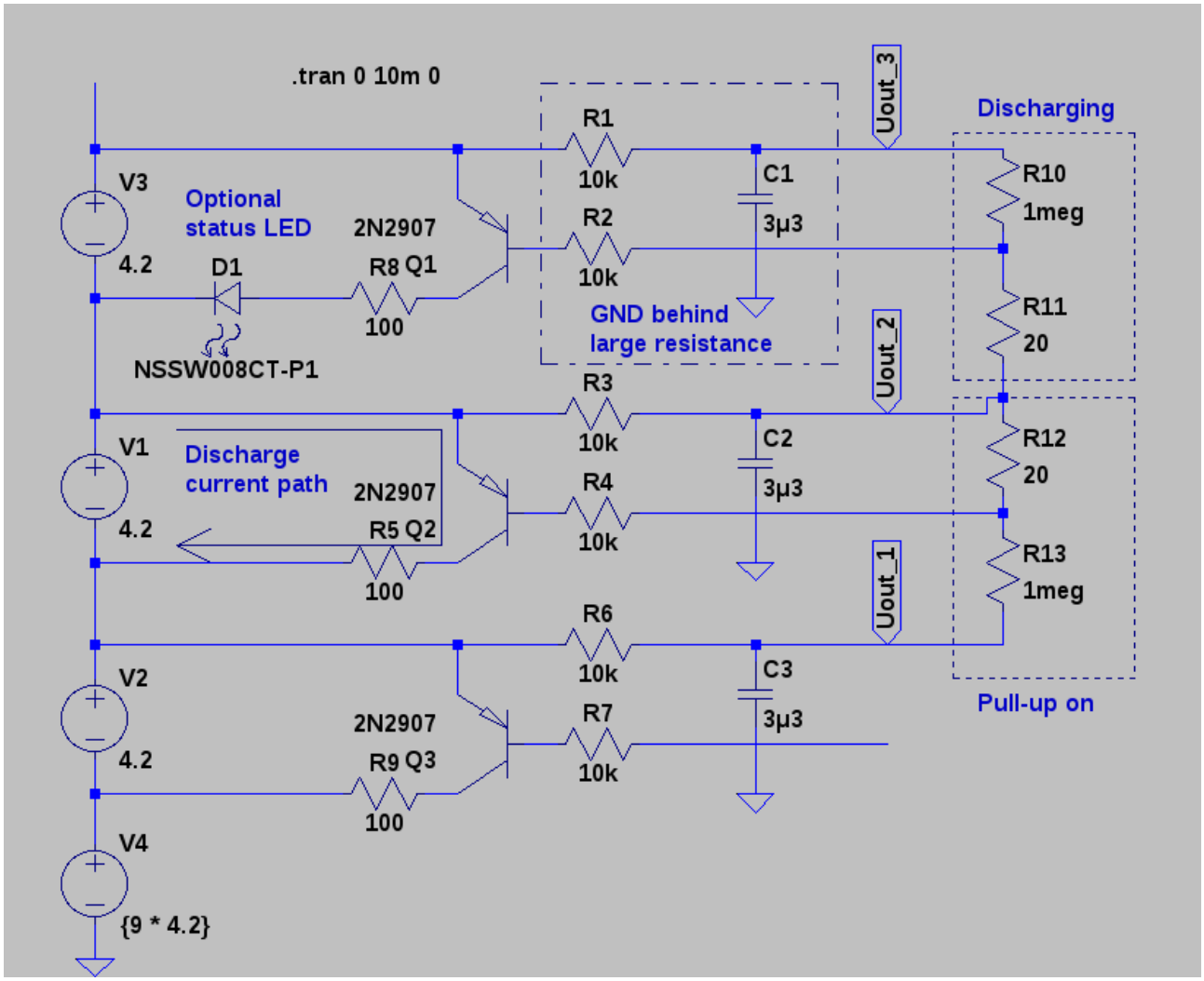

Illustration 3: Battery interface of circuit

Following design choices must be made:

1) Will LPF be included?

1a) If yes, 100 ohm / 100nF or 10k ohm / 3.3 uF?

2) Will discharge circuit be included

2a) Will status leds be included in discharge path?

Power supply

Isolated PSU

Battery powered mode

PSU Bypassing

Configuration

Software

Undervoltage and overvoltage limits

LTC6803-3 has registers which define under- and overvoltage limits. They're set at startup by:

<TODO>

Jumpers

JMP 1 – Top Of Stack (TOS)

This jumpers sets the device as TOP-OF-STACK.

<TODO> Figure out how to set it and what effects there are.

<TODO> What if only one monitor IC is used?

JMP 2 – Vmode

This jumper sets mode of IC

<TODO> Figure out connections and significance of this setting.

Fault conditions

Table 15 of LTC6803 (p.30) lists a number of fault conditions. Ensure that all are accounted for.

<TODO>