



# Quad,16-Bit,4 MSPS, Simultaneous Sampling, μModule Data Acquisition System

## Preliminary Datasheet

ADAQ4380-4

### FEATURES

- Easy to use μModule data acquisition system
- All active components designed by Analog Devices, Inc.
- 11x footprint reduction versus discrete solution
- Includes critical passive components
- 5V Single Supply Operation
- Guaranteed 16-bit no missing codes
- On-chip oversampling function
- 2-bit Resolution Boost
- Out of Range Indicator (ALERT)
- INL: ±1 LSB typical, ±2 LSB maximum
- SNR (typical)
  - 91.1 dB at Gain = 1.0, f<sub>IN</sub> = 1 kHz
  - 98.6 dB with x8 OSR

Channel-to-Channel Phase Matching: 0.1° max @ 20 kHz

Integrated High Precision Reference, 5 ppm/°C max drift

Gain error: 0.005% typical

Gain drift: 1 ppm/°C typical

Integrated Internal Buffer with VCM generation

Integrated Fully Differential ADC driver with signal scaling

Wide Input Common Range

High Common Mode Rejection

Single-ended to differential conversion

Pin selectable input range with over-range

Input Ranges: ±2V, ±3.3V, ±5.5V, ±11V

Gain/Attenuation: G = 0.3, 0.6, 0.625, 1.0, and 1.6

High Speed Serial Interface

8 mm x 8 mm, 0.8 mm pitch, 81-ball CSP\_BGA package

### APPLICATIONS

Motor Control Position Feedback

Motor control current sense

Lab Grade Battery Test System

Sonar

Power quality monitoring

Data acquisition systems

Erbium doped fiber amplifier applications

I and Q demodulation

### GENERAL DESCRIPTION

The ADAQ4380-4 is a quad channel, 16-bit precision data acquisition (DAQ) μModule® system that reduces the development cycle of a precision measurement system by transferring the signal chain design challenges of component selection, optimization, and layout from the designer to the device.

Using System-in-Package (SIP) technology, the ADAQ4380-4 reduces end system component count by combining multiple common signal processing and conditioning blocks into a single device. The ADAQ4380-4 consists of:

- A Quad channel high resolution 16-bit, 4 MSPS simultaneous sampling SAR ADC
- Low noise, fully differential ADC drivers
- A Precision 3.3V voltage reference
- A low noise, low dropout linear regulator
- Reference buffers
- Critical passive components required to achieve optimum performance of the signal chain.

Using Analog Devices, Inc. iPassives® technology, the ADAQ4380-4 incorporates crucial passive components with superior matching and drift characteristics to minimize temperature dependent error sources and offer the best performance from each individual blocks.

ADAQ4380-4 has an on-chip oversampling blocks to improve the dynamic range and reduce noise at lower bandwidths. This block can boost up to two bits of added resolution.

The ADAQ4380-4 is designed with a configurable ADC Driver stage, providing user selectable gain or attenuation settings. The ADAQ4380-4 can be operated in either fully differential or single ended-to-differential input configurations.

Housed in an 8mm x 8mm, 0.8 mm pitch, 81-ball BGA, the ADAQ4380-4 μModule® enables a compact design without sacrificing performance and simplifies end system bill of materials management.

The serial peripheral interface (SPI)-compatible, serial user interface is compatible with 1.8 V, 2.5 V, and 3.3 V logic. ADAQ4380-4 is specified to operate from -40°C to +105°C.

Table 1. μModule Data Acquisition Solutions

Type	250 - 500 kSPS	1 - 2 MSPS	4 MSPS
16-Bit	ADAQ7988	ADAQ7980, ADAQ4001	ADAQ4380-4(Quad Channel)

#### Rev. PRH

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## TYPICAL APPLICATION DIAGRAM

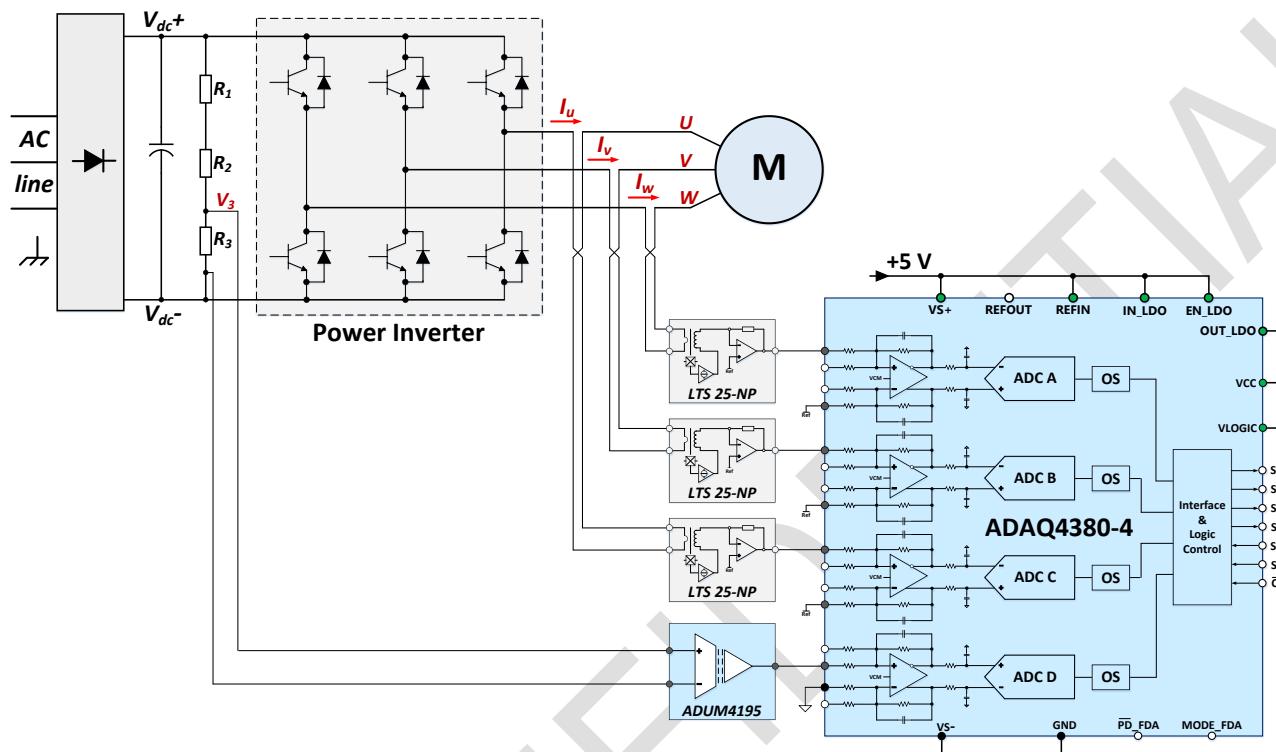


Figure 1. Motor Control Current and Voltage Sensing for High Power Servo Motors using ADAQ4380-4

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## REVISION HISTORY

### 2/20—Rev. PrA to Rev. PrB

Changes to Features Section .....	1
Changes to General Description .....	2
Changes to Specifications Section.....	3
Changes to Theory of Operation .....	15

### 6/20—Rev. PrB to Rev. PrC

Changes to Application Diagram.....	1
Changes to BGA pitch .....	1
Updates to Specifications Section .....	3
Changes to Figure 21 .....	15
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### 9/20—Rev. PrC to Rev. PrD

Changes to Features Section .....	1
Updates to Figure 1 .....	1
Changes to General Description .....	2
Changes to Specifications Section.....	3
Changes to Figure 21 .....	15
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### 11/20—Rev. PrD to Rev. PrE

Changes to Features Section .....	1
Added Channel-to-Channel Phase Matching .....	1
Changes to Figure 1 .....	1
Changes to General Description .....	2

Changes to Specifications Section .....	3
Changes to Table 3 .....	6
Added Figure 9 .....	12
Added Table 6 and Table 7 .....	12
Added Figure 10 and Figure 13 .....	14
Changes to Figure 21 .....	17
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### 01/21—Rev. PrE to Rev. PrF

Changes to Figure 1 .....	1
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### 03/21—Rev. PrF to Rev. PrG

Changes to Table 2 .....	5
Changes to Figure 9 .....	12
Updates to Figure 25-32 .....	37

### 02/22—Rev. PrG to Rev. PrH

Changes to Figure 1.....	2	Added input impedance section.....	25
Changes to Table 2.....	4		

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## SPECIFICATIONS

$V_{S+} = 5 \text{ V} \pm 5\%$ ,  $V_{S-} = 0 \text{ V}$ ,  $\text{IN\_LDO} = \text{EN\_LDO} = 5 \text{ V} \pm 5\%$ ,  $V_{CC} = V_{LOGIC} = 3.4 \text{ V}$ , Reference Voltage ( $V_{REF}$ ) = 3.3 V Internal,  $f_{SAMPLE} = 4 \text{ MSPS}$ , Fully Differential Input Configuration, Full Power mode,  $T_A = 25^\circ\text{C}$ , oversampling disabled, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT CHARACTERISTICS					
Full-Scale Input Range	Gain = 0.3, $V_{IN} = 22 \text{ V p-p}$ Gain = 0.6, $V_{IN} = 11 \text{ V p-p}$ Gain = 1.0, $V_{IN} = 6.6 \text{ V p-p}$ Gain = 1.6, $V_{IN} = 4.125 \text{ V p-p}$		$\pm 11$ $\pm 5.5$ $\pm 3.3$ $\pm 2.0625$		V
Input Common-Mode Voltage Range, $V_{IN}^1$	Fully Differential Input configuration Gain = 0.3 Gain = 0.6 Gain = 1.0 Gain = 1.6	-5.5 -2.9 -1.7 -1.0		+5.5 +6.9 +5.6 +4.9	V
INPUT RESISTANCE ( $R_{IN}$ ), $V_{IN}^1$	Fully Differential Input configuration Gain = 0.3, 0.6 Gain = 1.0 Gain = 1.6 Single-Ended Input configuration Gain = 0.3 Gain = 0.6 Gain = 1.0 Gain = 1.6		2.70 1.62 1.013		kΩ
-3 dB Bandwidth			3.05 3.32 2.11 1.46		kΩ
Input Capacitance	Gain = 0.3 Gain = 0.6, 1.0, 1.6 INx+, INx-		9.8 5.8		MHz
			TBD		pF
THROUGHPUT					
Complete Cycle		250			ns
Conversion Time			190		ns
Acquisition Phase		110			ns
Conversion Rate				4	MSPS
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Delay Match			20		ps
Aperture Jitter			20		ps
OVERALL SYSTEM DC ACCURACY					
No Missing Codes	DNL	16			Bits
Differential Nonlinearity Error	INL	-0.99	$\pm 0.5$	+1	LSB
Integral Nonlinearity Error <sup>2</sup>	All Gains, Referred-to-Input (RTI)	-2	$\pm 1$	+2	LSB
Gain Error	RTI, Endpoint Method		0.005		%FS
Gain Error Drift	RTI		1		ppm/°C
Offset Error	RTI, Box Method	-0.2	$\pm 0.03$	+0.2	mV
Offset Error Drift	$\Delta V_{CM}/\Delta V_{OSDIFF}$	-2	$\pm 0.5$	+2	$\mu\text{V}/^\circ\text{C}$
Common Mode Rejection Ratio			-75		dB
Power Supply Rejection Ratio					
Positive	$V_{CC} = 3.25 \text{ V to } 3.35 \text{ V}$		85		dB
Negative	$VS+ = 4.75 \text{ V to } 5.25 \text{ V}, VS- = 0 \text{ V}$		110		dB
1/f Noise	$VS+ = 5 \text{ V}, VS- = 0 \text{ V to } -0.5 \text{ V}$		103		dB
	Bandwidth = 0.1 Hz to 10 Hz		20		$\mu\text{Vpp}$

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL SYSTEM AC ACCURACY <sup>3</sup>					
Total RMS Noise	RTI, at 1 kHz Gain = 0.3 Gain = 0.6 Gain = 1.0 Gain = 1.6		200 101 62 39		µVrms µVrms µVrms µVrms
Signal-to-Noise Ratio	$V_{IN} = -0.5 \text{ dBFS}$ , $f_{IN} = 1 \text{ kHz}$ Gain = 0.3 Gain = 0.6 Gain = 1.0 OSR = 8, RES = 1, ROLLING AVERAGE Gain = 1.6 Gain = 1.0, Low Power Mode Gain = 1.0, $f_{IN} = 100 \text{ kHz}$ Gain = 1.0, $f_{IN} = 200 \text{ kHz}$		91.2 91.1 91.0 98.6 90.8 90.6 90.4 89.2		dB dB dB dB dB dB dB dB
Signal-to-Noise + Distortion (SINAD)	$V_{IN} = -0.5 \text{ dBFS}$ , $f_{IN} = 1 \text{ kHz}$ Gain = 0.3 Gain = 0.6 Gain = 1.0 Gain = 1.6 Gain = 1.0, Low Power Mode Gain = 1.0, $f_{IN} = 100 \text{ kHz}$ Gain = 1.0, $f_{IN} = 200 \text{ kHz}$		91.1 91.1 91.1 91.0 91.0 90.5 90.2 88.6		dB dB dB dB dB dB dB dB
Total Harmonic Distortion	$V_{IN} = -0.5 \text{ dBFS}$ , $f_{IN} = 1 \text{ kHz}$ Gain = 0.3 Gain = 0.6 Gain = 1.0 Gain = 1.6 Gain = 1.0, Low Power Mode Gain = 1.0, $f_{IN} = 100 \text{ kHz}$ Gain = 1.0, $f_{IN} = 200 \text{ kHz}$		-103 -103 -103 -103 -103 -103 -101 -98		dB dB dB dB dB dB dB dB
Spurious-Free Dynamic Range	$V_{IN} = -0.5 \text{ dBFS}$ , $f_{IN} = 1 \text{ kHz}$ Gain = 0.3 Gain = 0.6 Gain = 1.0 Gain = 1.6		103 103 102 102		dB dB dB dB
Channel-to-Channel Isolation Channel-to-Channel Phase Matching	All gains, $f_{IN} = 20 \text{ kHz}$		TBD	0.1	Degrees
REFERENCE CHARACTERISTICS					
$V_{REF}$ Input Voltage Range	Internal REF Supply Voltage	4.5	5.0	5.5	V
$V_{REF}$ Input Current	Internal REF Quiescent Current	350	600		µA
$V_{REF}$ Output Voltage	REFOUT	3.3			V
$V_{REF}$ Temperature Coefficient	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ $TCV_{OUT}$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$	TBD		TBD	V
$V_{REF}$ Line Regulation			5		ppm/V
$V_{REF}$ Load Regulation			10		ppm/mA
$V_{REF}$ Noise			1.2 3 9	5 8	µVrms
LDO CHARACTERISTIC					
IN_LDO Voltage Range		4.5	5.0	5.5	V
IN_LDO Supply Current	$I_{OUT} = 150 \text{ mA}$		130	190	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUT_LDO Voltage		3.35	3.46	3.5	V
Maximum Output Current			150		mA
Shutdown Current	IN_LDO = GND		0.1	1	μA
Load Regulation	I <sub>OUT</sub> = 1 mA to 150 mA		0.0005		%/mA
Dropout Voltage	I <sub>OUT</sub> = 150 mA		45	75	mV
Start-Up Time			350		μs
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C
DIGITAL INPUTS (SCLK, SDI, /CS)					
Logic Levels					
V <sub>IL</sub>	V <sub>LOGIC</sub> < 2.3 V			0.45	V
	V <sub>LOGIC</sub> ≥ 2.3 V			0.7	V
V <sub>IH</sub>	V <sub>LOGIC</sub> < 2.3 V		V <sub>LOGIC</sub> - 0.45V		V
	V <sub>LOGIC</sub> ≥ 2.3 V		0.8×V <sub>LOGIC</sub>		V
I <sub>IL</sub>	-1		+1		μA
I <sub>IH</sub>	-1		+1		μA
DIGITAL OUTPUTS (SDOA, SDOB, SDOC, SDOD/ALERT)					
Output Coding				Twos complement	Bits
V <sub>OL</sub>	I <sub>SINK</sub> = +300 μA				
V <sub>OH</sub>	I <sub>SOURCE</sub> = -300 μA			V <sub>LOGIC</sub> - 0.3	
Floating-State Leakage Current					
Floating-State Output Capacitance				10	pF
POWER-DOWN/MODE SIGNALING					
Low	PD_FDA/MODE_FDA			<1	V
High	Disabled, Low Power mode			>1.5	V
Turn-Off Time	Enabled, Full Power mode			5	TBD
	50% of ENABLE to <10% of enabled quiescent current				ms
Turn-On Time	Specified performance			5	TBD
POWER SUPPLY REQUIREMENTS					
Operating Voltage Range					
V <sub>CC</sub>		3.2	3.3	3.6	V
V <sub>LOGIC</sub>		1.65	3.3	3.6	V
VS+		4.5	5.0	5.5	V
VS-		-5	0		V
ADAQ4380-4 Current Draw	V <sub>CC</sub> =V <sub>LOGIC</sub> = 3.46 V, VS+=5 V, VS-=0				
I <sub>VCC</sub>					
Normal Mode (Dynamic)		22	35		mA
Normal Mode (Static)		1.7	2		mA
Shutdown Mode		80	200		μA
I <sub>VLOGIC</sub>					
Normal Mode (Dynamic)		7.3	8		mA
Normal Mode (Static)		10	200		nA
Shutdown Mode		10	200		nA
I <sub>VS+/VS-</sub>					
Full Power Mode		18	19		mA
Low Power Mode		7.6	8.6		mA
Total	Dynamic, Full Power Mode	47.3	62		mA
	Dynamic, Low Power Mode	36.9	37.9		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADAQ4380-4 Power Dissipation $P_{VCC}$	$V_{CC} = V_{LOGIC} = 3.46\text{ V}$ , $VS+ = 5\text{ V}$ , $VS- = 0$		76 5.9	121 6.9	mW mW
$P_{VLOGIC}$	Normal Mode (Dynamic) Normal Mode (Static)		15.9 6.6	19.4 36	mW $\mu\text{W}$
$P_{VS+/VS-}$	Normal Mode (Dynamic) Normal Mode (Static) Full Power Low Power		90 40	100 45	mW mW
Total Power Dissipation	Dynamic, Full Power Mode Dynamic, Low Power Mode	182 132	240 185		mW mW
TEMPERATURE RANGE Specified Performance	$T_{MIN}$ to $T_{MAX}$ <sup>4</sup>	-40		+105	°C

<sup>1</sup> The absolute differential input ranges,  $V_{IN}$ , must be within the allowed input common-mode range as per Figure 23 to Figure 30.  $V_{IN}$  is dependent on the  $VS+$  and  $VS-$  supply rails used.

<sup>2</sup> Limit the absolute differential input range,  $V_{IN}$  to 95% of full scale to allow enough footroom for the ADC driver with  $VS- = 0$  to achieve specified performance.

<sup>3</sup> All AC specifications expressed in decibels are referenced to the full-scale input range (FSR) and are tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

<sup>4</sup> ADAQ4380-4 is rated for performance over extended industrial temperature range,  $T_{CASE} = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ .

**TIMING SPECIFICATIONS**

$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $V_{LOGIC} = 1.65 \text{ V to } 3.6 \text{ V}$ ,  $V_{REF} = 3.3 \text{ V}$ ,  $T_A = -40^\circ\text{C} \text{ to } +105^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Min	Typ	Max	Unit	Description
$t_{CYC}$	250			ns	Time between conversions
$t_{SCLKED}$	5			ns	$\overline{CS}$ falling edge to first SCLK falling edge
$t_{SCLK}$	12.5			ns	SCLK period
$t_{SCLKH}$	5.5			ns	SCLK high time
$t_{SCLKL}$	5.5			ns	SCLK low time
$t_{CSH}$	20			ns	$\overline{CS}$ pulse width
$t_{QUIET}$	20			ns	Interface quiet time prior to conversion
$t_{SDOEN}$		5.5		ns	$\overline{CS}$ low to SDOx enabled
$t_{SDOH}$	3			ns	SCLK rising edge to SDOx hold time
$t_{SDOS}$		5		ns	SCLK rising edge to SDOx setup time
$t_{SDOT}$		8		ns	$\overline{CS}$ rising edge to SDOx high impedance
$t_{SDIS}$	4			ns	SDI setup time prior to SCLK falling edge
$t_{SDIH}$	4			ns	SDI hold time after SCLK falling edge
$t_{SCLKCS}$	0			ns	SCLK rising edge to $\overline{CS}$ rising edge
$t_{CONVERT}$		190		ns	Conversion time
$t_{ACQUIRE}$	110			ns	Acquire time
$t_{RESET}$		250		ns	Valid time to start conversion after soft reset
		800		ns	Valid time to start conversion after hard reset
$t_{POWERUP}$				ms	Supply active to conversion
		5		ms	First conversion allowed
		5		ms	Settled to within 1%
$t_{REGWRITE}$		5		ms	Supply active to register read write access allowed
$t_{STARTUP}$					Exiting shutdown mode to conversion
		200		ns	Settled to within 1%
$t_{CONVERT0}$	6	8	10	ns	Conversion time for first sample in OS Normal Mode
$t_{CONVERTx}$		$t_{CONVERT0} + (320 \times (x - 1))$		ns	Conversion time for $x^{\text{th}}$ sample in OS Normal Mode
$t_{ALERTS}$			220	ns	Time from $\overline{CS}$ to $\overline{\text{ALERT}}$ indication
$t_{ALERTC}$			10	ns	Time from $\overline{CS}$ to $\overline{\text{ALERT}}$ clear
$t_{ALERTS\_NOS}$			20	ns	Time from internal conversion with exceeded threshold to $\overline{\text{ALERT}}$ indication

## Timing Diagrams

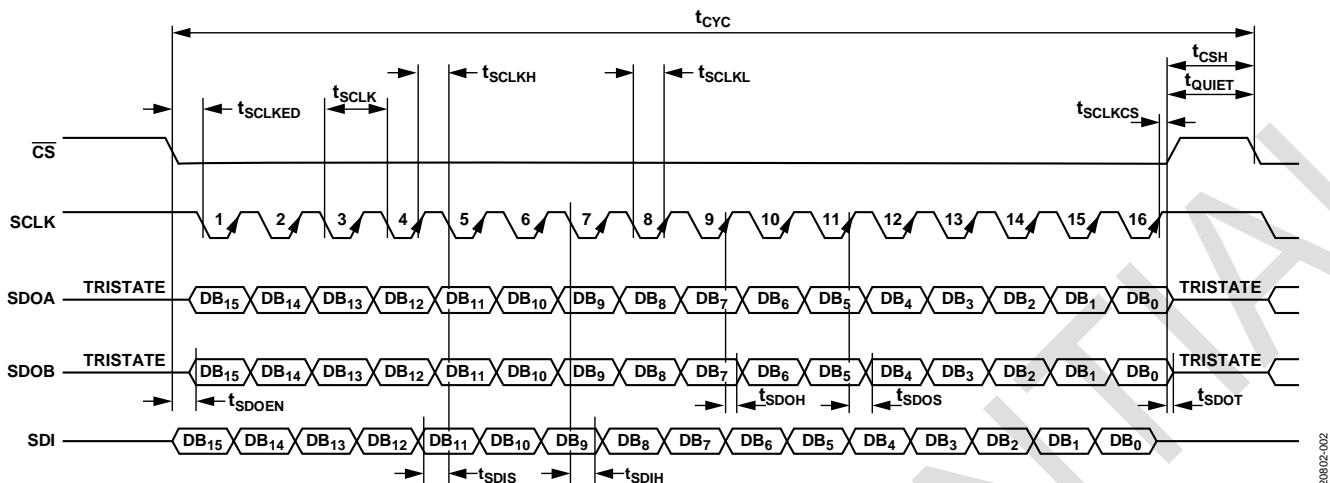


Figure 2. Serial Interface Timing Diagram

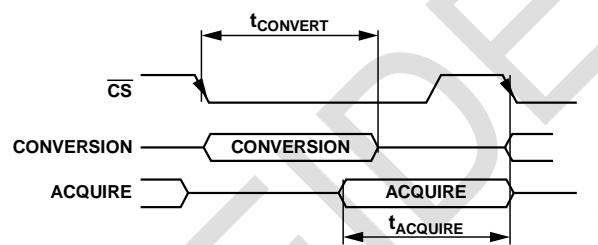


Figure 3. Internal Conversion Acquire Timing

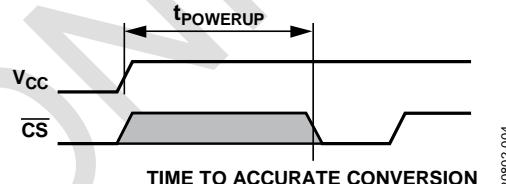


Figure 4. Power Up Time to Conversion

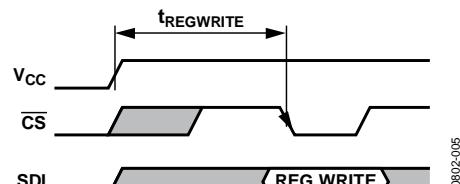


Figure 5. Power Up Time to Register Read Write Access

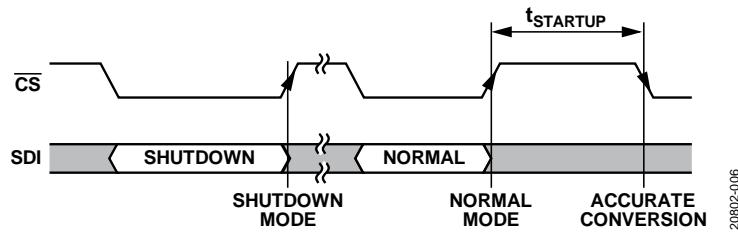


Figure 6. Power Down to Normal Mode Timing

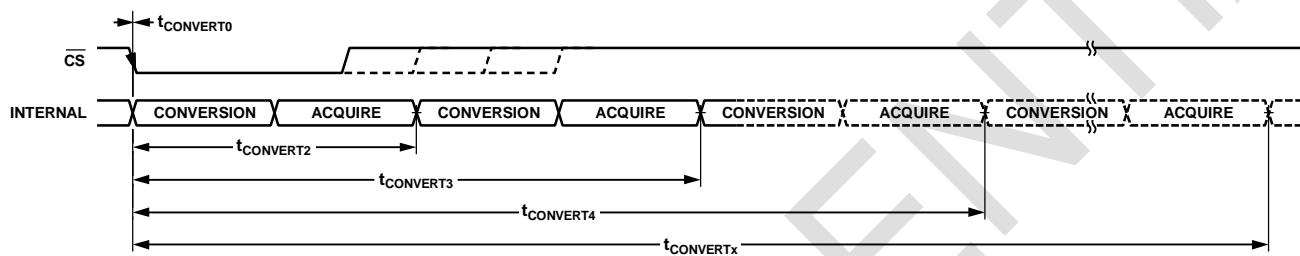


Figure 7. Conversion Timing During OS Normal Mode

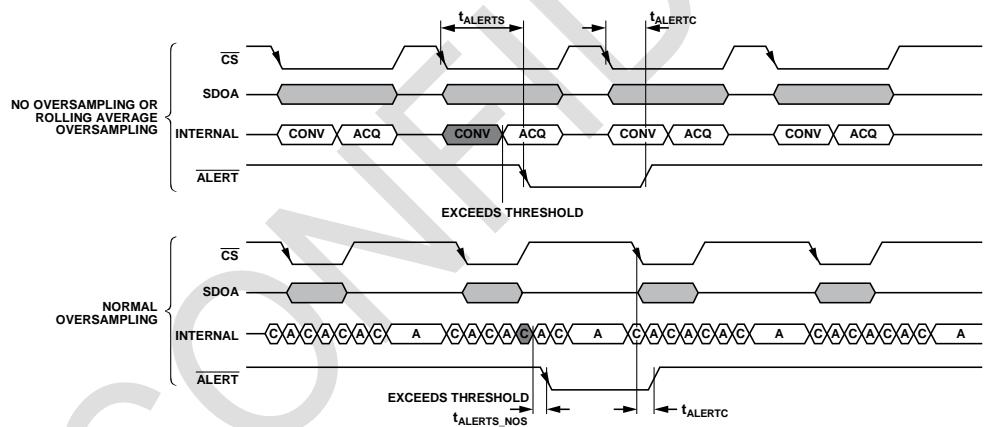


Figure 8. ALERT Timing

## ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs INx1+, INx1-, INx2+, INx2- to GND	-12.5 V to +12.5 V $\pm 10\text{mA}$
Supply Voltages VS+ - VS-	11 V
IN_LDO to GND	-0.3 V to +6.5 V
EN_LDO to GND	-0.3 V to +6.5 V
V <sub>LOGIC</sub> to GND	-0.3 V to +4 V
V <sub>CC</sub> to GND	-0.3 V to +4 V
REFIN to GND	-0.3 V to +38 V
REFOUT to GND	-0.3 V to V <sub>CC</sub> + 0.3 V
Digital Inputs to GND	-0.3 V to V <sub>LOGIC</sub> + 0.3 V
Digital Outputs to GND	-0.3 V to V <sub>LOGIC</sub> + 0.3 V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature Soldering	260°C reflow as per JEDEC J-STD-020
Human Body Model (HBM)	TBD
Field Induced Charged Device Model (FICDM)	TBD

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type <sup>1</sup>	$\theta_{JA}$ (°C/W)	$\theta_{JC\_TOP}$ (°C/W)	$\theta_{JC\_BOTTOM}$ (°C/W)	$\theta_{IB}$ (°C/W)	$\Psi_{JT}$ (°C/W)	$\Psi_{JB}$ (°C/W)
BC-81-7	27.2	38.1	TBD	TBD	5.7	12.0

<sup>1</sup> Test Condition 1: Thermal impedance simulated values are based on use of a 2S2P with via JEDEC PCB excluding the  $\theta_{JC_{top}}$  which uses 1SOP JEDEC PCB.

Thermal resistance values specified in table 5 are simulated based on JEDEC specs (unless specified otherwise) and should be used in compliance with JESD51-12.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9
A	GND	INC1+	INC1-	IND2+	IND2-	IND1+	IND1-	GND	GND
B	GND	OUTC-	OUTC+	SJD+	SJD-	OUTD-	OUTD+	GND	SDOD
C	INC2-	SJC-	VS+	VS+	IN_LDO	EN_LDO	GND	VLOGIC	SDOC
D	INC2+	SJC+	VS+	VS+	IN_LDO	OUT_LDO	OUT_LDO	GND	SCLK
E	GND	PD_FDA	MODE_FDA	GND	GND	DNC	VCC	GND	SDI
F	INB2+	SJB+	VS-	VS-	DNC	DNC	REFIN	GND	SDOB
G	INB2-	SJB-	VS-	VS-	GND	DNC	REFOUT	GND	SDOA
H	GND	OUTB-	OUTB+	SJA+	SJA-	OUTA-	OUTA+	GND	CS
J	GND	INB1+	INB1-	INA2+	INA2-	INA1+	INA1-	GND	GND

Figure 9. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
A1, A8, A9, B1, B8, C7, D8, E1, E4, E5, E8, F8, G5, G8, H1, H8, J1, J8, J9	GND	P	Power Supply Ground.
A2	INC1+	AI	Channel C Positive Input to 1.62 kΩ Gain Resistor Network.
A3	INC1-	AI	Channel C Negative Input to 1.62 kΩ Gain Resistor Network.
A4	IND2+	AI	Channel D Positive Input to 2.70 kΩ Gain Resistor Network.
A5	IND2-	AI	Channel D Negative Input to 2.70 kΩ Gain Resistor Network.
A6	IND1+	AI	Channel D Positive Input to 1.62 kΩ Gain Resistor Network.
A7	IND1-	AI	Channel D Negative Input to 1.62 kΩ Gain Resistor Network.
B2	OUTC-	AO	ADC Driver's Negative Output Voltage Node for Channel C.
B3	OUTC+	AO	ADC Driver's Positive Output Voltage Node for Channel C.
B4	SJD+	AI	ADC Driver's Positive Input Summing Node for Channel D.
B5	SJD-	AI	ADC Driver's Negative Input Summing Node for Channel D.
B6	OUTD-	AO	ADC Driver's Negative Output Voltage Node for Channel D.
B7	OUTD+	AO	ADC Driver's Positive Output Voltage Node for Channel D.
B9	SDOD	DO	Serial Data Output D. This pin functions as a serial data output pin to access the conversion results and register contents or ALERT Indication Output.
C1	INC2-	AI	Channel C Negative Input to 2.70 kΩ Gain Resistor Network.
C2	SJC-	AI	ADC Driver's Negative Input Summing Node for Channel C.

C3, C4, D3, D4	VS+	P	Amplifiers Positive Supply. These pins are decoupled to ground internally. Additional decoupling capacitors may not be necessary.
C5, D5	IN_LDO	P	Integrated LDO's Input Voltage. Connect to VS+ (or 3.6 V < IN_LDO < 5.5V). This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
C6	EN_LDO	P	LDO enable. Connect to IN_LDO or VS+ to enable the internal LDO. Connect to GND if otherwise.
C8	V <sub>LOGIC</sub>	P	ADC's Logic Interface Supply Voltage. This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
C9	SDOC	DO	Serial Data Output C. This pin functions as a serial data output pin to access the conversion results and register contents.
D1	INC2+	AI	Channel C Positive Input to 2.70 kΩ Gain Resistor Network.
D2	SJC+	AI	ADC Driver's Positive Input Summing Node for Channel C.
D6, D7	OUT_LDO	AO	Integrated LDO's Output Voltage. The voltage at this pin is 3.4V typical.
D9	SCLK	DI	Serial Clock Input. This serial clock input is for data transfers to and from the ADC.
E2	<u>PD_FDA</u>	P	Active low. Connect this pin to GND to power down (disable) the ADC Drivers. Connect VS+ for normal operation.
E3	MODE_FDA	P	Power Mode for ADC Drivers. Connect to VS+ for Full Power Mode. Connect to GND to enter Low Power Mode.
E6, F5, F6, G6	DNC	-	Do Not Connect. Leave these pins floating/unconnected.
E7	V <sub>CC</sub>	P	ADC's Analog Supply Voltage. This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
E9	SDI	DI	Serial Data Input. This input provides the data written to the on-chip control registers.
F1	INB2+	AI	Channel B Positive Input to 2.70 kΩ Gain Resistor Network.
F2	SJB+	AI	ADC Driver's Positive Input Summing Node for Channel B.
F3, F4, G3, G4	VS-	P	Amplifiers Negative Supply. These pins are decoupled to ground internally. Additional decoupling capacitors may not be necessary.
F7	REFIN	P	Internal Reference's Supply Voltage. Connect to VS+ for normal operation. This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
F9	SDOB	DO	Serial Data Output B. This pin functions as a serial data output pin to access the conversion results and register contents.
G1	INB2-	AI	Channel B Negative Input to 2.70 kΩ Gain Resistor Network.
G2	SJB-	AI	ADC Driver's Negative Input Summing Node for Channel B.
G7	REFOUT	AI, AO	Internal Reference's Voltage Output and Reference Buffer's Input. This pin is optional. Only utilize this pin if more precise reference voltage is necessary.
G9	SDOA	DO	Serial Data Output A. This pin functions as a serial data output pin to access the conversion results and register contents.
H2	OUTB-	AO	ADC Driver's Negative Output Voltage Node for Channel B.
H3	OUTB+	AO	ADC Driver's Positive Output Voltage Node for Channel B.
H4	SJA+	AI	ADC Driver's Positive Input Summing Node for Channel A.
H5	SJA-	AI	ADC Driver's Negative Input Summing Node for Channel A.
H6	OUTA-	AO	ADC Driver's Negative Output Voltage Node for Channel A.
H7	OUTA+	AO	ADC Driver's Positive Output Voltage Node for Channel A.
H9	<u>CS</u>	DI	Chip Select Input. Active low, logic input. This input provides the dual function of initiating conversions on the ADAQ4380-4 and framing the serial data transfer. <u>CS</u> pin must be pulled high during power-up.
J2	INB1+	AI	Channel B Positive Input to 1.62 kΩ Gain Resistor Network.
J3	INB1-	AI	Channel B Negative Input to 1.62 kΩ Gain Resistor Network.
J4	INA2+	AI	Channel A Positive Input to 2.70 kΩ Gain Resistor Network.
J5	INA2-	AI	Channel A Negative Input to 2.70 kΩ Gain Resistor Network.
J6	INA1+	AI	Channel A Positive Input to 1.62 kΩ Gain Resistor Network.
J7	INA1-	AI	Channel A Negative Input to 1.62 kΩ Gain Resistor Network.

<sup>1</sup> AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = 5V$ ,  $IN\_LDO = EN\_LDO = 5V$ ,  $V_{CC} = V_{LOGIC} = 3.3V$ , Reference Voltage ( $V_{REF}$ ) = 3.3 V Internal,  $f_{SAMPLE} = 4$  MSPS, Fully-Differential Input Configuration, Full Power mode,  $T_A = 25^\circ C$ , oversampling disabled, unless otherwise noted.

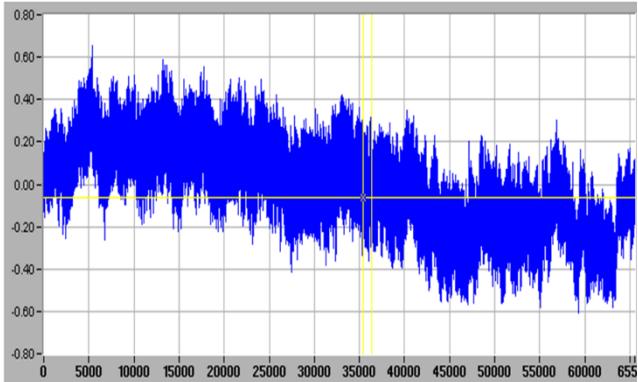


Figure 10. INL (LSB) vs. Code, Gain = 1.0

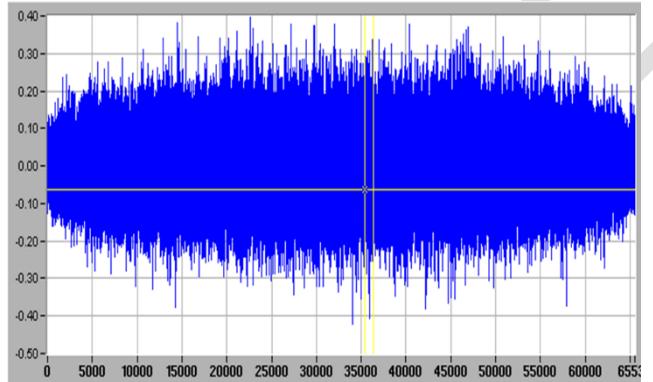


Figure 13. DNL (LSB) vs. Code, Gain = 1.0

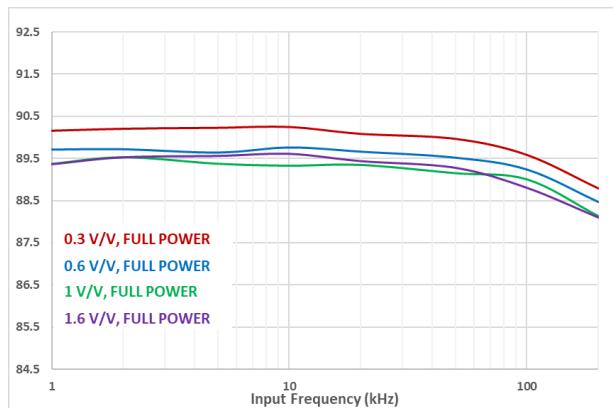


Figure 11. SNR vs.  $f_{IN}$  across gain modes

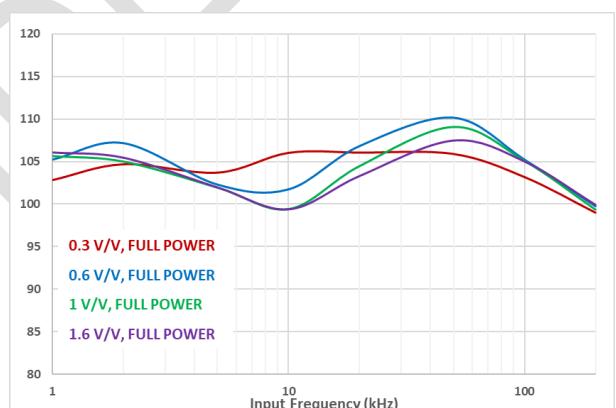


Figure 14 THD vs.  $f_{IN}$  across gain modes

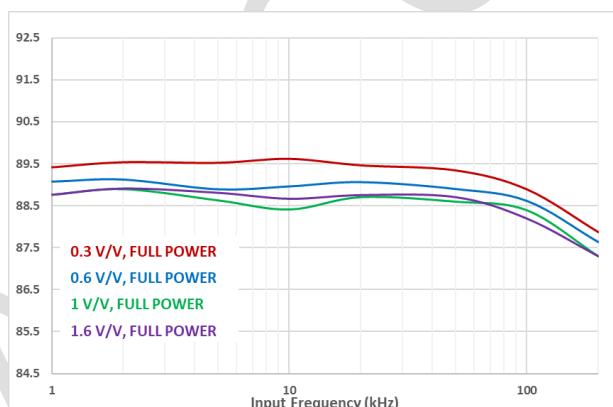


Figure 12. SINAD vs.  $f_{IN}$  across gain modes

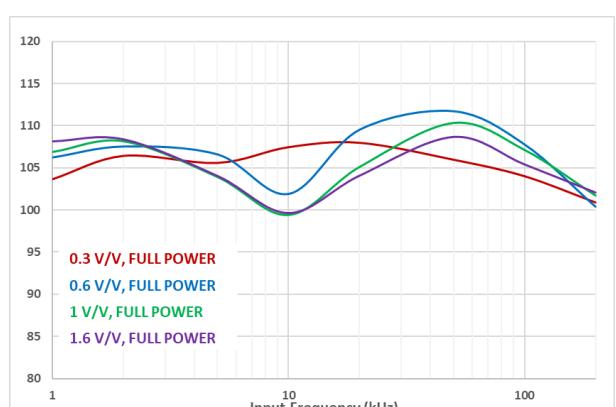
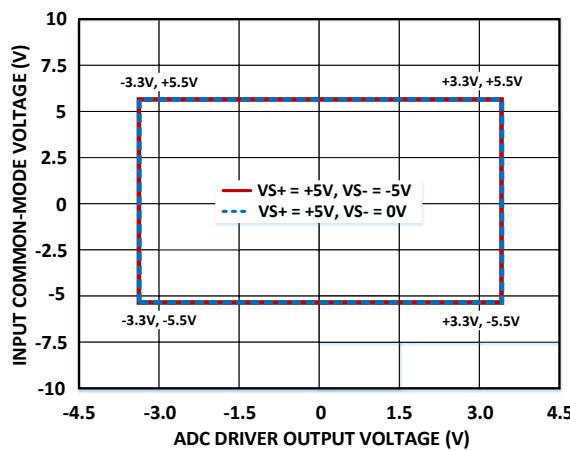
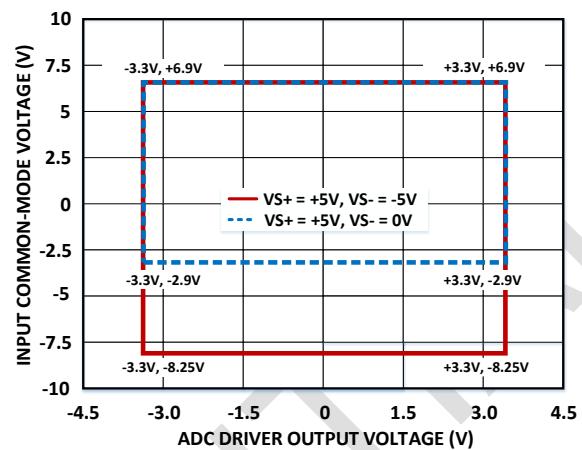
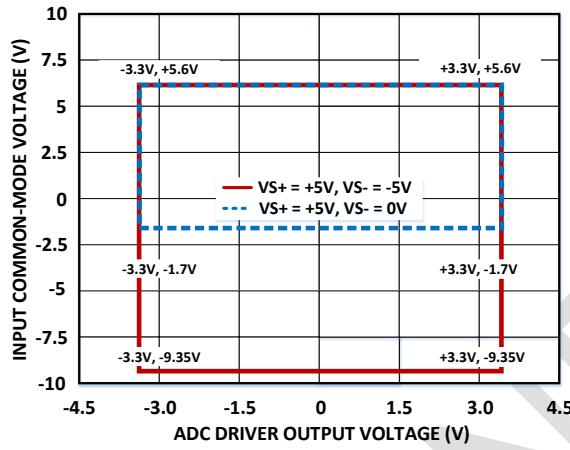
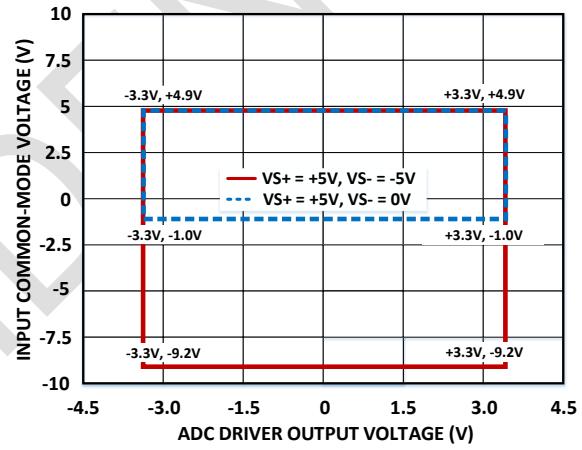


Figure 15. SFDR vs.  $f_{IN}$  across gain modes

Figure 16. Wide Input Common-Mode, Gain=0.3,  $\pm 11V$ Figure 18. Wide Input Common-Mode, Gain=0.6,  $\pm 5.5V$ Figure 17. Wide Input Common-Mode, Gain=1.0,  $\pm 3.3V$ Figure 19. Wide Input Common-Mode, Gain=1.6,  $\pm 2.0625V$

## TERMINOLOGY

### Differential Voltage

Differential voltage is the difference between two node voltages. For example, the differential input voltage (or equivalently, input differential mode voltage) is defined as

$$V_{IN, dm} = (V_{AINA+} - V_{AINA-})$$

where  $V_{AINA+}$  and  $V_{AINA-}$  refer to the voltages at the AINA+ and AINA- terminals with respect to a common reference.

### Common-Mode Voltage (CMV)

CMV is the average of two node voltages. The input common-mode voltage is defined as

$$V_{IN, cm} = (V_{AINA+} + V_{AINA-})/2$$

### Differential Nonlinearity (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

### Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs  $\frac{1}{2}$  LSB before the first code transition. Positive full scale is defined as a level  $1\frac{1}{2}$  LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

### Gain Error

The first transition (from 100 ... 000 to 100 ... 001) should occur at a level  $\frac{1}{2}$  LSB above nominal negative full scale. The last transition (from 011 ... 110 to 011 ... 111) occurs for an analog voltage  $1\frac{1}{2}$  LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

### Gain Error Drift

The gain error change due to a temperature change of  $1^{\circ}\text{C}$ .

### Gain Error Matching

Gain error matching is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

### Zero Error

Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

### Zero Error Drift

The zero-error change due to a temperature change of  $1^{\circ}\text{C}$ .

### Zero Error Matching

Zero error match is the difference in zero error between the input channels.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

### Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

### Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

### Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

### Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of IN+ and IN- of frequency, f.

$$\text{CMRR (dB)} = 10\log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:

$P_{ADC\_IN}$  is the common-mode power at the frequency, f, applied to the IN+ and IN- inputs.

$P_{ADC\_OUT}$  is the power at the frequency, f, in the ADC output.

### Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the  $\overline{CS}$  input and when the input signal is held for a conversion.

### Aperture Jitter

Aperture jitter is the variation in aperture delay.

## THEORY OF OPERATION

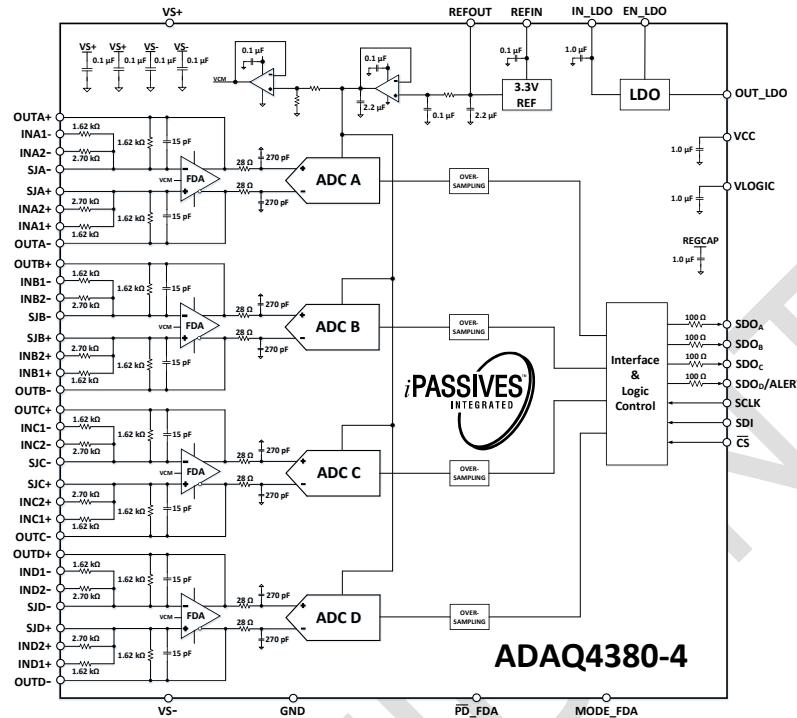


Figure 20. Simplified Block Diagram

## CIRCUIT INFORMATION

The ADAQ4380-4 μModule® system in package (SiP) is a fast, precise data acquisition (DAQ) signal chain that uses a simultaneous sampling SAR architecture. As shown in Figure 20, ADAQ4380-4 μModule® DAQ system is consist of a quad, 16-bit SAR ADC, high bandwidth, fully differential ADC driver, a precision low noise 3.3V reference, low noise and stable reference buffers, and a 3.4V low noise LDO, along with critical precision passive components required to achieve optimal performance with pin selectable gain options of 0.3, 0.6, 0.625, 1.0, and 1.6. All active components in the circuit, including *iPassives* thin film resistors with  $\pm 0.005\%$  matching, are designed by Analog Devices, Inc. and are factory calibrated to achieve a high degree of specified accuracy and minimize temperature dependent error sources.

The ADAQ4380-4 can simultaneously convert all the channels with a high throughput rate of 4 MSPS. The ADAQ4380-4 has an integrated on-chip oversampling blocks to further improve the dynamic range and reduce noise at lower bandwidths. See ADC Modes of Operation section for details. All the decoupling capacitors required by the ADC's voltage pins are all included internally. Any external capacitors won't be necessary.

## TRANSFER FUNCTIONS

ADAQ4380-4 uses a 3.3 V reference. The ADAQ4380-4 converts the differential voltage of the analog inputs (AINX+ and AINX-) into a digital output.

The conversion result is MSB first, two's complement. The LSB size is  $(2 \times VREF) / 2^N$ , where N is the ADC resolution. The ADC Resolution is determined by the resolution of the device chosen, and if Resolution Boost mode is enabled. Table 7 outlines the LSB size expressed in volts for different resolutions and reference voltages options.

The ideal transfer characteristic of the ADAQ4380-4 is shown in Figure 21.

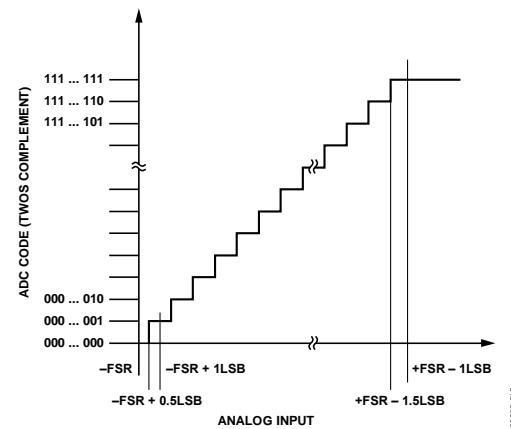


Figure 21. ADC Ideal Transfer Function (FSR Is Full-Scale Range)

Table 7. LSB Size

Resolution	2.5 V Reference	3.3 V Reference	Units
16-bit	76.3	100.7	μV
18-bit	19.1	25.2	μV

## APPLICATIONS INFORMATION

### TYPICAL APPLICATION DIAGRAMS

Figures 22 to 29 show the typical connections diagram for each channel of ADAQ4380-4 when applying differential, or single-ended input signals on four different gain combinations with varying common mode voltage.

The four differential channels of the ADAQ4380-4 can accept wide input voltage range and has a wide common-mode range that allows to convert a variety of signals. Differential and Common-mode Voltage ranges are highly dependent with the gain configuration per channel. Table 8 shows how the input signal should be applied for a given gain or input range option.

**Table 8. Gain Configurations and Input Range**

Gain	Input Range	Input Signal on Pins	Test Conditions
0.3	$\pm 11$	IN2+, IN2-	Connect IN1+ to OUT-, and IN1- to OUT+. See Figure 22 and Figure 27.
0.6	$\pm 5.5$	IN2+, IN2-	Leave IN1+, IN1-, OUT+ and OUT- floating. Figure 24 and Figure 28.
1.0	$\pm 3.3$	IN1+, IN1-	Leave IN2+, IN2-, OUT+ and OUT- floating. Figure 25 and Figure 29.
1.6	$\pm 2.06$	IN1+, IN1-, IN2+, IN2-	Connect IN1+ to IN2+, and IN1- to IN2-. Leave OUT+ and OUT- floating. See Figure 26 and Figure 30.

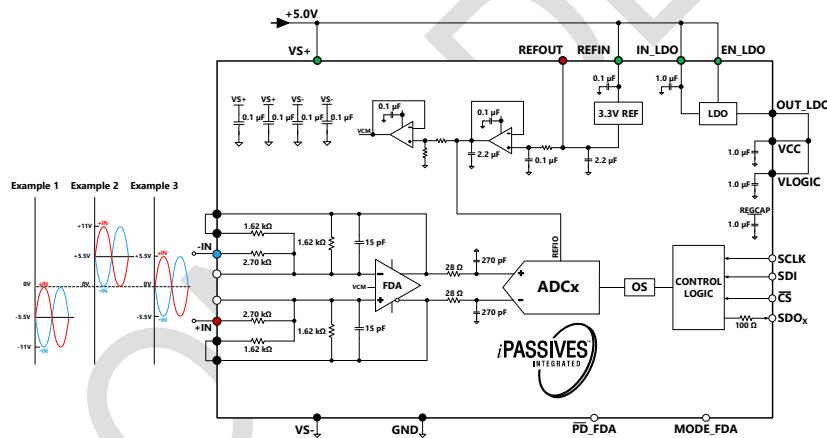


Figure 23. Fully Differential Input configuration with Gain=0.3,  $\pm 11$ V input.

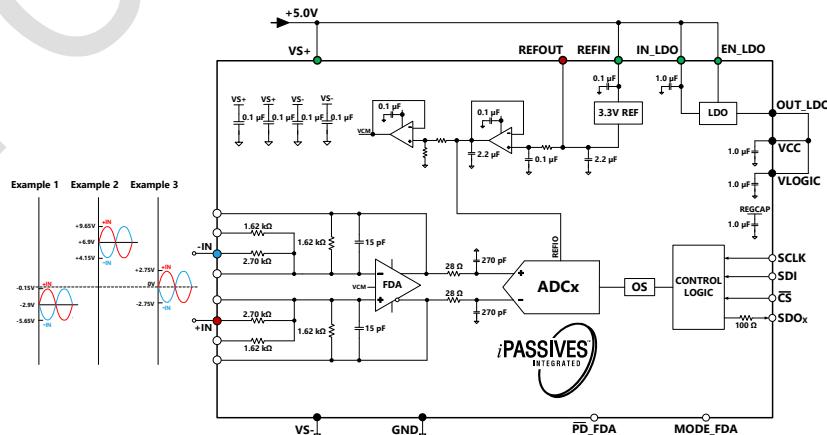
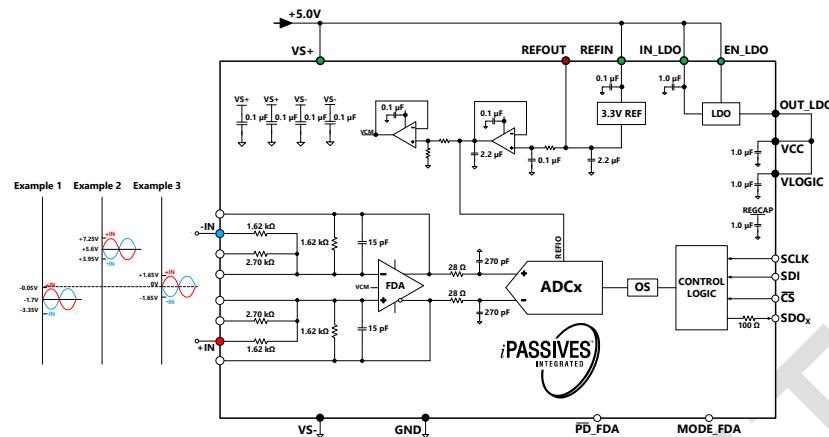
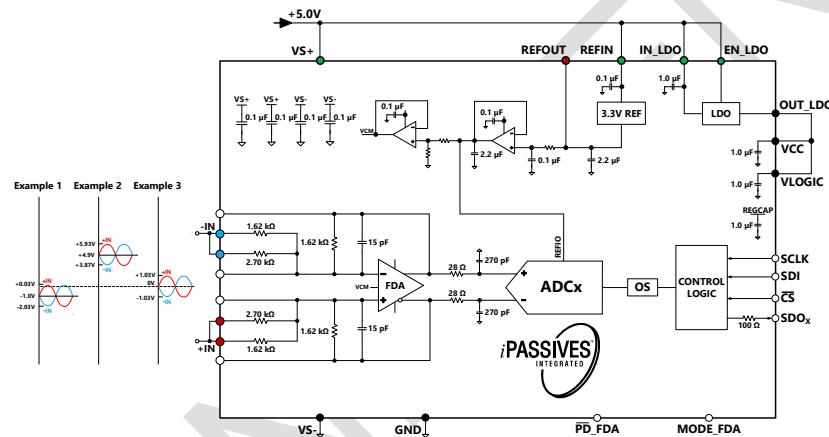
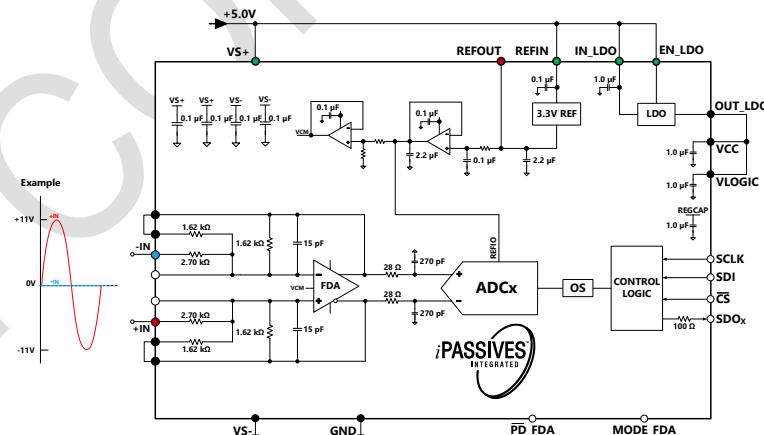


Figure 24. Fully Differential Input configuration with Gain=0.6,  $\pm 5.5$ V input.

Figure 25. Fully Differential Input configuration with Gain=1.0,  $\pm 3.3\text{V}$  input.Figure 26. Fully Differential Input configuration with Gain=1.6,  $\pm 2.06\text{V}$  input.Figure 27. Single-Ended to Differential Input configuration with Gain=0.3,  $\pm 11\text{V}$  input.

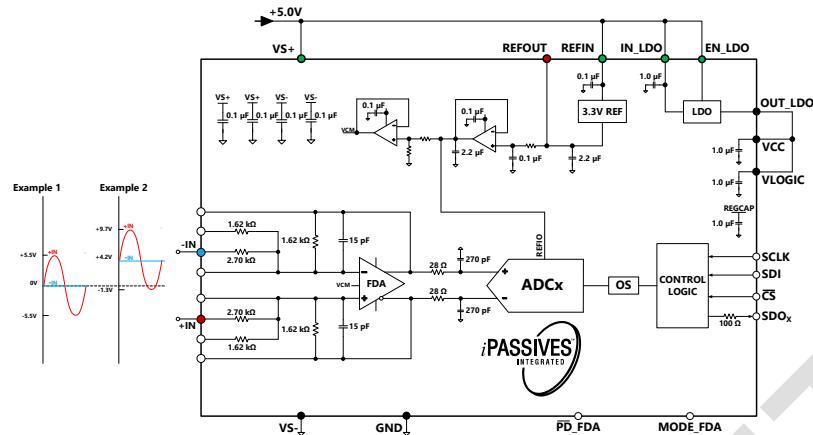


Figure 28. Single-Ended to Differential Input configuration with Gain=0.6,  $\pm 5.5\text{V}$  input.

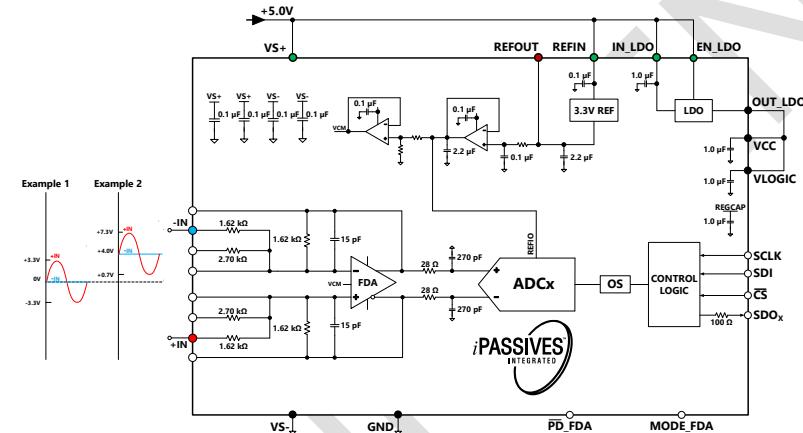


Figure 29. Single-Ended to Differential Input configuration with Gain=1.0,  $\pm 3.3\text{V}$  input.

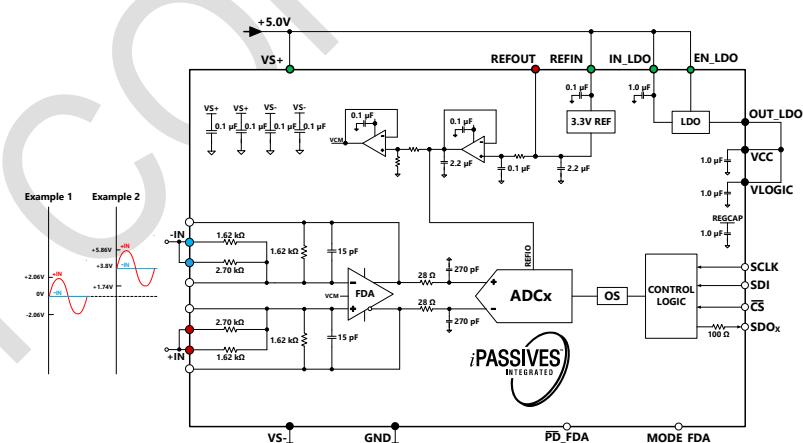


Figure 30. Single-Ended to Differential Input configuration with Gain=1.6,  $\pm 2.06\text{V}$  input.

## CALCULATING THE INPUT IMPEDANCE OF THE APPLICATION CIRCUIT

The effective input impedance depends on whether the signal source is single-ended or differential. For a balanced differential input signal, as shown in Figure 31, the input impedance ( $R_{IN}$ ) between the inputs (+IN and -IN) is  $R_{IN,dm} = 2 \times R_G$ .

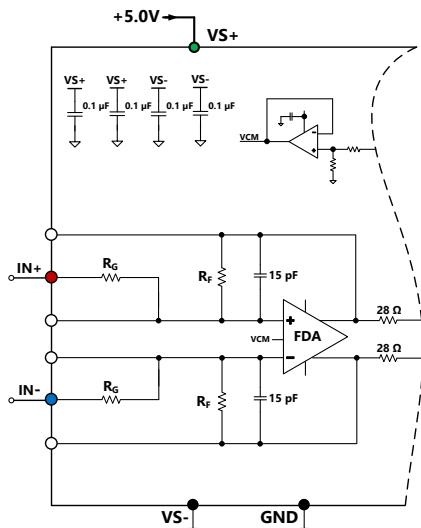


Figure 31. Fully Differential Input configuration

For a single-ended input signal, as shown in Figure 32, the input impedance is

$$R_{IN,SE} = \frac{R_G}{1 - \frac{R_F}{2(R_G + R_F)}}$$

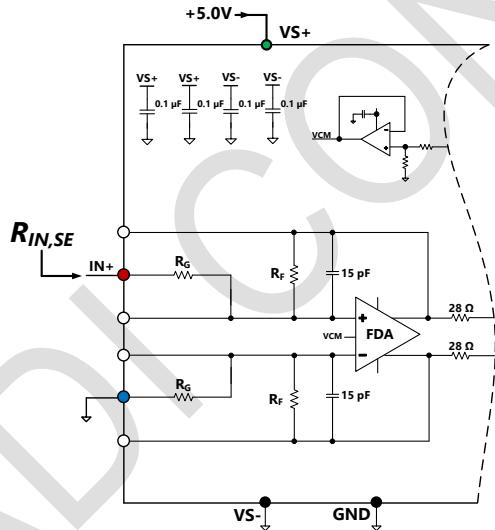


Figure 32. Single-Ended Input configuration

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the  $R_G$  input resistor.

## Terminating a Single-Ended Input

When the circuitry driving the inputs has a very low output impedance, there is no need for an additional termination on the +IN and -IN inputs of ADAQ4380-4. However, when there is a considerable amount of resistance from the driving circuitry, we recommend that a balancing network should be added on the inputs of ADAQ4380-4. Kindly refer to AN-1206 for techniques on how to properly terminate the inputs for a single-ended input operation.

## SNR ENHANCEMENT

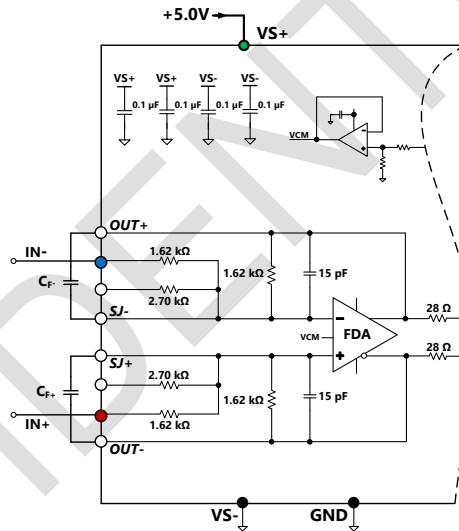


Figure 33. Connections with external feedback capacitance, configured with Gain = 1.0 V/V

ADAQ4380-4 has an integrated lowpass filter on its ADC Driver stage. The LPF has an effective -3dB cutoff frequency of 6.55 MHz when Gain is set to 0.3, and 3.27 MHz when Gain is 0.6, 1.0, or 1.6. In certain instances where the applications will only need to operate at lower frequencies, the user can tune the -3dB bandwidth with an external capacitor connected between IN- and OUT+, and IN+ and OUT-, as shown in Figure 33.

With an external feedback capacitor connected, the signal bandwidth will be limited to  $\frac{1}{2\pi * RF * (15pF + CF)}$ . Depending on the bandwidth of interest, user can install an external feedback capacitor in pF to nF range for tuning and to improve SNR performance of ADAQ4380. Figure 34 shows a range of possible CF values with corresponding SNR performance for ADAQ4380, when configured @ Gain=1. A capacitance range of 1 pF to 1 nF shows maximum attainable ADAQ4380 SNR performance.

Referring to Figure 34, connecting a 220 pF on the feedback will significantly reduce the bandwidth of ADAQ4380 to

$\frac{1}{2\pi * 1.62k\Omega * (15pF + 220pF)} = 411$  kHz. The equivalent noise bandwidth for this configuration is then 645 kHz. These changes will in effect improve the SNR of ADAQ4380-4, a 1.3

dB improvement for Full Power Mode, and 1.5 dB when in Low Power Mode.

Going beyond this range has little to no effect on the SNR of ADAQ4380-4. When this feature is employed, SNR is improved while preserving the THD performance. Thus, in effect enhances SINAD and ENOB.

Figure 35 shows the effective -3dB bandwidth versus the range of feedback capacitance values. This improvement in SNR will vary depending on the gain setting of ADAQ4380. Table 9 details the ADC Driver's noise performance across gains.

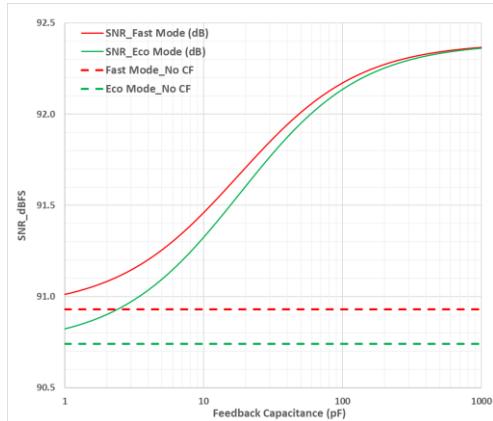


Figure 34. SNR Enhancement vs. External Feedback Capacitance

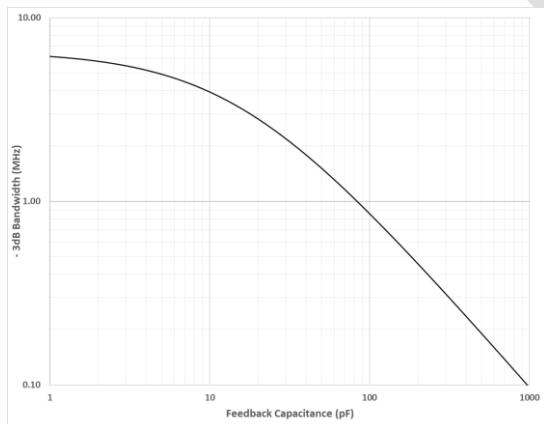


Figure 35. -3 dB Bandwidth vs External Feedback Capacitance

Table 9. ADC Driver Noise vs Gain

Gain (V/V)	R <sub>F</sub> (Ω)	V <sub>n</sub> Fast Mode (nV/√Hz)	V <sub>n</sub> Eco Mode (nV/√Hz)
0.3	810	6.36	7.03
0.6	1620	9.82	10.39
1.0	1620	11.04	11.90
1.6	1620	12.73	14.05

Without an external capacitance, the amount broadband noise shown in Table 9 is passed through the system and can only be filtered out by the LPF cutoff. The external feedback capacitor ensures that the effects of these noise artifacts are limited to

improve the noise performance of ADAQ4380. Equations 1 and 2 shows the effective noise and SNR when this technique is implemented.

$$en_0 = V_n * \sqrt{1.57 * \frac{1}{2\pi * RF * (15pF + CF)}} \quad (1)$$

$$SNR_{dBFS} = 20\log \frac{\frac{V_{REF}}{\sqrt{2}}}{(en_0)^2 + (56.6 \mu V)^2} \quad (2)$$

## POWER SUPPLY AND DECOUPLING

The ADAQ4380-4 has six independent power supplies, Vs+, and Vs-, REFIN, IN\_LDO, V<sub>CC</sub>, and V<sub>LOGIC</sub> that supply the analog circuitries and digital interface, respectively. Refer to **Table 6** for the detailed description of each supply pins. The ADAQ4380-4 is guaranteed to achieve its optimum performance at single, 5V supply operation. Decoupling these supply pins may not be necessary since decoupling capacitors are already integrated in ADAQ4380-4 internal circuitry. Additionally, ADAQ4380-4 features an internal reference buffer decoupled to ground. There's no need to add external decoupling caps on the REFOUT pin.

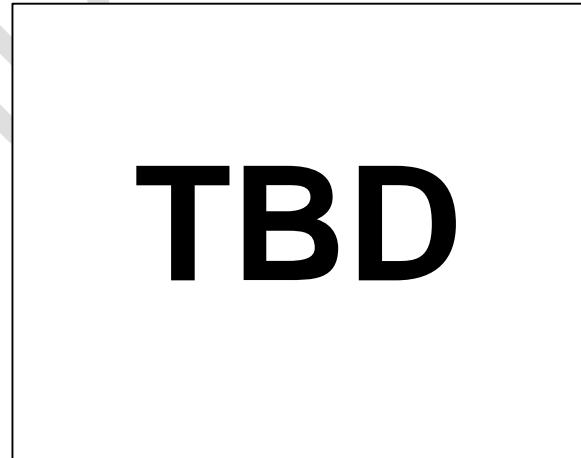


Figure 36.

### Power-up

The ADAQ4380-4 is robust to power supply sequencing. VCC and VLOGIC can be applied in any sequence.

The ADAQ4380-4 require a t<sub>POWER-UP</sub> time from applying VCC and VLOGIC until the ADC conversion results are stable. See Figure 4 for the recommended signal condition during power-up. It is recommended to pull the CS pin high during power-up and have a software reset after the power-up. Conversion results are not guaranteed to meet data sheet specifications during this time and must be ignored.

## ADC MODES OF OPERATION

The ADAQ4380-4 have several on-chip configuration registers for controlling the operational mode of the device.

### OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC) of the ADC. The ADAQ4380-4 offer an oversampling function on-chip and have two user configurable oversampling modes, normal averaging and rolling average. The oversampling functionality is configured by programming the OS\_MODE bit and OSR [2:0] bits in the CONFIGURATION1 register. See the Resolution Boost section for further details.

#### Normal Averaging Oversampling

Normal oversampling mode can be used in applications where slower output data rates are allowable and where higher SNR or dynamic range is desirable. Normal averaging involves taking a number of samples, adding the samples together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is cleared after the process is completed.

Normal oversampling mode is configured by setting the OS\_MODE bit to Logic 0 and having a valid nonzero value in the OSR [2:0] bits. Writing to the OSR [2:0] bits has a two-cycle

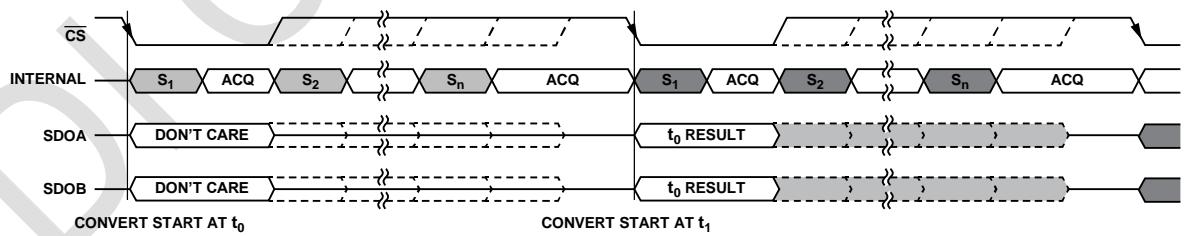
latency before the register gets updated. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR [2:0], which provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution for the ADAQ4380-4. If additional resolution is required, this can be achieved by configuring the resolution boost bit in the CONFIGURATION1 register. See the Resolution Boost section for further details.

The number of samples, n, defined by the OSR [2:0] bits are taken, added together, and the result is divided by n. The initial ADC conversion is initiated by the falling edge of CS, and the ADAQ4380-4 control all subsequent samples in the oversampling sequence internally. The sampling rate of the additional n samples is at 3 MSPS for the ADAQ4380-4 in oversampling mode. The oversampled conversion result is ready for read back on the next serial interface access. After the technique is applied, the sample data used in the calculation is discarded. This process is repeated every time the application needs a new conversion result and initiates by the falling edge of CS.

As the output data rate is reduced by the oversampling ratio, the SPI SCLK frequency required to transmit the data is also reduced accordingly.

**Table 10. ADAQ4380-4, G=1 Normal Averaging Oversampling Performance Overview**

OSR [2:0]	OS Ratio	SNR (dB typical) $V_{REF} = 3.3\text{ V}$ Internal		Data Output Rate (kSPS max)
		RES = 0	RES = 1	
000	No OS	91.1	91.1	4000
001	2	92.8	94.0	1500
010	4	94.3	96.9	750
011	8	95.4	99.1	375
100	16	TBD	TBD	187.5



*Figure 37. Normal Averaging Oversampling Operation*

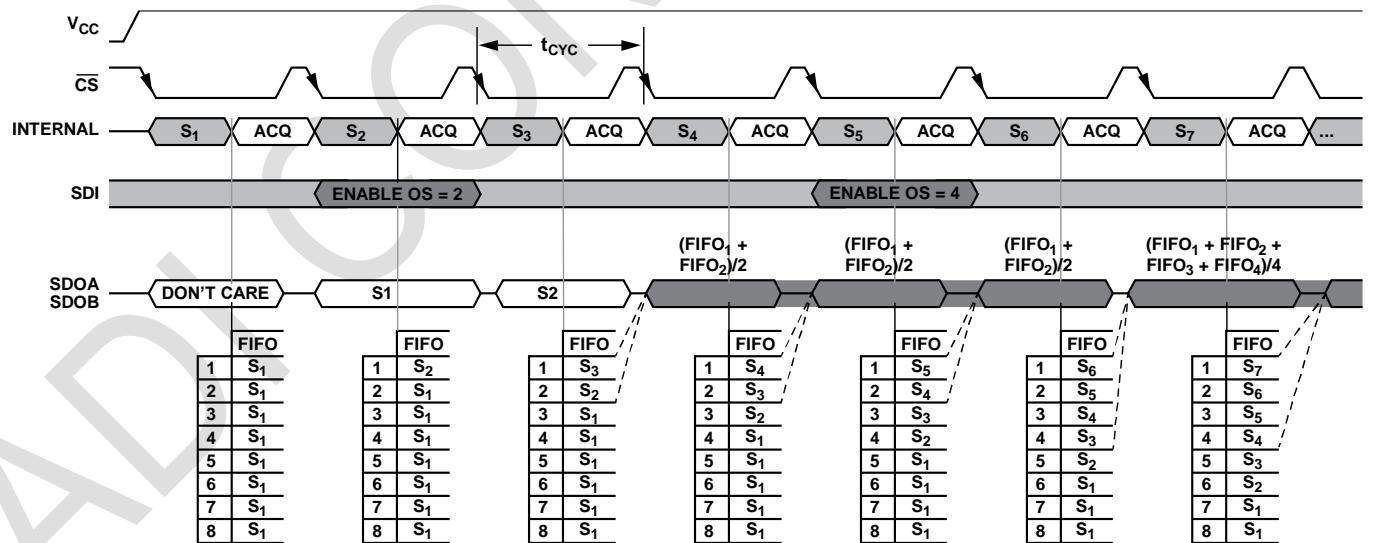
### **Rolling Average Oversampling**

Rolling oversampling mode can be used in applications where higher output data rates are required and where higher signal-to-noise ratio or dynamic range is desirable. Rolling averaging involves taking a number of samples, adding them together and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared once the process is completed. The rolling oversampling mode uses a FIFO buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

Rolling oversampling mode is configured by setting the OS\_MODE bit to logic 1 and having a valid nonzero value in the OSR [2:0] bits. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR [2:0] (see Table 11). Table 11 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution for the ADAQ4380-4. If additional resolution is required this can be achieved by configuring the resolution boost bit in the CONFIGURATION1. See Resolution Boost section for further details.

**Table 11. ADAQ4380-4, G = 1 Rolling Average Oversampling Performance Overview**

OSR [2:0]	OS Ratio	SNR (dB typical) $V_{REF} = 3.3\text{ V Internal}$		Data Output Rate (kSPS max)
		RES = 0	RES = 1	
000	No OS	91.1	91.1	4000
001	2	91.9	92.8	4000
010	4	93.7	96.0	4000
011	8	95.2	98.5	4000



**Figure 38. Rolling Average Oversampling Mode Configuration**

## RESOLUTION BOOST

The default resolution and output data size for the ADAQ4380-4 is 16-bits. When the on-chip oversampling function is enabled the performance of the ADC can exceed the default resolution. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution. If the RES bit in the CONFIGURATION1 is set to logic 1 and the ADAQ4380-4 is in a valid oversampling mode, the conversion result size for the ADAQ4380-4 is 18-bit. In this mode, 18 SCLKs are required to propagate the data for the ADAQ4380-4.

## ALERT

The alert functionality is an out-of-range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the value in the conversion result register exceeds the alert high limit value in the Alert High Threshold Register or falls below the alert low limit value in the Alert Low Threshold Register. The Alert High Threshold Register and the Alert Low Threshold Register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the ALERT register.

The register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the ALERT function of the ALERT/SDOD pin. The ALERT/SDOD pin is configured as ALERT by configuring the following bits in the CONFIGURATION1 and the CONFIGURATION2:

- Set the SDO [1:0] bits to any value other than 0b00.
- Set the ALERTEN bit to 1.
- Set a valid value to the Alert High Threshold Register and the Alert Low Threshold Register.

The alert indication function is available in oversampling, both rolling average and normal averaging and in non-oversampling modes.

The alert function of the SDOB/ALERT pin gets updated at the end of conversion. The alert indication status bits in the ALERT register get updated as well and must be read before the end of next conversion.

The alert indication bits in the Alert Indication Register are cleared by reading the alert register contents. The alert function of the ALERT/SDOD pin is cleared with a falling edge of CS. Issuing a software reset also clears the alert status in the Alert Indication Register.

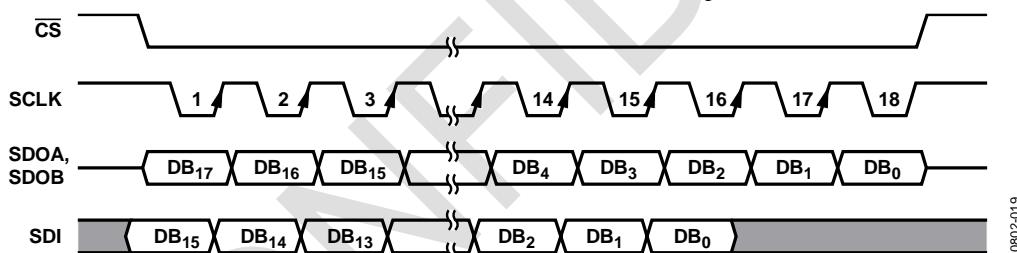


Figure 39. Resolution Boost

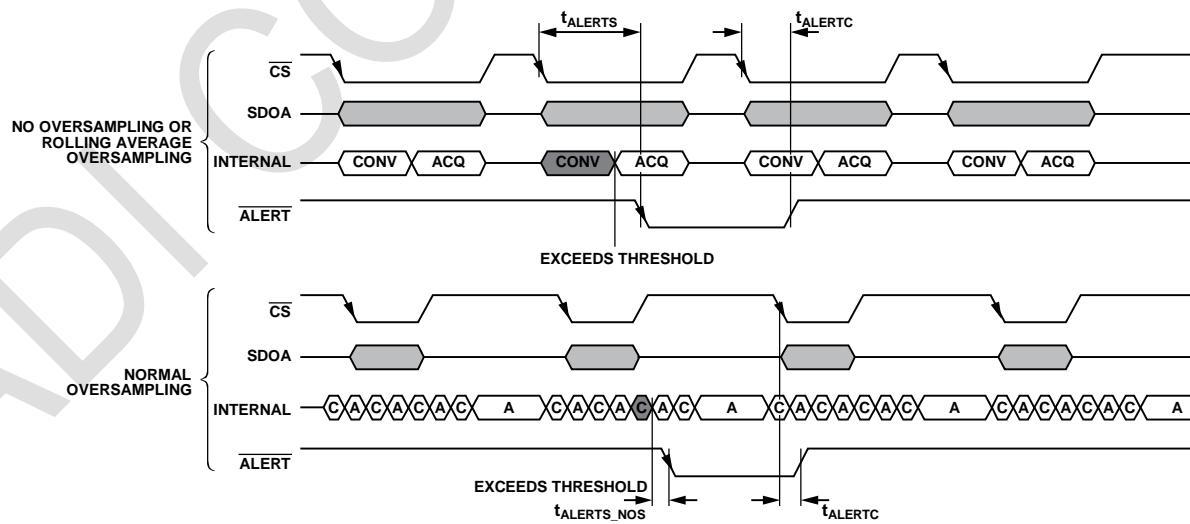


Figure 40. Alert Operation

## POWER MODES

The ADAQ4380-4's ADC Core has two power modes, Normal Mode and Shutdown Mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the CONFIGURATION1 to configure the power modes in the ADAQ4380-4. Set PMODE to logic 0 for normal mode and logic 1 for shutdown mode.

### NORMAL MODE

Keep the ADAQ4380-4 in normal mode to achieve the fastest throughput rate. All ADC blocks within the ADAQ4380-4 always remain fully powered and an ADC conversion can be initiated by a falling edge of  $\overline{CS}$  when required. When the ADAQ4380-4 is not converting it is in static mode and power consumption is automatically reduced. Additional current is required to perform a conversion. Therefore, power consumption of the ADAQ4380-4 scales with throughput.

### SHUTDOWN MODE

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the ADAQ4380-4 is in shutdown mode, all of the ADC's analog circuitry powers down. The serial interface remains active during shutdown mode to allow the ADAQ4380-4 to exit shutdown mode.

To enter shutdown mode, write to the power mode configuration bit, PMODE, in the CONFIGURATION1.

The ADAQ4380-4 will shut down and current consumption will reduce. To exit shutdown mode and return to normal mode set the PMODE bit in the CONFIGURATION1 to logic 0. All register configuration settings remain unchanged entering or leaving shutdown mode. After exiting shutdown mode sufficient time has to be allowed for the circuitry to turn on before starting a conversion.

### INTERNAL AND EXTERNAL REFERENCE

The ADAQ4380-4 have a 3.3 V internal reference voltage. Alternatively, if a more accurate reference is preferred, an external reference voltage should be supplied to the REFOUT pin. This pin can accept a voltage ranging from 2.5 V to 3.3 V, however it is recommended to use a 3.3V precision reference.

### SOFTWARE RESET

The ADAQ4380-4 has two reset modes, a soft reset and a hard reset. A reset is initiated by writing to the RESET [7:0] bits in the CONFIGURATION2.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The  $\overline{\text{ALERT}}$  register is cleared. The reference and LDO remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, resets the reference buffer, and resets the internal oscillator block.

### DIAGNOSTIC SELF-TEST

The ADAQ4380-4 run a diagnostic self-test after a power-on reset (POR) or after a software hard reset to ensure correct configuration is loaded into the device.

The result of the self-test is displayed in the SETUP\_F bit in the Alert Indication Register. If the SETUP\_F bit is set to logic 1, the diagnostic self-test has failed. If the test fails, perform a software hard reset to reset the ADAQ4380-4 registers to the default status.

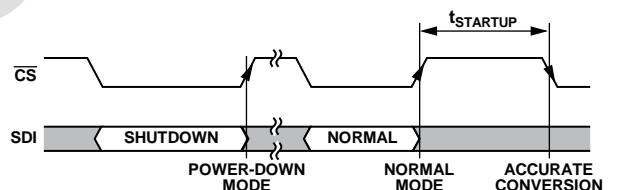


Figure 41. Shutdown Mode Operation

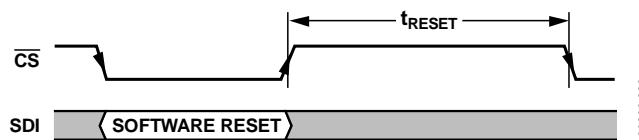


Figure 42. Software Reset Operation

## INTERFACE

The interface to the ADAQ4380-4 is via a serial interface. The interface consists of a  $\overline{\text{CS}}$ , SCLK, SDOA, SDOB, SDOC and SDOD and SDI pins.

The CS signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of  $\overline{\text{CS}}$  puts the track-and-hold into hold mode at which point the analog input is sampled and the bus is taken out of three-state. The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, SDOC, SDOD and SDI signals. A minimum of 16 SCLKs are required for a write to or read from a register. The minimum numbers of SCLKs for a conversion read is dependent on the resolution of the device and the configuration settings, see Table 12.

The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The ADAQ4380-4 has four serial output signals, SDOA, SDOB, SDOC and SDOD. Programming the SDO [1:0] bits in the CONFIGURATION2 configures 2-wire, 1-wire or 4-wire mode. To achieve the highest throughput of the device it is required to use either the, 2-wire or 4-wire mode, to read conversion results. If a reduced throughput is required or oversampling is used it is possible to use 1-wire mode, SDOA signal only, for reading conversion results.

Configuring CRC operation for SPI reads, SPI writes and oversampling mode with resolution boost mode enabled will alter the operation of the interface. The relevant sections of this data sheet should be consulted to ensure correct operation.

## READING CONVERSION RESULTS

The  $\overline{\text{CS}}$  signal initiates the conversion process. A high to low transition on the  $\overline{\text{CS}}$  signal initiates a simultaneous conversion of the four ADCs, ADC A, ADC B, ADC C and ADC D. The ADAQ4380-4 has a one cycle read back latency. Therefore, the conversion results are available on the next SPI access. Then, take the  $\overline{\text{CS}}$  signal low, and the conversion result clocks out on

the serial output pins. The next conversion is also initiated at this point.

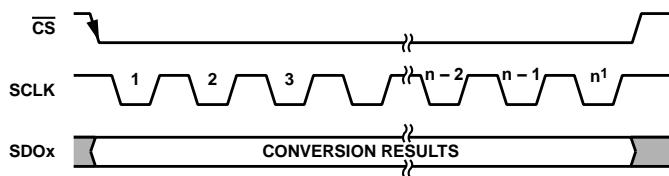
The conversion result is shifted out of the device as a 16-bit result for the ADAQ4380-4. The MSB of the conversion result is shifted out on the CS falling edge. The remaining data is shifted out of the device under the control of the serial clock (SCLK) input. The data is shifted out on the rising edge of SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take  $\overline{\text{CS}}$  high again to return the SDOx pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the SDOx pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled, see Figure 43 and Table 12 for details. If CRC on reading is enabled this will require additional SCLK pulse to propagate the CRC information, see the CRC Section for more details.

As the  $\overline{\text{CS}}$  signal initiates a conversion as well as framing the data any data access must be completed within a single frame.

**Table 12. Number of SCLKs (n) required for reading conversion results**

Interface Configuration	Resolution Boost Mode	CRC Read	No. of SCLK Cycles
4-Wire	Disabled	Disabled	16
	Enabled	Enabled	24
	Disabled	Disabled	18
	Enabled	Enabled	26
2-Wire	Disabled	Disabled	32
	Enabled	Enabled	40
	Disabled	Disabled	36
	Enabled	Enabled	44
1-Wire	Disabled	Disabled	64
	Enabled	Enabled	72
	Disabled	Disabled	72
	Enabled	Enabled	80



<sup>1</sup>CONSULT TABLE 12 FOR VALUES FOR n, THE NUMBER OF SCLK PULSES REQUIRED.

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Figure 43. Reading Conversion Result

### Serial 4-Wire Mode

Configure 4-wire mode by setting the SDO [1:0] bits in the CONFIGURATION2 to 0b10. In 4-wire mode the conversion results for ADC A is output on the SDOA pin. ADC B on the SDOb pin, ADC C on the SDOC pin and ADC D on the SDOD pin.

### Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO [1:0] bits in the CONFIGURATION2 to 0b00. In 2-wire mode the conversion results for ADC A and ADC C are output on the SDOA pin. The conversion result for ADC B and ADC D are output on the SDOb pin.

### Serial 1-Wire Mode

In applications where slower throughput rates are allowed or normal averaging oversampling is used the serial interface can be configured to operate in 1-wire mode. In 1-wire mode the conversion results from ADC A, ADC B, ADC C and ADC D are output on serial output SDOA. Additional SCLK cycles are required to propagate all the data. ADC A data is output first followed by ADC B, ADC C and ADC D conversion results.

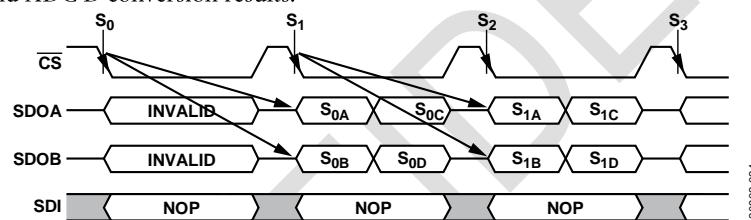


Figure 44. Read Conversion Results - 4 Wire Mode

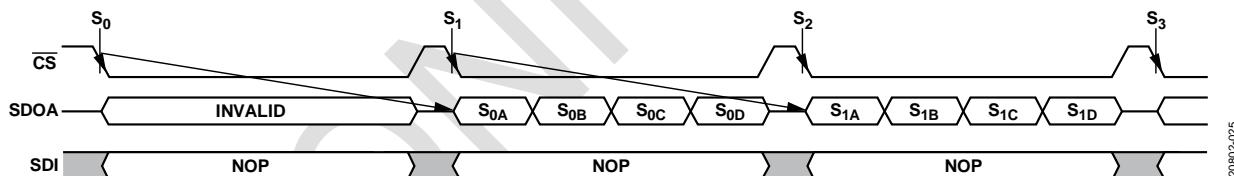


Figure 45. Reading Conversion Results - 2-wire Mode

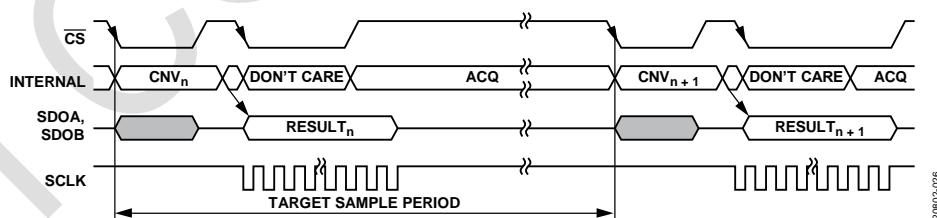


Figure 46. Read Conversion Results - 1 Wire Mode

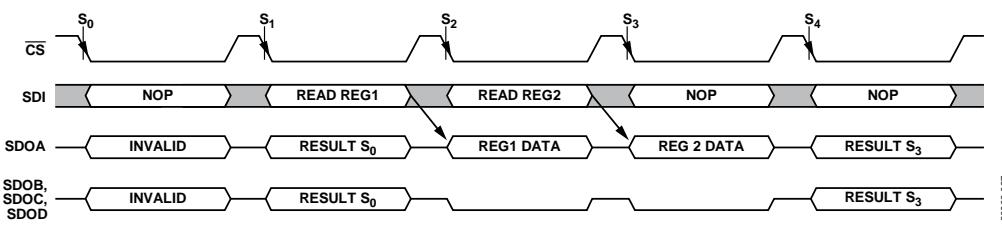


Figure 47. Low Throughput Low Latency

## WRITING TO DEVICE REGISTERS

All the read/write registers in the ADAQ4380-4 can be written to over the serial interface. The length of a SPI write access is determined by the CRC write function. An SPI access is 16-bit if CRC write is disabled and 24-bit when CRC write is enabled. The format for a write command is shown in Table 15. Bit D15 must be set to 1 to select a write command. Bits [D14:D12] contain the register address. The subsequent twelve bits, Bits [D11:D0], contain the data to be written to the selected register.

### CRC

The ADAQ4380-4 has cyclic redundancy check (CRC) checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI interface reads and

SPI interface writes. For example, you can enable the CRC function for SPI writes to prevent unexpected changes to the device configuration but not enable it on SPI reads thus maintaining a higher throughput rate. The CRC feature is controlled by programming of the CRC\_W bit and CRC\_R bit in the CONFIGURATION1 register.

#### **CRC Read**

If enabled, a CRC is appended to the conversion result or register reads and consists of an 8-bit word. The CRC is calculated on the conversion result for ADC A, ADC B, ADC C and ADC D and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, 4-wire SPI mode and resolution boost mode.

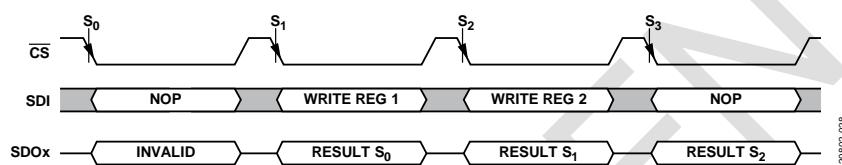


Figure 48. Register Read

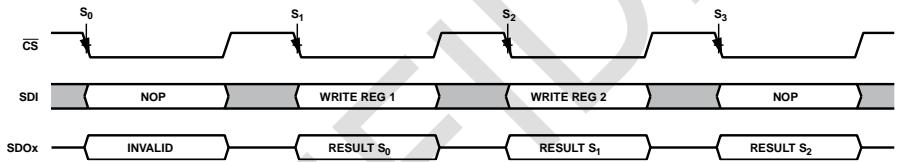


Figure 49. Register Write

### CRC Write

To enable the CRC write function the CRC\_W bit in the . Must be set to 1. To set the CRC\_W bit to 1 to enable the CRC feature the request frame must have a valid CRC appended to it. Once enabled all register write requests are ignored unless they are accompanied by a valid CRC command. It therefore requires a valid CRC to both enable and disable the CRC write feature.

#### **CRC Polynomial**

For CRC checksum calculations, the polynomial  $x^8 + x^2 + x + 1$  is always used.

To generate the checksum, the 16-bit data conversion result of the four channels are combined to produce a 64-bit data stream. The 8 MSBs of the 64-bit data are inverted and then the data is appended by eight bits to create a number ending in

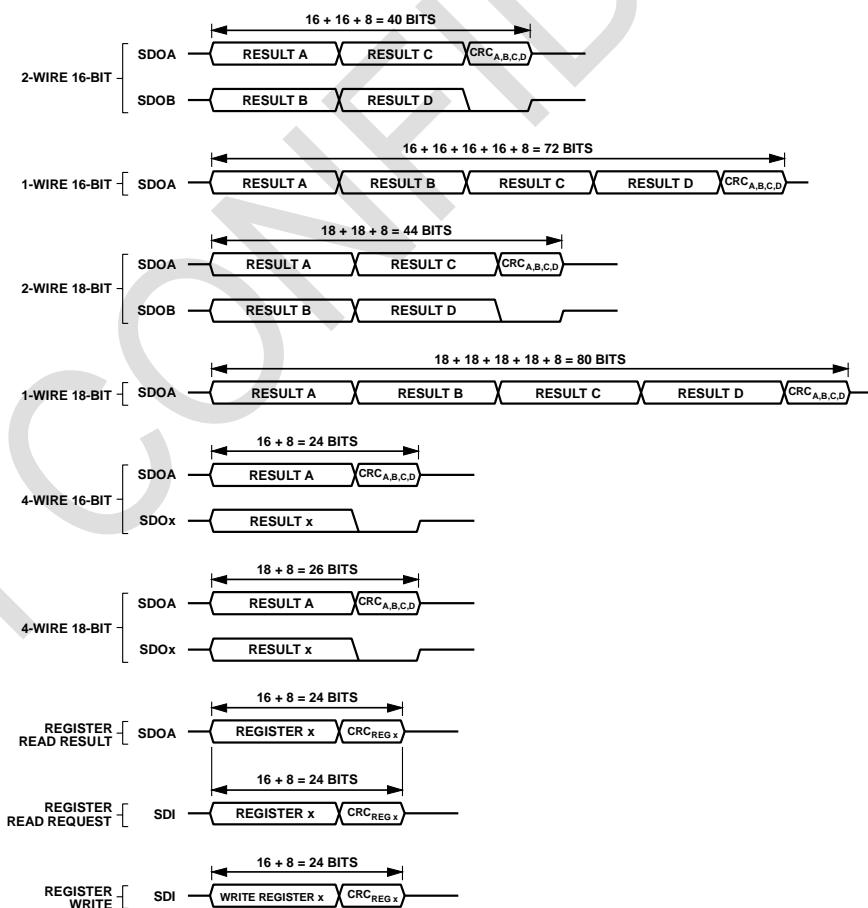
eight logic 0s. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

For example, our polynomial is 100000111. Let the original data of four channels be 0xAAAA, 0x5555, 0xAAAA and 0x5555. The 8 MSBs of the data are inverted. The data is then appended to include eight 0's on right. In the final XOR operation, the reduced data is less than the polynomial. Hence, the remainder is the CRC for the assumed data.

Table 13. Example CRC Calculation for 4-Channel, 16-Bit Data

Data	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	X <sup>1</sup>						
Process	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0
Data	1	0	0	0	0	0	1	1	1																				
	1	0	1	0	0	0	0	1	1	0																			
	1	0	0	0	0	0	1	1	1																				
CRC																													

<sup>1</sup> X means don't care.



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Figure 50. CRC Operation

## REGISTERS

The ADAQ4380-4 has user programmable on-chip registers for configuring the device. Table 14 shows a complete overview of the registers available on the ADAQ4380-4.

The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored. Any write to a read only register is ignored. Writes to the NOP registers and the reserved register are ignored. Any read request to the NOP registers or reserved registers are considered a no operation and the data transmitted in the next SPI frame are the conversion results.

**Table 14. Register Description**

Reg	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Default	R/W
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0x1	Configuration 1	[15:8]	WR	ADDRESSING			RESERVED		OS_MODE	OSR, Bit 2	0x0000	R/W
		[7:0]	OSR, Bits[1:0]		CRC_W	CRC_R	ALERTEN	RES	RESERVED	PMODE		
0x2	Configuration 2	[15:8]	WR	ADDRESSING			RESERVED		SDO, Bits[1:0]		0x0000	R/W
		[7:0]	RESET, Bits[7:0]									
0x3	Alert	[15:8]	WR	ADDRESSING			RESERVED		CRCW_F	SETUP_F	0x0000	R
		[7:0]	AI_D_HI G H W	AI_D_LO W	AI_C_HI G H W	AI_C_LO W	AI_B_HI G H W	AI_B_LO W	AI_A_HI G H W	AI_A_LO W		
0x4	Alert Low threshold	[15:8]	WR	ADDRESSING			ALERT_LOW, Bits[11:8]				0x0800	R
		[7:0]	ALERT_LOW, Bits[7:0]									
0x5	Alert high threshold	[15:8]	WR	ADDRESSING			ALERT_HIGH, Bits[11:8]				0x07FF	RW
		[7:0]	ALERT_HIGH, Bits[7:0]									

## ADDRESSING REGISTERS

A serial register transfer on the ADAQ4380-4 consists of 16 SCLK cycles. The 4 MSBs written to the device are decoded to determine which register is addressed. The 4 MSBs consist of the register address (REGADDR) Bits[2:0] and the read/write bit (WR). The register address bits determine which on-chip register is selected. The read/write bit determines if the remaining 12 bits of data on the SDI input are loaded into the addressed register if the addressed register is a valid write register. If the read/write bit is 1, the bits load into the register addressed by the register select bits. If the read/write bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

**Table 15. Addressing Register Format**

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REG ADDR[2:0]														

**Table 16. Bit Descriptions for Addressing Registers**

Bit	Mnemonic	Description
D15	WR	If a 1 is written to this bit then bits [11:0] of this register are written to the register specified by REGADDR[2:0] if it is a valid address. Alternatively, if a 0 is written the next data sent out on the SDO pin is a read from the designated register if it is a valid address.
D14 to D12	REGADDR[2:0]	When WR = 1, the contents of REGADDR[2:0]determine register for selection as outlined in Table 14. When WR = 0, and REGADDR[2:0]contains a valid register address the contents on the requested register are output on the SDOA pin during the next interface access. When WR = 0, and REGADDR[2:0]contains 0x0, 0x6 or 0x7 the contents on the SDI line are ignored. The next interface access will result in the conversion results being read back.
D11 to D0	DATA[11:0]	These bits are written into the corresponding register specified by bits REGADDR[2:0] when the WR bit is equal to 1 and the REGADDR[2:0] bit contain a valid address

## CONFIGURATION1 REGISTER

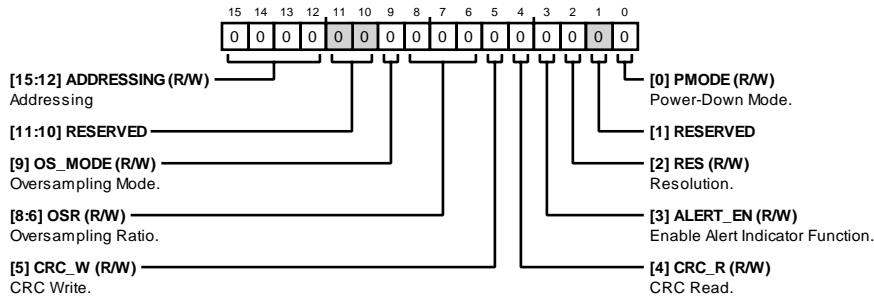


Table 17. Bit Descriptions for Error! Reference source not found.

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits [15:12] define the address of the relevant register. See the Addressing Registers Section for further details.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	OS_MODE	Oversampling Mode. Sets the oversampling mode of the ADC. 0: normal average. 1: rolling average.	0x0	R/W
[8:6]	OSR	Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the relevant mode. Normal averaging mode supports oversampling ratios of x2, x4, x8, x16, and x32. Rolling average mode supports oversampling ratios of x2, x4, and x8. 000: disabled. 001: 2X. 010: 4X. 011: 8X. 100: 16X. 101: 32X. 110: disabled. 111: disabled.	0x0	R/W
5	CRC_W	CRC Write. Controls the CRC functionality for the SDI interface When setting this bit from a 0 to a 1 the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received the entire frame is ignored. If the bit is set to 1 it requires a CRC to clear it to 0. 0: no CRC function. 1: CRC function.	0x0	R/W
4	CRC_R	CRC Read. Controls the CRC functionality for the SDOx interface 0: no CRC function. 1: CRC function.	0x0	R/W
3	ALERT_EN	Enable Alert Indicator Function. This register function when SDO = 1 otherwise the ALERTEN bit is ignored. 0: SDOB. 1: ALERT.	0x0	R/W
2	RES	Resolution. Sets the size of the conversion result data. If OSR = 0 these bits are ignored and the resolution is set to default resolution. 0: normal resolution. 1: 2-bit higher resolution.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	PMODE	Power-Down Mode. Sets the power modes 0: Normal Mode. 1: power down mode.	0x0	R/W

## CONFIGURATION2 REGISTER

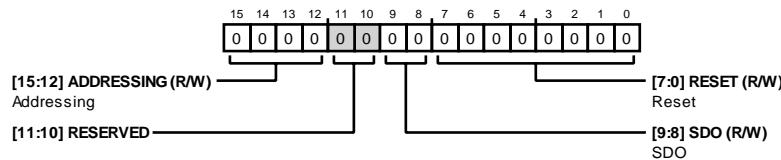


Table 18. Bit Descriptions for Error! Reference source not found.

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits [15:12] define the address of the relevant register. See the Addressing Registers Section for further details.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
[9:8]	SDO	SDO. Conversion Results Serial Data Output 00: Two Wire - Conversion Data are output on both SDOA and SDOB. 01: One Wire - Conversion Data are output on SDOA only. 10: Four Wire - Conversion data are output on SDOA, SDOB, SDOC, and SDOD/ALERT. 11: One Wire - Conversion Data are output on SDOA only.	0x0	R/W
[7:0]	RESET	Reset. 0x3C: Performs a soft reset. Refreshes some blocks, Register contents remain unchanged. (Clears ALERT register and flushes any oversampling stored variables or active state machine) 0xFF: Performs a hard reset. Resets all possible blocks in the device. Registers contents are set to defaults All other values are ignored.	0x0	R/W

## ALERT INDICATION REGISTER

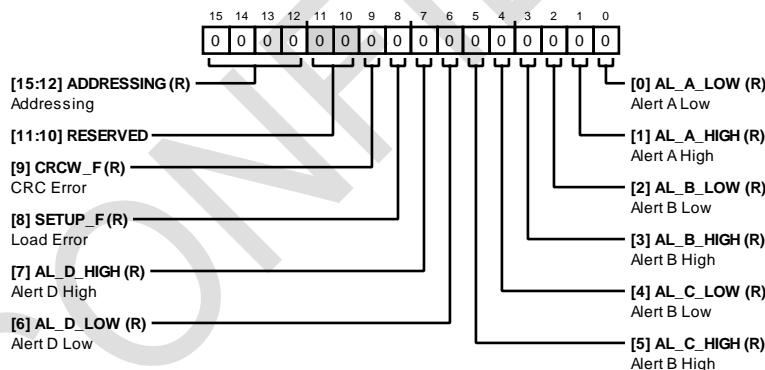


Table 19. Bit Descriptions for Alert Indication Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits [15:12] define the address of the relevant register. See the Addressing Registers Section for further details.	0x0	R
[11:10]	RESERVED	Reserved.	0x0	R
9	CRCW_F	CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read 0: No CRC Error. 1: CRC Error.	0x0	R
8	SETUP_F	Load Error. The SETUP_F indicates that the device configuration data did not load correctly on startup. This bit does not clear on an Alert Indication Register read. A hard reset via the Configuration Register 2 is required to clear this bit and restart the device setup again. 0 – No setup error detected 1 – Setup error detected 0: No Set-Up Error. 1: Set-up Error.	0x0	R

Bits	Bit Name	Description	Reset	Access
7	AL_D_HIGH	Alert D High. The alert indication high bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert High Threshold Register. This fault bit is sticky and remains set until the register is read. 1: Alert Indication. 0: No Alert Indication.	0x0	R
6	AL_D_LOW	Alert D Low. The alert indication low bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert Low Threshold Register. This fault bit is sticky and remains set until the register is read. 0: No Alert Indication. 1: Alert Indication.	0x0	R
5	AL_C_HIGH	Alert B High. The alert indication high bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert High Threshold Register. This fault bit is sticky and remains set until the register is read. 1: Alert Indication. 0: No Alert Indication.	0x0	R
4	AL_C_LOW	Alert B Low. The alert indication low bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert Low Threshold Register. This fault bit is sticky and remains set until the register is read. 1: Alert Indication. 0: No Alert Indication.	0x0	R
3	AL_B_HIGH	Alert B High. The alert indication high bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert High Threshold Register. This fault bit is sticky and remains set until the register is read. 1: Alert Indication. 0: No Alert Indication.	0x0	R
2	AL_B_LOW	Alert B Low. The alert indication low bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert Low Threshold Register. This fault bit is sticky and remains set until the register is read. 1: Alert Indication. 0: No Alert Indication.	0x0	R
1	AL_A_HIGH	Alert A High. The alert indication high bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert High Threshold Register. This fault bit is sticky and remains set until the register is read. 0: No Alert Indication. 1: Alert Indication.	0x0	R
0	AL_A_LOW	Alert A Low. The alert indication low bits Indicate if a conversion result for the respective input channel exceeds the value set in the Alert Low Threshold Register. This fault bit is sticky and remains set until the register is read. 1: Alert Indication. 0: No Alert Indication.	0x0	R

## ALERT LOW THRESHOLD REGISTER

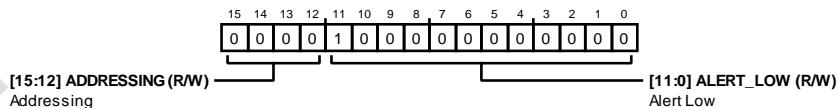


Table 20. Bit Descriptions for Alert Low Threshold Registers

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits [15:12] define the address of the relevant register. See the Addressing Registers Section for further details.	0x0	R/W
[11:0]	ALERT_LOW	Alert Low. The D [11:0] bits from ALERT_LOW move to the MSBs of the internal alert low register D [15:4]. The remaining bits, D [3:0] of the internal register are fixed at 0x0. Sets alert when the converter result is below ALERT_LOW_THRESHOLD and Alert disabled when it is above ALERT_LOW_THRESHOLD.	0x800	R/W

## ALERT HIGH THRESHOLD REGISTER

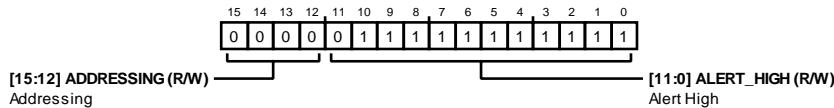


Table 21. Bit Descriptions for Alert High Threshold Registers

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits [15:12] define the address of the relevant register. See the Addressing Registers Section for further details.	0x0	R/W
[11:0]	ALERT_HIGH	Alert High. The D[11:0] bits from ALERT_HIGH move to the MSBs of the internal alert high register D[15:4]. The remaining bits, D[3:0] of the internal register ALERT_HIGH_INT are fixed at 0xF. Sets alert when the converter result is above ALERT_HIGH threshold and Alert disabled when it is below ALERT_HIGH threshold.	0x7FF	R/W

## PCB LAYOUT

The PCB layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ4380-4. A multilayer board with an internal, clean ground plane in the first layer beneath the ADAQ4380-4 is recommended. Care must be taken with the placement of individual components and routing of various signals on the PCB. It is highly recommended to route input and output signals symmetrically. Solder the ground pins of the ADAQ4380-4 directly to the ground plane of the PCB using multiple vias. Remove the ground and power planes under the analog input/output and digital input/output pins of ADAQ4380-4 to avoid undesired parasitic capacitance. Any undesired parasitic capacitance could impact the distortion and linearity performance of the ADAQ4380-4. The pinout of the ADAQ4380-4 eases the layout, allowing its analog and digital signals be easily accessible for routing. The sensitive analog and digital sections

must be separated on the PCB while keeping the power supply circuitry away from the analog signal path. Utilize the ground pins to isolate analog signals from digital signals. Fast switching signals, such as CS or SCLK, and digital outputs, SDOA, SDOB, SDOC and SDOD, must not run near or cross over analog signal paths to prevent noise coupling to the ADAQ4380-4. Good quality ceramic bypass capacitors of at least 2.2  $\mu$ F (0402, X7R) must be placed at the output of the LDO regulators generating the  $\mu$ Module supply rails (VCC, VLOGIC, VS+, and VS-) to GND to minimize EMI susceptibility and to reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the ADAQ4380-4, saving extra board space and cost.

Figure 51 shows the example layout where ADAQ4380-4 is configured at gain=0.6.

## OUTLINE DIMENSIONS

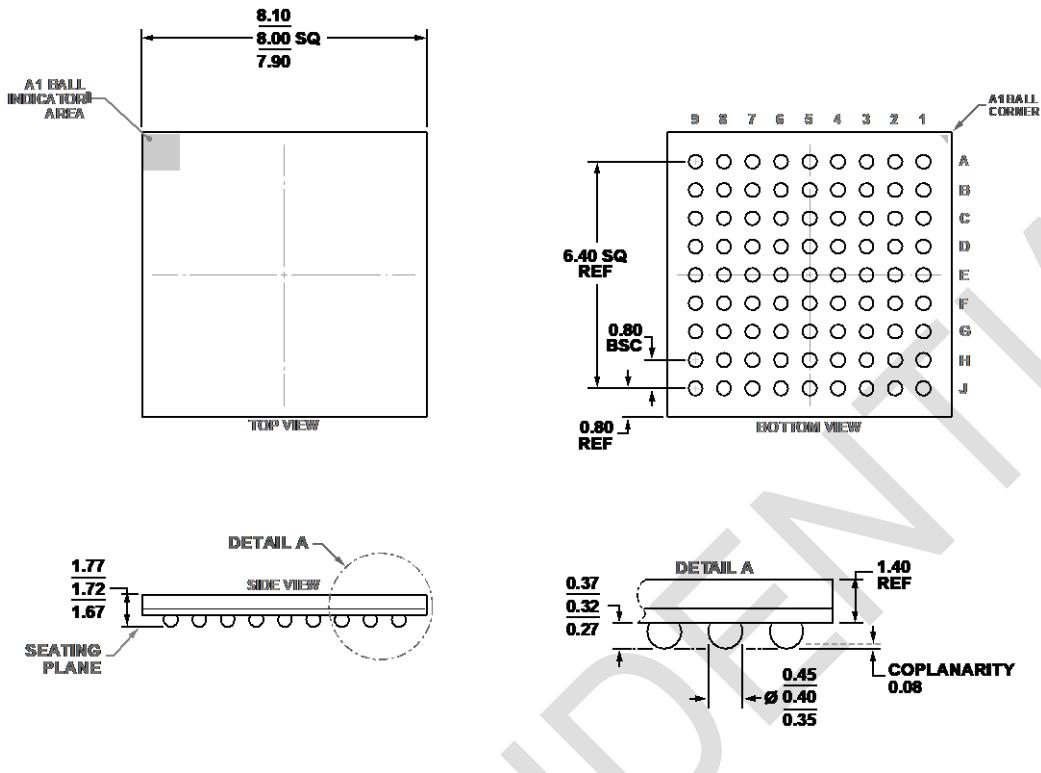


Figure 51. 81-Ball Chip Scale Package Ball Grid Array [CSP\_BGA]  
(BC-81-7)  
Dimensions shown in millimeters