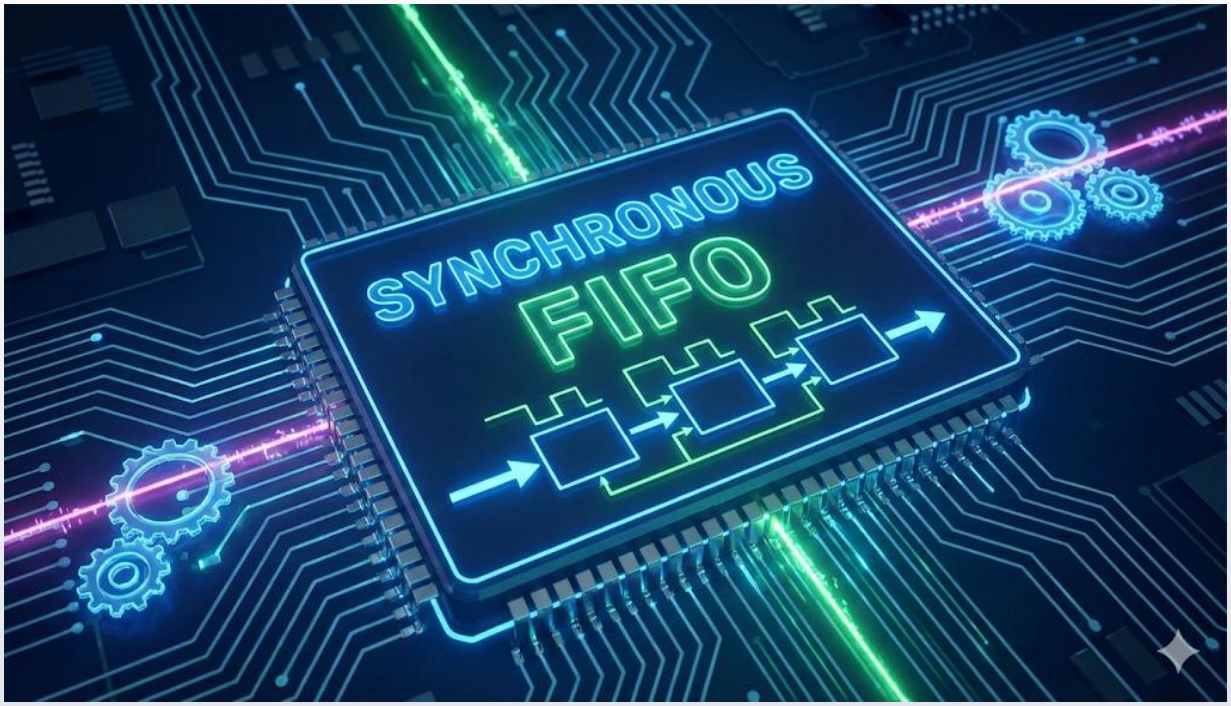
Verifying Synchronous FIFO

Using System Verilog



Prepared by: Marwan Yasser Rifaat Sadeek

Under the supervision of Eng Kareem waseem

synchronous FIFO (Overview)

A **synchronous FIFO** is a type of First-In-First-Out memory buffer used to transfer data between two systems operating on **different clock domains**. Unlike a synchronous FIFO, where both read and write operations share the same clock, an asynchronous FIFO has **separate write and read clocks**, typically denoted as wr_clk and rd_clk.

This design is essential in digital systems where modules run at different frequencies or are not phase-aligned, such as communication interfaces or mixed-speed data paths.

The synchronous FIFO ensures **safe and reliable data transfer** by employing **clock domain crossing (CDC)** techniques, such as **Gray code pointers** and **synchronizer flip-flops**, to prevent metastability and timing violations.

Synchronous FIFO

Read the important notes and the requirements carefully at the end of the document.

Parameters

- FIFO_WIDTH: DATA in/out and memory word width (default: 16)
- FIFO_DEPTH: Memory depth (default: 8)

Ports

Port	Direction	Function
data_in	Input	Write Data: The input data bus used when writing the FIFO.
wr_en		Write Enable: If the FIFO is not full, asserting this signal causes data (on data_in) to be written into the FIFO
rd_en		Read Enable: If the FIFO is not empty, asserting this signal causes data (on data_out) to be read from the FIFO
clk		Clock signal
rst_n		Active low asynchronous reset
data_out	Output	Read Data: The sequential output data bus used when reading from the FIFO.
full		Full Flag: When asserted, this combinational output signal indicates that the FIFO is full. Write requests are ignored when the FIFO is full, initiating a write when the FIFO is full is not destructive to the contents of the FIFO.
almostfull		Almost Full: When asserted, this combinational output signal indicates that only one more write can be performed before the FIFO is full.
empty		Empty Flag: When asserted, this combinational output signal indicates that the FIFO is empty. Read requests are ignored when the FIFO is empty, initiating a read while empty is not destructive to the FIFO.
almostempty		Almost Empty: When asserted, this output combinational signal indicates that only one more read can be performed before the FIFO goes to empty.
overflow		Overflow: This sequential output signal indicates that a write request (wr_en) was rejected because the FIFO is full. Overflowing the FIFO is not destructive to the contents of the FIFO.
underflow		Underflow: This sequential output signal Indicates that the read request (rd_en) was rejected because the FIFO is empty. Under flowing the FIFO is not destructive to the FIFO.
wr_ack		Write Acknowledge: This sequential output signal indicates that a write request (wr_en) has succeeded.

FIFO Verification Plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
FIFO1	**Reset behavior:** On reset, all pointers and count are zero.	Drive rst_n=0 for multiple cycles during simulation.	Cover final (wr_ptr==0 && rd_ptr==0 && count==0)	Assertion a_reset, scoreboard reference model resets memory and flags.
FIFO2	**Write acknowledge:** When wr_en=1 and FIFO not full, wr_ack must be asserted next cycle.	Randomized wr_en and full=0 conditions.	cover property(Write_Acknowledge)	Assertion Write_Acknowledge, scoreboard compares wr_ack vs ref model.
FIFO3	**Overflow detection:** If FIFO full and write occurs without read, overflow=1.	Generate wr_en=1, full=1, rd_en=0.	cover property(Overflow_Detection)	Assertion Overflow_Detection, scoreboard compares overflow_ref.
FIFO4	**Underflow detection:** If FIFO empty and read occurs without write, underflow=1.	Generate rd_en=1, empty=1, wr_en=0.	cover property(Underflow_Detection)	Assertion Underflow_Detection, scoreboard checks underflow_ref.
FIFO5	**Empty flag correctness:** When count==0, empty=1.	Simulate FIFO draining to zero elements.	cover property(Empty_Flag_Assertion)	Assertion Empty_Flag_Assertion, scoreboard empty_ref check.
FIFO6	**Full flag correctness:** When count==FIFO_DEPTH, full=1.	Fill FIFO completely via random writes.	cover property(Full_Flag_Assertion)	Assertion Full_Flag_Assertion, scoreboard full_ref check.
FIFO7	**Almost full threshold:** When count = DEPTH−1, almostfull=1.	Generate write operations until near full.	cover property(Almost_Full_Condition)	Assertion Almost_Full_Condition, scoreboard almostfull_ref check.
FIFO8	**Almost empty threshold:** When count = 1, almostempty=1.	Generate read operations until one element left.	cover property(Almost_Empty_Condition)	Assertion Almost_Empty_Condition, scoreboard almostempty_ref check.
FIFO9	**Write pointer wraparound:** When wr_ptr reaches end, it resets to 0.	Generate continuous writes exceeding FIFO depth.	cover property(Pointer_Wraparound_1)	Assertion Pointer_Wraparound_1, scoreboard implicit pointer size check.
FIFO10	**Read pointer wraparound:** When rd_ptr reaches end, it resets to 0.	Generate continuous reads exceeding FIFO depth.	cover property(Pointer_Wraparound_2)	Assertion Pointer_Wraparound_2.
FIFO11	**Pointer threshold validity:** wr_ptr, rd_ptr, count always ≤ FIFO_DEPTH.	Randomized write/read sequences.	cover property(Pointer_threshold)	Assertion Pointer_threshold ensures bounds.
FIFO12	**Simultaneous wr/rd when empty:** FIFO should not remain empty.	Generate wr_en=1, rd_en=1, empty=1.	cover property(wr_rd_simul_empty)	Assertion wr_rd_simul_empty, scoreboard verifies empty_ref change.
FIFO13	**Simultaneous wr/rd when full:** FIFO should not remain full.	Generate wr_en=1, rd_en=1, full=1.	cover property(wr_rd_simul_full)	Assertion wr_rd_simul_full, scoreboard verifies full_ref change.
FIFO14	**FIFO data integrity:** Data read = oldest written (FIFO order).	Randomized writes and reads.	Covered implicitly in transaction coverage crosses.	Scoreboard compares data_out vs expected FIFO model order.
FIFO15	**Overflow prevention during concurrent wr/rd:** No overflow if both active.	Randomized sequences with wr_en=rd_en=1.	Covered in cross wr_en_rd_en_OVERFLOW.	Scoreboard reference model checks overflow_ref.
FIFO16	**Underflow prevention during concurrent wr/rd:** No underflow if both active.	Randomized sequences with both enables high.	Cross wr_en_rd_en_UNDERFLOW.	Scoreboard underflow_ref check.
FIFO17	**Functional cross coverage:** Check all combinations of write/read with flags.	Randomized enables in 100k cycles.	Coverage crosses for WR_EN, RD_EN, and each flag.	Coverage bins ensure all operational modes tested.
FIFO18	**Final test termination check:** Report total correct/error counts.	End simulation when test_finished=1.	Coverage all goals reached.	$display("error_count=%d, correct_count=%d") at end.

FIFO Design before fixing Bugs:

```
////////////////////////////////////////////////////////////////////////////////
module FIFO(data_in, wr_en, rd_en, clk, rst_n, full, empty, almostfull, almostempty, wr_ack, overflow, underflow, data_out);
parameter FIFO_WIDTH = 16;
parameter FIFO_DEPTH = 8;
input [FIFO_WIDTH-1:0] data_in;
input clk, rst_n, wr_en, rd_en;
output reg [FIFO_WIDTH-1:0] data_out;
output reg wr_ack, overflow;
output full, empty, almostfull, almostempty, underflow;

localparam max_fifo_addr = $clog2(FIFO_DEPTH);

reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];

reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
reg [max_fifo_addr:0] count;

always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        wr_ptr <= 0;
    end
    else if (wr_en && count < FIFO_DEPTH) begin
        mem[wr_ptr] <= data_in;
        wr_ack <= 1;
        wr_ptr <= wr_ptr + 1;
    end
    else begin
        wr_ack <= 0;
        if (full & wr_en)
            overflow <= 1;
        else
            overflow <= 0;
    end
end

 always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        rd_ptr <= 0;
    end
    else if (rd_en && count != 0) begin
        data_out <= mem[rd_ptr];
        rd_ptr <= rd_ptr + 1;
    end
end

always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        count <= 0;
    end
    else begin
        if  ( ({wr_en, rd_en} == 2'b10) && !full)
            count <= count + 1;
        else if ( ({wr_en, rd_en} == 2'b01) && !empty)
            count <= count - 1;
    end
end

assign full = (count == FIFO_DEPTH)? 1 : 0;
assign empty = (count == 0)? 1 : 0;
assign underflow = (empty && rd_en)? 1 : 0;
assign almostfull = (count == FIFO_DEPTH-2)? 1 : 0;
assign almostempty = (count == 1)? 1 : 0;

endmodule
```

FIFO Bug Report and Fix Summary

Bug ID	Category	Description (in Buggy Design)	Root Cause / Impact	Fix Implemented (in Fixed Design)	Verification / Check Used
Bug1	Reset Handling	wr_ack and overflow not reset to 0 during reset.	Left undefined after reset; may cause random outputs or false flags.	Added explicit reset assignments:fifoif.wr_ack <= 0;fifoif.overflow <= 0;	Assertion a_reset, scoreboard reset check.
Bug2	Overflow Condition	Overflow asserted when full && wr_en, but ignored concurrent read (rd_en).	During simultaneous wr_en and rd_en, overflow was incorrectly set.	Fixed condition:if (fifoif.full && fifoif.wr_en && !fifoif.rd_en)	Assertion Overflow_Detection, coverage cross WR_EN_RD_EN_OVERFLOW.
Bug3	Underflow Signal Type	underflow was **combinational** (assign underflow = ...)	Glitchy, unstable underflow output since it changes without clock edge.	Changed to **sequential logic** under clock in always block:fifoif.underflow <= 1/0;	Assertion Underflow_Detection, scoreboard underflow_ref check.
Bug4	Underflow Reset	underflow not reset when rst_n=0.	May retain '1' from previous cycles after reset.	Added reset logic:fifoif.underflow <= 0; in reset branch.	Assertion a_reset, scoreboard reset verification.
Bug5	Count Update (Concurrent wr/rd)	No handling for simultaneous write and read (wr_en && rd_en).	FIFO depth counter count incorrect; causes flag misbehavior near boundaries.	Added explicit handling: if(wr_en&&rd_en&&empty) count++ if(wr_en&&rd_en&&full) count--	Assertions wr_rd_simul_empty and wr_rd_simul_full.
Bug6	Almost Full Threshold	almostfull asserted at count == FIFO_DEPTH-2.	Flag activated too early, misguiding flow control.	Fixed threshold to:count == FIFO_DEPTH-1.	Assertion Almost_Full_Condition, scoreboard check.
Bug7	Missing Sequential Underflow Logic	No sequential control for underflow when empty and rd_en.	underflow would not remain asserted for a full clock; unstable flag.	Added registered control:Underflow asserted/deasserted inside clocked block.	Assertion Underflow_Detection, coverage cross with RD_EN.
Bug8	Write Acknowledge Missing Reset	wr_ack uninitialized after reset.	May start high on first cycle.	Added reset initialization fifoif.wr_ack <= 0;	Assertion Write_Acknowledge, reset assertion.
Bug9	Missing Overflow Reset Behavior	overflow not reset during rst_n=0.	Overflow could stay high after reset.	Added fifoif.overflow <= 0; in reset block.	Assertion a_reset, scoreboard reset phase check.

FIFO Interface

FIFO.IF.sv > ...

```
1  interface FIFO_IF(clk);
2  parameter FIFO_WIDTH = 16;
3  parameter FIFO_DEPTH = 8;
4  input  bit clk;
5  logic [FIFO_WIDTH-1:0] data_in;
6  bit rst_n, wr_en, rd_en;
7  logic [FIFO_WIDTH-1:0] data_out;
8  logic wr_ack, overflow;
9  logic full, empty, almostfull, almostempty, underflow;
10
11 localparam max_fifo_addr = $clog2(FIFO_DEPTH);
12
13 modport TEST   (output data_in, wr_en, rd_en, rst_n,
14                  input clk, full, empty, almostfull, almostempty, wr_ack, overflow, underflow, data_out);
15
16 modport DUT    (input data_in, wr_en, rd_en, clk, rst_n,
17                  output full, empty, almostfull, almostempty, wr_ack, overflow, underflow, data_out);
18
19 modport MONITOR(input data_in, wr_en, rd_en, clk, rst_n, full, empty, almostfull, almostempty, wr_ack, overflow, underflow, data_out);
20
21 endinterface
```

FIFO Design after fixing bugs :

FIFO.sv > ...

```
7   ////////////////////////////////////////////////////////////////////////////////
8   module FIFO(FIFO_IF.DUT fifoif);
9
10  reg [fifoif.FIFO_WIDTH-1:0] mem [fifoif.FIFO_DEPTH-1:0];
11
12  reg [fifoif.max_fifo_addr-1:0] wr_ptr, rd_ptr;
13  reg [fifoif.max_fifo_addr:0] count;
14
15  always @(posedge fifoif.clk or negedge fifoif.rst_n) begin
16      if (!fifoif.rst_n) begin
17          wr_ptr <= 0;
18          fifoif.wr_ack <= 0; // bug
19          fifoif.overflow <= 0; //bug
20
21      end
22      else if (fifoif.wr_en && count < fifoif.FIFO_DEPTH) begin
23          mem[wr_ptr] <= fifoif.data_in;
24          fifoif.wr_ack <= 1;
25          wr_ptr <= wr_ptr + 1;
26      end
27      else begin
28          fifoif.wr_ack <= 0;
29          if (fifoif.full && fifoif.wr_en && !fifoif.rd_en)  //bug foget condition of !rd_en
30              fifoif.overflow <= 1;
31          else
32              fifoif.overflow <= 0;
33      end
34  end
35
36  always @(posedge fifoif.clk or negedge fifoif.rst_n) begin
37      if (!fifoif.rst_n) begin
38          rd_ptr <= 0;
39          fifoif.underflow<=0; //bug
40      end
41      else if (fifoif.rd_en && count != 0) begin
42          fifoif.data_out <= mem[rd_ptr];
43          rd_ptr <= rd_ptr + 1;
44      end
45      // underflow is a sequential output here
46      else begin
47          if(fifoif.empty && fifoif.rd_en && !fifoif.wr_en)
48              fifoif.underflow<=1;
49       else
50          fifoif.underflow<=0;
51      end
52  end
53
54  always @(posedge fifoif.clk or negedge fifoif.rst_n) begin
55      if (!fifoif.rst_n) begin
56          count <= 0;
57      end
58      else begin
59          if  ( ({fifoif.wr_en, fifoif.rd_en} == 2'b10) && !fifoif.full)
60              count <= count + 1;
61          else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b01) && !fifoif.empty)
62              count <= count - 1;
63          else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b11) && fifoif.empty)
64              count <= count+1;
65          else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b11) && fifoif.full)
66              count <= count-1;
67      end
68  end
69
70  assign fifoif.full = (count == fifoif.FIFO_DEPTH)? 1 : 0;
71  assign fifoif.empty = (count == 0)? 1 : 0;
72  //bug  underflow was combinational
73  assign fifoif.almostfull = (count == fifoif.FIFO_DEPTH-1)? 1 : 0; //bug fifoif.FIFO_DEPTH-2
74  assign fifoif.almostempty = (count == 1)? 1 : 0;
75
76
```

FIFO Assertions :

```
77
78  // assertions
79  // 1
80  always_comb begin
81      if(!fifoif.rst_n)
82       a_reset: assert final( (wr_ptr==0) && (rd_ptr==0)  && (count==0));
83  end
84  // 2
85  property Write_Acknowledge;
86      @(posedge fifoif.clk) disable iff(!fifoif.rst_n)   (fifoif.wr_en && !fifoif.full) |=> fifoif.wr_ack;
87  endproperty
88  // 3
89  property Overflow_Detection;
90      @(posedge fifoif.clk) disable iff(!fifoif.rst_n)   (fifoif.wr_en && fifoif.full && !fifoif.rd_en)  |=> fifoif.overflow ;
91  endproperty
92  // 4
93  property Underflow_Detection;
94     @(posedge fifoif.clk) disable iff(!fifoif.rst_n)   (fifoif.rd_en && !fifoif.wr_en && fifoif.empty) |=> fifoif.underflow ;
95  endproperty
96  // 5
97  property Empty_Flag_Assertion;
98     @(posedge fifoif.clk) disable iff(!fifoif.rst_n)   (count==0)  |-> fifoif.empty ;
99  endproperty
100 // 6
101 property Full_Flag_Assertion;
102    @(posedge fifoif.clk) disable iff(!fifoif.rst_n)   (count == fifoif.FIFO_DEPTH)  |-> fifoif.full ;
103 endproperty
104 // 7
105 property Almost_Full_Condition;
106    @(posedge fifoif.clk) disable iff(!fifoif.rst_n)   (count == fifoif.FIFO_DEPTH-1)  |-> fifoif.almostfull ;
107 endproperty
108 // 8
109 property Almost_Empty_Condition;
110    @(posedge fifoif.clk) disable iff(!fifoif.rst_n)   (count == 1)  |-> fifoif.almostempty ;
111 endproperty
112 // 9
113  property Pointer_Wraparound_1;
114     @(posedge fifoif.clk)  disable iff(!fifoif.rst_n)  ( (wr_ptr==fifoif.FIFO_DEPTH-1) && fifoif.wr_en && (count<=fifoif.FIFO_DEPTH-1)) |=>  $fell(wr_ptr);
115 endproperty
116  property Pointer_Wraparound_2;
117    @(posedge fifoif.clk)  disable iff(!fifoif.rst_n)  ( (rd_ptr==fifoif.FIFO_DEPTH-1) && fifoif.rd_en && (count>0) )  |=>  $fell(rd_ptr);
118 endproperty
119  property Pointer_Wraparound_3;
120     @(!fifoif.rst_n)   ( $past(count)==fifoif.FIFO_DEPTH) |-> (count==0);
121 endproperty
122 // 10
123 property Pointer_threshold;
124    @(posedge fifoif.clk)  disable iff(!fifoif.rst_n)  ((wr_ptr < fifoif.FIFO_DEPTH) && (rd_ptr < fifoif.FIFO_DEPTH) && (count <= fifoif.FIFO_DEPTH));
125 endproperty
126 // 11
127 property wr_rd_simul_empty;
128   @(posedge fifoif.clk) disable iff(!fifoif.rst_n)    (fifoif.wr_en && fifoif.rd_en && fifoif.empty) |=> (!fifoif.empty);
129 endproperty
```

```
130  // 12
131  property wr_rd_simul_full;
132    @(posedge fifoif.clk) disable iff(!fifoif.rst_n)    (fifoif.wr_en && fifoif.rd_en && fifoif.full) |=> (!fifoif.full);
133  endproperty
134
135  assert property(Write_Acknowledge);
136  assert property(Overflow_Detection);
137  assert property(Underflow_Detection);
138  assert property(Empty_Flag_Assertion);
139  assert property(Full_Flag_Assertion);
140  assert property(Almost_Full_Condition);
141  assert property(Almost_Empty_Condition);
142  assert property(Pointer_Wraparound_1);
143  assert property(Pointer_Wraparound_2);
144  assert property(Pointer_Wraparound_3);
145  assert property(Pointer_threshold);
146  assert property (wr_rd_simul_empty);
147  assert property (wr_rd_simul_full);
148
149  // cover
150  cover   final( (wr_ptr==0) && (rd_ptr==0)  && (count==0));
151  cover  property(Write_Acknowledge);
152  cover  property(Overflow_Detection);
153  cover  property(Underflow_Detection);
154  cover  property(Empty_Flag_Assertion);
155  cover  property(Full_Flag_Assertion);
156  cover  property(Almost_Full_Condition);
157  cover  property(Almost_Empty_Condition);
158  cover  property(Pointer_Wraparound_1);
159  cover  property(Pointer_Wraparound_2);
160  cover  property(Pointer_Wraparound_3);
161  cover  property(Pointer_threshold);
162  cover  property (wr_rd_simul_empty);
163  cover  property (wr_rd_simul_full);
164
165
166  endmodule
167
```

FIFO packages:

1) shared package

shared_pkg.sv > ...

```
package shared_pkg;
bit test_finished;
int error_count;
int correct_count;
event etrigger;
endpackage

```

2) Transaction package

FIFO_transaction_pkg.sv > ...

```
package FIFO_transaction_pkg;
parameter FIFO_WIDTH = 16;
parameter FIFO_DEPTH = 8;
class FIFO_transaction;
bit clk;
rand bit [FIFO_WIDTH-1:0] data_in;
rand bit rst_n, wr_en, rd_en;
logic [FIFO_WIDTH-1:0] data_out;
logic wr_ack, overflow;
logic full, empty, almostfull, almostempty, underflow;

int RD_EN_ON_DIST , WR_EN_ON_DIST;

function new(int  RD_EN_ON_DIST=30 , WR_EN_ON_DIST=70);
 this.RD_EN_ON_DIST=RD_EN_ON_DIST ;
 this.WR_EN_ON_DIST=WR_EN_ON_DIST ;
endfunction

constraint reset{ rst_n  dist {0:/10 , 1:/90};}
constraint WR_EN{ wr_en  dist {1:/WR_EN_ON_DIST , 0:/(100-WR_EN_ON_DIST)};}
constraint RD_EN{ rd_en  dist {1:/RD_EN_ON_DIST , 0:/(100-RD_EN_ON_DIST)};}

endclass
endpackage

```

3) coverage package

FIFO_coverage_pkg.sv > {} FIFO_coverage_pkg > FIFO_coverage

```
1  package FIFO_coverage_pkg;
2  import FIFO_transaction_pkg::*;
3  class FIFO_coverage;
4  FIFO_transaction   F_cvg_txn=new();
5  covergroup g1;
6  WR_EN       : coverpoint F_cvg_txn.wr_en ;
7  RD_EN       : coverpoint F_cvg_txn.rd_en ;
8  WR_ACK      : coverpoint F_cvg_txn.wr_ack ;
9  OVERFLOW    : coverpoint F_cvg_txn.overflow ;
10 FULL        : coverpoint F_cvg_txn.overflow ;
11 EMPTY       : coverpoint F_cvg_txn.empty ;
12 ALMOSTFULL  : coverpoint F_cvg_txn.almostfull ;
13 ALMOSTEMPTY : coverpoint F_cvg_txn.almostempty ;
14 UNDERFLOW   : coverpoint F_cvg_txn.underflow ;
15
16 wr_en_rd_en_WR_ACK      :cross WR_EN , RD_EN , WR_ACK  ;
17 wr_en_rd_en_OVERFLOW    :cross WR_EN , RD_EN , OVERFLOW ;
18 wr_en_rd_en_FULL        :cross WR_EN , RD_EN ,FULL      ;
19 wr_en_rd_en_EMPTY       :cross WR_EN , RD_EN ,EMPTY     ;
20 wr_en_rd_en_ALMOSTFULL  :cross WR_EN , RD_EN ,ALMOSTFULL ;
21 wr_en_rd_en_ALMOSTEMPTY :cross WR_EN , RD_EN ,ALMOSTEMPTY;
22 wr_en_rd_en_UNDERFLOW   :cross WR_EN , RD_EN ,UNDERFLOW  ;
23 endgroup
24
25 //constructor
26 function new();
27   g1 =new;
28 endfunction
29 //
30 function void sample_data(input FIFO_transaction F_txn);
31 F_cvg_txn=F_txn;
32 g1.sample();
33 endfunction
34
35 endclass
36 endpackage
```

4) scoreboard package

FIFO_scoreboard_pkg.sv > {} FIFO_scoreboard_pkg > FIFO_scoreboard

```
package FIFO_scoreboard_pkg;
import FIFO_transaction_pkg::*;
import shared_pkg::*;
logic full_ref=0, empty_ref=1,almostfull_ref=0,almostempty_ref=0,overflow_ref=0,underflow_ref=0;
logic [FIFO_WIDTH-1:0] data_out_ref;
class FIFO_scoreboard;
// logic full_ref=0, empty_ref=1,almostfull_ref=0,almostempty_ref=0,overflow_ref=0,underflow_ref=0;
logic [FIFO_WIDTH-1:0]data_mem [$];


function void reference_model(input FIFO_transaction F_ref_txn);

if(!F_ref_txn.rst_n)begin
   data_mem.delete();
   full_ref<=0;
   empty_ref<=1;
   overflow_ref<=0;
   underflow_ref<=0;
end
else begin

if(F_ref_txn.wr_en && (data_mem.size() < FIFO_DEPTH) )
    data_mem.push_back(F_ref_txn.data_in);
if(F_ref_txn.rd_en && !empty_ref)
    data_out_ref<=data_mem.pop_front;

if(F_ref_txn.wr_en && !F_ref_txn.rd_en && full_ref )
    overflow_ref<=1;
else
    overflow_ref<=0;

if(F_ref_txn.rd_en && !F_ref_txn.wr_en &&  empty_ref)
   underflow_ref<=1;
else
   underflow_ref<=0;

   if (data_mem.size()==FIFO_DEPTH) full_ref<=1;
   else full_ref<=0;

   if(data_mem.size()==0) empty_ref<=1;
   else    empty_ref<=0;

 end
   if(data_mem.size() == FIFO_DEPTH-1)  almostfull_ref  <=   1 ;
   else  almostfull_ref<= 0;

   if(data_mem.size() == 1)  almostempty_ref <=1 ;
   else  almostempty_ref <= 0;

 endfunction

task check_data(input FIFO_transaction F_chk_txn);
reference_model(F_chk_txn);
if(data_out_ref!=F_chk_txn.data_out  ||  full_ref!=F_chk_txn.full || empty_ref!=F_chk_txn.empty
   ||almostfull_ref!=F_chk_txn.almostfull ||almostempty_ref!=F_chk_txn.almostempty
   ||overflow_ref!=F_chk_txn.overflow|| underflow_ref!=F_chk_txn.underflow )begin
     $display("ERROR: incorrect data_out   , data_out =%h    ,EXPECTED =%h",F_chk_txn.data_out,data_out_ref);
     $display("rst_n=%b , wr_en=%b , rd_en =%b , data_in =%h , full=%b ,full_ref=%b, empty=%b ,empty_ref=%b ,
     almostfull=%b,almostfull_ref=%b ,almostempty=%b,almostempty_ref=%b,overflow=%b,overflow_ref=%b,underflow=%b,
      underflow_ref=%b ",
     F_chk_txn.rst_n,F_chk_txn.wr_en,F_chk_txn.rd_en,F_chk_txn.data_in,F_chk_txn.full,full_ref,F_chk_txn.empty,empty_ref,
     F_chk_txn.almostfull,almostfull_ref,F_chk_txn.almostempty,almostempty_ref,F_chk_txn.overflow,overflow_ref,
     F_chk_txn.underflow, underflow_ref);
     $display("----------------------------------");
    error_count=error_count+1;
end
else begin
    correct_count=correct_count+1;
end

endtask
endclass
endpackage
```

FIFO Monitor :

FIFO_monitor.sv > ...

```
import FIFO_transaction_pkg::*;
import FIFO_scoreboard_pkg::*;
import FIFO_coverage_pkg::*;
import shared_pkg::*;

module FIFO_monitor(FIFO_IF.MONITOR fifoif);
FIFO_transaction fifo_txn;
FIFO_scoreboard  fifo_board;
FIFO_coverage  fifo_cvg;

initial begin
fifo_txn=new();
fifo_board=new();
fifo_cvg=new();

 forever begin

//     wait(etrigger.triggered);
    @etrigger;

     fifo_txn.data_in=fifoif.data_in;
     fifo_txn.wr_en=fifoif.wr_en;
     fifo_txn.rd_en=fifoif.rd_en;
     fifo_txn.rst_n=fifoif.rst_n;
     fifo_txn.full=fifoif.full;
     fifo_txn.empty=fifoif.empty;
     fifo_txn.almostfull=fifoif.almostfull;
     fifo_txn.almostempty=fifoif.almostempty;
     fifo_txn.wr_ack=fifoif.wr_ack;
     fifo_txn.overflow=fifoif.overflow;
     fifo_txn.underflow=fifoif.underflow;
     fifo_txn.data_out=fifoif.data_out;

    fork
    begin
        fifo_cvg.sample_data(fifo_txn);
    end

    begin
        fifo_board.check_data(fifo_txn) ;
    end
    join

    if(test_finished==1)begin
    $display("error_count =%d  ,correct_count =%d ",error_count,correct_count);
    $stop;
    end
    end
end

endmodule
```

FIFO Testbench :

FIFO_tb.sv > FIFO_tb

```
1   import FIFO_transaction_pkg::*;
2   import FIFO_scoreboard_pkg::*;
3   import FIFO_coverage_pkg::*;
4   import shared_pkg::*;
5   module FIFO_tb(FIFO_IF.TEST fifoif);
6
7   FIFO_transaction fifo_txn_tb=new();
8
9   initial begin
10      fifo_txn_tb.data_in=0;
11      fifo_txn_tb.wr_en=0;
12      fifo_txn_tb.rd_en=0;
13      fifo_txn_tb.rst_n=0;
14
15  fifoif.rst_n=0;
16  @(negedge fifoif.clk);
17  fifoif.rst_n=1;
18
19  repeat(100000)begin
20      @(negedge fifoif.clk);
21      assert(fifo_txn_tb.randomize());
22      fifoif.data_in=fifo_txn_tb.data_in;
23      fifoif.wr_en=fifo_txn_tb.wr_en;
24      fifoif.rd_en=fifo_txn_tb.rd_en;
25      fifoif.rst_n=fifo_txn_tb.rst_n;
26
27
28
29       -> etrigger;
30
31  end
32        test_finished=1;
33  end
34
35  endmodule
```

SRC_files & DO_file :

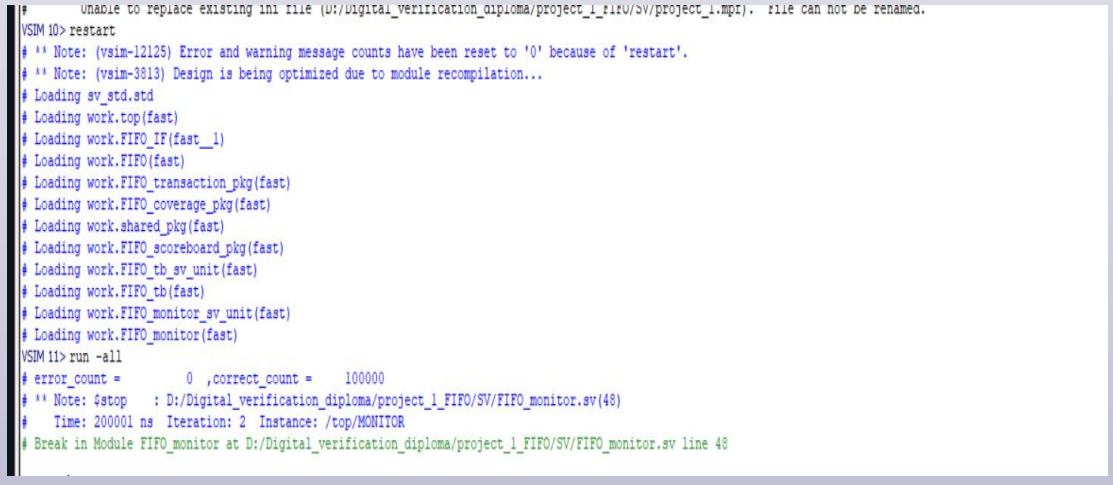
src_file.list

```
FIFO.IF.sv
FIFO.sv
shared_pkg.sv
FIFO_coverage_pkg.sv
FIFO_transaction_pkg.sv
FIFO_scoreboard_pkg.sv
FIFO_TOP.sv
FIFO_tb.sv
FIFO_monitor.sv
```

run_FIFO.do

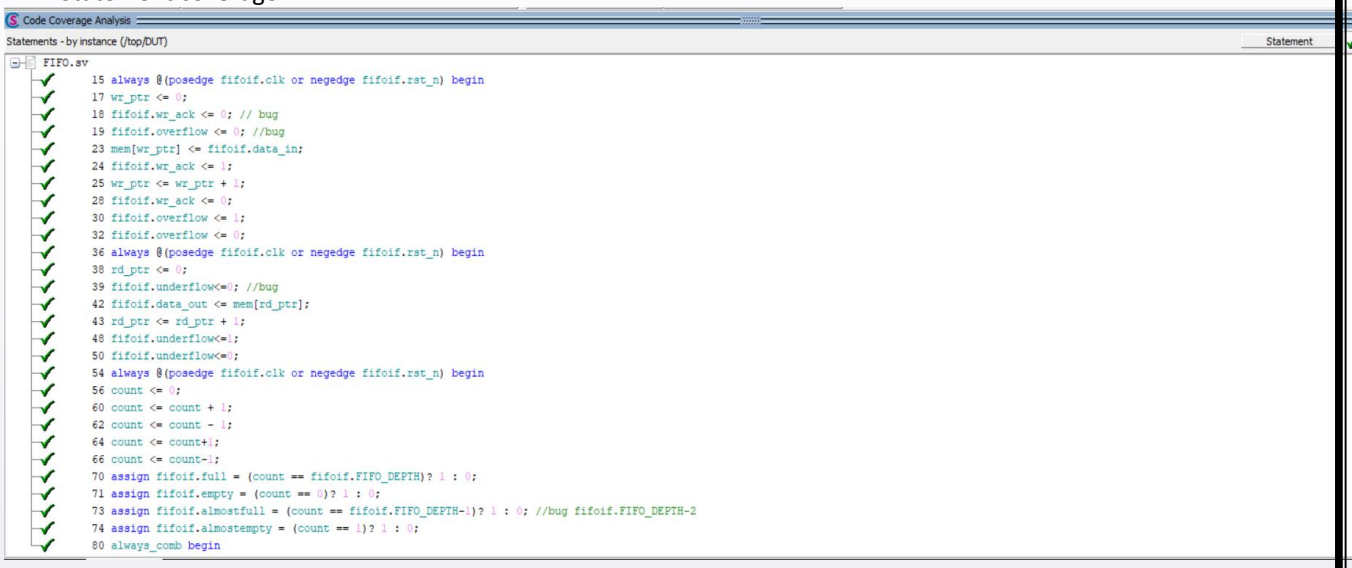
```
vlib work
vlog  -f src_file.list +cover -covercells
vsim -voptargs=+acc work.top -cover  -sv_seed random
add wave /top/fifoif/*
add wave -position insertpoint sim:/FIFO_scoreboard_pkg/*
coverage save TOP_FIFO.ucdb -du FIFO   -onexit
run -all
```

FIFO Results

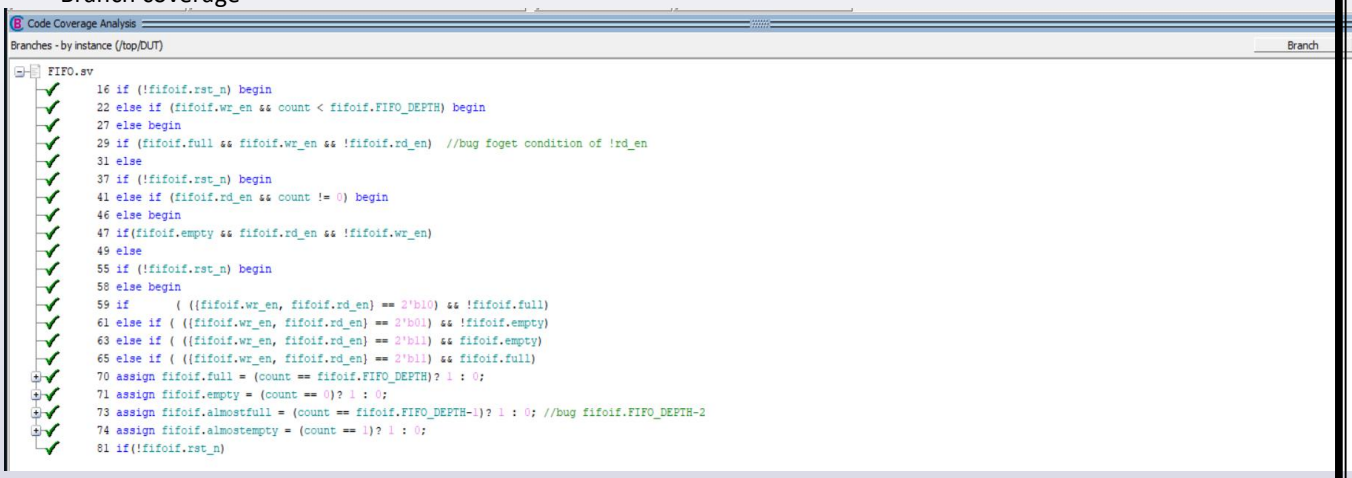


CODE coverage report :

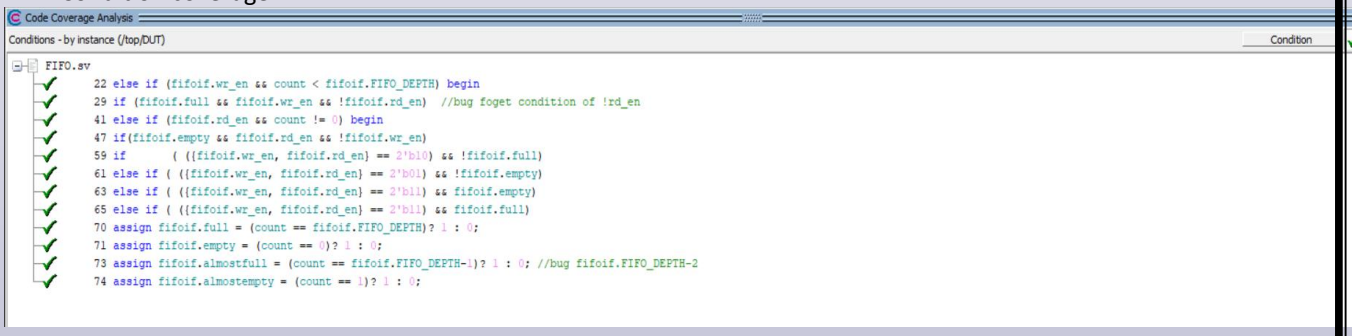
- Statement coverage



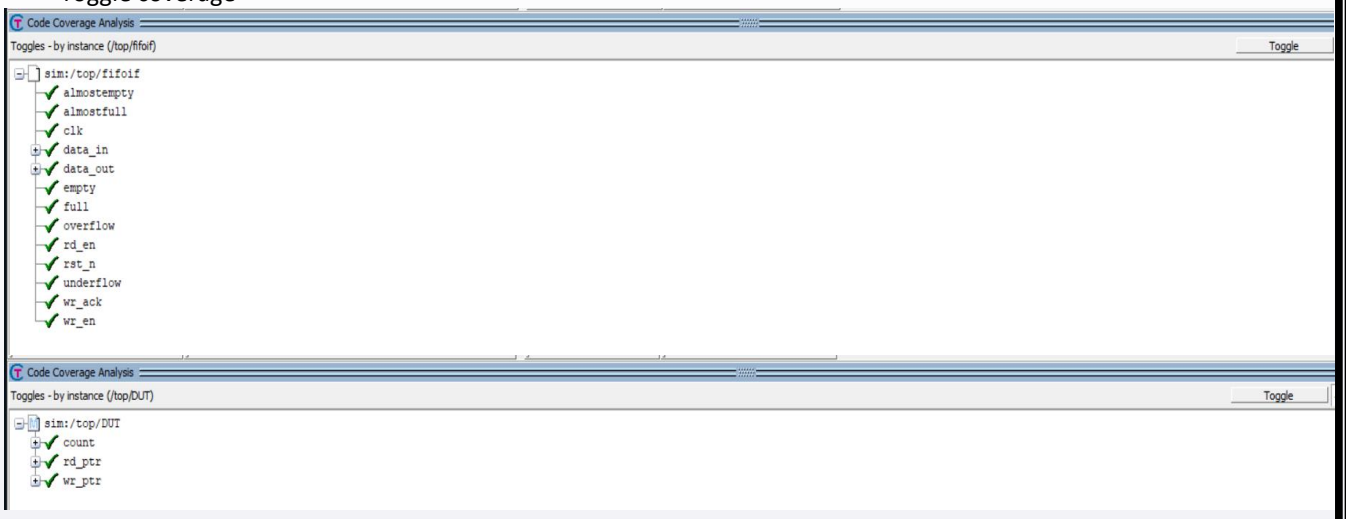
- Branch coverage



- Condition coverage



- Toggle coverage




```
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        27        27         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\top#DUT

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File FIFO.sv
------------------------------------IF Branch------------------------------------
    16                                    109052     Count coming in to IF
    16              1                      19120        if (!fifoif.rst_n) begin

    22              1                      56238        else if (fifoif.wr_en && count < fifoif.FIFO_DEPTH) begin

    27              1                      33694        else begin

Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    29                                     33694     Count coming in to IF
    29              1                       4529                if (fifoif.full && fifoif.wr_en && !fifoif.rd_en)  //bug foget condition of !rd_en

    31              1                      29165                else

Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    37                                    109052     Count coming in to IF
    37              1                      19120        if (!fifoif.rst_n) begin

    41              1                      22689        else if (fifoif.rd_en && count != 0) begin

    46              1                      67243        else begin

Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    47                                     67243     Count coming in to IF
    47              1                       1290                if(fifoif.empty && fifoif.rd_en && !fifoif.wr_en)

    49              1                      65953                else

Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    55                                  100294     Count coming in to IF
    55              1                    18762        if (!fifoif.rst_n) begin

    58              1                    81532        else begin

Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    59                                  81532     Count coming in to IF
    59              1                   39273               if      ( ({fifoif.wr_en, fifoif.rd_en} == 2'b10) && !fifoif.full)

    61              1                    6755               else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b01) && !fifoif.empty)

    63              1                    3027               else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b11) && fifoif.empty)

    65              1                    1996               else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b11) && fifoif.full)

                                         30481     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    70                                  59532     Count coming in to IF
    70              1                    3898     assign fifoif.full = (count == fifoif.FIFO_DEPTH)? 1 : 0;

    70              2                   55634     assign fifoif.full = (count == fifoif.FIFO_DEPTH)? 1 : 0;

Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    71                                  59532     Count coming in to IF
    71              1                    9911     assign fifoif.empty = (count == 0)? 1 : 0;

    71              2                   49621     assign fifoif.empty = (count == 0)? 1 : 0;

Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    73                                  59532     Count coming in to IF
    73              1                    5484     assign fifoif.almostfull = (count == fifoif.FIFO_DEPTH-1)? 1 : 0; //bug fifoif.FIFO_DEPTH-2

    73              2                   54048     assign fifoif.almostfull = (count == fifoif.FIFO_DEPTH-1)? 1 : 0; //bug fifoif.FIFO_DEPTH-2

Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    74                                  59532     Count coming in to IF
    74              1                   11130     assign fifoif.almostempty = (count == 1)? 1 : 0;
    74              2                   48402     assign fifoif.almostempty = (count == 1)? 1 : 0;

Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    81                                  91768     Count coming in to IF
    81              1                   17727        if(!fifoif.rst_n)

                                        74041     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      26        26         0   100.00%

================================Condition Details================================

Condition Coverage for instance /\top#DUT  --

  File FIFO.sv
----------------Focused Condition View-------------------
Line       22 Item    1  (fifoif.wr_en && (count < fifoif.FIFO_DEPTH))
Condition totals: 2 of 2 input terms covered = 100.00%

                  Input Term   Covered  Reason for no coverage   Hint
                 -----------  --------  -----------------------  --------------
                fifoif.wr_en         Y
  (count < fifoif.FIFO_DEPTH)        Y

     Rows:       Hits  FEC Target                    Non-masking condition(s)
 ---------  ---------  --------------------          -------------------------
  Row   1:          1  fifoif.wr_en_0                -
  Row   2:          1  fifoif.wr_en_1                (count < fifoif.FIFO_DEPTH)
  Row   3:          1  (count < fifoif.FIFO_DEPTH)_0  fifoif.wr_en
  Row   4:          1  (count < fifoif.FIFO_DEPTH)_1  fifoif.wr_en

----------------Focused Condition View-------------------
Line       29 Item    1  ((fifoif.full && fifoif.wr_en) && ~fifoif.rd_en)
Condition totals: 3 of 3 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  -----------------------  --------------
   fifoif.full         Y
  fifoif.wr_en         Y
  fifoif.rd_en         Y
```

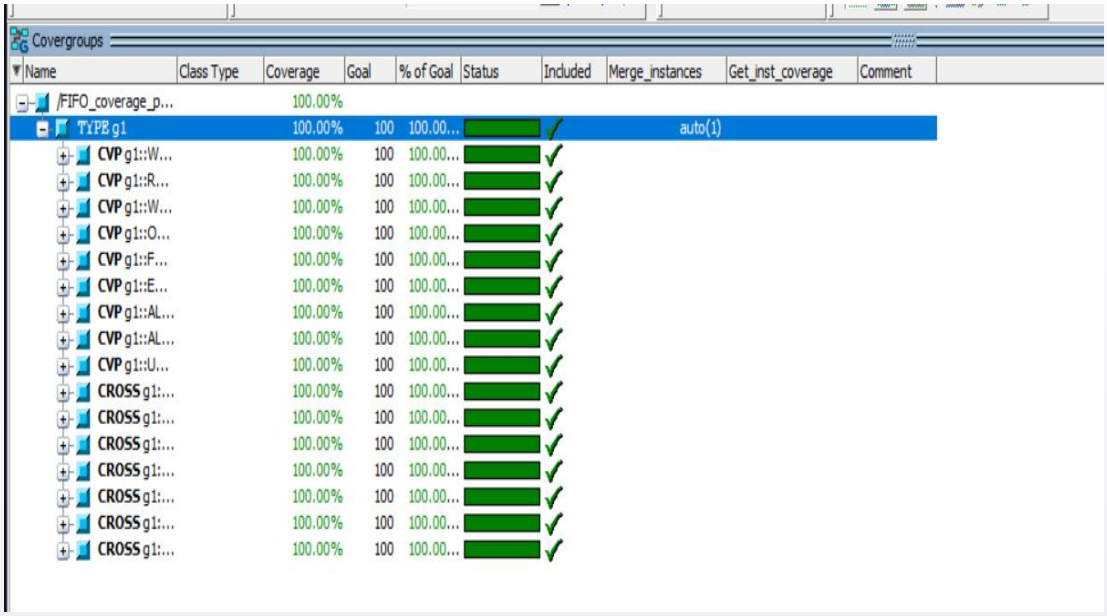
```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  fifoif.full_0         -
  Row   2:          1  fifoif.full_1         (~fifoif.rd_en && fifoif.wr_en)
  Row   3:          1  fifoif.wr_en_0        fifoif.full
  Row   4:          1  fifoif.wr_en_1        (~fifoif.rd_en && fifoif.full)
  Row   5:          1  fifoif.rd_en_0        (fifoif.full && fifoif.wr_en)
  Row   6:          1  fifoif.rd_en_1        (fifoif.full && fifoif.wr_en)

----------------Focused Condition View-------------------
Line       41 Item    1  (fifoif.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  -----------------------  --------------
  fifoif.rd_en          Y
  (count != 0)          Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  fifoif.rd_en_0        -
  Row   2:          1  fifoif.rd_en_1        (count != 0)
  Row   3:          1  (count != 0)_0        fifoif.rd_en
  Row   4:          1  (count != 0)_1        fifoif.rd_en

----------------Focused Condition View-------------------
Line       47 Item    1  ((fifoif.empty && fifoif.rd_en) && ~fifoif.wr_en)
Condition totals: 3 of 3 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  -----------------------  --------------
  fifoif.empty          Y
  fifoif.rd_en          Y
  fifoif.wr_en          Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  fifoif.empty_0        -
  Row   2:          1  fifoif.empty_1        (~fifoif.wr_en && fifoif.rd_en)
  Row   3:          1  fifoif.rd_en_0        fifoif.empty
  Row   4:          1  fifoif.rd_en_1        (~fifoif.wr_en && fifoif.empty)
  Row   5:          1  fifoif.wr_en_0        (fifoif.empty && fifoif.rd_en)
  Row   6:          1  fifoif.wr_en_1        (fifoif.empty && fifoif.rd_en)

----------------Focused Condition View-------------------
Line       59 Item    1  ((~fifoif.rd_en && fifoif.wr_en) && ~fifoif.full)
Condition totals: 3 of 3 input terms covered = 100.00%
```

```
    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  -----------------------  --------------
  fifoif.rd_en          Y
  fifoif.wr_en          Y
   fifoif.full          Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  fifoif.rd_en_0        (~fifoif.full && fifoif.wr_en)
  Row   2:          1  fifoif.rd_en_1        -
  Row   3:          1  fifoif.wr_en_0        ~fifoif.rd_en
  Row   4:          1  fifoif.wr_en_1        (~fifoif.full && ~fifoif.rd_en)
  Row   5:          1  fifoif.full_0         (~fifoif.rd_en && fifoif.wr_en)
  Row   6:          1  fifoif.full_1         (~fifoif.rd_en && fifoif.wr_en)

----------------Focused Condition View-------------------
Line       61 Item    1  ((fifoif.rd_en && ~fifoif.wr_en) && ~fifoif.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  -----------------------  --------------
  fifoif.rd_en          Y
  fifoif.wr_en          Y
  fifoif.empty          Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  fifoif.rd_en_0        -
  Row   2:          1  fifoif.rd_en_1        (~fifoif.empty && ~fifoif.wr_en)
  Row   3:          1  fifoif.wr_en_0        (~fifoif.empty && fifoif.rd_en)
  Row   4:          1  fifoif.wr_en_1        fifoif.rd_en
  Row   5:          1  fifoif.empty_0        (fifoif.rd_en && ~fifoif.wr_en)
  Row   6:          1  fifoif.empty_1        (fifoif.rd_en && ~fifoif.wr_en)

----------------Focused Condition View-------------------
Line       63 Item    1  ((fifoif.rd_en && fifoif.wr_en) && fifoif.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  -----------------------  --------------
  fifoif.rd_en          Y
  fifoif.wr_en          Y
  fifoif.empty          Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  fifoif.rd_en_0        -
  Row   2:          1  fifoif.rd_en_1        (fifoif.empty && fifoif.wr_en)
```

```
  Row   3:          1  fifoif.wr_en_0        fifoif.rd_en
  Row   4:          1  fifoif.wr_en_1        (fifoif.empty && fifoif.rd_en)
  Row   5:          1  fifoif.empty_0        (fifoif.rd_en && fifoif.wr_en)
  Row   6:          1  fifoif.empty_1        (fifoif.rd_en && fifoif.wr_en)

----------------Focused Condition View-------------------
Line       65 Item    1  ((fifoif.rd_en && fifoif.wr_en) && fifoif.full)
Condition totals: 3 of 3 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  fifoif.rd_en         Y
  fifoif.wr_en         Y
   fifoif.full         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ----------  --------------------  -------------------------
  Row   1:          1  fifoif.rd_en_0        -
  Row   2:          1  fifoif.rd_en_1        (fifoif.full && fifoif.wr_en)
  Row   3:          1  fifoif.wr_en_0        fifoif.rd_en
  Row   4:          1  fifoif.wr_en_1        (fifoif.full && fifoif.rd_en)
  Row   5:          1  fifoif.full_0         (fifoif.rd_en && fifoif.wr_en)
  Row   6:          1  fifoif.full_1         (fifoif.rd_en && fifoif.wr_en)

----------------Focused Condition View-------------------
Line       70 Item    1  (count == fifoif.FIFO_DEPTH)
Condition totals: 1 of 1 input term covered = 100.00%

                    Input Term   Covered  Reason for no coverage   Hint
                   -----------  --------  ----------------------  --------------
  (count == fifoif.FIFO_DEPTH)         Y

     Rows:       Hits  FEC Target                       Non-masking condition(s)
 ---------  ----------  -------------------------------  -------------------------
  Row   1:          1  (count == fifoif.FIFO_DEPTH)_0  -
  Row   2:          1  (count == fifoif.FIFO_DEPTH)_1  -

----------------Focused Condition View-------------------
Line       71 Item    1  (count == 0)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  (count == 0)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ----------  --------------------  -------------------------
  Row   1:          1  (count == 0)_0        -

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ----------  --------------------  -------------------------
  Row   1:          1  (count == 0)_0        -
  Row   2:          1  (count == 0)_1        -

----------------Focused Condition View-------------------
Line       73 Item    1  (count == (fifoif.FIFO_DEPTH - 1))
Condition totals: 1 of 1 input term covered = 100.00%

                     Input Term   Covered  Reason for no coverage   Hint
                    -----------  --------  ----------------------  --------------
  (count == (fifoif.FIFO_DEPTH - 1))         Y

     Rows:       Hits  FEC Target                                 Non-masking condition(s)
 ---------  ----------  -----------------------------------------  -------------------------
  Row   1:          1  (count == (fifoif.FIFO_DEPTH - 1))_0  -
  Row   2:          1  (count == (fifoif.FIFO_DEPTH - 1))_1  -

----------------Focused Condition View-------------------
Line       74 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  (count == 1)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ----------  --------------------  -------------------------
  Row   1:          1  (count == 1)_0        -
  Row   2:          1  (count == 1)_1        -

Statement Coverage:
    Enabled Coverage             Bins      Hits    Misses  Coverage
    ----------------             ----      ----    ------  --------
    Statements                     28        28         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\top#DUT  --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File FIFO.sv
    8                                                module FIFO(FIFO_IF.DUT fifoif);

    9

    10                                               reg [fifoif.FIFO_WIDTH-1:0] mem [fifoif.FIFO_DEPTH-1:0];

    11

    12                                               reg [fifoif.max_fifo_addr-1:0] wr_ptr, rd_ptr;

    13                                               reg [fifoif.max_fifo_addr:0] count;

    14

    15              1                       109052   always @(posedge fifoif.clk or negedge fifoif.rst_n) begin

    16                                                  if (!fifoif.rst_n) begin

    17              1                        19120             wr_ptr <= 0;

    18              1                        19120             fifoif.wr_ack <= 0; // bug

    19              1                        19120             fifoif.overflow <= 0; //bug

    20

    21                                                  end

    22                                                  else if (fifoif.wr_en && count < fifoif.FIFO_DEPTH) begin

    23              1                        56238             mem[wr_ptr] <= fifoif.data_in;

    24              1                        56238             fifoif.wr_ack <= 1;

    25              1                        56238             wr_ptr <= wr_ptr + 1;
```

```
    26                                          end
    27                                          else begin
    28              1                   33694               fifoif.wr_ack <= 0;
    29                                          if (fifoif.full && fifoif.wr_en && !fifoif.rd_en)  //bug foget condition of !rd_en
    30              1                    4529                      fifoif.overflow <= 1;
    31                                          else
    32              1                   29165                      fifoif.overflow <= 0;
    33                                          end
    34                                      end
    35
    36              1                  109052     always @(posedge fifoif.clk or negedge fifoif.rst_n) begin
    37                                            if (!fifoif.rst_n) begin
    38              1                   19120               rd_ptr <= 0;
    39              1                   19120           fifoif.underflow<=0; //bug
    40                                            end
    41                                            else if (fifoif.rd_en && count != 0) begin
    42              1                   22689               fifoif.data_out <= mem[rd_ptr];
    43              1                   22689               rd_ptr <= rd_ptr + 1;
    44                                            end
    45                                            // underflow is a sequential output here
    46                                            else begin
    47                                                    if(fifoif.empty && fifoif.rd_en && !fifoif.wr_en)
    48              1                    1290                fifoif.underflow<=1;
    49                                                    else
    50              1                   65953               fifoif.underflow<=0;
    51                                            end
    52                                        end
    53
    54              1                  100294     always @(posedge fifoif.clk or negedge fifoif.rst_n) begin
    55                                            if (!fifoif.rst_n) begin
    56              1                   18762               count <= 0;
    57                                            end
    58                                            else begin
    59                                                    if      ( ({fifoif.wr_en, fifoif.rd_en} == 2'b10) && !fifoif.full)
    60              1                   39273                       count <= count + 1;
    61                                                    else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b01) && !fifoif.empty)
    62              1                    6755                       count <= count - 1;
    63                                                    else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b11) && fifoif.empty)
    64              1                    3027                   count <= count+1;
    65                                                    else if ( ({fifoif.wr_en, fifoif.rd_en} == 2'b11) && fifoif.full)
    66              1                    1996                   count <= count-1;
    67                                            end
    68                                        end
    69
    70              1                   59533     assign fifoif.full = (count == fifoif.FIFO_DEPTH)? 1 : 0;
    71              1                   59533     assign fifoif.empty = (count == 0)? 1 : 0;
    72                                            //bug  underflow was combinational
    73              1                   59533     assign fifoif.almostfull = (count == fifoif.FIFO_DEPTH-1)? 1 : 0; //bug fifoif.FIFO_DEPTH-2
File Edit Format View Help
    74             1                    59533     assign fifoif.almostempty = (count == 1)? 1 : 0;
    75
    76
    77
    78                                          // assertions
    79                                          // 1
    80              1                   91768     always_comb begin


Toggle Coverage:
    Enabled Coverage             Bins      Hits    Misses  Coverage
    ----------------             ----      ----    ------  --------
    Toggles                        20        20         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\top#DUT  --

                                       Node      1H->0L      0L->1H  "Coverage"
                                       ----------------------------------------
                                  count[3-0]           1           1      100.00
                                 rd_ptr[2-0]           1           1      100.00
                                 wr_ptr[2-0]           1           1      100.00

Total Node Count     =         10
Toggled Node Count   =         10
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (20 of 20 bins)
```

Functional coverage report :



Covergroups

Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	Get_inst_coverage	Comment
/FIFO_coverage_p...		100.00%							
TYPE g1		100.00%	100	100.00...		✓	auto(1)		
CVP g1::W...		100.00%	100	100.00...		✓			
CVP g1::R...		100.00%	100	100.00...		✓			
CVP g1::W...		100.00%	100	100.00...		✓			
CVP g1::O...		100.00%	100	100.00...		✓			
CVP g1::F...		100.00%	100	100.00...		✓			
CVP g1::E...		100.00%	100	100.00...		✓			
CVP g1::AL...		100.00%	100	100.00...		✓			
CVP g1::AL...		100.00%	100	100.00...		✓			
CVP g1::U...		100.00%	100	100.00...		✓			
CROSS g1:...		100.00%	100	100.00...		✓			
CROSS g1:...		100.00%	100	100.00...		✓			
CROSS g1:...		100.00%	100	100.00...		✓			
CROSS g1:...		100.00%	100	100.00...		✓			
CROSS g1:...		100.00%	100	100.00...		✓			
CROSS g1:...		100.00%	100	100.00...		✓			
CROSS g1:...		100.00%	100	100.00...		✓			

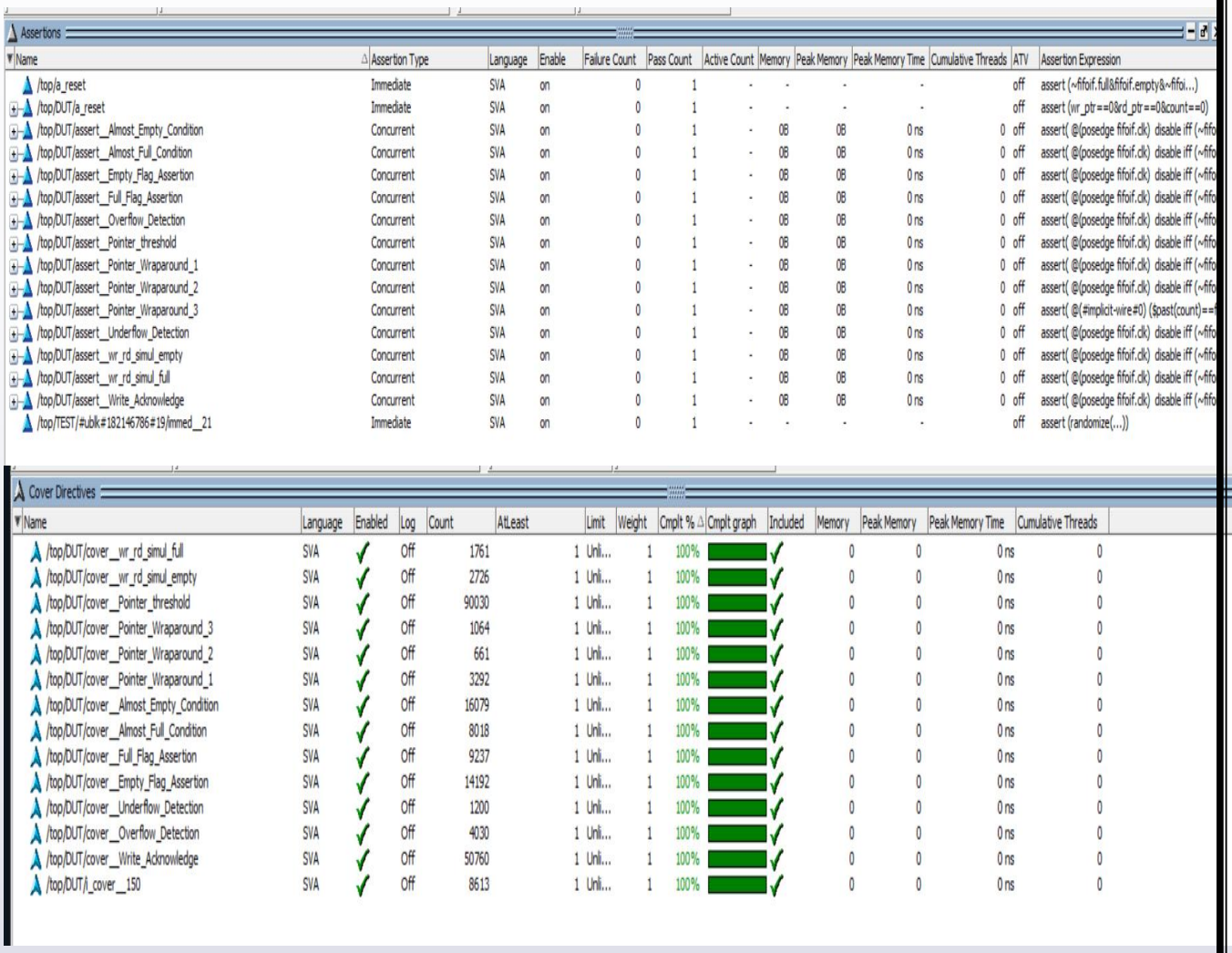
```
Coverage Report by instance with details

================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
================================================================================

Covergroup Coverage:
    Covergroups                     1        na        na   100.00%
        Coverpoints/Crosses        16        na        na        na
            Covergroup Bins        74        74         0   100.00%
----------------------------------------------------------------------------------------------------------------
Covergroup                                             Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------------
 TYPE /FIFO_coverage_pkg/FIFO_coverage/g1            100.00%        100          -    Covered
    covered/total bins:                                  74         74          -
    missing/total bins:                                   0         74          -
    % Hit:                                           100.00%        100          -
    Coverpoint WR_EN                                 100.00%        100          -    Covered
        covered/total bins:                                2          2          -
        missing/total bins:                                0          2          -
        % Hit:                                       100.00%        100          -
        bin auto[0]                                    30349          1          -    Covered
        bin auto[1]                                    69651          1          -    Covered
    Coverpoint RD_EN                                 100.00%        100          -    Covered
        covered/total bins:                                2          2          -
        missing/total bins:                                0          2          -
        % Hit:                                       100.00%        100          -
        bin auto[0]                                    69788          1          -    Covered
        bin auto[1]                                    30212          1          -    Covered
    Coverpoint WR_ACK                                100.00%        100          -    Covered
        covered/total bins:                                2          2          -
        missing/total bins:                                0          2          -
        % Hit:                                       100.00%        100          -
        bin auto[0]                                    43729          1          -    Covered
        bin auto[1]                                    56271          1          -    Covered
    Coverpoint OVERFLOW                              100.00%        100          -    Covered
        covered/total bins:                                2          2          -
        missing/total bins:                                0          2          -
        % Hit:                                       100.00%        100          -
        bin auto[0]                                    95492          1          -    Covered
        bin auto[1]                                     4508          1          -    Covered
    Coverpoint FULL                                  100.00%        100          -    Covered
        covered/total bins:                                2          2          -
        missing/total bins:                                0          2          -
        % Hit:                                       100.00%        100          -
        bin auto[0]                                    95492          1          -    Covered
```

bin auto[1]	4508	1	-	Covered
Coverpoint EMPTY	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	84254	1	-	Covered
bin auto[1]	15746	1	-	Covered
Coverpoint ALMOSTFULL	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	91112	1	-	Covered
bin auto[1]	8888	1	-	Covered
Coverpoint ALMOSTEMPTY	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	82139	1	-	Covered
bin auto[1]	17861	1	-	Covered
Coverpoint UNDERFLOW	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	98658	1	-	Covered
bin auto[1]	1342	1	-	Covered
Cross wr_en_rd_en_WR_ACK	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	11754	1	-	Covered
bin <auto[0],auto[1],auto[1]>	5180	1	-	Covered
bin <auto[1],auto[0],auto[1]>	27342	1	-	Covered
bin <auto[0],auto[0],auto[1]>	11995	1	-	Covered
bin <auto[1],auto[1],auto[0]>	9281	1	-	Covered
bin <auto[0],auto[1],auto[0]>	3997	1	-	Covered
bin <auto[1],auto[0],auto[0]>	21274	1	-	Covered
bin <auto[0],auto[0],auto[0]>	9177	1	-	Covered
Cross wr_en_rd_en_OVERFLOW	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	945	1	-	Covered
bin <auto[0],auto[1],auto[1]>	426	1	-	Covered
bin <auto[1],auto[0],auto[1]>	2251	1	-	Covered
bin <auto[0],auto[0],auto[1]>	886	1	-	Covered
bin <auto[1],auto[1],auto[0]>	20090	1	-	Covered
bin <auto[0],auto[1],auto[0]>	8751	1	-	Covered
bin <auto[1],auto[0],auto[0]>	46365	1	-	Covered
bin <auto[0],auto[0],auto[0]>	20286	1	-	Covered
Cross wr_en_rd_en_FULL	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	945	1	-	Covered
bin <auto[0],auto[1],auto[1]>	426	1	-	Covered
bin <auto[1],auto[0],auto[1]>	2251	1	-	Covered
bin <auto[0],auto[0],auto[1]>	886	1	-	Covered
bin <auto[1],auto[1],auto[0]>	20090	1	-	Covered
bin <auto[0],auto[1],auto[0]>	8751	1	-	Covered
bin <auto[1],auto[0],auto[0]>	46365	1	-	Covered
bin <auto[0],auto[0],auto[0]>	20286	1	-	Covered
Cross wr_en_rd_en_EMPTY	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	3358	1	-	Covered
bin <auto[0],auto[1],auto[1]>	1470	1	-	Covered
bin <auto[1],auto[0],auto[1]>	7592	1	-	Covered
bin <auto[0],auto[0],auto[1]>	3326	1	-	Covered
bin <auto[1],auto[1],auto[0]>	17677	1	-	Covered
bin <auto[0],auto[1],auto[0]>	7707	1	-	Covered
bin <auto[1],auto[0],auto[0]>	41024	1	-	Covered
bin <auto[0],auto[0],auto[0]>	17846	1	-	Covered
Cross wr_en_rd_en_ALMOSTFULL	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1860	1	-	Covered
bin <auto[0],auto[1],auto[1]>	761	1	-	Covered
bin <auto[1],auto[0],auto[1]>	4325	1	-	Covered
bin <auto[0],auto[0],auto[1]>	1942	1	-	Covered
bin <auto[1],auto[1],auto[0]>	19175	1	-	Covered
bin <auto[0],auto[1],auto[0]>	8416	1	-	Covered
bin <auto[1],auto[0],auto[0]>	44291	1	-	Covered
bin <auto[0],auto[0],auto[0]>	19230	1	-	Covered
Cross wr_en_rd_en_ALMOSTEMPTY	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	3727	1	-	Covered

```
            bin <auto[0],auto[1],auto[1]>              1607          1          -    Covered
            bin <auto[1],auto[0],auto[1]>              8711          1          -    Covered
            bin <auto[0],auto[0],auto[1]>              3816          1          -    Covered
            bin <auto[1],auto[1],auto[0]>             17308          1          -    Covered
            bin <auto[0],auto[1],auto[0]>              7570          1          -    Covered
            bin <auto[1],auto[0],auto[0]>             39905          1          -    Covered
            bin <auto[0],auto[0],auto[0]>             17356          1          -    Covered
    Cross wr_en_rd_en_UNDERFLOW                     100.00%        100          -    Covered
        covered/total bins:                               8          8          -
        missing/total bins:                               0          8          -
        % Hit:                                      100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>              285          1          -    Covered
            bin <auto[0],auto[1],auto[1]>              115          1          -    Covered
            bin <auto[1],auto[0],auto[1]>              657          1          -    Covered
            bin <auto[0],auto[0],auto[1]>              285          1          -    Covered
            bin <auto[1],auto[1],auto[0]>            20750          1          -    Covered
            bin <auto[0],auto[1],auto[0]>             9062          1          -    Covered
            bin <auto[1],auto[0],auto[0]>            47959          1          -    Covered
            bin <auto[0],auto[0],auto[0]>            20887          1          -    Covered

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------------
 TYPE /FIFO_coverage_pkg/FIFO_coverage/g1         100.00%        100          -    Covered
    covered/total bins:                                74         74          -
    missing/total bins:                                 0         74          -
    % Hit:                                        100.00%        100          -
    Coverpoint WR_EN                              100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   30349          1          -    Covered
        bin auto[1]                                   69651          1          -    Covered
    Coverpoint RD_EN                              100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   69788          1          -    Covered
        bin auto[1]                                   30212          1          -    Covered
    Coverpoint WR_ACK                             100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   43729          1          -    Covered
        bin auto[1]                                   56271          1          -    Covered
    Coverpoint OVERFLOW                           100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   95492          1          -    Covered
        bin auto[1]                                    4508          1          -    Covered
    Coverpoint FULL                               100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   95492          1          -    Covered
        bin auto[1]                                    4508          1          -    Covered
    Coverpoint EMPTY                              100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   84254          1          -    Covered
        bin auto[1]                                   15746          1          -    Covered
    Coverpoint ALMOSTFULL                         100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   91112          1          -    Covered
        bin auto[1]                                    8888          1          -    Covered
    Coverpoint ALMOSTEMPTY                        100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   82139          1          -    Covered
        bin auto[1]                                   17861          1          -    Covered
    Coverpoint UNDERFLOW                          100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                   98658          1          -    Covered
        bin auto[1]                                    1342          1          -    Covered
    Cross wr_en_rd_en_WR_ACK                      100.00%        100          -    Covered
        covered/total bins:                               8          8          -
        missing/total bins:                               0          8          -
        % Hit:                                    100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>             11754          1          -    Covered
            bin <auto[0],auto[1],auto[1]>              5180          1          -    Covered
            bin <auto[1],auto[0],auto[1]>             27342          1          -    Covered
            bin <auto[0],auto[0],auto[1]>             11995          1          -    Covered
            bin <auto[1],auto[1],auto[0]>              9281          1          -    Covered
            bin <auto[0],auto[1],auto[0]>              3997          1          -    Covered
            bin <auto[1],auto[0],auto[0]>             21274          1          -    Covered
```

```
            bin <auto[0],auto[0],auto[0]>                9177          1          -    Covered
    Cross wr_en_rd_en_OVERFLOW                         100.00%        100          -    Covered
        covered/total bins:                                  8          8          -
        missing/total bins:                                  0          8          -
        % Hit:                                         100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>                 945          1          -    Covered
            bin <auto[0],auto[1],auto[1]>                 426          1          -    Covered
            bin <auto[1],auto[0],auto[1]>                2251          1          -    Covered
            bin <auto[0],auto[0],auto[1]>                 886          1          -    Covered
            bin <auto[1],auto[1],auto[0]>               20090          1          -    Covered
            bin <auto[0],auto[1],auto[0]>                8751          1          -    Covered
            bin <auto[1],auto[0],auto[0]>               46365          1          -    Covered
            bin <auto[0],auto[0],auto[0]>               20286          1          -    Covered
    Cross wr_en_rd_en_FULL                             100.00%        100          -    Covered
        covered/total bins:                                  8          8          -
        missing/total bins:                                  0          8          -
        % Hit:                                         100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>                 945          1          -    Covered
            bin <auto[0],auto[1],auto[1]>                 426          1          -    Covered
            bin <auto[1],auto[0],auto[1]>                2251          1          -    Covered
            bin <auto[0],auto[0],auto[1]>                 886          1          -    Covered
            bin <auto[1],auto[1],auto[0]>               20090          1          -    Covered
            bin <auto[0],auto[1],auto[0]>                8751          1          -    Covered
            bin <auto[1],auto[0],auto[0]>               46365          1          -    Covered
            bin <auto[0],auto[0],auto[0]>               20286          1          -    Covered
    Cross wr_en_rd_en_EMPTY                            100.00%        100          -    Covered
        covered/total bins:                                  8          8          -
        missing/total bins:                                  0          8          -
        % Hit:                                         100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>                3358          1          -    Covered
            bin <auto[0],auto[1],auto[1]>                1470          1          -    Covered
            bin <auto[1],auto[0],auto[1]>                7592          1          -    Covered
            bin <auto[0],auto[0],auto[1]>                3326          1          -    Covered
            bin <auto[1],auto[1],auto[0]>               17677          1          -    Covered
            bin <auto[0],auto[1],auto[0]>                7707          1          -    Covered
            bin <auto[1],auto[0],auto[0]>               41024          1          -    Covered
            bin <auto[0],auto[0],auto[0]>               17846          1          -    Covered
    Cross wr_en_rd_en_ALMOSTFULL                       100.00%        100          -    Covered
        covered/total bins:                                  8          8          -
        missing/total bins:                                  0          8          -
        % Hit:                                         100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>                1860          1          -    Covered
            bin <auto[0],auto[1],auto[1]>                 761          1          -    Covered
            bin <auto[1],auto[0],auto[1]>                4325          1          -    Covered
          bin <auto[0],auto[1],auto[1]>                   761          1          -    Covered
          bin <auto[1],auto[0],auto[1]>                  4325          1          -    Covered
          bin <auto[0],auto[0],auto[1]>                  1942          1          -    Covered
          bin <auto[1],auto[1],auto[0]>                 19175          1          -    Covered
          bin <auto[0],auto[1],auto[0]>                  8416          1          -    Covered
          bin <auto[1],auto[0],auto[0]>                 44291          1          -    Covered
          bin <auto[0],auto[0],auto[0]>                 19230          1          -    Covered
    Cross wr_en_rd_en_ALMOSTEMPTY                      100.00%        100          -    Covered
        covered/total bins:                                  8          8          -
        missing/total bins:                                  0          8          -
        % Hit:                                         100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>                3727          1          -    Covered
            bin <auto[0],auto[1],auto[1]>                1607          1          -    Covered
            bin <auto[1],auto[0],auto[1]>                8711          1          -    Covered
            bin <auto[0],auto[0],auto[1]>                3816          1          -    Covered
            bin <auto[1],auto[1],auto[0]>               17308          1          -    Covered
            bin <auto[0],auto[1],auto[0]>                7570          1          -    Covered
            bin <auto[1],auto[0],auto[0]>               39905          1          -    Covered
            bin <auto[0],auto[0],auto[0]>               17356          1          -    Covered
    Cross wr_en_rd_en_UNDERFLOW                        100.00%        100          -    Covered
        covered/total bins:                                  8          8          -
        missing/total bins:                                  0          8          -
        % Hit:                                         100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>                 285          1          -    Covered
            bin <auto[0],auto[1],auto[1]>                 115          1          -    Covered
            bin <auto[1],auto[0],auto[1]>                 657          1          -    Covered
            bin <auto[0],auto[0],auto[1]>                 285          1          -    Covered
            bin <auto[1],auto[1],auto[0]>               20750          1          -    Covered
            bin <auto[0],auto[1],auto[0]>                9062          1          -    Covered
            bin <auto[1],auto[0],auto[0]>               47959          1          -    Covered
            bin <auto[0],auto[0],auto[0]>               20887          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%
```

Assertion coverage report :



Assertions

Name	Assertion Type	Language	Enable	Failure Count	Pass Count	Active Count	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	ATV	Assertion Expression
/top/a_reset	Immediate	SVA	on	0	1	-	-	-	-		off	assert (~fifoif.full&fifoif.empty&~fifoi...)
/top/DUT/a_reset	Immediate	SVA	on	0	1	-	-	-	-		off	assert (wr_ptr==0&rd_ptr==0&count==0)
/top/DUT/assert__Almost_Empty_Condition	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Almost_Full_Condition	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Empty_Flag_Assertion	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Full_Flag_Assertion	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Overflow_Detection	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Pointer_threshold	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Pointer_Wraparound_1	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Pointer_Wraparound_2	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Pointer_Wraparound_3	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(#implicit-wire#0) ($past(count)==
/top/DUT/assert__Underflow_Detection	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__wr_rd_simul_empty	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__wr_rd_simul_full	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/DUT/assert__Write_Acknowledge	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disable iff (~fifo
/top/TEST/#ublk#182146786#19/immed__21	Immediate	SVA	on	0	1	-	-	-	-		off	assert (randomize(...))

Cover Directives

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads
/top/DUT/cover__wr_rd_simul_full	SVA	✓	Off	1761	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__wr_rd_simul_empty	SVA	✓	Off	2726	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Pointer_threshold	SVA	✓	Off	90030	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Pointer_Wraparound_3	SVA	✓	Off	1064	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Pointer_Wraparound_2	SVA	✓	Off	661	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Pointer_Wraparound_1	SVA	✓	Off	3292	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Almost_Empty_Condition	SVA	✓	Off	16079	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Almost_Full_Condition	SVA	✓	Off	8018	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Full_Flag_Assertion	SVA	✓	Off	9237	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Empty_Flag_Assertion	SVA	✓	Off	14192	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Underflow_Detection	SVA	✓	Off	1200	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Overflow_Detection	SVA	✓	Off	4030	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/cover__Write_Acknowledge	SVA	✓	Off	50760	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/i_cover__150	SVA	✓	Off	8613	1	Unli...	1	100%		✓	0	0	0 ns	0

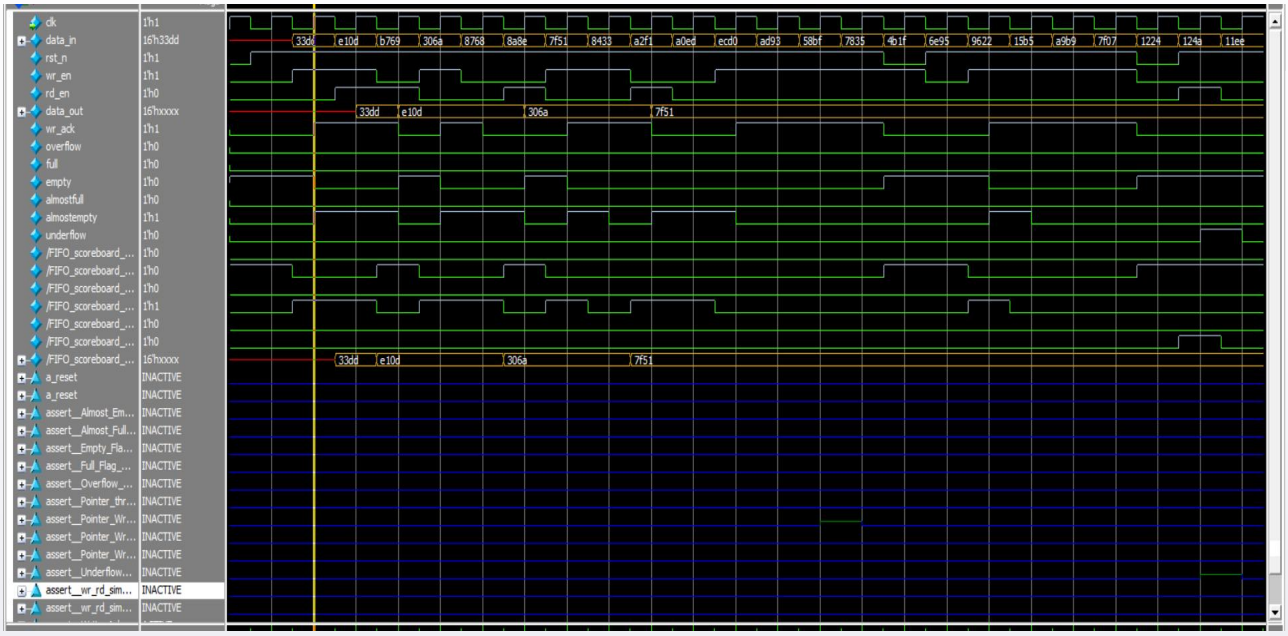
```
================================================================================
=== Instance: /top/DUT
=== Design Unit: work.FIFO
================================================================================

Assertion Coverage:
    Assertions                      14        14         0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/top/DUT/assert__wr_rd_simul_full
                     FIFO.sv(147)                       0          1
/top/DUT/assert__wr_rd_simul_empty
                     FIFO.sv(146)                       0          1
/top/DUT/assert__Pointer_threshold
                     FIFO.sv(145)                       0          1
/top/DUT/assert__Pointer_Wraparound_3
                     FIFO.sv(144)                       0          1
/top/DUT/assert__Pointer_Wraparound_2
                     FIFO.sv(143)                       0          1
/top/DUT/assert__Pointer_Wraparound_1
                     FIFO.sv(142)                       0          1
/top/DUT/assert__Almost_Empty_Condition
                     FIFO.sv(141)                       0          1
/top/DUT/assert__Almost_Full_Condition
                     FIFO.sv(140)                       0          1
/top/DUT/assert__Full_Flag_Assertion
                     FIFO.sv(139)                       0          1
/top/DUT/assert__Empty_Flag_Assertion
                     FIFO.sv(138)                       0          1
/top/DUT/assert__Underflow_Detection
                     FIFO.sv(137)                       0          1
/top/DUT/assert__Overflow_Detection
                     FIFO.sv(136)                       0          1
/top/DUT/assert__Write_Acknowledge
                     FIFO.sv(135)                       0          1
/top/DUT/a_reset     FIFO.sv(82)                        0          1
```

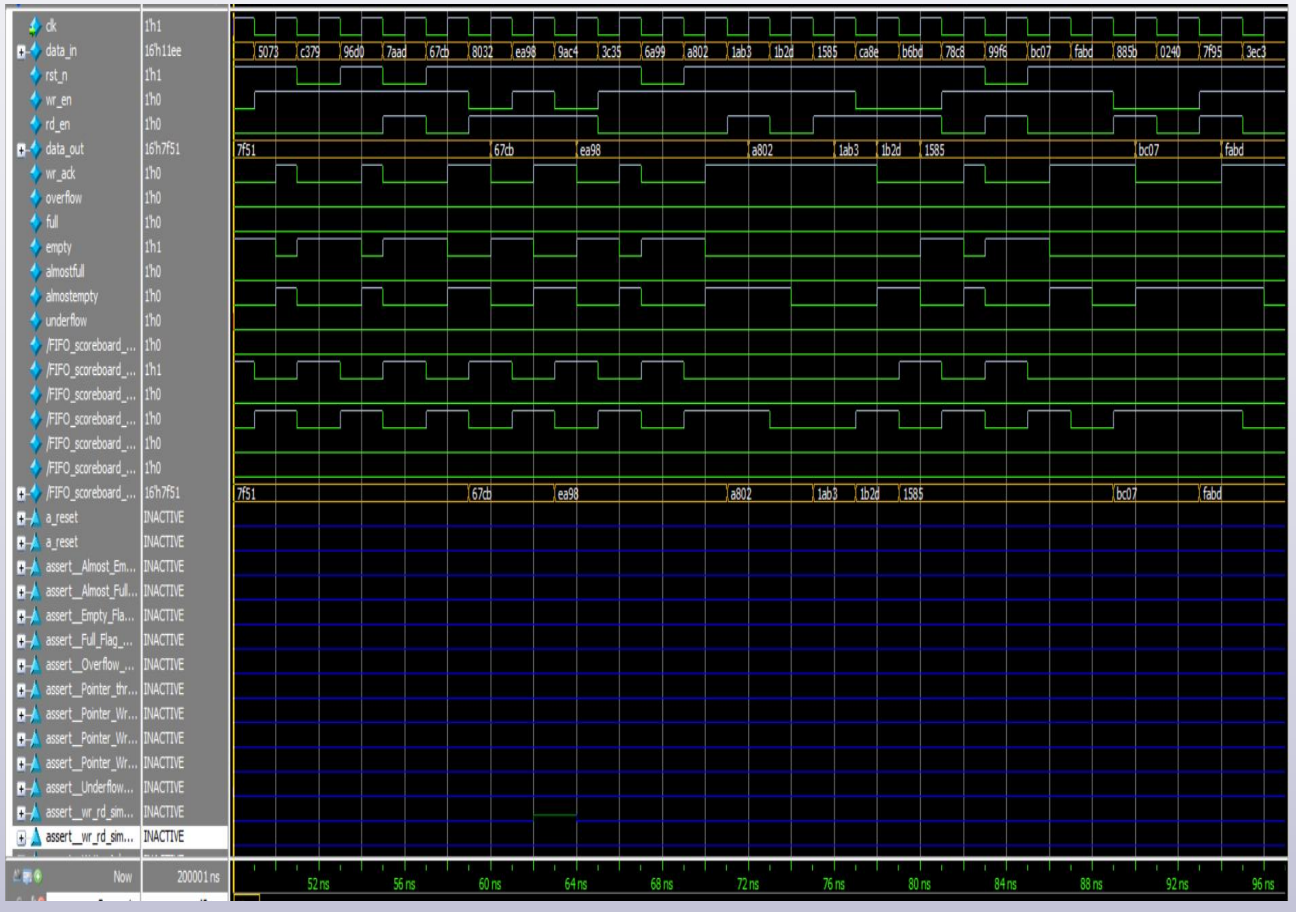
```
Directive Coverage:
    Directives                  14        14         0   100.00%

DIRECTIVE COVERAGE:
-----------------------------------------------------------------------------------------
Name                                 Design Design   Lang File(Line)      Hits Status
                                     Unit   UnitType
-----------------------------------------------------------------------------------------
/top/DUT/cover__wr_rd_simul_full     FIFO   Verilog  SVA  FIFO.sv(163)    1761 Covered
/top/DUT/cover__wr_rd_simul_empty    FIFO   Verilog  SVA  FIFO.sv(162)    2726 Covered
/top/DUT/cover__Pointer_threshold    FIFO   Verilog  SVA  FIFO.sv(161)    90030 Covered
/top/DUT/cover__Pointer_Wraparound_3 FIFO   Verilog  SVA  FIFO.sv(160)    1064 Covered
/top/DUT/cover__Pointer_Wraparound_2 FIFO   Verilog  SVA  FIFO.sv(159)     661 Covered
/top/DUT/cover__Pointer_Wraparound_1 FIFO   Verilog  SVA  FIFO.sv(158)    3292 Covered
/top/DUT/cover__Almost_Empty_Condition FIFO  Verilog  SVA  FIFO.sv(157)    16079 Covered
/top/DUT/cover__Almost_Full_Condition FIFO   Verilog  SVA  FIFO.sv(156)    8018 Covered
/top/DUT/cover__Full_Flag_Assertion  FIFO   Verilog  SVA  FIFO.sv(155)    9237 Covered
/top/DUT/cover__Empty_Flag_Assertion FIFO   Verilog  SVA  FIFO.sv(154)    14192 Covered
/top/DUT/cover__Underflow_Detection  FIFO   Verilog  SVA  FIFO.sv(153)    1200 Covered
/top/DUT/cover__Overflow_Detection   FIFO   Verilog  SVA  FIFO.sv(152)    4030 Covered
/top/DUT/cover__Write_Acknowledge    FIFO   Verilog  SVA  FIFO.sv(151)    50760 Covered
/top/DUT/i_cover__150                FIFO   Verilog  SVA  FIFO.sv(150)    8613 Covered

================================================================================
```

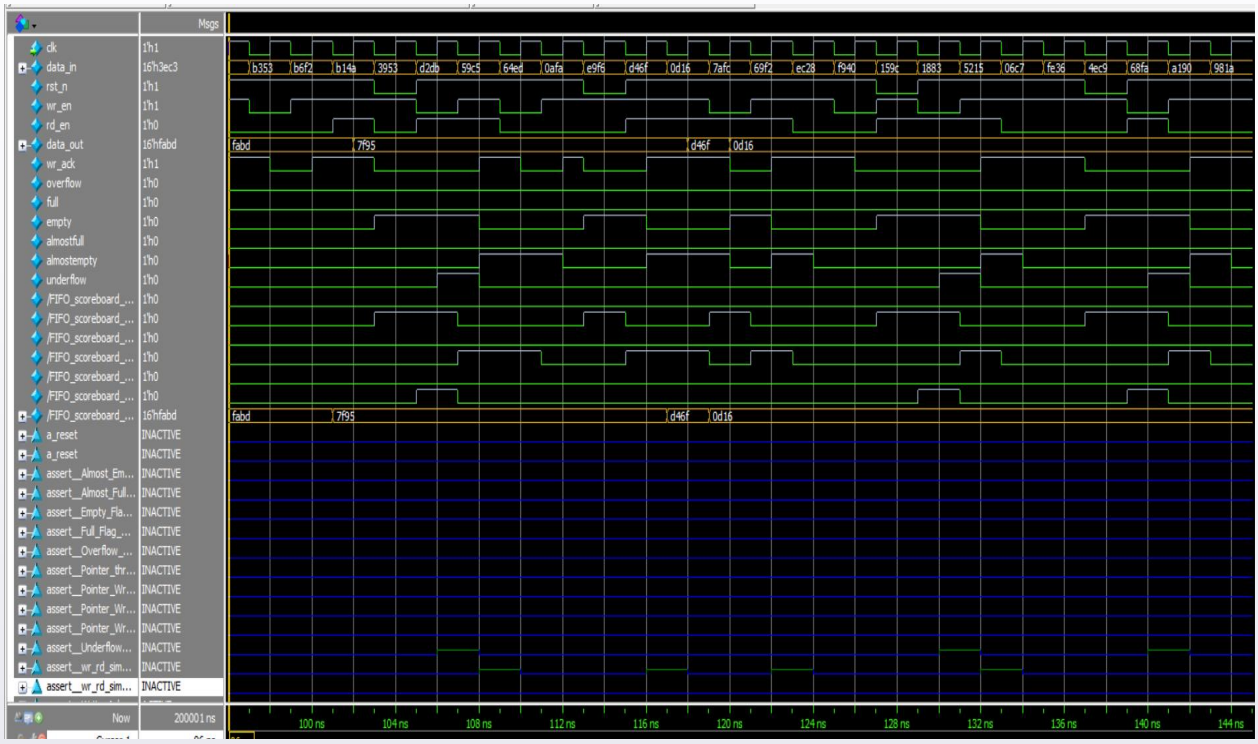
```
================================================================================
=== Instance: /top/TEST
=== Design Unit: work.FIFO_tb
================================================================================

Assertion Coverage:
    Assertions                      1         1         0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/top/TEST/#ublk#182146786#19/immed__21
                     FIFO_tb.sv(21)                     0          1

================================================================================
=== Instance: /top
=== Design Unit: work.top
================================================================================

Assertion Coverage:
    Assertions                      1         1         0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/top/a_reset         FIFO_TOP.sv(21)                    0          1
```

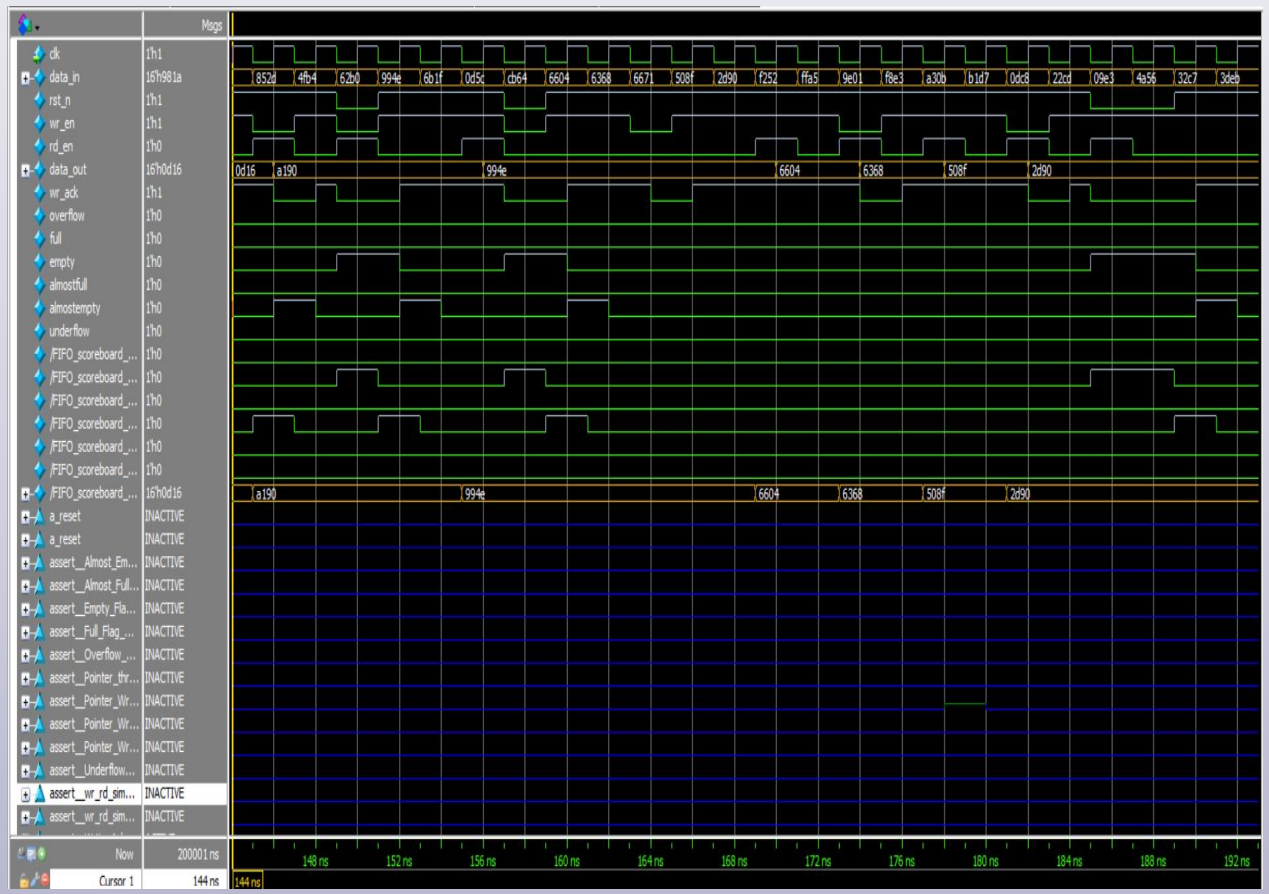
```
DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------------------
Name                                     Design Design   Lang File(Line)      Hits Status
                                         Unit   UnitType
--------------------------------------------------------------------------------------------------------
/top/DUT/cover__wr_rd_simul_full         FIFO   Verilog  SVA  FIFO.sv(163)    1761 Covered
/top/DUT/cover__wr_rd_simul_empty        FIFO   Verilog  SVA  FIFO.sv(162)    2726 Covered
/top/DUT/cover__Pointer_threshold        FIFO   Verilog  SVA  FIFO.sv(161)   90030 Covered
/top/DUT/cover__Pointer_Wraparound_3     FIFO   Verilog  SVA  FIFO.sv(160)    1064 Covered
/top/DUT/cover__Pointer_Wraparound_2     FIFO   Verilog  SVA  FIFO.sv(159)     661 Covered
/top/DUT/cover__Pointer_Wraparound_1     FIFO   Verilog  SVA  FIFO.sv(158)    3292 Covered
/top/DUT/cover__Almost_Empty_Condition   FIFO   Verilog  SVA  FIFO.sv(157)   16079 Covered
/top/DUT/cover__Almost_Full_Condition    FIFO   Verilog  SVA  FIFO.sv(156)    8018 Covered
/top/DUT/cover__Full_Flag_Assertion      FIFO   Verilog  SVA  FIFO.sv(155)    9237 Covered
/top/DUT/cover__Empty_Flag_Assertion     FIFO   Verilog  SVA  FIFO.sv(154)   14192 Covered
/top/DUT/cover__Underflow_Detection      FIFO   Verilog  SVA  FIFO.sv(153)    1200 Covered
/top/DUT/cover__Overflow_Detection       FIFO   Verilog  SVA  FIFO.sv(152)    4030 Covered
/top/DUT/cover__Write_Acknowledge        FIFO   Verilog  SVA  FIFO.sv(151)   50760 Covered
/top/DUT/i_cover__150                    FIFO   Verilog  SVA  FIFO.sv(150)    8613 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 14

ASSERTION RESULTS:
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/top/a_reset         FIFO_TOP.sv(21)                    0          1
/top/DUT/assert__wr_rd_simul_full
                     FIFO.sv(147)                       0          1
/top/DUT/assert__wr_rd_simul_empty
                     FIFO.sv(146)                       0          1
/top/DUT/assert__Pointer_threshold
                     FIFO.sv(145)                       0          1
/top/DUT/assert__Pointer_Wraparound_3
                     FIFO.sv(144)                       0          1
/top/DUT/assert__Pointer_Wraparound_2
                     FIFO.sv(143)                       0          1
/top/DUT/assert__Pointer_Wraparound_1
                     FIFO.sv(142)                       0          1
/top/DUT/assert__Almost_Empty_Condition
                     FIFO.sv(141)                       0          1
/top/DUT/assert__Almost_Full_Condition
                     FIFO.sv(140)                       0          1
/top/DUT/assert__Full_Flag_Assertion
                     FIFO.sv(139)                       0          1
/top/DUT/assert__Empty_Flag_Assertion
                     FIFO.sv(138)                       0          1
/top/DUT/assert__Underflow_Detection
                     FIFO.sv(137)                       0          1
/top/DUT/assert__Overflow_Detection
                     FIFO.sv(136)                       0          1
/top/DUT/assert__Write_Acknowledge
                     FIFO.sv(135)                       0          1
/top/DUT/a_reset     FIFO.sv(82)                        0          1
/top/TEST/#ublk#182146786#19/immed__21
                     FIFO_tb.sv(21)                     0          1

Total Coverage By Instance (filtered view): 100.00%
```

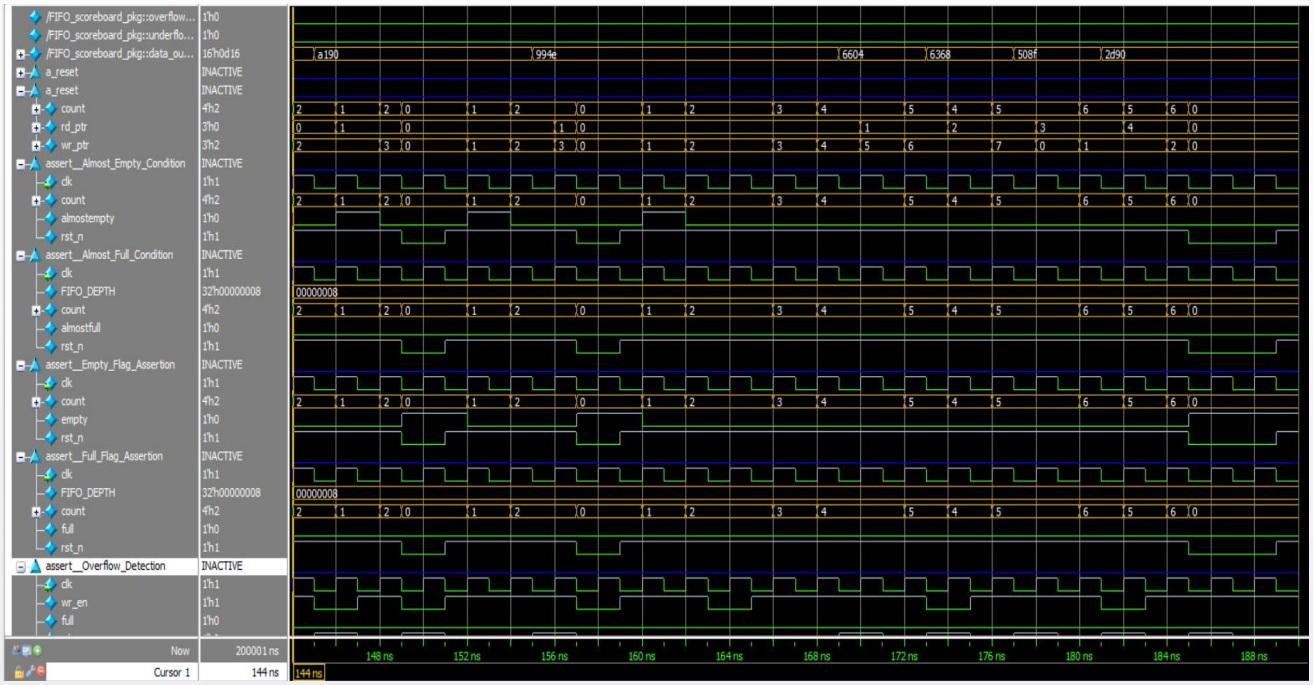
Waveform snippts:

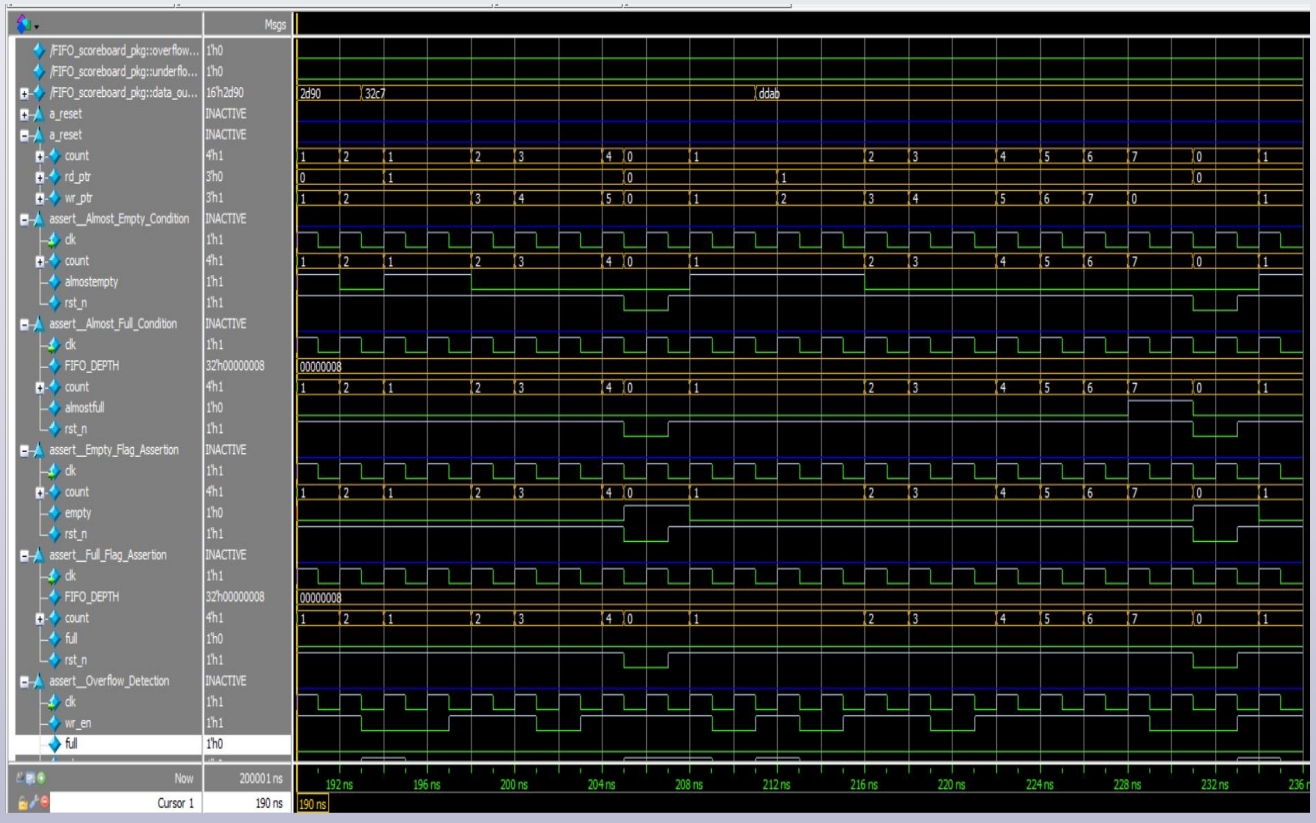





Msgs
clk
data_in
rst_n
wr_en
rd_en
data_out
wr_ack
overflow
full
empty
almostfull
almostempty
underflow
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
a_reset
a_reset
assert__Almost_Em...
assert__Almost_Full...
assert__Empty_Fla...
assert__Full_Flag_...
assert__Overflow_...
assert__Pointer_thr...
assert__Pointer_Wr...
assert__Pointer_Wr...
assert__Pointer_Wr...
assert__Underflow...
assert__wr_rd_sim...
assert__wr_rd_sim...
Now
Cursor 1
1'h1
16'h3ec3
1'h1
1'h1
1'h0
16'hfabd
1'h1
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
16'hfabd
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
200001 ns
144 ns
b353 b6f2 b14a 3953 d2db 59c5 64ed 0afa e9f6 d46f 0d16 7afc 69f2 ec28 f940 159c 1883 5215 06c7 fe36 4ec9 68fa a190 981a
fabd 7f95 d46f 0d16
fabd 7f95 d46f 0d16
100 ns 104 ns 108 ns 112 ns 116 ns 120 ns 124 ns 128 ns 132 ns 136 ns 140 ns 144 ns


Msgs
clk
data_in
rst_n
wr_en
rd_en
data_out
wr_ack
overflow
full
empty
almostfull
almostempty
underflow
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
/FIFO_scoreboard_...
a_reset
a_reset
assert__Almost_Em...
assert__Almost_Full...
assert__Empty_Fla...
assert__Full_Flag_...
assert__Overflow_...
assert__Pointer_thr...
assert__Pointer_Wr...
assert__Pointer_Wr...
assert__Pointer_Wr...
assert__Underflow...
assert__wr_rd_sim...
assert__wr_rd_sim...
Now
Cursor 1
1'h1
16'h981a
1'h1
1'h1
1'h0
16'h0d16
1'h1
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
16'h0d16
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
INACTIVE
200001 ns
144 ns
852d 4fb4 62b0 994e 6b1f 0d5c cb64 6604 6368 6671 508f 2d90 f252 ffa5 9e01 f8e3 a30b b1d7 0dc8 22cd 09e3 4a56 32c7 3deb
0d16 a190 994e 6604 6368 508f 2d90
a190 994e 6604 6368 508f 2d90
148 ns 152 ns 156 ns 160 ns 164 ns 168 ns 172 ns 176 ns 180 ns 184 ns 188 ns 192 ns
144 ns


/FIFO_scoreboard_pkg::overflow... 1'h0
/FIFO_scoreboard_pkg::underflo... 1'h0
/FIFO_scoreboard_pkg::data_ou... 16'h0d16
a_reset INACTIVE
a_reset INACTIVE
count 4'h2
rd_ptr 3'h0
wr_ptr 3'h2
assert__Almost_Empty_Condition INACTIVE
clk 1'h1
count 4'h2
almostempty 1'h0
rst_n 1'h1
assert__Almost_Full_Condition INACTIVE
clk 1'h1
FIFO_DEPTH 32'h00000008
count 4'h2
almostfull 1'h0
rst_n 1'h1
assert__Empty_Flag_Assertion INACTIVE
clk 1'h1
count 4'h2
empty 1'h0
rst_n 1'h1
assert__Full_Flag_Assertion INACTIVE
clk 1'h1
FIFO_DEPTH 32'h00000008
count 4'h2
full 1'h0
rst_n 1'h1
assert__Overflow_Detection INACTIVE
clk 1'h1
wr_en 1'h1
full 1'h0
a190
994e
6604
6368
508f
2d90
00000008
Now 200001 ns
Cursor 1 144 ns
148 ns
152 ns
156 ns
160 ns
164 ns
168 ns
172 ns
176 ns
180 ns
184 ns
188 ns
144 ns


Msgs
/FIFO_scoreboard_pkg::overflow... 1'h0
/FIFO_scoreboard_pkg::underflo... 1'h0
/FIFO_scoreboard_pkg::data_ou... 16'h2d90
a_reset INACTIVE
a_reset INACTIVE
count 4'h1
rd_ptr 3'h0
wr_ptr 3'h1
assert__Almost_Empty_Condition INACTIVE
clk 1'h1
count 4'h1
almostempty 1'h1
rst_n 1'h1
assert__Almost_Full_Condition INACTIVE
clk 1'h1
FIFO_DEPTH 32'h00000008
count 4'h1
almostfull 1'h0
rst_n 1'h1
assert__Empty_Flag_Assertion INACTIVE
clk 1'h1
count 4'h1
empty 1'h0
rst_n 1'h1
assert__Full_Flag_Assertion INACTIVE
clk 1'h1
FIFO_DEPTH 32'h00000008
count 4'h1
full 1'h0
rst_n 1'h1
assert__Overflow_Detection INACTIVE
clk 1'h1
wr_en 1'h1
full 1'h0
2d90
32c7
ddab
Now 200001 ns
Cursor 1 190 ns
192 ns
196 ns
200 ns
204 ns
208 ns
212 ns
216 ns
220 ns
224 ns
228 ns
232 ns
190 ns