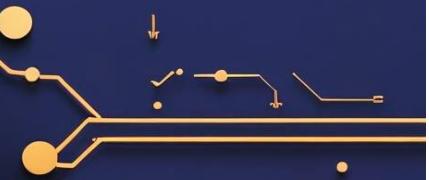


DIGITAL IC DESIGN PROJECT



SPI Slave with Single Port RAM

Prepared by: Marwan Yasser Rifaat Sadeek

Under the supervision of Eng. Kareem waseem

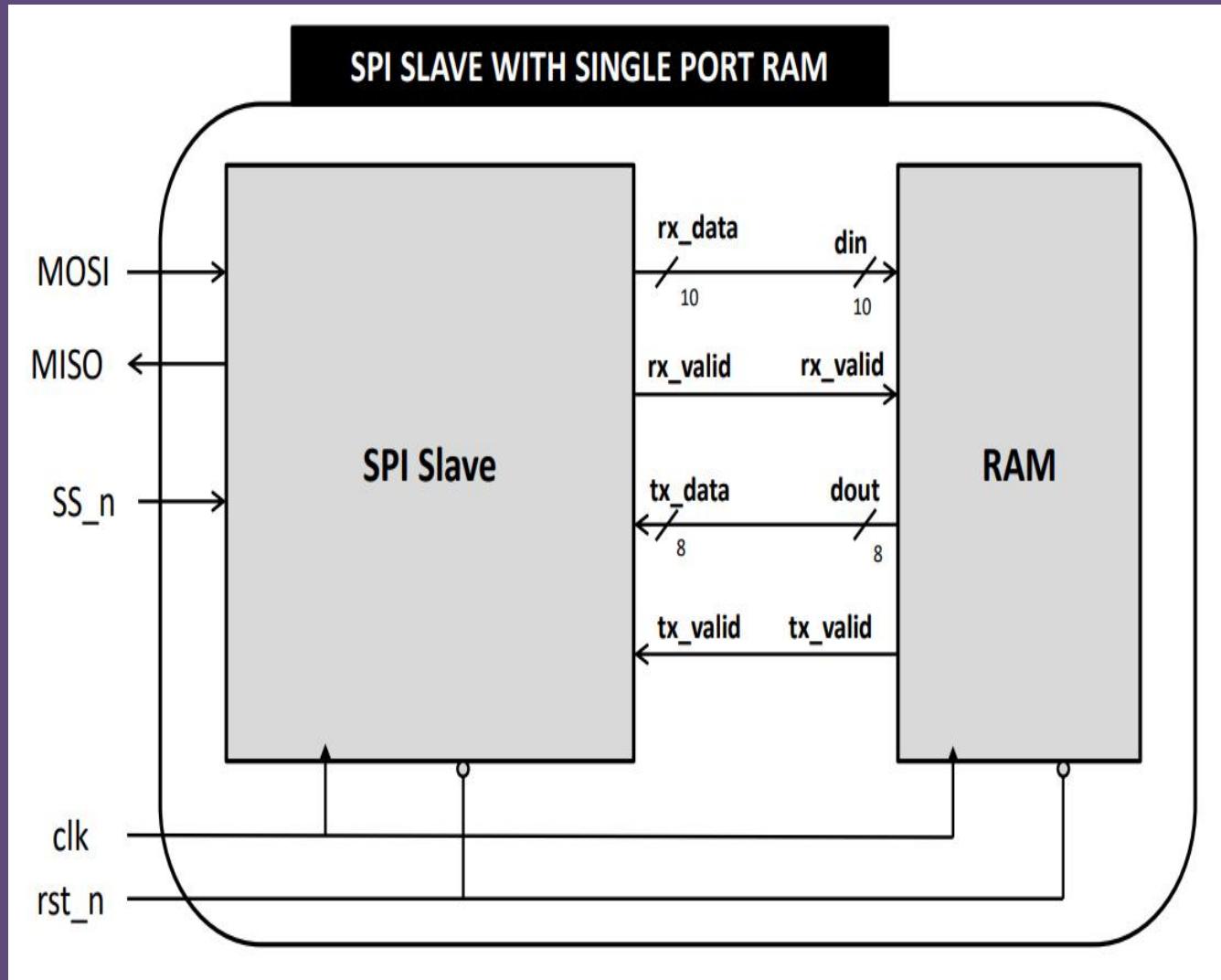
Introduction

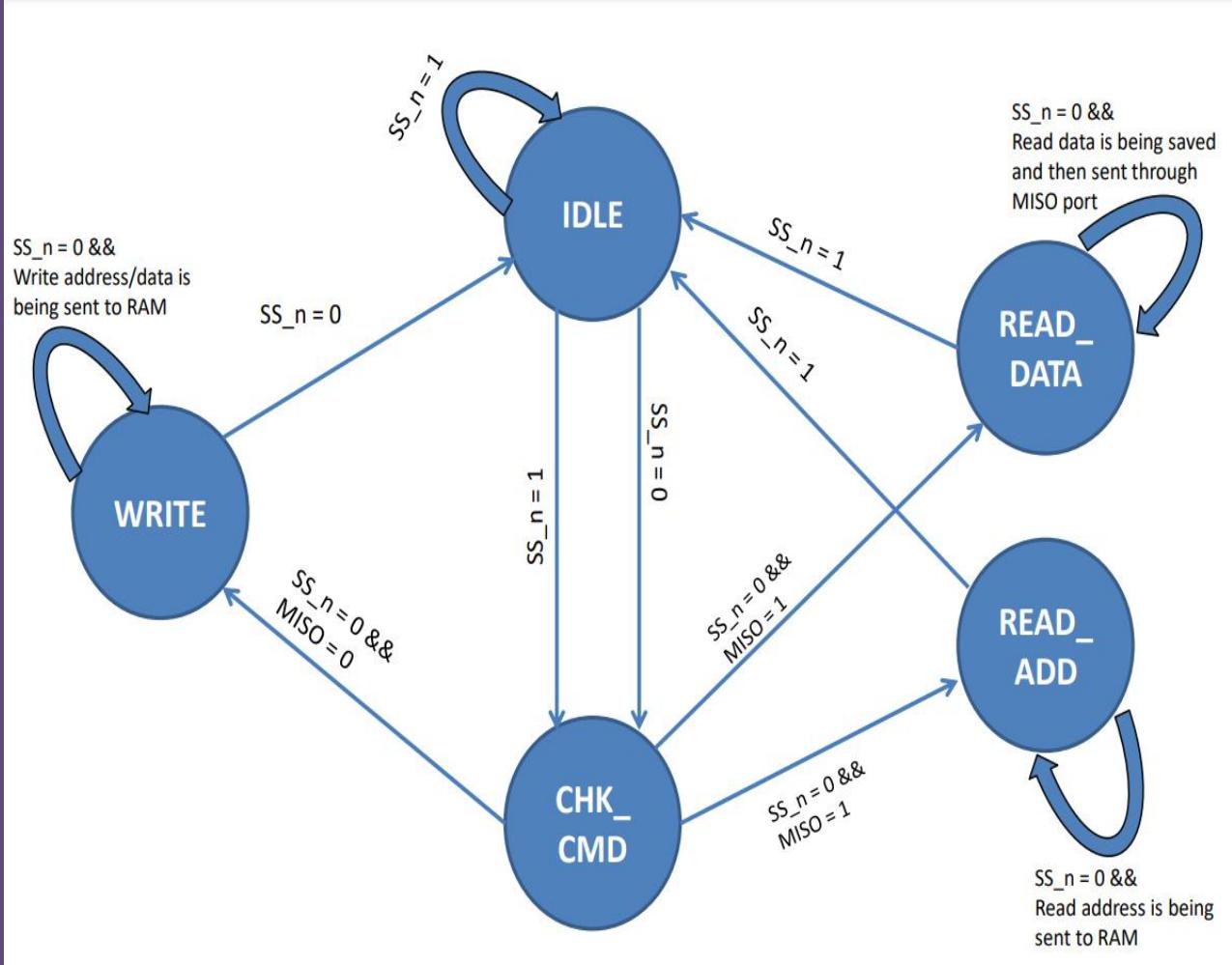
The Serial Peripheral Interface (SPI) is a widely used synchronous communication protocol that enables high-speed data exchange between a master device and peripheral components. In this project, an SPI Slave module is designed and integrated with a Single Port RAM to facilitate efficient data storage and retrieval. The SPI Slave receives and transmits serial data from the SPI Master, converting it into parallel format for RAM operations. The Single Port RAM serves as a temporary data buffer, enabling storage of received data and retrieval of stored data for transmission. This design finds applications in embedded systems, sensor data logging, configuration storage, and high-speed data acquisition systems.

Objective

The primary objective of this project is to implement and verify an SPI Slave module interfaced with a Single Port RAM to achieve reliable, synchronized, and efficient data transfer between an SPI Master and memory storage. Specific goals include:

- Designing an SPI Slave capable of receiving and transmitting data according to SPI protocol specifications.
- Implementing a Single Port RAM for temporary storage of received data and retrieval of stored data.
- Ensuring correct synchronization between the SPI interface and RAM operations.
- Verifying functional correctness through simulation and ensuring compatibility for FPGA implementation.





>>spi_slave

D: > DIPLOMA > Assigments > SPI_project > SPI_slave.v > SPI_slave

```
1  module SPI_slave(
2      input  MOSI,
3      output reg MISO,
4      input  ss_n,
5      input  clk,
6      input  rst_n,
7      input  [7:0] tx_data,
8      input          tx_valid,
9      output reg [9:0] rx_data,
10     output reg       rx_valid
11 );
12
13     parameter IDLE      =3'b000;
14     parameter CHK_CMD   =3'b001;
15     parameter WRITE     =3'b010;
16     parameter READ_ADD =3'b011;
17     parameter READ_DATA=3'b100;
18
19     (*fsm_encoding = "gray")
20 // (fsm_encoding = "one_hot")
21 // (fsm_encoding = "sequential")
22
23
24     reg [2:0] cs, ns;
25     reg      rd_check;
26     reg [3:0] counter ;
27     reg [2:0] counter2 ;
28     reg [9:0] rx_data_reg;
29     reg  rx_done;
30
31     always @ (posedge clk) begin
32         if (~rst_n)
33             cs <= IDLE;
34         else
35             cs <= ns;
36     end
```

```
36
37     always @(*) begin
38         case (cs)
39             IDLE:  ns = (~ss_n)?  CHK_CMD :  IDLE;
40
41             CHK_CMD: begin
42                 if (ss_n)
43                     ns = IDLE;
44                 else if (MOSI == 0)
45                     ns = WRITE;
46                 else if (MOSI == 1 && rd_check == 0)
47                     ns = READ_ADD;
48                 else if (MOSI == 1 && rd_check == 1)
49                     ns = READ_DATA;
50                 else
51                     ns = CHK_CMD;
52             end
53
54
55             WRITE: ns = (ss_n) ? IDLE : WRITE;
56
57             READ_ADD: ns = (ss_n) ? IDLE : READ_ADD;
58
59             READ_DATA:ns = (ss_n) ? IDLE : READ_DATA;
60
61         endcase
62     end
63
64     always @ (posedge clk) begin
65         if (~rst_n) begin
66             rx_data    <= 0;
67             rx_data_reg<=0;
68             rx_valid   <= 1'b0;
69             counter    <= 9;
70             counter2   <= 7;
71             rd_check   <= 0;
```

```
72           MISO      <= 1'b0;
73           rx_done<=0;
74       end else begin
75
76           case (cs)
77               IDLE: begin
78                   rx_valid<=0;
79                   counter <= 9;
80                   counter2 <= 7;
81                   rx_data_reg<=0;
82                   MISO<=1'b0;
83                   rx_done<=0;
84               end
85
86               WRITE: begin
87                   rx_data_reg[counter] <= MOSI;
88                   if (counter > 0) begin
89                       counter <= counter - 1;
90                   end
91                   else begin
92                       rx_valid <= 1;
93                       rx_done<=1;
94                   end
95               end
96
97               READ_ADD: begin
98                   rx_data_reg[counter] <= MOSI;
99                   if (counter > 0) begin
100                      counter <= counter - 1;
101                  end else begin
102                      rx_valid<=1;
103                      rd_check<=1;
104                      rx_done<=1;
105                  end
106              end
107          end
```

```
108     READ_DATA: begin
109         rx_data_reg[counter] <= MOSI;
110         if (counter > 0) begin
111             counter <= counter - 1;
112         end
113         else begin
114             rx_valid <= 1;
115             rd_check<=0;
116             rx_done<=1;
117         end
118
119         if (tx_valid ==1) begin
120             rx_done<=0;
121             MISO <= tx_data[counter2];
122             if (counter2 > 0)
123                 counter2 <= counter2 - 1;
124         end
125     end
126 endcase
127
128     if (rx_done) begin
129         rx_data  <= rx_data_reg;
130         rx_valid <= 1;
131         rx_done  <= 0;
132     end else begin
133         rx_valid <= 0;
134     end
135
136 end
137 end
138 endmodule
139
```

```
D: > DIPLOMA > Assigments > SPI_project > V Ram.v > ...
1  module syn_ram(din,rx_valid_ram,dout,tx_valid_ram,clk_ram,rst_n_ram);
2
3  parameter MEM_DEPTH=256;
4  parameter ADD_SIZE=8;
5  input [9:0]din;
6  input rx_valid_ram,clk_ram,rst_n_ram;
7  output reg [7:0]dout;
8  output reg tx_valid_ram;
9
10 reg [7:0] mem[MEM_DEPTH-1:0];
11 reg [ADD_SIZE-1:0]rd_add;
12 reg [ADD_SIZE-1:0]wr_add;
13
14
15 always@(posedge clk_ram)begin
16   if(~rst_n_ram)begin
17     dout<=0;
18     tx_valid_ram<=0;
19   end
20   else begin
21     if(rx_valid_ram==1)begin
22       case(din[9:8])
23         2'b00: wr_add<=din[7:0];
24         2'b01:mem[wr_add]<=din[7:0];
25         2'b10:rd_add<=din[7:0];
26         2'b11:begin
27           dout<=mem[rd_add];
28           tx_valid_ram<=1;
29         end
30       endcase
31     end
32   end
33 end
34 endmodule
```

Project_2

>>spi_warpper_ram

Marwan Yasser Rifaat Sadeek

```
D:\DIPLOMA\Assigments\SPI_project> V SPI_Wrapper.v & spi_ram
1 module spi_ram(MOSI_main,MISO_main,SS_N,clk,RST_N);
2
3 parameter IDLE=3'b000;
4 parameter CHK_CMD=3'b001;
5 parameter WRITE=3'b010;
6 parameter READ_ADD=3'b011;
7 parameter READ_DATA=3'b100;
8
9
10 parameter MEM_DEPTH=256;
11 parameter ADD_SIZE=8;
12
13 input MOSI_main,SS_N,clk,RST_N;
14 output MISO_main;
15
16
17 wire rx_valid_main;
18 wire tx_valid_main;
19 wire [9:0]rx_data_main;
20 wire [7:0]tx_data_main;
21
22 syn_ram #(.MEM_DEPTH(MEM_DEPTH),.ADD_SIZE(ADD_SIZE))
23     my_ram(.din(rx_data_main),.rx_valid_ram(rx_valid_main),.dout(tx_data_main),
24         .tx_valid_ram(tx_valid_main),.clk_ram(clk),.rst_n_ram(RST_N));
25
26 SPI_slave #(.IDLE(IDLE),.CHK_CMD(CHK_CMD),.WRITE(WRITE),.READ_ADD(READ_ADD),.READ_DATA(READ_DATA))
27     spi(.MOSI(MOSI_main),.MISO(MISO_main),.ss_n(SS_N),.clk(clk),.rst_n(RST_N),.tx_data(tx_data_main),
28         .tx_valid(tx_valid_main),.rx_data(rx_data_main),.rx_valid(rx_valid_main));
29
30 endmodule
```

Project_2

Testbench

Marwan Yasser Rifaat Sadeek

```
D:\> DIPLOMA > Assigments > SPI_project > V spi_tb.v > spi_tb
 1 module spi_tb();
 2   parameter IDLE=3'b000;
 3   parameter CHK_CMD=3'b001;
 4   parameter WRITE=3'b010;
 5   parameter READ_ADD=3'b011;
 6   parameter READ_DATA=3'b100;
 7
 8
 9   parameter MEM_DEPTH=256;
10   parameter ADD_SIZE=8;
11
12   reg MOSI_main_tb,SS_N_tb,CLK_tb,RST_N_tb;
13   wire MISO_main_tb;
14
15
16
17   spi_ram #( .IDLE(IDLE), .CHK_CMD(CHK_CMD), .WRITE(WRITE), .READ_ADD(READ_ADD), .READ_DATA(READ_DATA))
18   | my_tb(.MOSI_main(MOSI_main_tb), .MISO_main(MISO_main_tb), .SS_N(SS_N_tb), .clk(CLK_tb), .RST_N(RST_N_tb));
19
20
21   initial begin
22     CLK_tb=0;
23     forever begin
24       #5 CLK_tb=~CLK_tb;
25     end
26   end
27
28   initial begin
29     RST_N_tb=0; MOSI_main_tb=0; SS_N_tb=1;
30     @(negedge CLK_tb)
31     RST_N_tb=1;
32
33     | repeat(10)  @(negedge CLK_tb);
34
35
36
37   | @(negedge CLK_tb);
38   | MOSI_main_tb=0;
39   | @(negedge CLK_tb);
40   | MOSI_main_tb=0;
41   | @(negedge CLK_tb);
42   | MOSI_main_tb=0;
43   | @(negedge CLK_tb);
44   | MOSI_main_tb=1;
45   | @(negedge CLK_tb);
46   | MOSI_main_tb=1;
47   | @(negedge CLK_tb);
48   | MOSI_main_tb=0;
49   | @(negedge CLK_tb);
50   | MOSI_main_tb=1;
51   | @(negedge CLK_tb);
52   | MOSI_main_tb=1;
53   | @(negedge CLK_tb);
54   | MOSI_main_tb=1;
55   | @(negedge CLK_tb);
56   | MOSI_main_tb=0;
57   | @(negedge CLK_tb);
58   | MOSI_main_tb=1;
59   | @(negedge CLK_tb);
60
61   | @(negedge CLK_tb);
62   | SS_N_tb=1;
63   | @(negedge CLK_tb);
64   | //////////////////////////////dd
65   | @(negedge CLK_tb);
66   | SS_N_tb=0;
67   | @(negedge CLK_tb);
68   | MOSI_main_tb=0;
69
70   | @(negedge CLK_tb);
71   | MOSI_main_tb=0;
72   | @(negedge CLK_tb);
73   | MOSI_main_tb=1;
```

Project 2

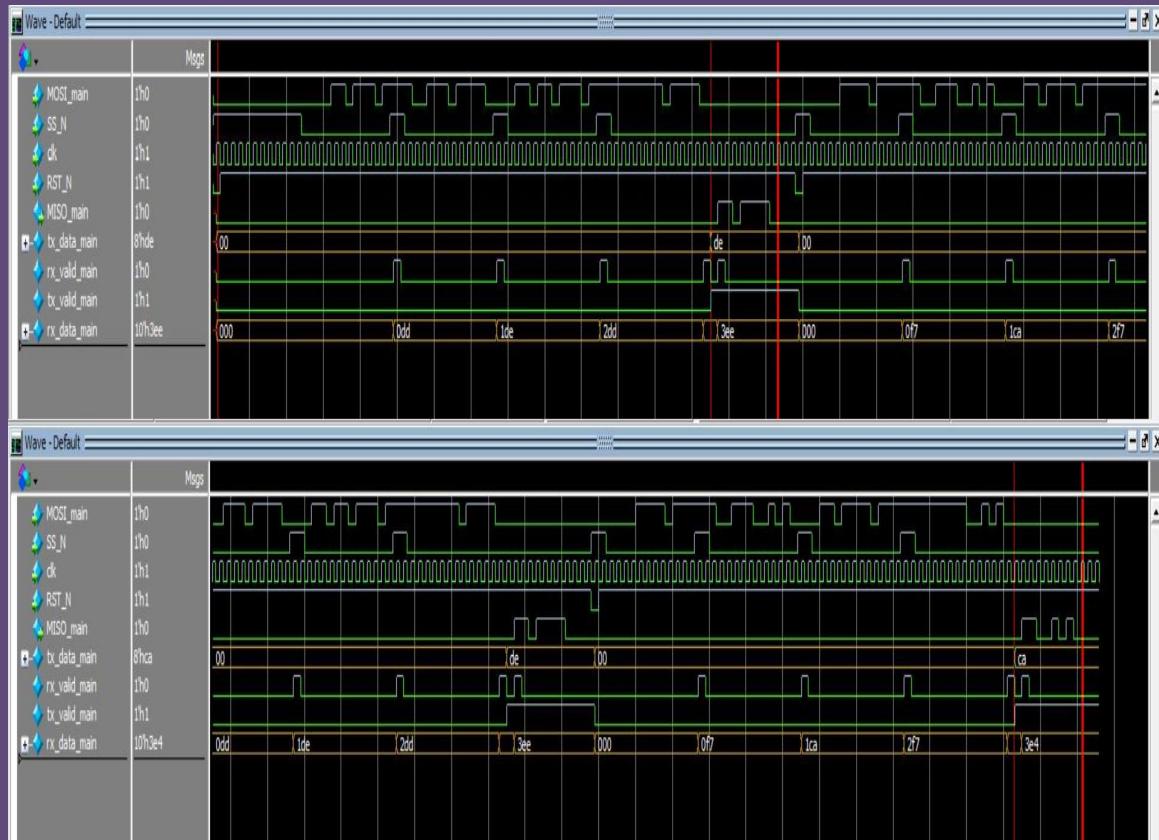
Marwan Yasser Rifaat Sadeek

```
74      @(negedge CLK_tb);
75      MOSI_main_tb=1;
76          @(negedge CLK_tb);
77      MOSI_main_tb=1;
78          @(negedge CLK_tb);
79      MOSI_main_tb=0;
80          @(negedge CLK_tb);
81      MOSI_main_tb=1;
82          @(negedge CLK_tb);
83      MOSI_main_tb=1;
84          @(negedge CLK_tb);
85      MOSI_main_tb=1;
86          @(negedge CLK_tb);
87      MOSI_main_tb=1;
88          @(negedge CLK_tb);
89      MOSI_main_tb=0;
90      ////////////////////miso=11011110  de
91          @(negedge CLK_tb);
92      SS_N_tb=1;
93
94          @(negedge CLK_tb);
95          @(negedge CLK_tb);
96      SS_N_tb=0;
97          @(negedge CLK_tb);
98      MOSI_main_tb=1;
99
100         @(negedge CLK_tb);
101     MOSI_main_tb=1;
102         @(negedge CLK_tb);
103     MOSI_main_tb=0;
104         @(negedge CLK_tb);
105     MOSI_main_tb=1;
106         @(negedge CLK_tb);
107     MOSI_main_tb=1;
108         @(negedge CLK_tb);
109     MOSI_main_tb=0;
110
111         @(negedge CLK_tb);
112     MOSI_main_tb=1;
113         @(negedge CLK_tb);
114     MOSI_main_tb=1;
115         @(negedge CLK_tb);
116     MOSI_main_tb=1;
117         @(negedge CLK_tb);
118     MOSI_main_tb=0;
119         @(negedge CLK_tb);
120     MOSI_main_tb=1;
121 //dd
122
123         @(negedge CLK_tb);
124     SS_N_tb=1;
125         @(negedge CLK_tb);
126
127         @(negedge CLK_tb);
128     SS_N_tb=0;
129         @(negedge CLK_tb);
130     MOSI_main_tb=1;
131         @(negedge CLK_tb);
132     MOSI_main_tb=1;
133         @(negedge CLK_tb);
134     MOSI_main_tb=1;
135         @(negedge CLK_tb);
136 //data
137         @(negedge CLK_tb);
138     MOSI_main_tb=1;
139         @(negedge CLK_tb);
140     MOSI_main_tb=1;
141         @(negedge CLK_tb);
142     MOSI_main_tb=0;
143         @(negedge CLK_tb);
144     MOSI_main_tb=1;
145         @(negedge CLK_tb);
```

Project 2

Marwan Yasser Rifaat Sadeek

```
146      MOSI_main_tb=1;
147      @(negedge CLK_tb);
148      MOSI_main_tb=1;
149      @(negedge CLK_tb);
150      MOSI_main_tb=1;
151      @(negedge CLK_tb);
152      MOSI_main_tb=0;
153      //de
154      repeat(12) @(negedge CLK_tb);
155
156
157      @(negedge CLK_tb);
158      SS_N_tb=1;
159
160
161      ///////////new test
162      RST_N_tb=0; MOSI_main_tb=0; SS_N_tb=1;
163      @(negedge CLK_tb)
164      RST_N_tb=1;
165
166
167      @(negedge CLK_tb);
168      SS_N_tb=0;
169      @(negedge CLK_tb);
170      MOSI_main_tb=0;
171      @(negedge CLK_tb);
172      MOSI_main_tb=0;
173      @(negedge CLK_tb);
174      MOSI_main_tb=0;
175      @(negedge CLK_tb);
176      MOSI_main_tb=1;
177      @(negedge CLK_tb);
178      MOSI_main_tb=1;
179      @(negedge CLK_tb);
180      MOSI_main_tb=1;
181      @(negedge CLK_tb);
182      MOSI_main_tb=1;
183      @(negedge CLK_tb);
184      MOSI_main_tb=0;
185      @(negedge CLK_tb);
186      MOSI_main_tb=1;
187      @(negedge CLK_tb);
188      MOSI_main_tb=1;
189      @(negedge CLK_tb);
190      MOSI_main_tb=1;
191
192      @(negedge CLK_tb);
193      SS_N_tb=1;
194      @(negedge CLK_tb);
195      ///////////
196      @(negedge CLK_tb);
197      SS_N_tb=0;
198      @(negedge CLK_tb);
199      MOSI_main_tb=0;
200
201      @(negedge CLK_tb);
202      MOSI_main_tb=0;
203      @(negedge CLK_tb);
204      MOSI_main_tb=1;
205      @(negedge CLK_tb);
206      MOSI_main_tb=1;
207      @(negedge CLK_tb);
208      MOSI_main_tb=1;
209      @(negedge CLK_tb);
210      MOSI_main_tb=0;
211      @(negedge CLK_tb);
212      MOSI_main_tb=0;
213      @(negedge CLK_tb);
214      MOSI_main_tb=1;
215      @(negedge CLK_tb);
216      MOSI_main_tb=0;
217      @(negedge CLK_tb);
```

1- QuestaSim Snippets

2- QuestaLint Snippet

Flow Navigator

Compile Design

This step will compile the design

Compile	Errors/Warnings
Status : Compilation Completed	Elapsed Time : 2601ms
Compile Design	

Status	Command	Results
✓	vlog D:/DIPLOMA/Final_project_Design/Ram.v -work work	0 Warning, 0 Error
✓	vlog D:/DIPLOMA/Final_project_Design/SPI_slave.v -work work	0 Warning, 0 Error
✓	vlog D:/DIPLOMA/Final_project_Design/SPI_Wrapper.v -work work	0 Warning, 0 Error

Select Methodology Compilation Progress 100%

File Edit View Design Metrics Window Help

Design D:/DIPLOMA/Final_project_Design/SPI_Wrapper.v [spi_ram]

Search: Type ...

Instance Mod

spi_ram (2) spi_r

```

1 module spi_ram(MOSI_main,MISO_main,SS_N,clk,RST_N);
2   parameter IDLE=3'b000;
3   parameter 0;
4   parameter CHK_CMD=3'b001;
5   parameter 1;
6   parameter WRITE=3'b010;
7   parameter 2;
8   parameter READ_ADD=3'b011;
9   parameter 3;
10  parameter READ_DATA=3'b100;
11  parameter 4;
12
13  parameter MEM_DEPTH=256;
14  256;
15  parameter ADD_SIZE=8;
16  8;
17
18  input MOSI_main,SS_N,clk,RST_N;
19
20  output MISO_main;
21
22  wire rx_valid_main;

```

Flow Na... D... SPI_Wrapper.v SPI_slave.v

Design Metrics

Quality Score: 100.0%

Design Readiness

	Design Readiness
Nomenclature Style	100.0%
Rtl Design Style	100.0%
Simulation	100.0%
Implementation	100.0%

Show Collated View

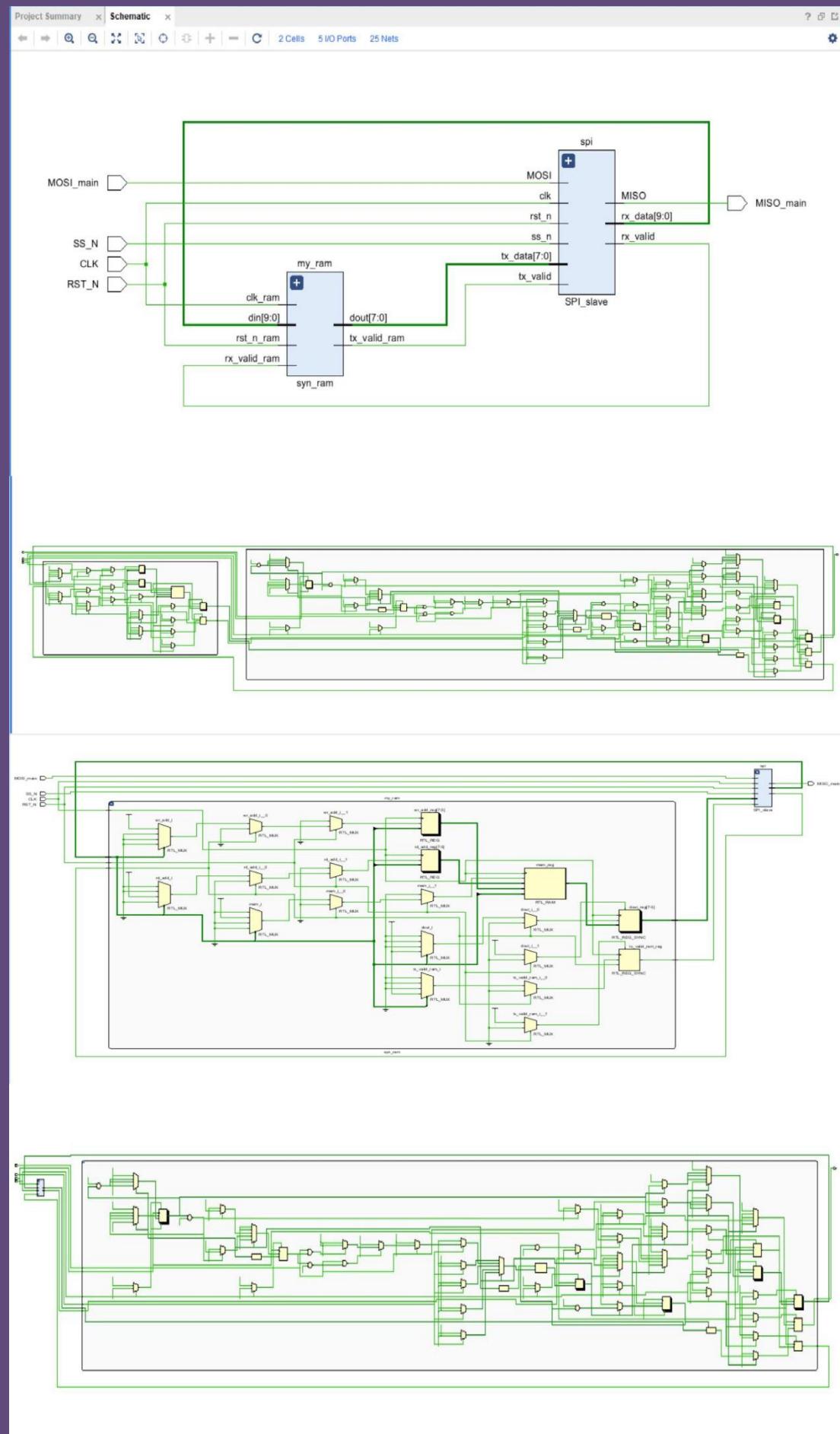
Lint Summary

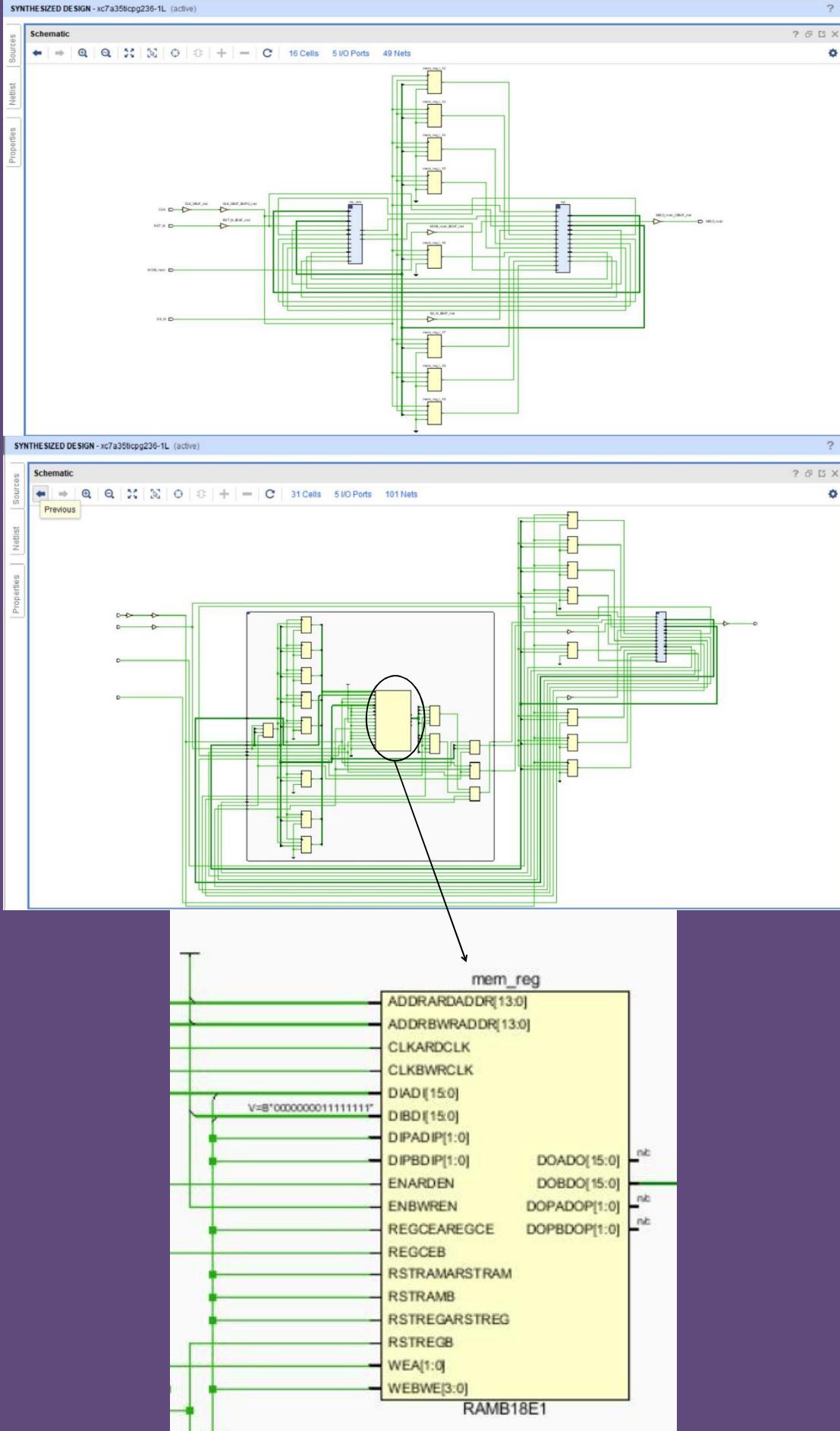
Type Search Text (Press Enter)

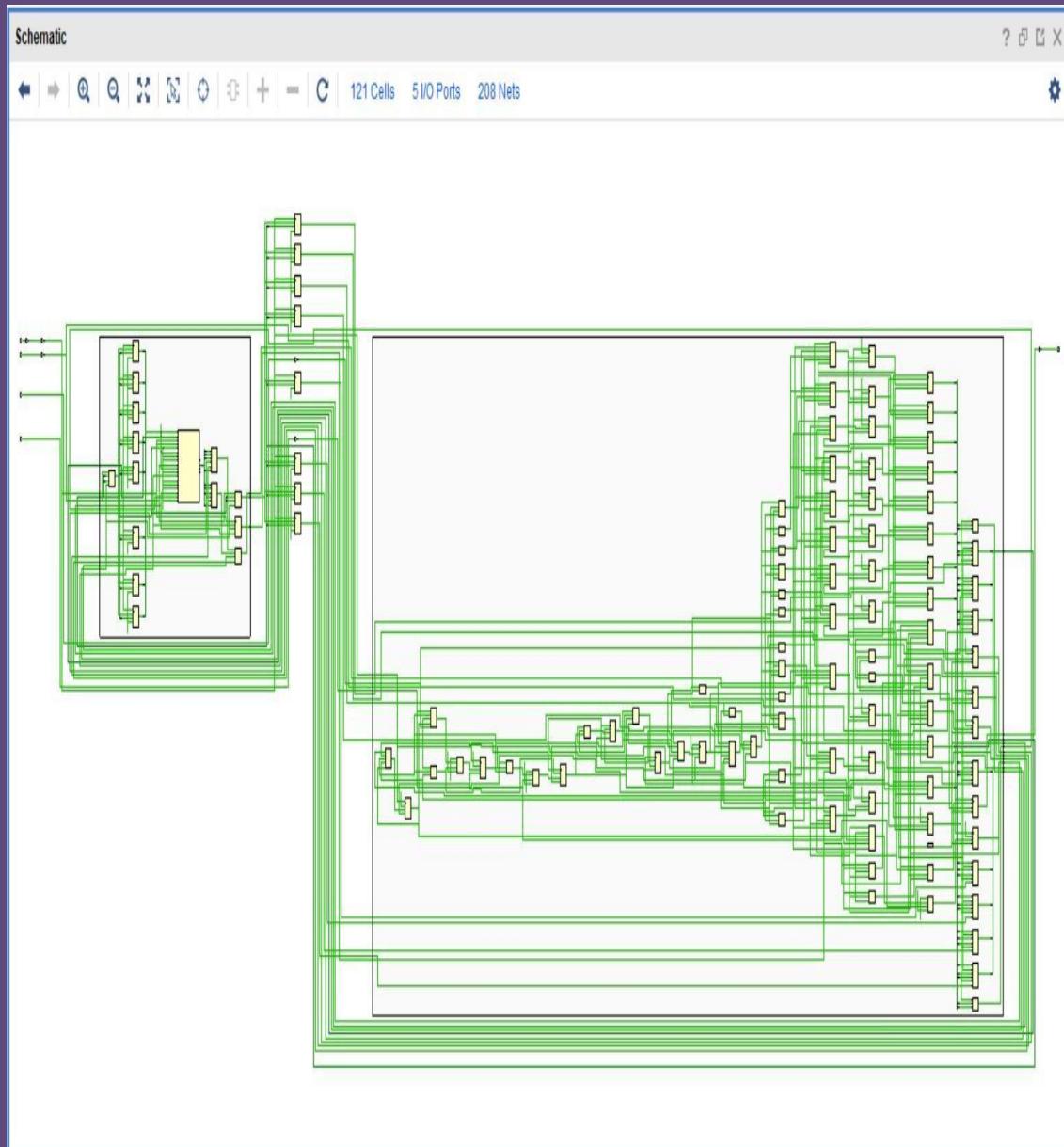
Name	Count
Resolved(verified, fixed, ...)	14
Info	14
parameter_name_du...	7
seq_block_has_duplic...	2
always_signal_assign...	1
line_char_larger...	2
multi_ports_in_single...	2

Filter: Clear Filters

Schematic after the elaboration



3) Synthesis snippets for each encoding :



1_ Gray-encoding

Schematic | synth_1_synth_synthesis_report_0 - synth_1 | D:/DIPLOMA/Final_project_Design/project_spi_3/project_spi_3/runs/synth_1/spi_ram.vds

Read-only |

```

91 -----
92 : Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:28 ; elapsed = 00:00:29 . Memory (MB): peak = 817.613 ; gain = 506.777
93 :
94 : INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
95 : INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
96 : INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
97 : INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
98 : INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
99 : INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
100: INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
101: INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
102: INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "yes" *) to avoid collis
103 -----
104 : State | New Encoding | Previous Encoding
105 -----
106: IDLE | 000 | 000
107: CHR_CMD | 001 | 001
108: WRITE | 011 | 010
109: READ_ADD | 010 | 011
110: READ_DATA | 111 | 100
111 -----
112: INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_slave'
113: WARNING: [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [D:/DIPLOMA/Final_project_Design/SPI_slave.v:35]
114:
115: Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:28 ; elapsed = 00:00:29 . Memory (MB): peak = 817.613 ; gain = 506.777
116 -----
117:
118: Report RTL Partitions:
119: +-----+
120: | RTL Partition | Replication | Instances |
121: +-----+
122: <-->

```

SYNTHESIZED DESIGN - xc7a35t-cpg236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | **Timing** | Debug | ? -

Design Timing Summary

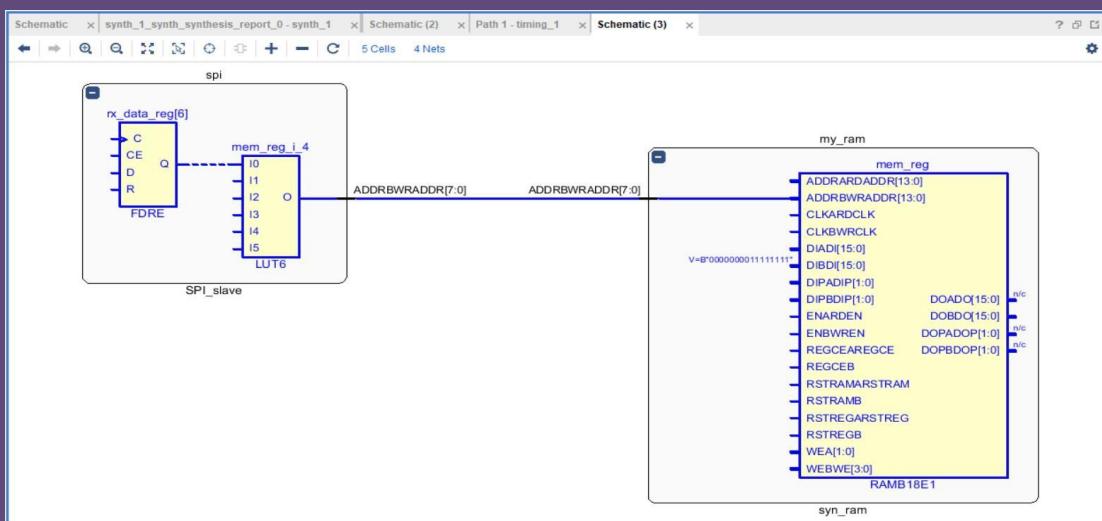
General Information		Setup	Hold	Pulse Width
Timer Settings		Worst Negative Slack (WNS): 6.714 ns	Worst Hold Slack (WHS): 0.152 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Design Timing Summary		Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Clock Summary (1)		Number of Falling Endpoints: 0	Number of Falling Endpoints: 0	Number of Falling Endpoints: 0
> Check Timing (16)		Total Number of Endpoints: 107	Total Number of Endpoints: 107	Total Number of Endpoints: 54
> Intra-Clock Paths				
Inter-Clock Paths				
Other Path Groups				
User Ignored Paths				
> Unconstrained Paths				

All user specified timing constraints are met.

Reports | Design Runs | **Utilization** | Timing | Debug | ? -

Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_ram		53	54	0.5	5	1
my_ram (syn_ram)		5	9	0.5	0	0
spi (SPI_slave)		48	37	0	0	0



2_ One-hot-encoding

Schematic x synth_1_synth_synthesis_report_0 - synth_1 x

D/DIPLOMA/Final_project_Design/project_spi8/project_spi8.rns/synth_1/spi_ram.vds

Read-only | |

```

94 ; -----
95 ; INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'.
96 ; INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
97 ; INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
98 ; INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
99 ; INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
100 ; INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
101 ; INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
102 ; INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "yes" *) to avoid collision
103 ; -----
104 ; State | New Encoding | Previous Encoding
105 -----
106 ; IDLE | 00001 | 000
107 ; CHK_CMD | 00010 | 001
108 ; WRITE | 00100 | 010
109 ; READ_ADD | 01000 | 011
110 ; READ_DATA | 10000 | 100
111 ; -----
112 ; INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_slave'
113 ; WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [D:/DIPLOMA/Final_project_Design/SPI_slave.v:39]
114 ; -----
115 ; Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:29 ; elapsed = 00:00:30 . Memory (MB): peak = 818.465 ; gain = 505.602
116 ; -----
117 ;
118 ; Report RTL Partitions:
119 ; +-----+
120 ; | RTL Partition | Replication | Instances |
121 ; +-----+
122 ; +-----+
123 ; -----
124 ; Start RTL Component Statistics
125 ; -----

```

Reports Design Runs Utilization x Timing Debug

Q % Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_ram		50	58	0.5	5	1
my_ram (syn_ram)		4	9	0.5	0	0
spi (SPI_slave)		46	41	0	0	0

Tcl Console Messages Log Reports Design Runs Timing x Debug

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (34)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

> Unconstrained Paths

Setup Hold Pulse Width

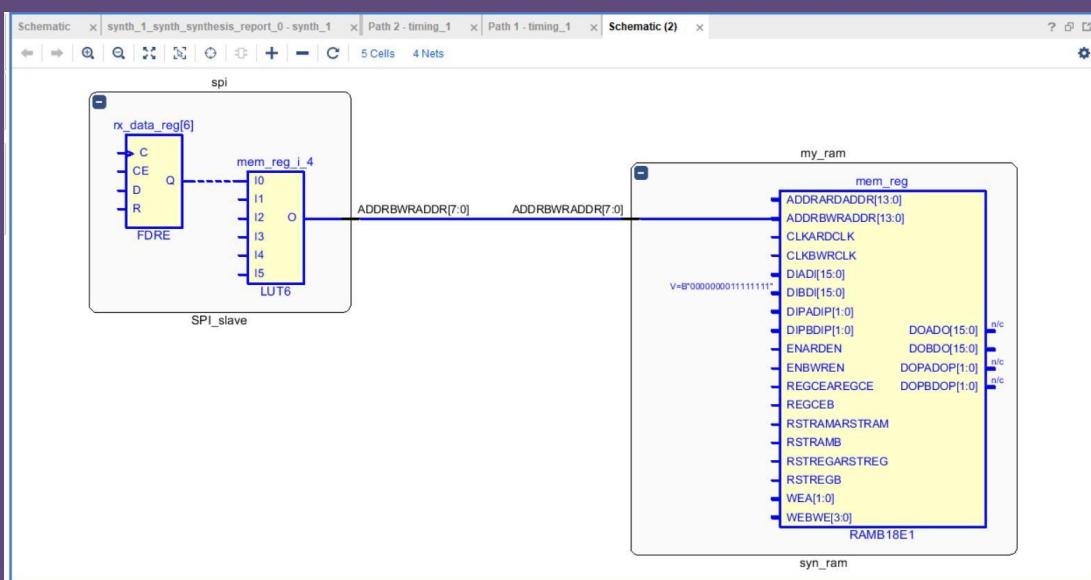
Worst Negative Slack (WNS): 6.714 ns Worst Hold Slack (WHS): 0.151 ns Worst Pulse Width Slack (WPWS): 4.500 ns

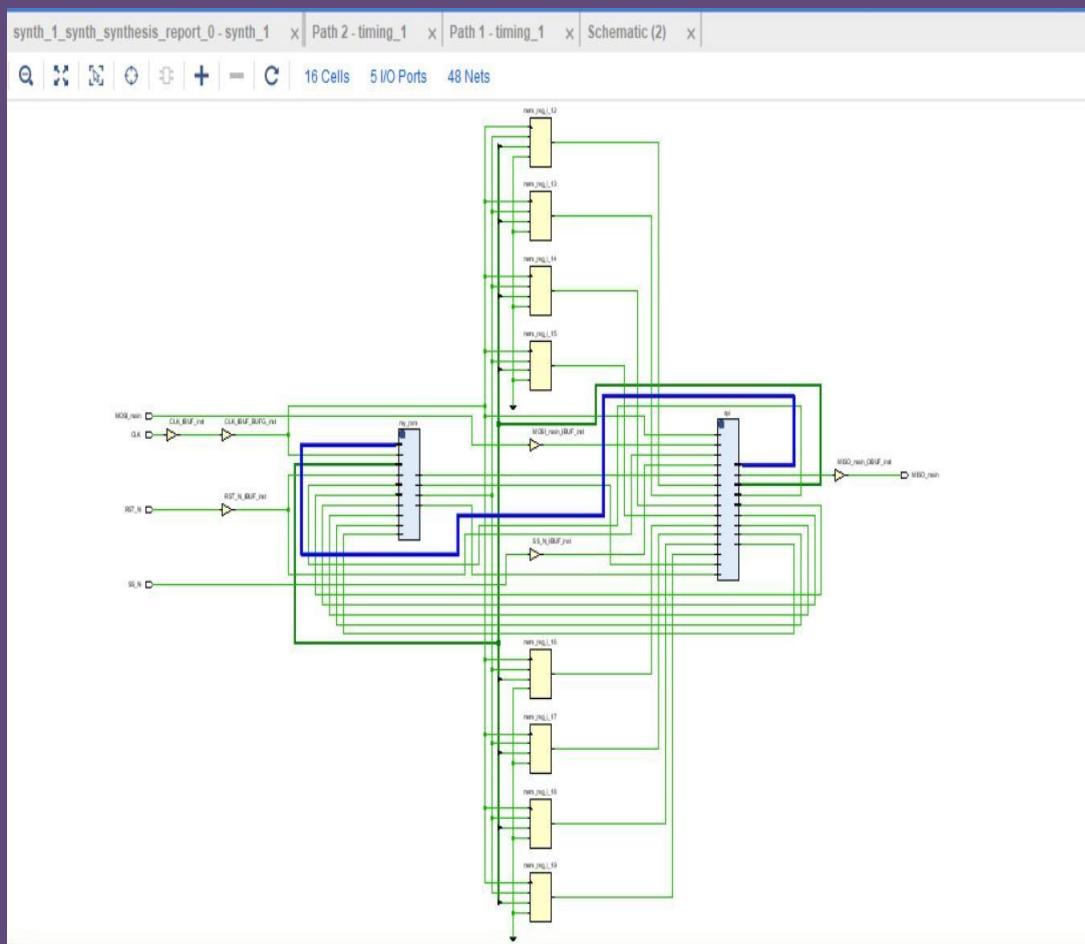
Total Negative Slack (TNS): 0.000 ns Total Hold Slack (THS): 0.000 ns Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0 Number of Failing Endpoints: 0 Number of Failing Endpoints: 0

Total Number of Endpoints: 107 Total Number of Endpoints: 107 Total Number of Endpoints: 56

All user specified timing constraints are met.





3_ Sequential-encoding

Schematic | synth_1_synth_synthesis_report_0 - synth_1 | D:/DIPLOMA/Final_project_Design/project_spi_sequential/project_spi_sequential/runs/synth_1/spi_ram.vds | Read-only |

```

91 Start Applying 'set_property' XDC Constraints
92 -----
93 -----
94 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:43 ; elapsed = 00:00:50 . Memory (MB): peak = 817.926 ; gain = 505.980
95 -----
96 [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
97 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
98 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
99 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
100 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
101 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
102 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
103 INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (' rw_addr_collision= "yes" ') to avoid collis
104 -----
105 State | New Encoding | Previous Encoding
106 -----
107 IDLE | 000 | 000
108 CHK_CMD | 001 | 001
109 WRITE | 010 | 010
110 READ_ADD | 011 | 011
111 READ_DATA | 100 | 100
112 -----
113 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_slave'
114 WARNING: [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_Reg' [D:/DIPLOMA/Final_project_Design/SPI_slave.v:39]
115 -----
116 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:43 ; elapsed = 00:00:50 . Memory (MB): peak = 817.926 ; gain = 505.980
117 -----
118 Report RTL Partitions:
119 +-----+-----+
120 | I RTL Partition | Replication | Instances |
121 +-----+-----+
122 <----->

```

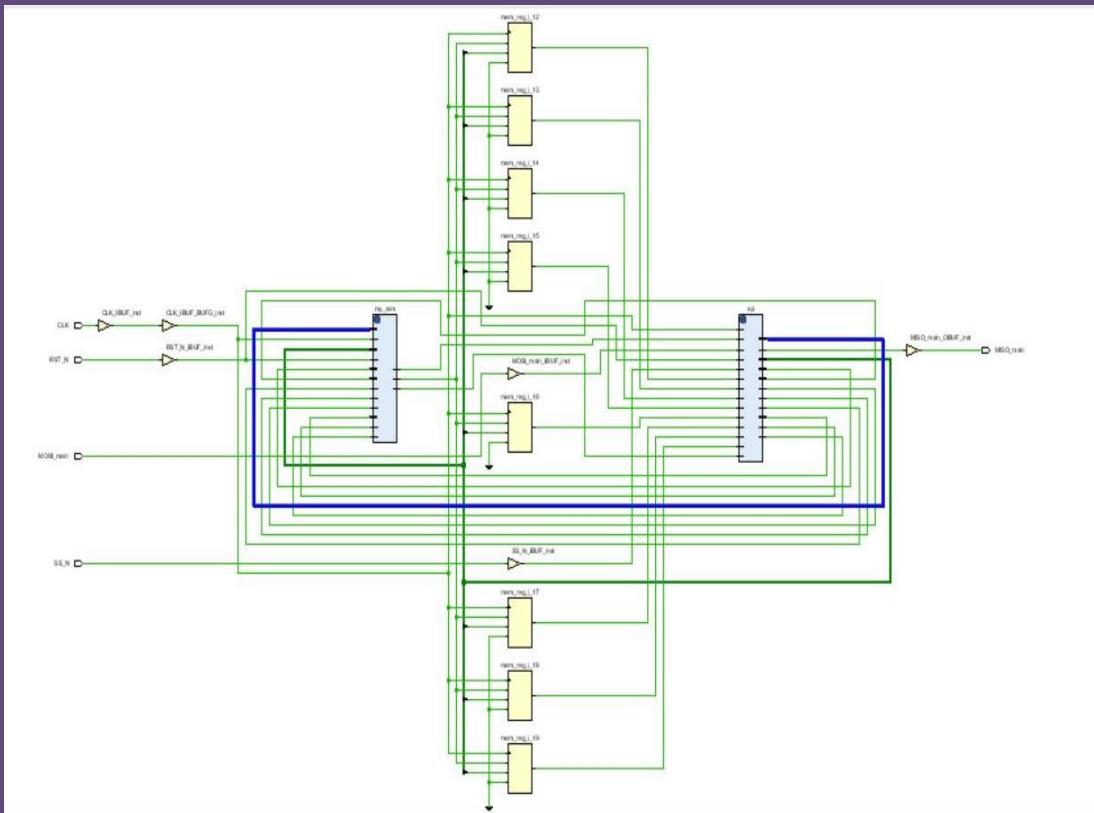
Timing | ? |

Design Timing Summary						
General Information	Setup		Hold		Pulse Width	
	Worst Negative Slack (WNS):	6.714 ns	Worst Hold Slack (WHS):	0.152 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Clock Summary(1)	Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWNS):	0.000 ns
> Check Timing (16)	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
> Intra-Clock Paths	Total Number of Endpoints:	107	Total Number of Endpoints:	107	Total Number of Endpoints:	54
Inter-Clock Paths						
Other Path Groups						
User Ignored Paths						
> Unconstrained Paths						
All user specified timing constraints are met.						

Hierarchy | ? |

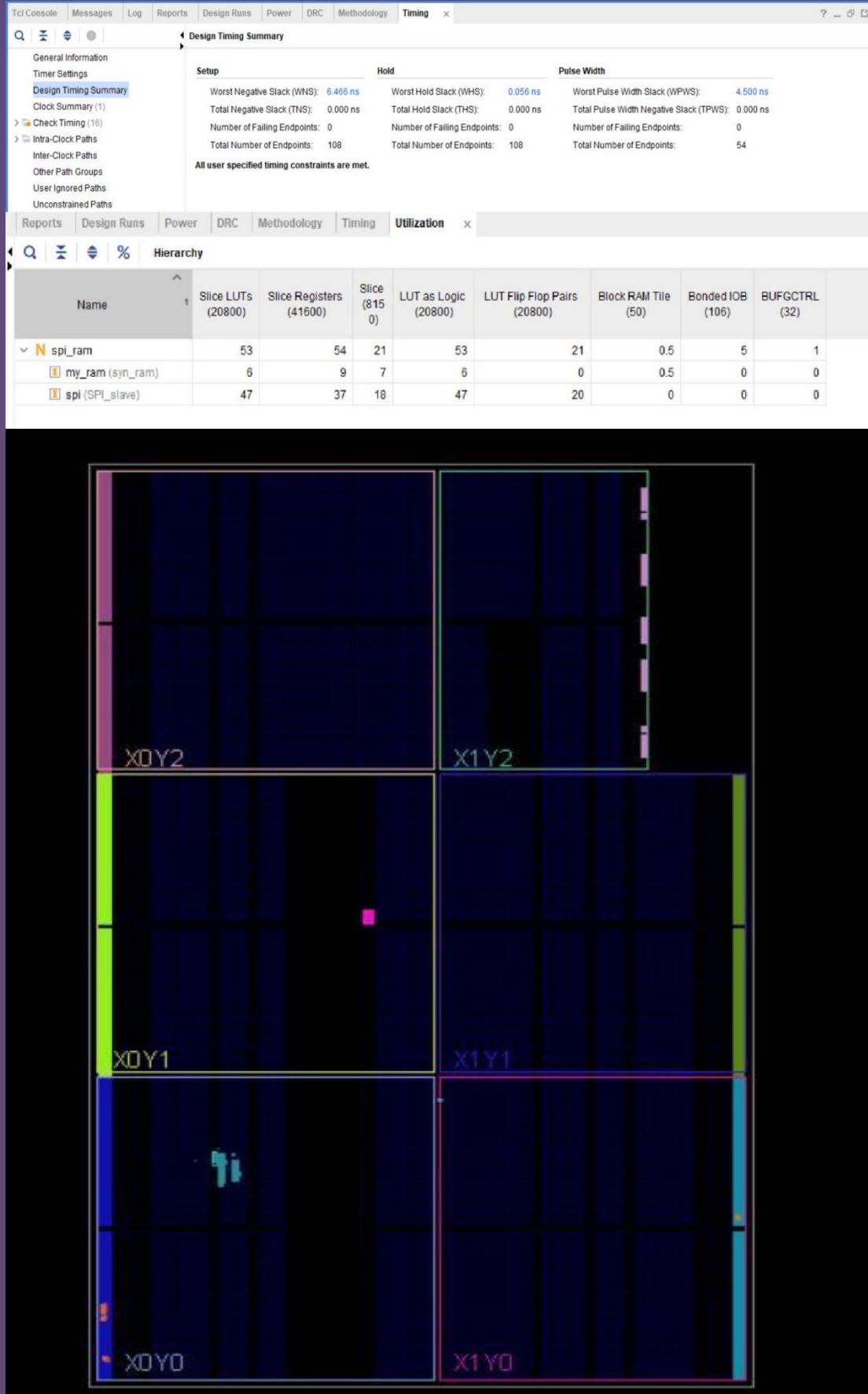
Name	1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_ram		51	54	0.5	5	1
my_ram (syn_ram)		5	9	0.5	0	0
spi (SPI_slave)		46	37	0	0	0

spi |

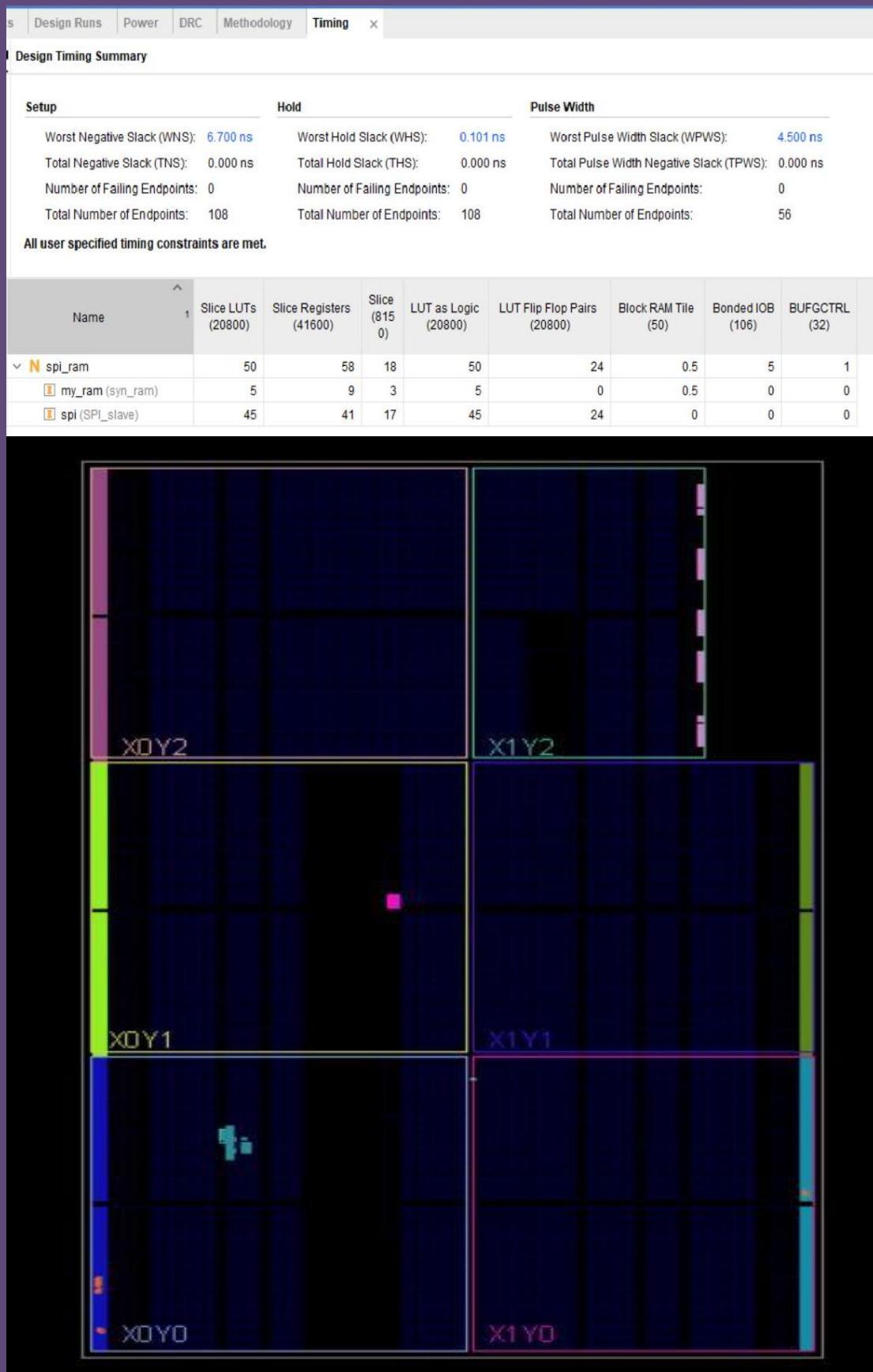


Implementation snippets:

1_ Gray-encoding



2_ One-hot-encoding

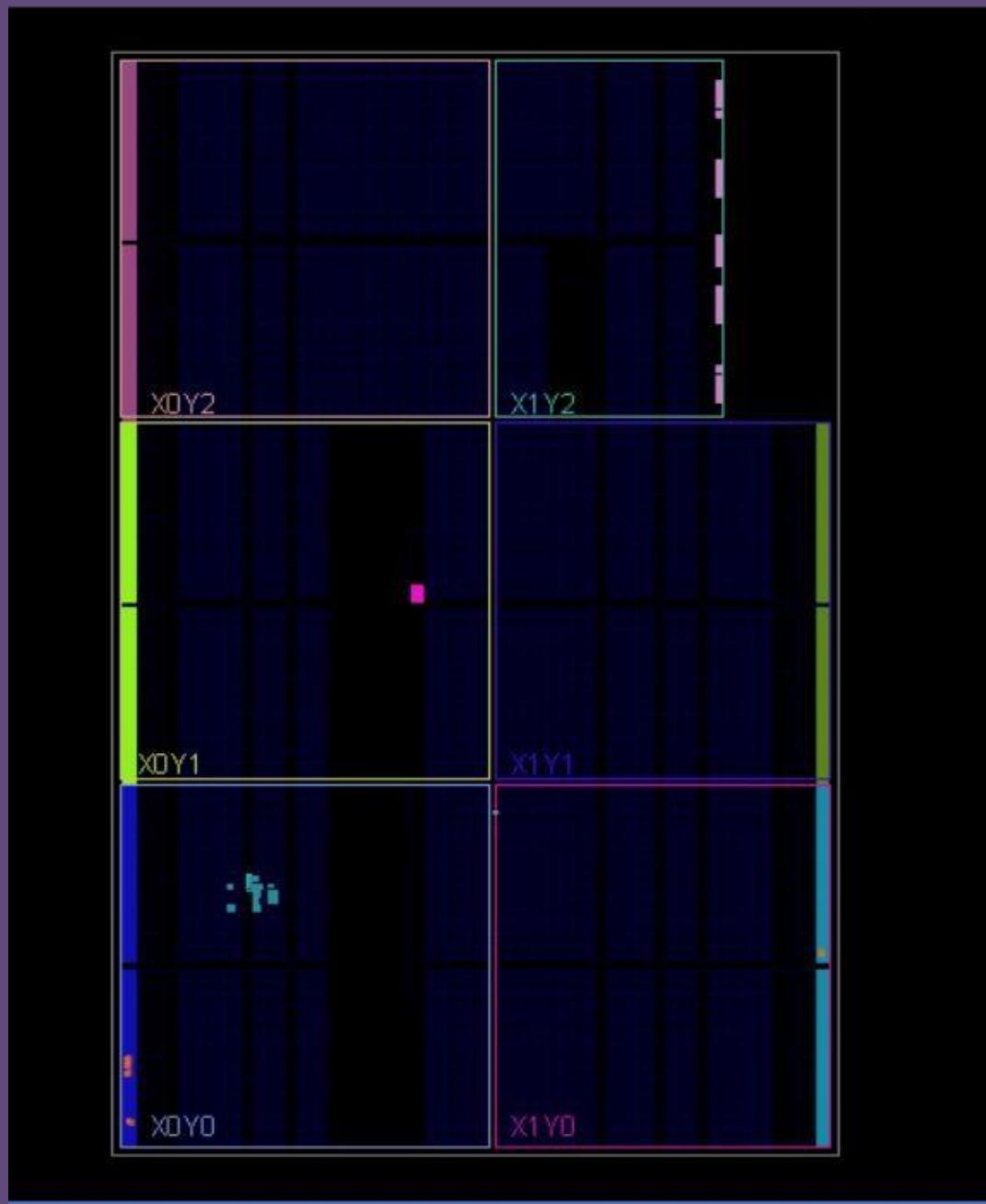


3_ Sequential-encoding

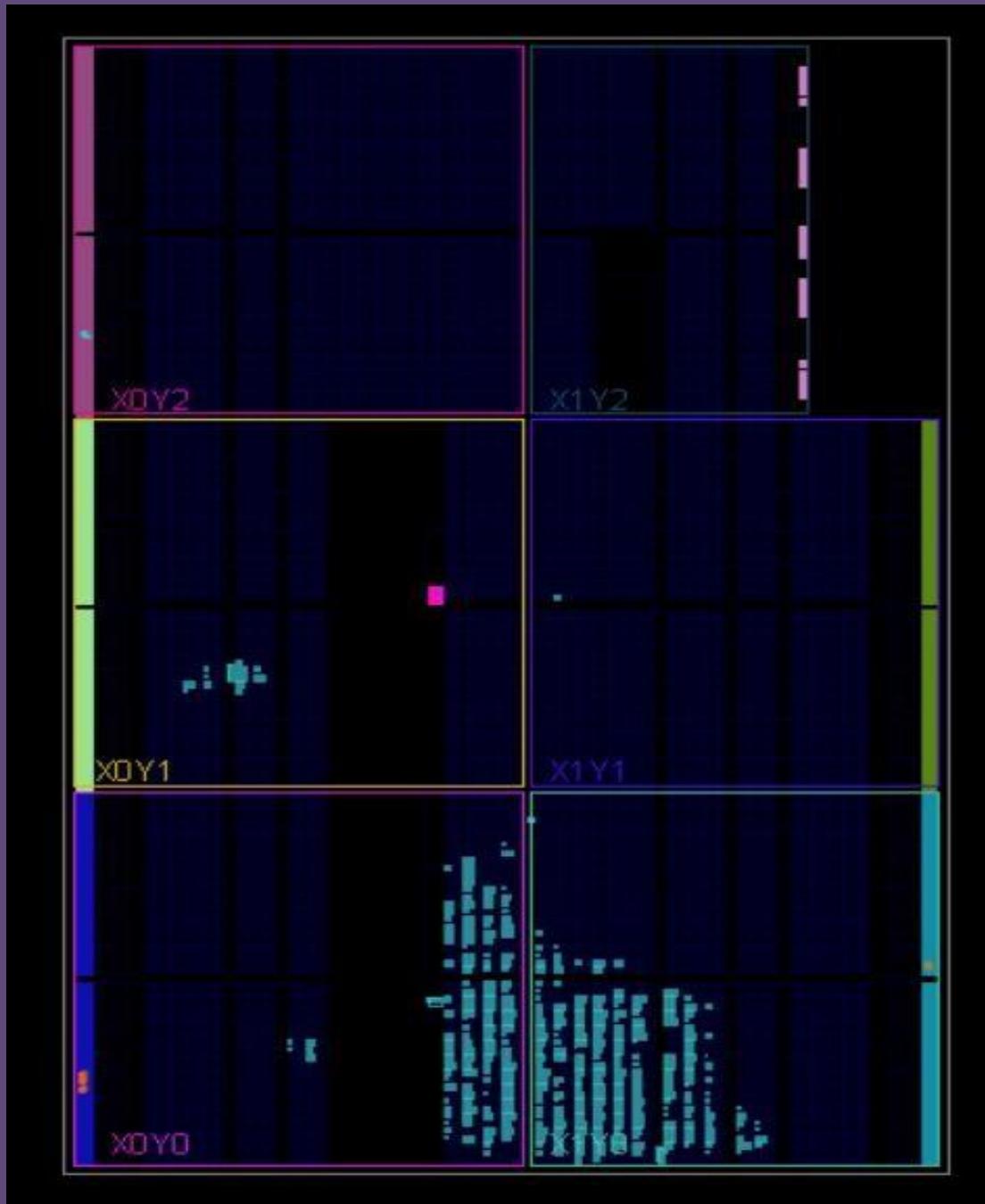
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.403 ns	Worst Hold Slack (WHS): 0.069 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 108	Total Number of Endpoints: 108	Total Number of Endpoints: 54

All user specified timing constraints are met.

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_ram	52	54	19	52		23	0.5	5	1
my_ram (syn_ram)	6	9	6	6		0	0.5	0	0
spi (SPI_slave)	46	37	17	46		22	0	0	0



➡ The Best Encoding is the one_hot_encoding:



5) Snippet of the “Messages” tab

```

▼ □ Vivado Commands (3 infos)
  ▼ □ General Messages (3 infos)
    ⓘ [IP_Flow 19-234] Refreshing IP repositories
    ⓘ [IP_Flow 19-1704] No user IP repositories specified
    ⓘ [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.

▼ □ Elaborated Design (12 infos)
  ▼ □ General Messages (12 infos)
    > ⓘ [Synth 8-6157] synthesizing module 'spi_ram' [SPI_Wrapper.v:1] (2 more like this)
    ⓘ [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI_slave.v:24]
    > ⓘ [Synth 8-155] case statement is not full and has no default [SPI_slave.v:38] (1 more like this)
    > ⓘ [Synth 8-6155] done synthesizing module 'syn_ram' (#1) [Ram.v:1] (2 more like this)
    ⓘ [Project 1-570] Preparing netlist for logic optimization
    ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    ⓘ [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

▼ □ Synthesized Design (6 infos)
  ▼ □ General Messages (6 infos)
    ⓘ [Netlist 29-17] Analyzing 5 Unisim elements for replacement
    ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
    ⓘ [Project 1-570] Preparing netlist for logic optimization
    ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    ⓘ [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

▼ □ Synthesis (2 warnings, 34 infos)
  ⓘ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
  > ⓘ [Synth 8-6157] synthesizing module 'spi_ram' [SPI_Wrapper.v:1] (2 more like this)
  ⓘ [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI_slave.v:24]
  > ⓘ [Synth 8-155] case statement is not full and has no default [SPI_slave.v:38] (1 more like this)
  > ⓘ [Synth 8-6155] done synthesizing module 'syn_ram' (#1) [Ram.v:1] (2 more like this)
  ⓘ [Device 21-403] Loading part xc7a35tcg236-1L
  ⓘ [Project 1-238] Implementation specific constraints were found while reading constraint file [D:/DIPLOMA/Final_project_Design/Constraints_basys3_new.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil spi_ram_propimpl.xdc].
  Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  ⓘ [Synth 8-602] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
  > ⓘ [Synth 8-554] ROM 'ns' won't be mapped to Block RAM because address size (3) smaller than threshold (5) (5 more like this)
  ⓘ [Synth 8-354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_slave'
  ⓘ [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [SPI_slave.v:39]
  > ⓘ [Synth 8-6430] The Block RAM mem._reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision="yes") to avoid collision (1 more like this)
  ⓘ [Project 1-571] Translating synthesized netlist
  ⓘ [Netlist 29-17] Analyzing 10 Unisim elements for replacement
  ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  > ⓘ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  > ⓘ [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed. (1 more like this)
  ⓘ [Common 17-83] Releasing license. Synthesis
  ⓘ [Constraints 18-5210] No constraint will be written out.
  ⓘ [Common 17-1381] The checkpoint D:/DIPLOMA/Final_project_Design/project_spi_44/project_spi_44.runs/synth_1/spi_ram.dcp has been generated.
  ⓘ [rundt-4] Executing : report_utilization -file spi_ram_utilization_rpt -pb spi_ram_utilization_synth.pb
  ⓘ [Common 17-206] Exiting Vivado at Mon Aug 4 00:16:52 2025.

```

```
Implementation (1 critical warning, 3 warnings, 100 infos)
  Design Initialization (11 infos)
    [Netlist 29-17] Analyzing 103 Unisim elements for replacement
    [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    [Project 1-479] Netlist was created with Vivado 2018.2
    [Device 21-403] Loading part xc7a35ticpg236-1L
    [Project 1-570] Preparing netlist for logic optimization
    [Timing 38-478] Restoring timing data from binary archive.
    [Timing 38-479] Binary timing data restore complete.
    [Project 1-856] Restoring constraints from binary archive.
    [Project 1-853] Binary constraint restore complete.
    [Project 1-111] Unisim Transformation Summary:
      A total of 54 instances were transformed.
      CFGlut5 => CFGlut5 (SRLC32E, SRL16E): 48 instances
      RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances
    [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  Opt Design (29 infos)
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
    [Project 1-461] DRC finished with 0 Errors
    [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    [Opt 31-49] Retargeted 0 cell(s).
    > [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
    > [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    > [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
    > [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
    > [Pwropt 34-9] Applying IDT optimizations ...
    > [Pwropt 34-10] Applying ODC optimizations ...
    > [Timing 38-35] Done setting XDC timing constraints.

    [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 2 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
    [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
    [Common 17-83] Releasing license: Implementation
    [Timing 38-480] Writing timing data to binary archive.
    [Common 17-1381] The checkpoint 'D:/DIPLOMA/Final_project_Design/project_spi_44/project_spi_44.runs/impl_1/spi_ram_opt.dcp' has been generated.
    [runrtl-4] Executing : report_drc -file spi_ram_drc_opted.rpt -pb spi_ram_drc_opted.pb -rpx spi_ram_drc_opted.rpx
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
    > [DRC 23-27] Running DRC with 2 threads (1 more like this)
    > [Corertl 2-168] The results of DRC are in file spi_ram_drc_opted.rpt.

  Place Design (24 infos)
    [Chipscope 16-240] Debug cores have already been implemented
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
    > [DRC 23-27] Running DRC with 2 threads (1 more like this)
    > [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
    > [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
    > [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
    > [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    > [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
    > [Physopt 32-65] No nets found for high-fanout optimization.
    > [Physopt 32-232] Optimized 0 net. Created 0 new instance.
    > [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
    > [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
    > [Place 30-746] Post Placement Timing Summary WNS=4.581. For the most accurate timing information please run report_timing.
    > [Common 17-83] Releasing license: Implementation
    > [Timing 38-480] Writing timing data to binary archive.
```

Project_2

Marwan Yasser Rifaat Sadeek

```
[Common 17-1381] The checkpoint 'D:/DIPLOMA/Final_project_Design/project_spi_44/project_spi_44.rns/impl_1/spi_ram_placed.dcp' has been generated.  
> [rundc-4] Executing : report_lj_file spi_ram_lj_placed.rpt (2 more like this)  
  Route Design (1 critical warning, 3 warnings, 36 infos)  
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'  
    [Vivado_Tcl 4-198] DRC finished with 0 Errors  
    [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.  
    [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs  
> [Route 35-416] Intermediate Timing Summary | WNS=4.606 | TNS=0.000 | WHS=1.242 | THS=-0.355| (5 more like this)  
  [Route 35-459] Router was unable to fix hold violation on 1 pins. This could be due to a combination of congestion, blockages and run-time limitations. Such pins are:  
    u_ilia_0/instrila_core_inst/probeDelay[10]_l_1/2  
  
    Resolution: You may try high effort hold fixing by turning on param route.enableGlobalHolder.  
  [Route 35-57] Estimated Timing Summary | WNS=2.419 | TNS=0.000 | WHS=-0.292 | THS=-0.292|  
  [Route 35-328] Router estimated timing not met.  
    Resolution: For a complete and accurate timing signoff, report_timing_summary must be run after route_design. Alternatively, route_design can be run with the -timing_summary option to enable a complete timing signoff at the end of route_design.  
  [Route 35-16] Router Completed Successfully  
  [Common 17-83] Releasing license: Implementation  
  [Timing 38-480] Writing timing data to binary archive.  
  [Common 17-1381] The checkpoint 'D:/DIPLOMA/Final_project_Design/project_spi_44/project_spi_44.rns/impl_1/spi_ram_routed.dcp' has been generated.  
> [DRC 23-27] Running DRC with 2 threads (1 more like this)  
  [CoreDc 2-168] The results of DRC are in file spi_ram_drc_routed.rpt.  
> [rundc-4] Executing : report_drc -file spi_ram_drc_routed.rpt -pb spi_ram_drc_routed.pb -pxp spi_ram_drc_routed.pxp (7 more like this)  
> [Timing 38-35] Done setting XDC timing constraints. (2 more like this)  
  [DRC 23-133] Running Methodology with 2 threads  
  [CoreDc 2-1520] The results of Report Methodology are in file spi_ram_methodology_drc_routed.rpt.  
  [Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.  
  [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.  
  [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.  
  [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.  
  [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.  
> [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)  
> [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)  
  Implemented Design (2 critical warnings, 2 warnings, 8 infos)  
  General Messages (2 critical warnings, 2 warnings, 8 infos)  
    [Netlist 29-17] Analyzing 103 Unisim elements for replacement  
    [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds  
    [Project 1-479] Netlist was created with Vivado 2018.2  
    [Project 1-570] Preparing netlist for logic optimization  
    [Timing 38-478] Restoring timing data from binary archive.  
    [Timing 38-479] Binary timing data restore complete.  
    [Project 1-856] Restoring constraints from binary archive.  
    [Project 1-853] Binary constraint restore complete.  
> [Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations. (1 more like this)  
  [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met. (1 more like this)
```