Memory IP Test Plan

IP Description:

The IP is a 16 × 32 bit memory. That is, a 16-word by 32-bit array. It allows read and write operations.

IP Signals Description:

Name	Direction	Size (bit)	Description
clk	input	1	**Clock Signal.**
rst_n	input	1	**Asynchronous Active LOW Reset Signal.** When LOW, the memory array is completely cleared (filled with zeros) and *data_out* and *valid_out* signals are driven LOW.
wr_en	input	1	**Data Write Enable Signal.** When HIGH, the value in *data_in* is written into the memory in the address specified in *address* signal.
data_in	input	32	**Input Data Signal.** Specifies the data to be written into the memory when *wr_en* signal is HIGH.
address	input	4	**Data Read and Write Address.** Specifies the address in and from which data is written or read.
data_out	output	32	**Output Data Signal.** Specifies the data read from the memory.

valid_out	output	1	**Valid Output Data Signal.** Specifies the validity of output data. Driven LOW when data is being written into the memory (*wr_en* signal is HIGH) or the memory has been reset (*rst_n* signal is LOW).

IP Test Items:

1- Reset:

- Set to 0: Memory array is completely cleared (filled with zeros).
- Set to 1: Memory array operates normally.

2- Enable:

- Set to 0: No write operation.
- Set to 1: Perform write operation.

3- Data:

- Valid input data.
- Invalid input data.

4- Address:

- Valid address
- Invalid address

IP Test Cases Definition

Test Name	*Reset*	*Enable*	*Data*	*Address*
test_01	reset	enabled	valid	valid
test_02	reset	enabled	valid	invalid
test_03	reset	enabled	invalid	valid
test_04	reset	enabled	invalid	invalid
test_05	reset	disabled	valid	valid
test_06	reset	disabled	valid	invalid
test_07	reset	disabled	invalid	valid
test_08	reset	disabled	invalid	invalid
test_09	no reset	enabled	valid	valid
test_10	no reset	enabled	valid	invalid
test_11	no reset	enabled	invalid	valid
test_12	no reset	enabled	invalid	invalid
test_13	no reset	disabled	valid	valid
test_14	no reset	disabled	valid	invalid
test_15	no reset	disabled	invalid	valid
test_16	no reset	disabled	invalid	invalid

IP Traceability Matrix:

Test Name	*Reset*		*Enable*		*Data*		*Address*	
	reset	no reset	enabled	disabled	valid	invalid	valid	invalid
test_01	☑		☑		☑		☑	
test_02	☑		☑		☑			☑
test_03	☑		☑			☑	☑	
test_04	☑		☑			☑		☑
test_05	☑			☑	☑		☑	
test_06	☑			☑	☑			☑
test_07	☑			☑		☑	☑	
test_08	☑			☑		☑		☑
test_09		☑	☑		☑		☑	
test_10		☑	☑		☑			☑
test_11		☑	☑			☑	☑	
test_12		☑	☑			☑		☑
test_13		☑		☑	☑		☑	
test_14		☑		☑	☑			☑
test_15		☑		☑		☑	☑	
test_16		☑		☑		☑		☑