# DSP

## 1-Design

## Wires name



BCOUT  M  CARRYOUT  CARRYOUTF

PCOUT

D:A:B Concatenated — Carry Cascade

D REG  Wd0

Pre-Adder/Subtracter

pre  B1 REG

Wb0  w  Wb1

wm  M REG

Wm2  X  X

A0 REG  Wa0  A1 REG  Wa1

Post-Adder/Subtracter

POST  REG

Z  Z

CIN  P

C REG  Dedicated C-Port  Wc0

CYI

Cin

Carry Cascade

opmode[6]  opmode[4]  opmode[5]  opmode[1:0]  opmode[7]

dedicated cascade (BCIN)  PCIN  CARRYIN  opmode[3:2]
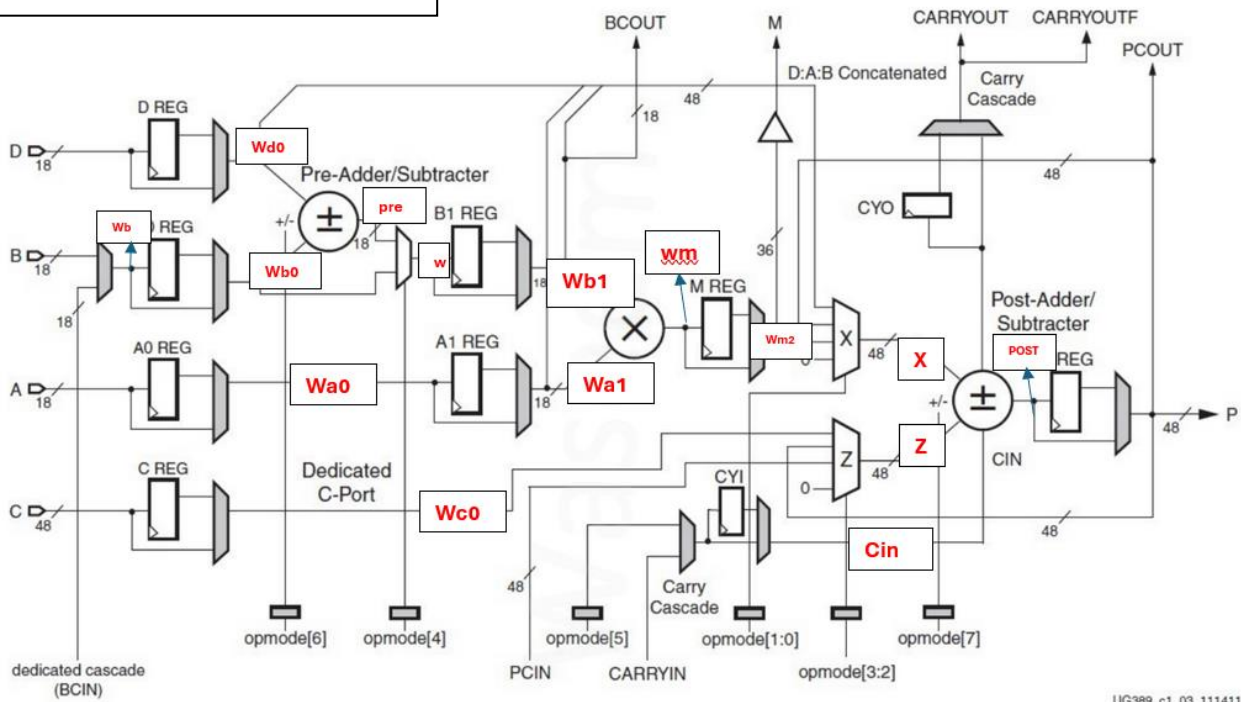
UG389_c1_03_111411

```verilog
module DSP (A,B,C,D,clk,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCI
input [17:0] A,B,D;
input [47:0] C;
input clk,CARRYIN;
input [7:0] OPMODE;
input [17:0] BCIN;
input RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
input [47:0]PCIN ;
output [17:0]BCOUT;
output [47:0]PCOUT;
output [47:0]P;
output [35:0]M;
output CARRYOUT;
output CARRYOUTF;
/////////////////////////////////////////////////////////////////////////////////////
parameter A0REG=0;
parameter A1REG=1;
parameter B0REG=0;
parameter B1REG=1;
parameter CREG=1;
parameter DREG=1;
parameter MREG=1;
parameter PREG=1;
parameter CARRYINREG=1;
parameter CARRYOUTREG=1;
parameter OPMODEREG=1;
parameter B_INPUT="DIRECT";
parameter CARRYINSEL="OPMODE5";
/////////////////////////////////////////////////////////////////////////////////////
reg [17:0] A0Q,A1Q;
wire [17:0] Wa0,Wa1;
assign Wa0=A0REG?A0Q:A ;
assign Wa1=A1REG?A1Q:Wa0 ;
///////////////////////////////////////////
reg [17:0] B0Q,B1Q;
wire [17:0] Wb0,Wb1,Wb;
wire [17:0] pre,w;
reg [17:0] DQ;
```

```verilog
reg [17:0] DQ;
wire [17:0] Wd0;

assign Wb=(B_INPUT=="DIRECT")?B:BCIN;
///////////

assign pre=OPMODE[6]?(Wd0-Wb0):(Wb0+Wd0);
assign w=OPMODE[4]?pre:Wb0;
///////////
assign Wb0=B0REG?B0Q:B ; // default Wb0=B just wire
assign Wb1=B1REG?B1Q:w ; // default Wb1=B1Q


/////////////////////////

assign Wd0=DREG?DQ:D ; // default wd0=DQ registered
/////////////////
reg [17:0] CQ;
wire [17:0] Wc0;
assign Wc0=CREG?CQ:C ; //default wc0=CQQ registered
/////////////////
wire [35:0]Wm2,Wm;
reg [35:0] MQ;
assign Wm=Wa1^Wb1;
assign Wm2=MREG?MQ:Wm ;
assign M=Wm2;
//////////////////////
wire [47:0] X,Z;
assign X=(OPMODE[1:0]==0)?0:(OPMODE[1:0]==1)?Wm2:(OPMODE[1:0]==2)?P:{6'b000000,D[11:0],A,B};
assign Z=(OPMODE[3:2]==0)?0:(OPMODE[3:2]==1)?PCIN:(OPMODE[3:2]==2)?P:Wc0;
////////////////////////////
wire carry_cascade,CIN;
reg CINQ;
assign carry_cascade=(CARRYINSEL=="OPMODE5")?OPMODE[5]:CARRYIN;
assign CIN=CARRYINREG?CINQ:carry_cascade;
////////////////////////////
wire [47:0] post;
assign post=OPMODE[7]?(Z-(X+CIN)):Z+X+CIN;
///////////
```

```verilog
always @(posedge clk ) begin
        if(RSTA==1)
                begin
                        A0Q<=0;
                        A1Q<=0;
                end
        else if ((CEA==1))
                begin
                        A0Q<=A;
                        A1Q<=Wa0;
                end



        if(RSTD==1)
                begin
                        DQ<=0;
                end
        else if ((CED==1))
                begin
                        DQ<=D;
                end


        if ((RSTB==1))
                begin
                        B0Q<=0;
                        B1Q<=0;
                end
        else if ((CEB==1))
                begin
                        B0Q<=Wb;
                        B1Q<=w;
                end


        if ((RSTC==1))
                begin
```

```verilog
if ((RSTC==1))
        begin
                CQ<=0;
        end
else if ((CEC==1))
        begin
                CQ<=C;
        end




if ((RSTM==1))
        begin
                MQ<=0;
        end
else if ((CEM==1))
        begin
                MQ<=Wm;
        end


if ((RSTCARRYIN==1))
        begin
                CINQ<=0;
        end
else if ((CECARRYIN==1))
        begin
                CINQ<=carry_cascade;
        end



if ((RSTP==1))
        begin
                PQ<=0;
        end
else if ((CEP==1))
```

```verilog
                begin
                        PQ<=post;
                end

end



endmodule
```

## 2-test bench
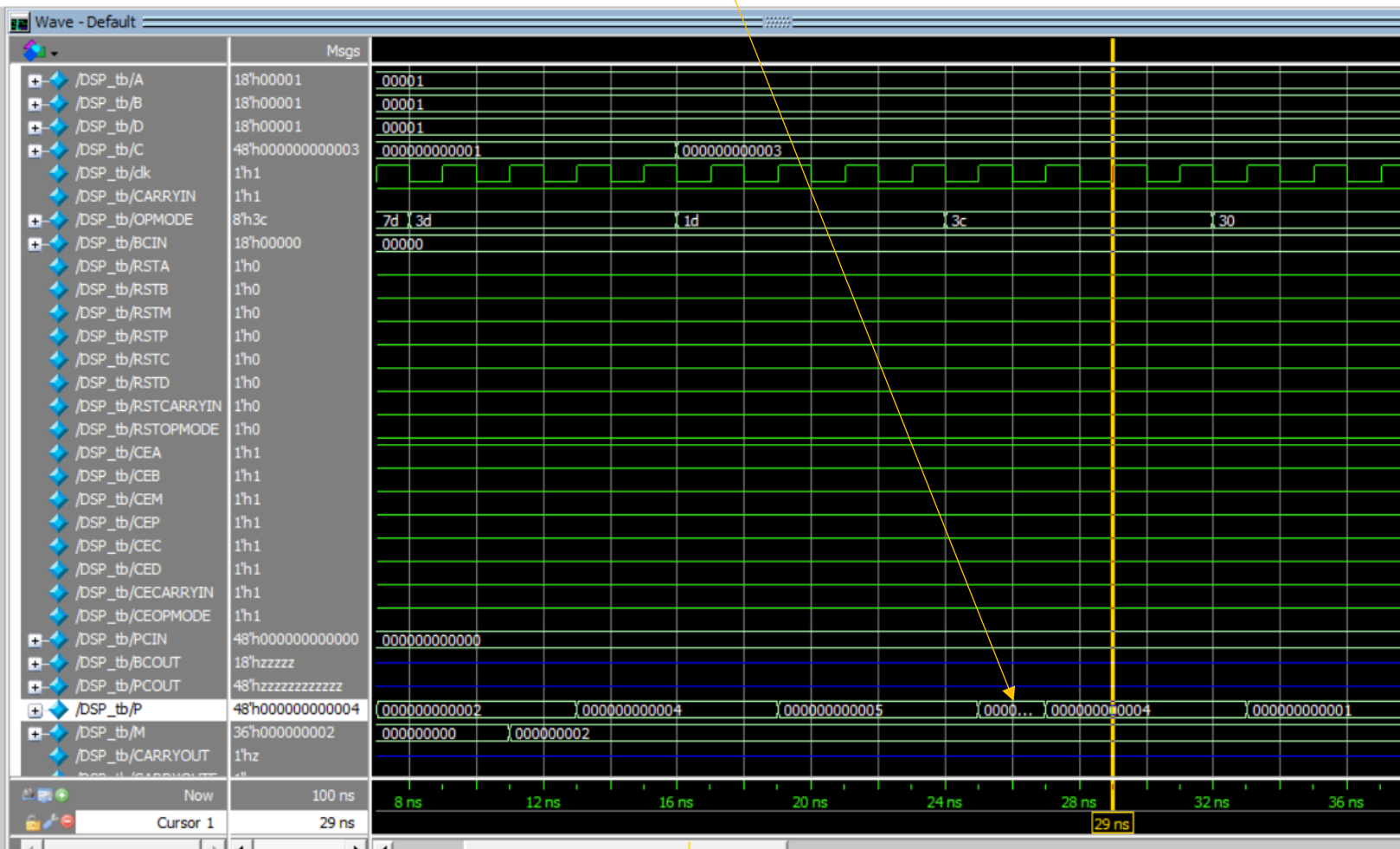
```verilog
module DSP_tb();

reg [17:0] A,B,D;
reg [47:0] C;
reg clk,CARRYIN;
reg [7:0] OPMODE;
reg [17:0] BCIN;
reg RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
reg [47:0] PCIN ;
wire [17:0]BCOUT;
wire [47:0]PCOUT;
wire [47:0]P;
wire [35:0]M;
wire CARRYOUT;
wire CARRYOUTF;
DSP DUT(A,B,C,D,clk,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCO

initial begin
        clk=0;
        forever
        #1 clk=~clk;
end

initial
begin

A=1;B=1;C=1;D=1;CARRYIN=1;OPMODE=8'b01111101;BCIN=0;RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;PCIN=0;
//p=[(B-D)^A+opmode[5]+c]=2
#8
A=1;B=1;C=1;D=1;CARRYIN=1;OPMODE=8'b00111101;BCIN=0;RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;PCIN=0;
//p=[(B+D)^A+opmode[5]+c]=4


#8

A=1;B=1;C=3;D=1;CARRYIN=1;OPMODE=8'b00011101;BCIN=0;RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;PCIN=0;
//p=[(B+D)^A+c]=5
#8

A=1;B=1;C=3;D=1;CARRYIN=1;OPMODE=8'b00111100;BCIN=0;RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;PCIN=0;
//p=c+opmode[5]=4

#8
A=1;B=1;C=3;D=1;CARRYIN=1;OPMODE=8'b00110000;BCIN=0;RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;PCIN=0;
//p=opmode[5]=1
#8
A=1;B=1;C=3;D=1;CARRYIN=1;OPMODE=8'b00010000;BCIN=0;RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;PCIN=0;
//p=opmode[5]=0


end
endmodule
```
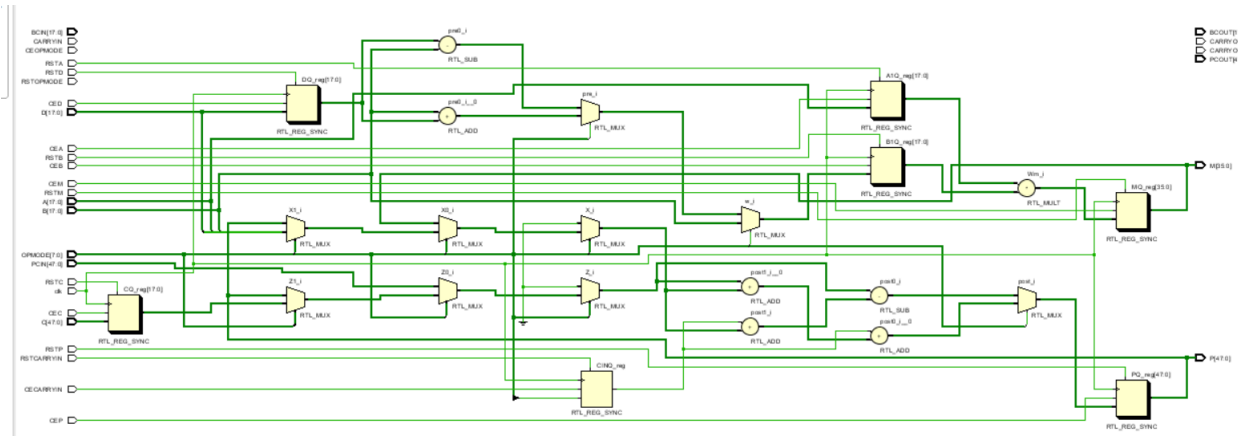
## 3-WaveForm

**Note: the output at max need for 4 rising edge to change but if we change 2 variable in different stage like D and C after 2 clock cycle just the change of C will effect the output so will appear at the output undesired value but after 4 clock cycle the change of all input will reach to the output so in summary the output may not be stable after change the output till 4 clock and that show in the wave form undesired value appear at the output for one clock cycle**

## 4-RTL analysis



## 5-Synthesis