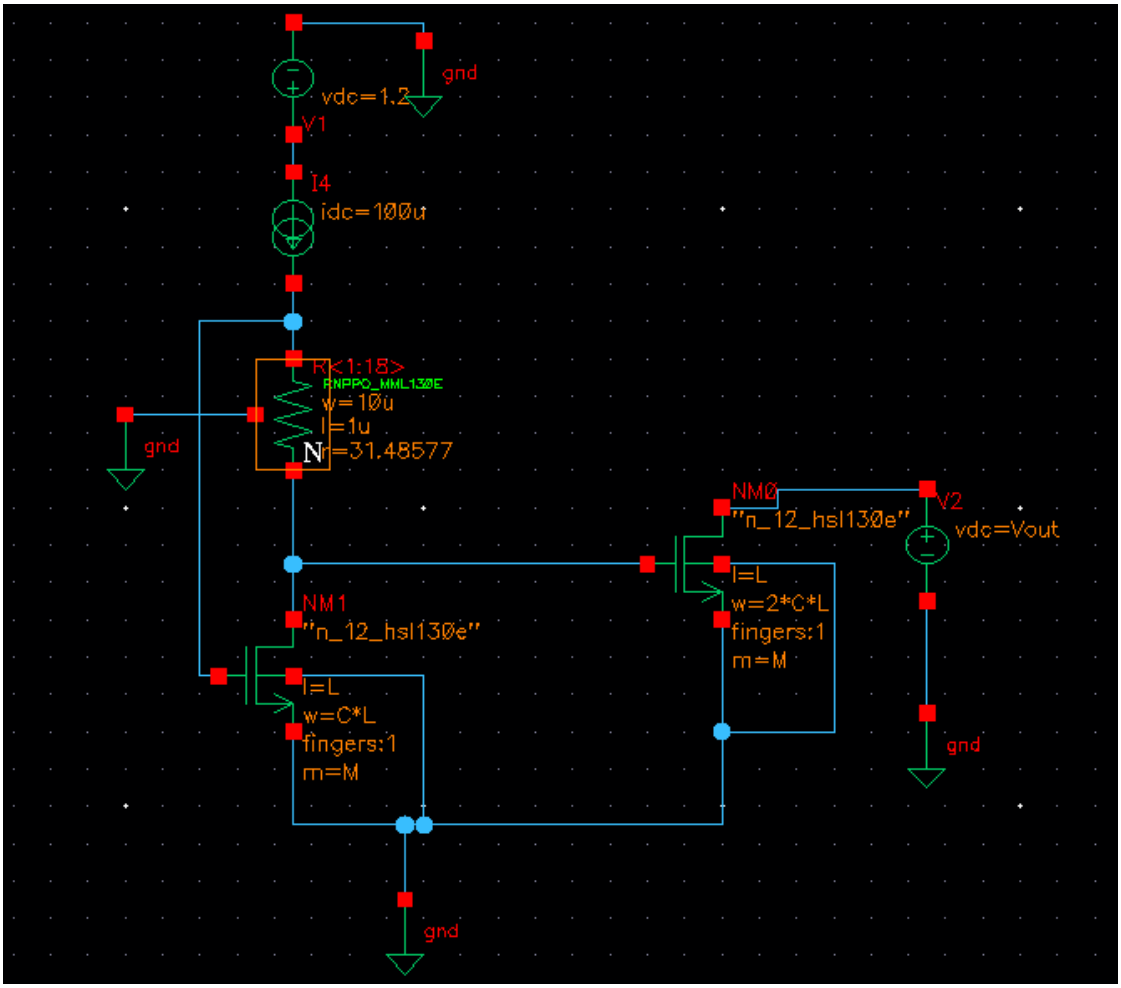
# Design 1

## 1. Schematic diagram with dimensions and component values annotated for both circuits...

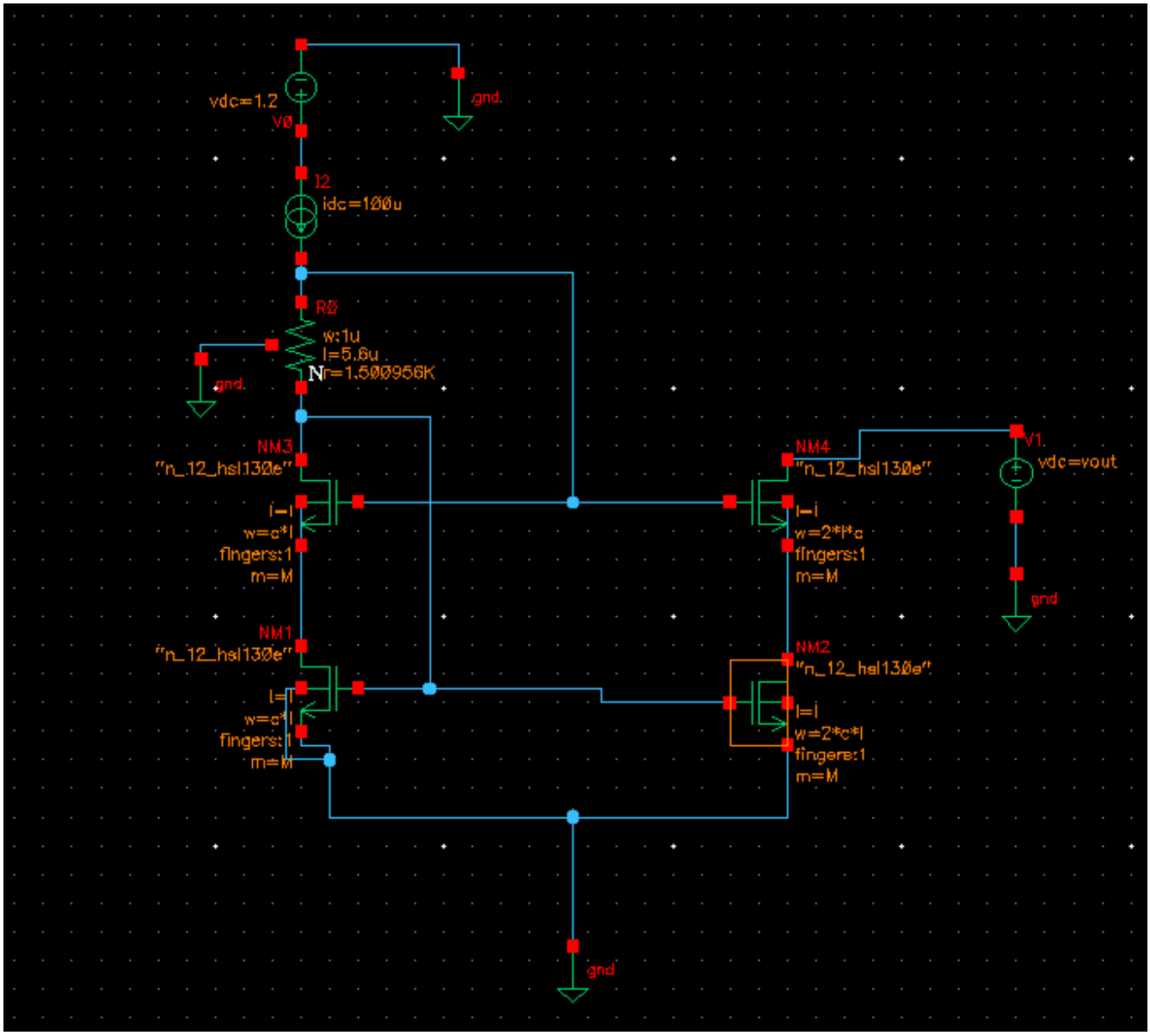



| | | |
|---|---|---|
| 1 | L | 50u |
| 2 | C | 1 |
| 3 | M | 40 |

**Notes: I put 18 Resistor in parallel with min resistor value to achieve Rtotal=1.5 and I requirement 6 I will explain in hand analysis steps why I choose Rtotal=1.5**

**-I sweep until I get the appropriate value of constant c but due to limitation on the width of technology I choose Multiplier to achieve the wanted width**

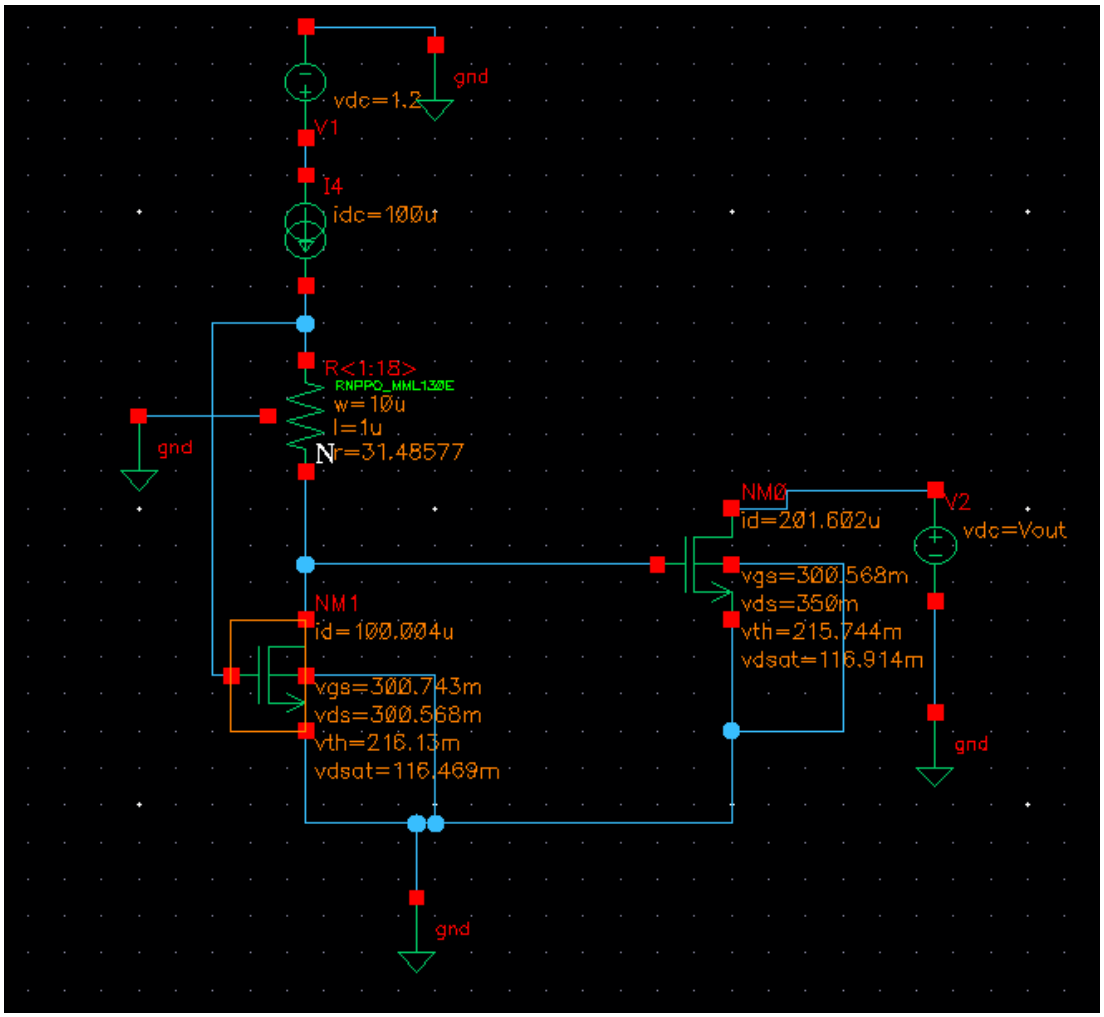
# Design 2




| | Name | Value |
|---|---|---|
| 1 | I | 10u |
| 2 | M | 4 |
| 3 | c | 5 |
| 4 | vout | 500m |

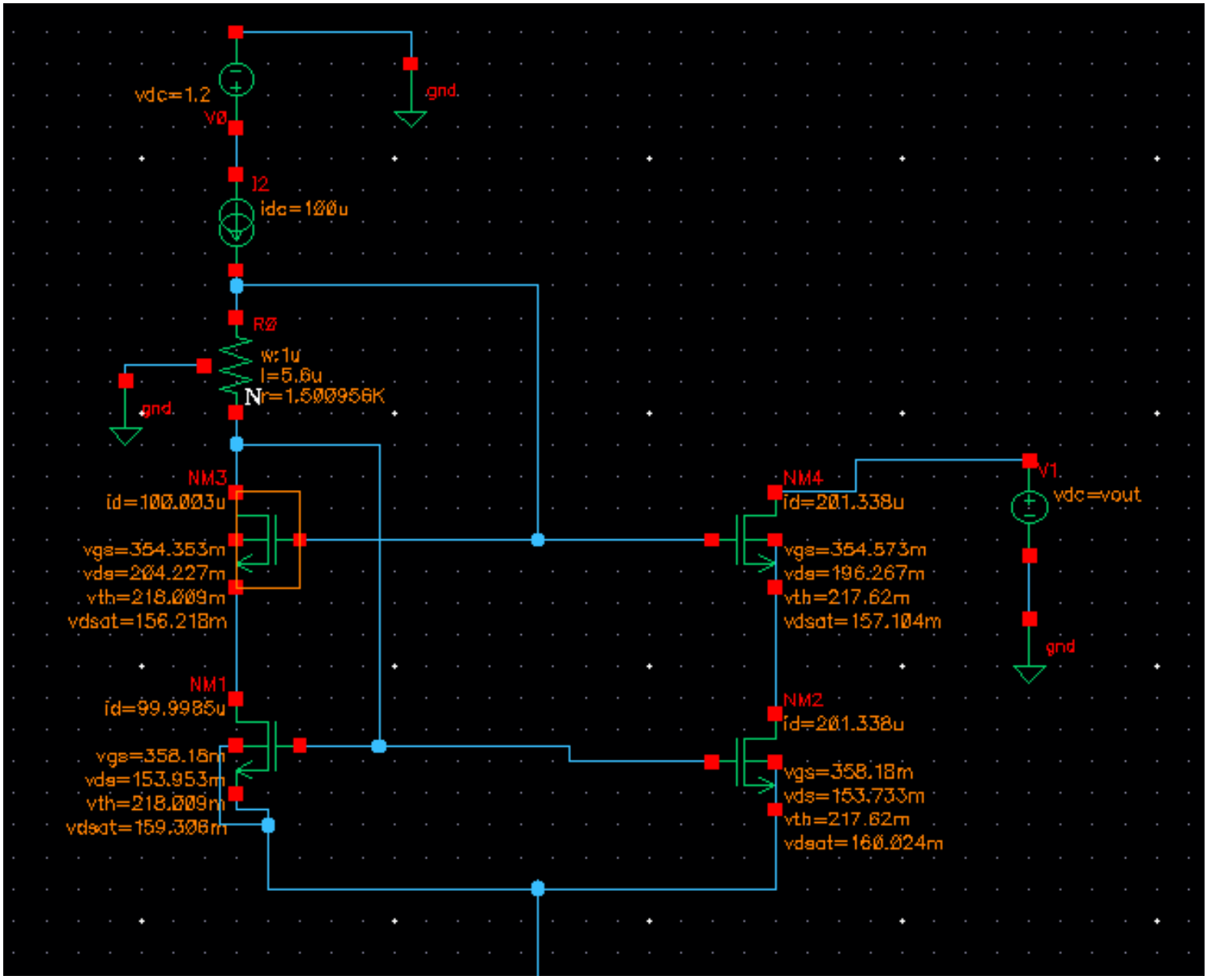
## 2- Schematic diagram with DC operating point annotated at Vout=350mV to verify the Vcomp specification for both circuits...

# Design 1




**Note: at Vds=350mv the current still 201 uA**

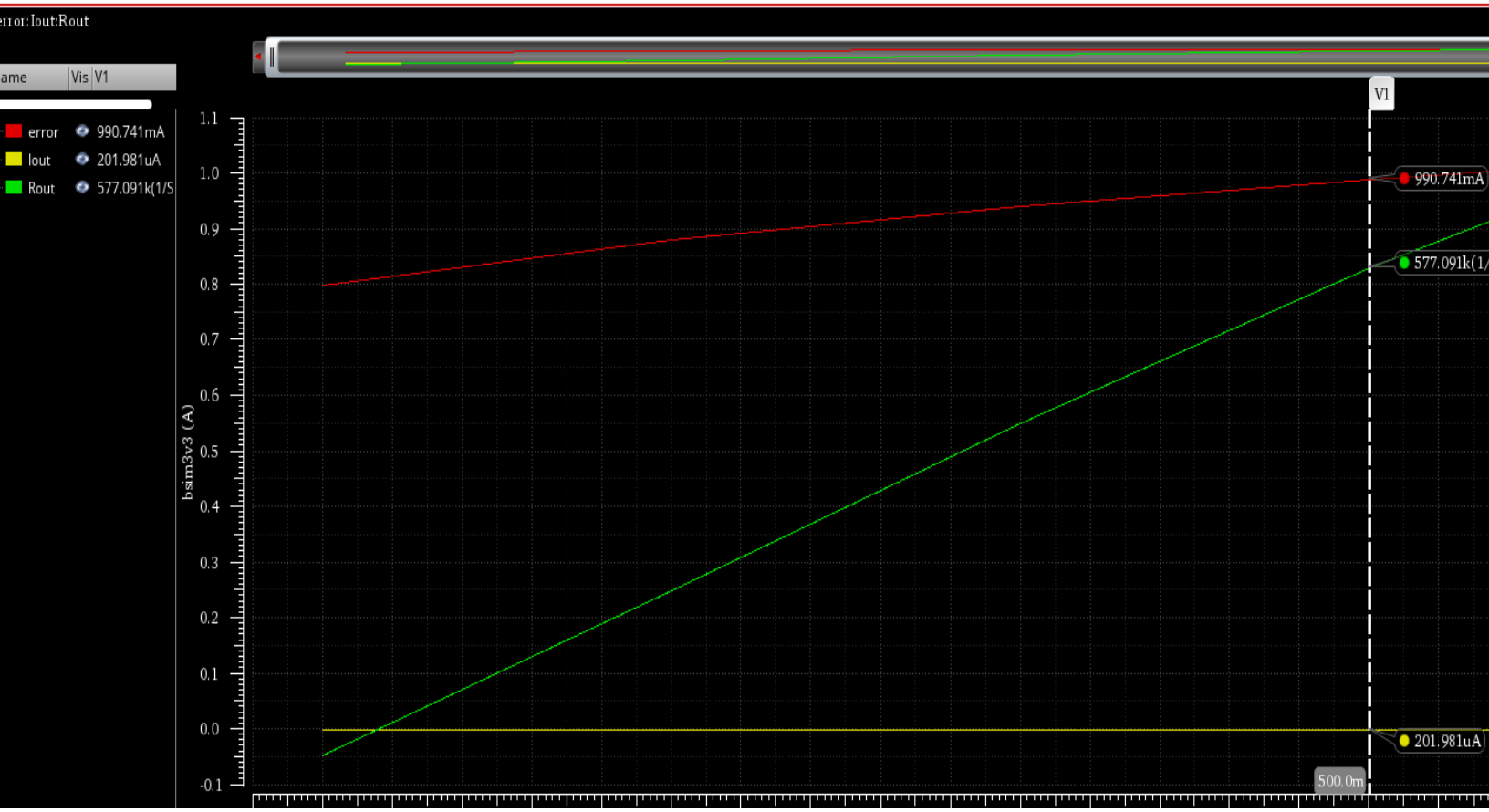
# Design 2


vdc=1.2
V0
gnd
I2
idc=100u
R0
w=1u
l=5.6u
r=1.500956K
gnd
NM3
id=100.003u
vgs=354.353m
vds=204.227m
vth=218.009m
vdsat=156.218m
NM1
id=99.9985u
vgs=358.18m
vds=153.953m
vth=218.009m
vdsat=159.306m
NM4
id=201.338u
vgs=354.573m
vds=196.267m
vth=217.62m
vdsat=157.104m
NM2
id=201.338u
vgs=358.18m
vds=153.733m
vth=217.62m
vdsat=160.024m
V1
vdc=vout
gnd

## 3: Simulation results to verify I*out* and *Rout* specifications for both circuits

### Design1

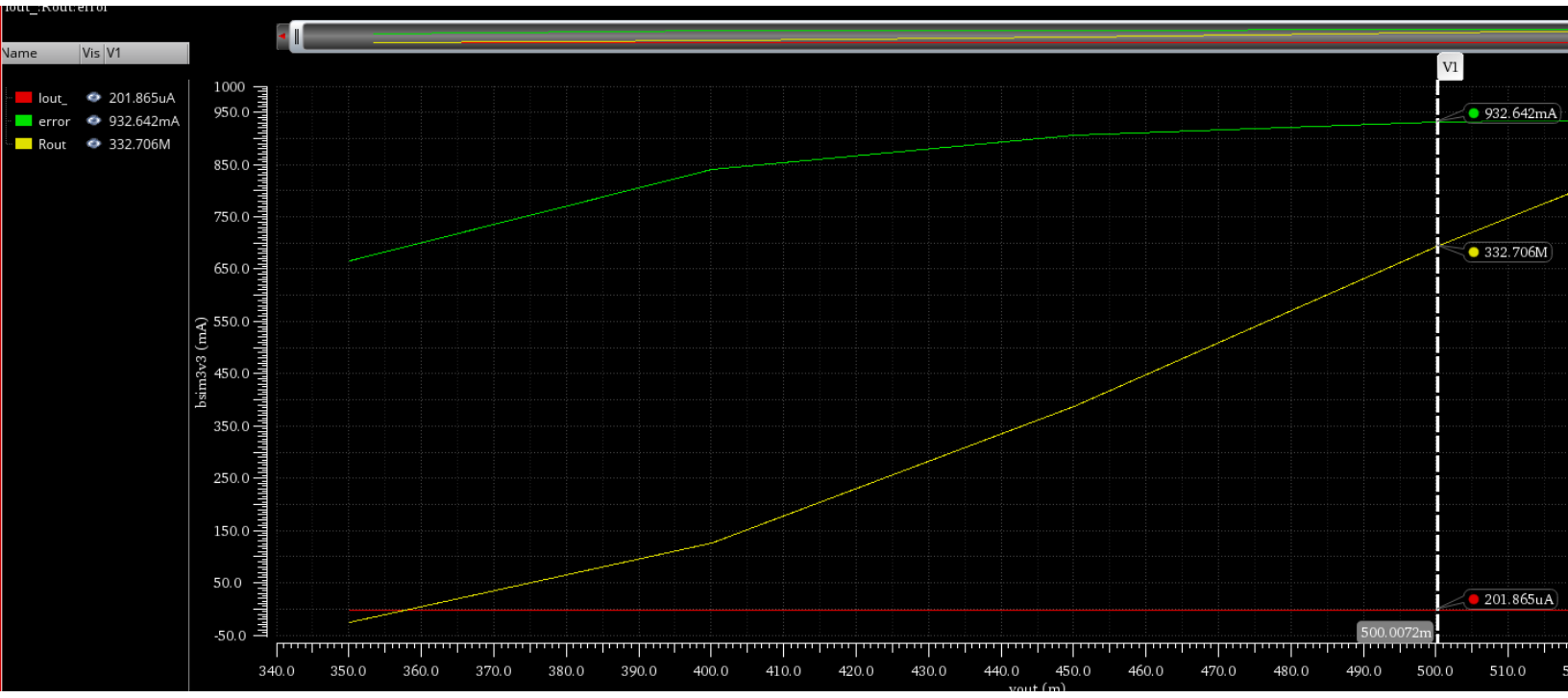
| | Name/Signal/Expr | Value |
|---|---|---|
| 1 | error | 990.741m |
| 2 | Iout | 201.981u |
| 3 | Vgs0 | 300.566m |
| 4 | Rout | 577.091K |
| 5 | Vdsat | 116.912m |




**Note: using ADE l and parametric sweep we find that ro >500k and Vcom<350mv and I=201.9u with error <1% at Vout=500m**

# Design2

| | Name/Signal/Expr | Value |
|---|---|---|
| 1 | Iout_ | 201.865u |
| 2 | NM4/D | |
| 3 | Vd3 | 358.174m |
| 4 | Vd1,2 | 155.491m |
| 5 | Rout | 332.689M |
| 6 | Vocmp | 155.68m |
| 7 | error | 932.641m |




**Note: using ADE l and parametric sweep we find that ro >500k and Vcom<350mv and I=201.9u with error <1% at Vout=500m**

## 4- An estimate of this mirror's area for both circuits.

### Design1

- Area of resistors =18*$10^{-11}$ $m^2$
- Area of transistors =3*$10^{-7}$ $m^2$
- Total Area=3.0018*$10^{-7}$ $m^2$

### Design2

- Area of resistors =5.6*$10^{-12}$ $m^2$
- Area of transistors =1.2*$10^{-8}$ $m^2$
- Total Area=1.20056*$10^{-8}$ $m^2$

Note: in both designs I neglect the area of the current mirror and assume we take the current directly from the ideal current source

## 5-If your manager told you the area you ended up with is too large and you need to sacrifice one of the specs to have reasonable area, suggest a modification and comment on what you'll gain and lose from it ..

### Design1

> Note: the area of resistor is negligible against the area of transistors, so I need to reduce the area of transistors not resistors

**to decrease the area we have to affect on the specs Vcomp , Rout**
**so we have 2 choice first Is decreasing the width and in this case we will increasing Vcomp and decreasing Rout so we will make both of Vcomp and Rout worth but on the other hand if we decreasing Length we will decreasing Vcomp and Rout so we will make Vcomp better but Rout worth**

> Note: the change in the length affect on the Rout more than the change in the width affect on Rout

**but at the end I choose to decreasing the Length**

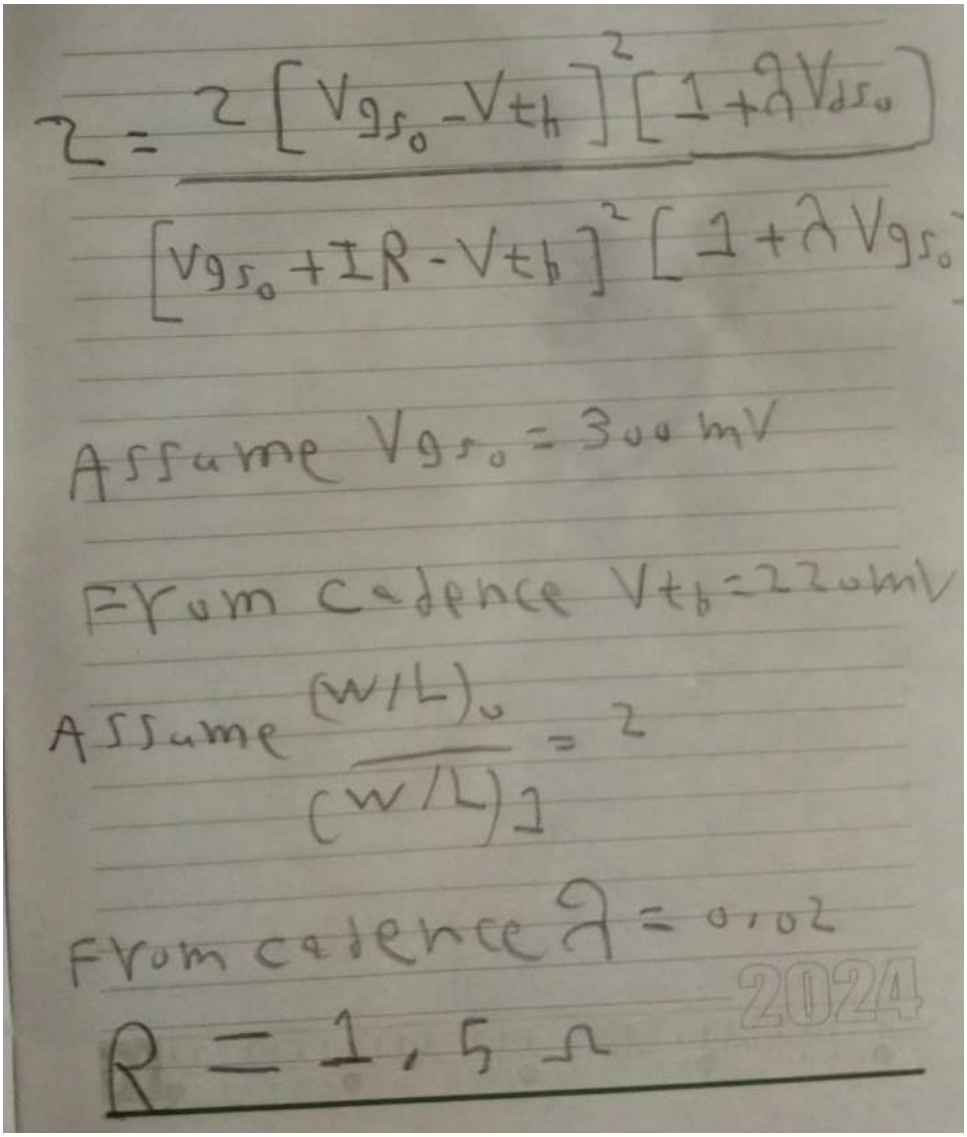
# Design 2

**We notice that we have cascode current mirror so the actual problem is to achieve low Vcomp because it's roughly =2Vov but it's so easy to have very big Rout since it's roughly =ro4*ro2 so we will decrease the length this will lead to decreasing rout  but it's already very big and decreasing Vcomp which is good**

**6- Compare both designs in a table by adding the analyzed results with the simulated results for both designs..**

## Design 1

**hand analysis steps to determine the value of R**

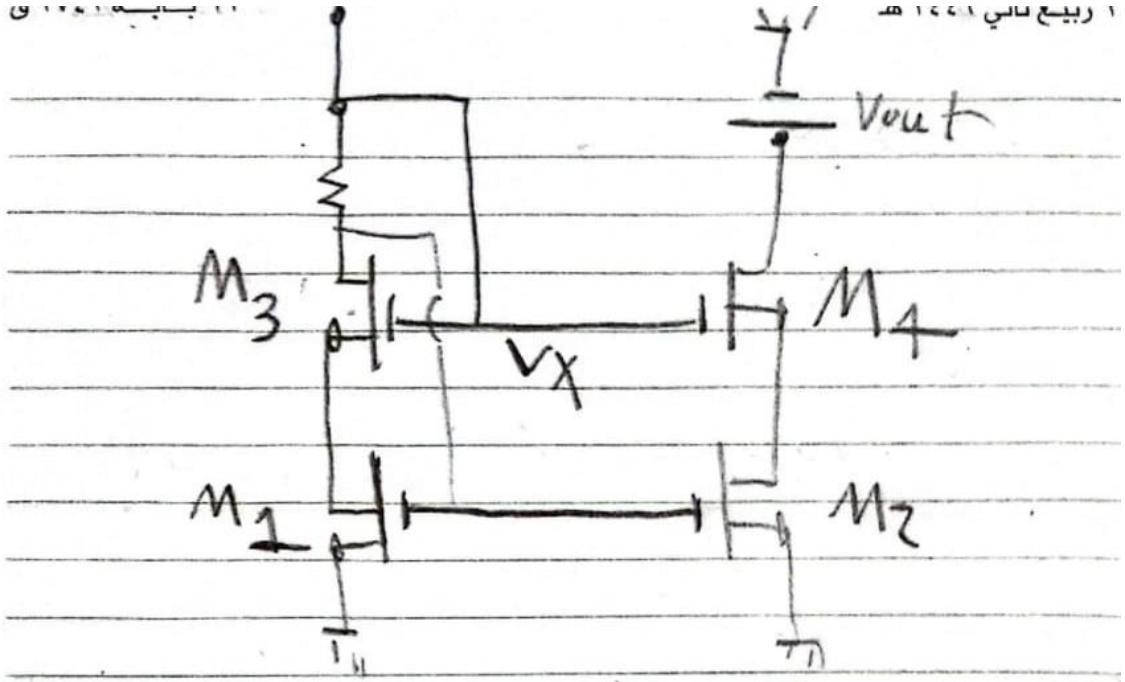


**Note: why I assume Vgs=300mv ? I choose it low to achieve low Vcomp to have high W/l so I can achieve high W assuming I choose the max length so I can have high Rout**

| Analyzed results | simulated results |
|---|---|
| Iout=200uA | **Iout=201.9uA** |
| Vgs0=300mv | **Vgs0=300.5mv** |
| Vcomp=vgs-vth=80mv | **Vcomp=vdsat=155mv** |

# Design 2

## hand analysis steps to determine the value of R




$V_{th\,1,2,3,4} = 0.216$

Assume $(W/L)_{2,4} = 2(W/L)_{1,3}$

equ → $M_1, M_2$

$$2 = \frac{2\,(1+\lambda V_{ds2})}{(1+\lambda V_{ds1})}$$

→ $V_{ds1} = V_{ds2} = C$

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equ → $M_4$, $M_3$

$$2 = 2\,\frac{(V_x - C - V_{th})^2\left(\frac{1}{} + \lambda_4(0.5 - C)\right)}{(V_x - C - V_{th})^2(1 + \lambda_3(V_{g_1} - C))}$$

From equ 2: $V_{d3} = V_{g_1} = 0.5$

But if we apply this condition and calculate (R)

From next equation we will find $M_4$ in triode so we will choose $V_{g_1} = 0.35$ V

→ But if we choose this value ∴ $V_{d3} \neq V_{d4}$

∴ equation (2) won't achived so the current will change But the change [error] in $I_{out}$ will be small

For many reasons:

First: $\eta_3 \neq \eta_4$

second: $\eta$ is small va

third: $\lambda V_{ds}$ is small value added to (1) so this term

$$\frac{(1+\lambda_4 V_{ds4})}{(1+\lambda_3 V_{ds3})}$$ will give

small error

→ For these reasons we can

Assume $V_{ds3} \neq V_{ds4}$

$V_{g1} = V_{d3} = 0.35\ V$

eqn → $M_2, M_4$

$$1 = \frac{(V_x - (-V_{th}))^2 (1 + \lambda(0.5 - C))}{(V_{g_1} - V_{th})^2 (1 + \lambda C)}$$

Let $C = 0.15$

Calculat $V_x$ ✓

$$\therefore R = \frac{V_x \cdot V_g}{I_{ref}} = 1500\,\Omega$$

| Analyzed results | simulated results |
|---|---|
| Iout=200uA | **Iout=201.865uA** |
| Vds1,2=150mv | **Vds1,2=155mv** |
| Vcomp=vx-vs3-vth=136mv | **Vcomp=vdsat=155mv** |
| Vgs1,Vd3=350mv | **Vgs1,Vd3=358mv** |

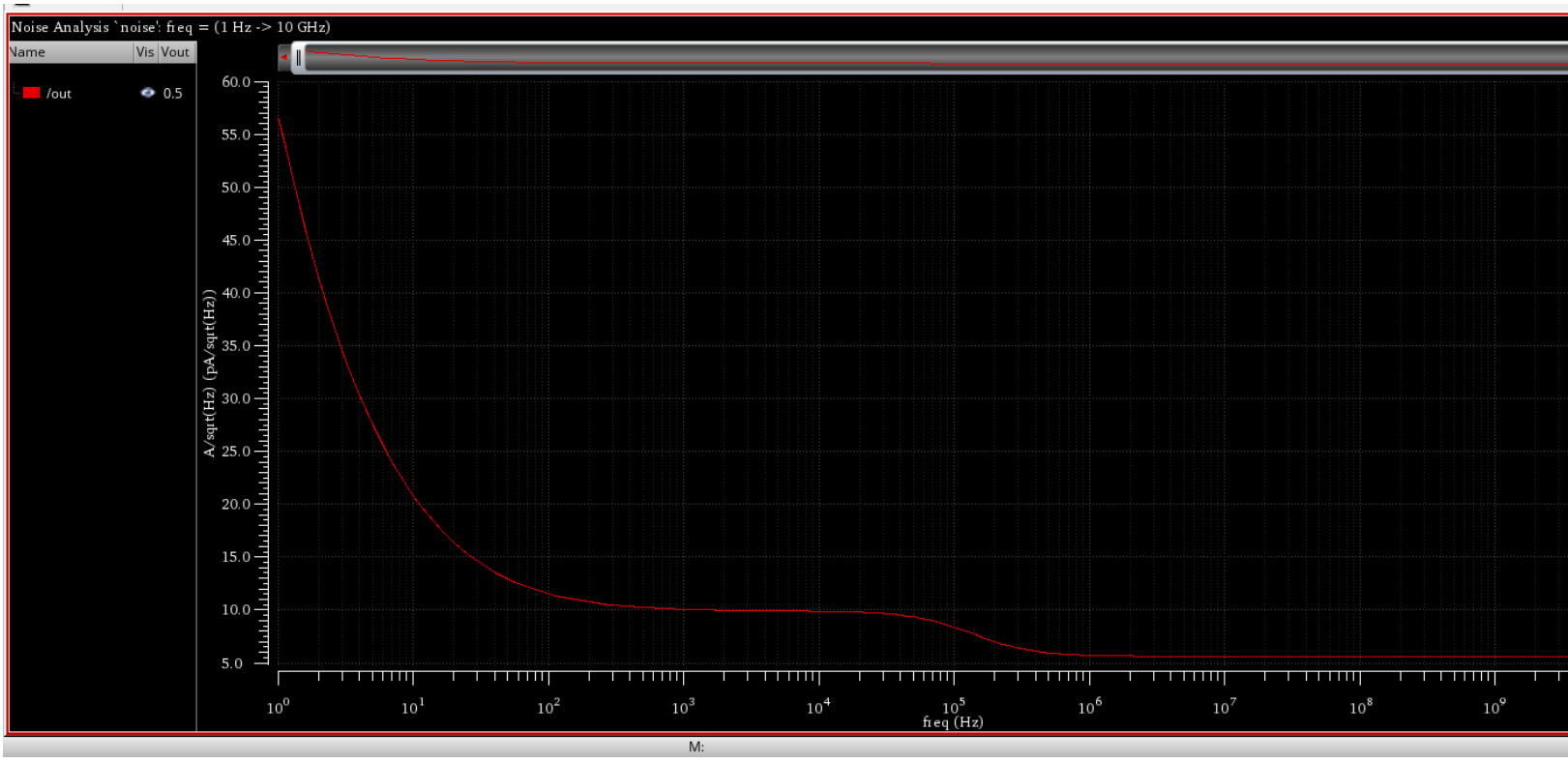
## 7- Discuss the circuits at which each circuit is more suitable to be used ..

- **If we want very low Vcomp we can use the design one because it's just =Vov while in the second design it's =2Vov on the other hand if we want to achieve very high Rout we use the second design because it has Rout=ro^2**
- **So if the circuit need to have very accurate current we must use design 2 because it has Very high Rout so there is no length modulation effect**
  **but if the circuit have big swing we need to choose design 1 because it's easy to achieve very low Vcomp**

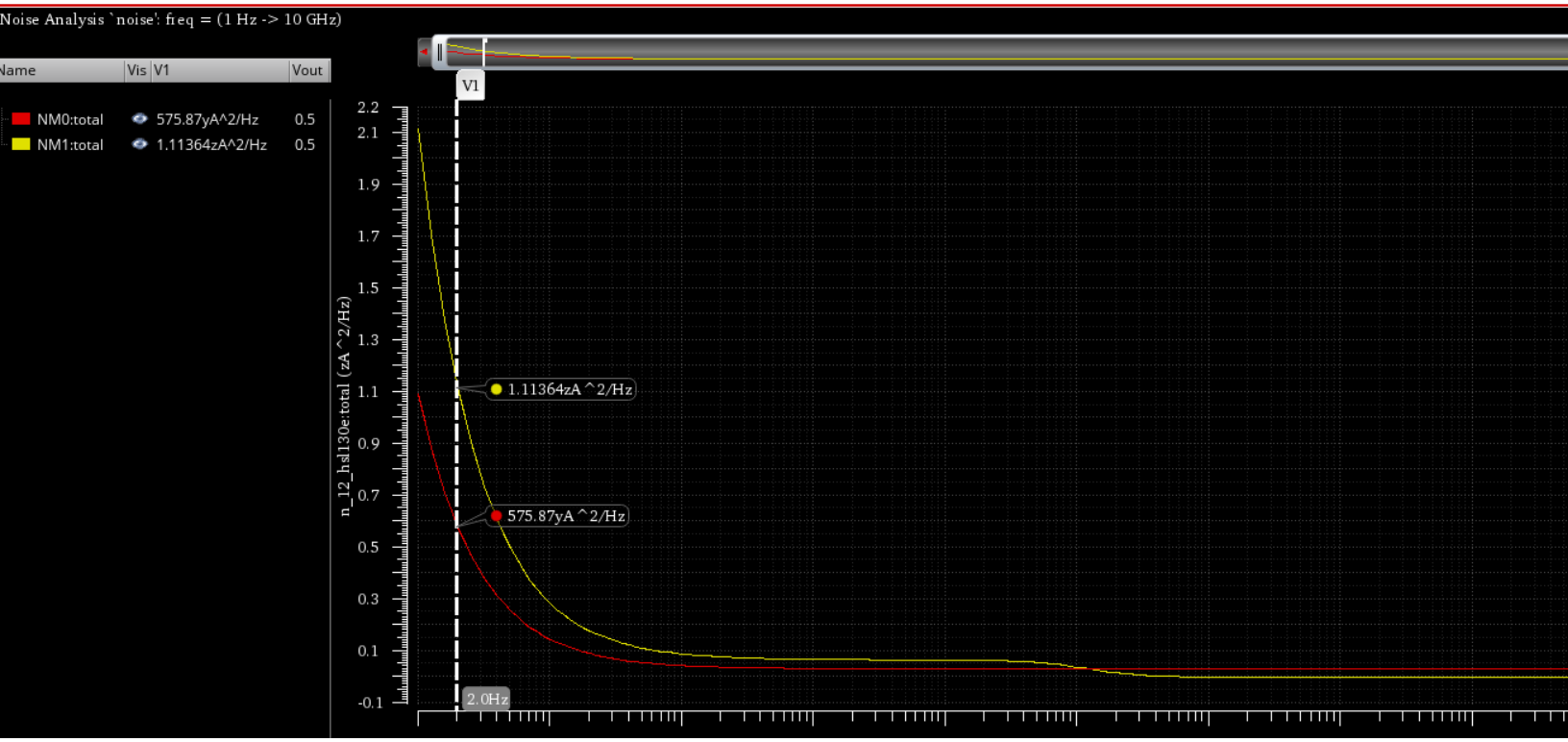
## 8- Draw and estimate the noise of both circuits and define which devices are more dominant in the total noise.

### Design1

### Total Output Noise

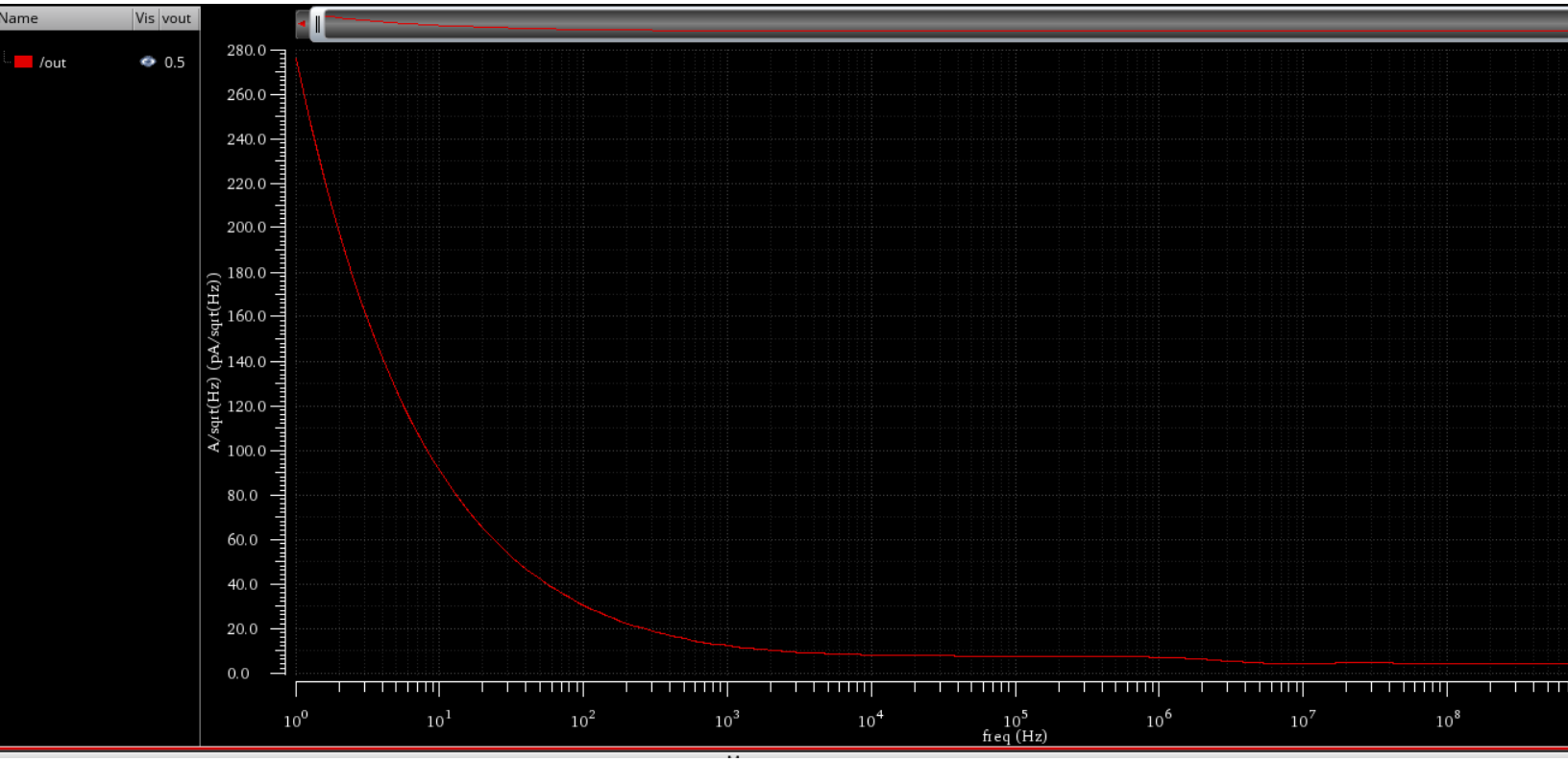


**Noise of left Transistor M1 is in yellow and it ‘s the dominant in noise and that’s because it has lower Width and they have the same lenght so has bigger flicker noise so the dominant one is M1 which at the output**



# Design 2

## Total Output Noise



**The dominant one is M1 which at the output  branch and exists at the bottom  in the main current mirror**