SPARTAN6 - DSP48A1 PROJECT

USING FPGA DESIGN FLOW

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Contents

1 Project specifications

1.1 Input – output ports

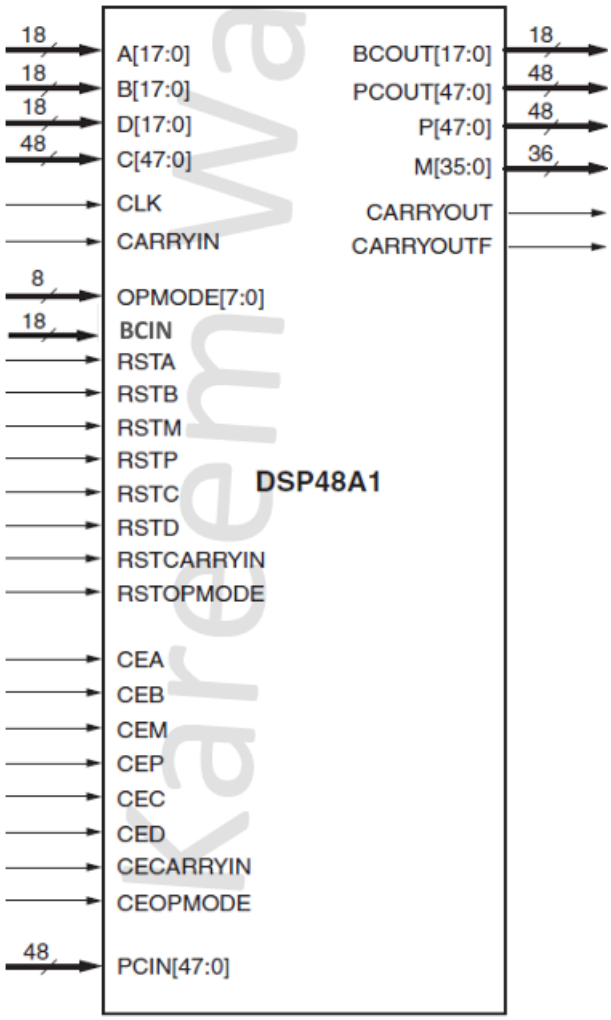

Figure 1: input output port

1.2 Schematic – internal signals

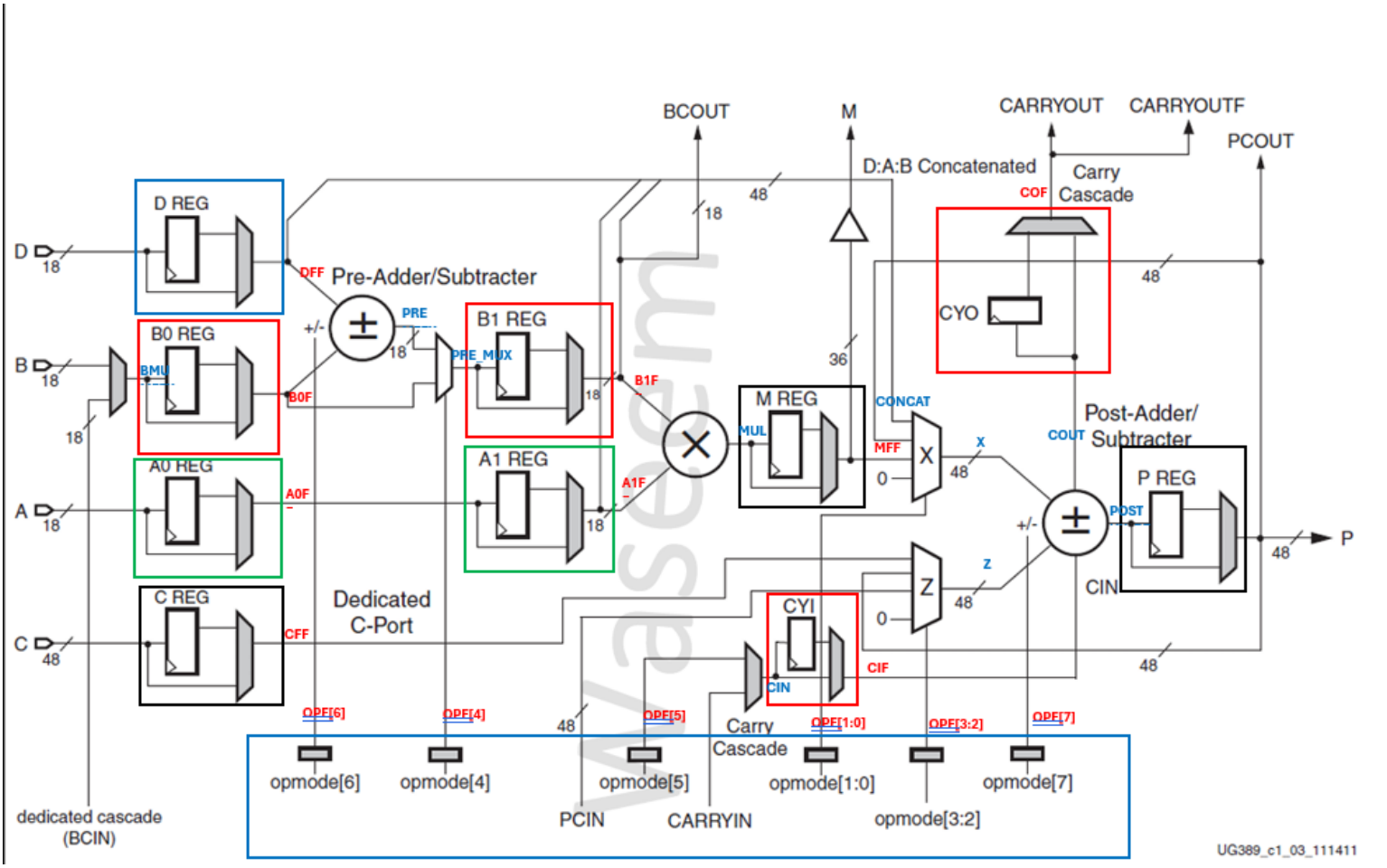

Figure 2 Schematic modified with the name of internal signals

2 Code

2.1 Design code

2.1.1 Basic block code

```
module MUX_REGISTER(the_input,clk,CE,rst,the_output);
parameter width=18;
parameter selection=1;
parameter RSTTYPE="SYNC";
input [width-1:0] the_input;
input clk,rst,CE;
output reg [width-1:0] the_output;

generate
    if(selection==1)
    begin
        if(RSTTYPE=="SYNC")
        begin
            always @(posedge clk ) begin
                if (rst)
                    the_output<=0;
                else if(CE==1)
                    the_output<=the_input;
            end

        end
        else if(RSTTYPE=="ASYNC") begin
            always @(posedge clk or posedge rst ) begin
                if (rst)
                    the_output<=0;
                else if(CE==1)
                    the_output<=the_input;
            end
        end
    end
    else if(selection==0)
    begin
        always @(the_input ) begin
        the_output=the_input;
         end
    end

endgenerate
endmodule
```

Figure 3: Basic Block Code

2.1.2 Top module Code

```
module DSP(A,B,C,D,CARRYIN,M,P,CARRYOUT,CARRYOUTF,CLK,OPMODE,CEA,CEB,CECARRYIN,CEC,CED,CEM,CEOPMODE
,CEP,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTP,RSTOPMODE,BCOUT,PCIN,BCIN,PCOUT);

input [17:0] A,B,D,BCIN;
input [47:0] C,PCIN;
input [7:0] OPMODE;
input CARRYIN,CLK,CEA,CEB,CECARRYIN,CEC,CED,CEM,CEOPMODE,CEP,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTP,RSTOPMODE;
output CARRYOUTF,CARRYOUT;
output [47:0] PCOUT,P;
output [17:0] BCOUT;
output [35:0] M;
/*.........................parameter.....................................*/
parameter A0REG=0;
parameter A1REG=1;

parameter B0REG=0;
parameter B1REG=1;

parameter CREG=1;
parameter DREG=1;
parameter MREG=1;
parameter PREG=1;
parameter CARRYINREG=1;
parameter CARRYOUTREG=1;
parameter OPMODEREG=1;

parameter CARRYINSEL="OPMODE5"; //CARRYIN
parameter B_INPUT="DIRECT"; //CASCADE
parameter RSTTYPE="SYNC"; //ASYNC
/*................................. instances wires.......................... */
wire [17:0] DFF,B0F,A0F,B1F,A1F;
wire [47:0] CFF;
```

Figure 4: Design Code Part1

```
33  wire [35:0] MFF;
34  wire CIF,COF;
35  wire [7:0] OPF;
36  wire [17:0] BMUX;
37
38  /*..................internal signals ..........................................*/
39  wire [17:0] PRE_MUX,PRE;
40  wire [35:0] MUL;
41  wire [47:0] POST;
42  wire [47:0] X,Z;
43  wire [47:0] CONCAT;
44  wire COUT,CIN;
45  /*................................. FIRST STAGE ..................................*/
46  MUX_REGISTER #(.width(18),.selection(DREG)) DUT_DREG(D,CLK,CED,RSTD,DFF);
47
48  assign BMUX=(B_INPUT=="DIRECT")? B:(B_INPUT=="CASCADE")?PCIN:0  ;
49  MUX_REGISTER #(.width(18),.selection(B0REG)) DUT_B0REG(BMUX,CLK,CEB,RSTB,B0F);
50
51  MUX_REGISTER #(.width(18),.selection(A0REG)) DUT_A0REG(A,CLK,CEA,RSTA,A0F);
52
53  MUX_REGISTER #(.width(48),.selection(CREG)) DUT_CREG(C,CLK,CEC,RSTC,CFF);
54
55  MUX_REGISTER #(.width(8),.selection(OPMODEREG)) DUT_OPMODEREG(OPMODE,CLK,CEOPMODE,RSTOPMODE,OPF);
56
57  /*................................. SECOND STAGE  ..................................*/
58  MUX_REGISTER #(.width(18),.selection(B1REG)) DUT_B1REG(PRE_MUX,CLK,CEB,RSTB,B1F);
59
60  MUX_REGISTER #(.width(18),.selection(A0REG)) DUT_A1REG(A0F,CLK,CEA,RSTA,A1F);
61
62  /*................................. THIRD STAGE  ..................................*/
63  MUX_REGISTER #(.width(36),.selection(MREG)) DUT_MREG(MUL,CLK,CEM,RSTM,MFF);
64
```

Figure 5: Design Code Part2

```
65  /*................................. FOURTH STAGE  ..................................*/
66  MUX_REGISTER #(.width(48),.selection(PREG)) DUT_PREG(POST,CLK,CEP,RSTP,P);
67  MUX_REGISTER #(.width(1),.selection(CARRYOUTREG)) DUT_COREG(COUT,CLK,CECARRYIN,RSTCARRYIN,COF);
68  MUX_REGISTER #(.width(1),.selection(CARRYINREG)) DUT_CINREG(CIN,CLK,CECARRYIN,RSTCARRYIN,CIF);
69
70  /*.............. Calculate the internal signal.............................*/
71
72  assign CIN=(CARRYINSEL=="OPMODE5")? OPMODE[5]:(CARRYINSEL=="CARRYIN")? CARRYIN:0;
73  assign MUL=A1F*B1F;
74  assign BCOUT=B1F;
75  assign M=MFF;
76  assign CONCAT={DFF[12:0],A1F,B1F};
77  assign CARRYOUT=COF;
78  assign CARRYOUTF=COF;
79  assign PCOUT=P;
80  assign PRE=(OPMODE[6]==0)? (DFF+B0F):(DFF-B0F) ;
81  assign PRE_MUX=(OPMODE[4]==0) ? B0F:PRE;
82  assign X=({OPMODE[1],OPMODE[0]}==2'b00)? 0: ({OPMODE[1],OPMODE[0]}==2'b01)? ({12'b000000000000,MFF}):({OPMODE[1],OPMODE[0]}==2'b10)?P:CONCAT;
83  assign Z=({OPMODE[3],OPMODE[2]}==2'b00)? 0: ({OPMODE[3],OPMODE[2]}==2'b01)? PCIN:({OPMODE[3],OPMODE[2]}==2'b10)?P:CFF;
84  assign {COUT,POST}=(OPMODE[7]==0)? (Z+X+CIF):(Z-(X+CIF));
85
86  endmodule
```

Figure 6: Design Code Part3

2.2 Testbench

```
module DSP_tb();

reg [17:0] A_tb,B_tb,D_tb,BCIN_tb;
reg [47:0] C_tb,PCIN_tb;
reg [7:0] OPMODE_tb;
reg CARRYIN_tb,CLK_tb,CEA_tb,CEB_tb,CECARRYIN_tb,CEC_tb,CED_tb,CEM_tb,CEOPMODE_tb,CEP_tb;
reg RSTA_tb,RSTB_tbRSTC_tb,RSTCARRYIN_tb,RSTD_tb,RSTM_tb,RSTP_tb,RSTOPMODE_tb;
wire CARRYOUTF,CARRYOUT;
wire [47:0] PCOUT,P;
wire [17:0] BCOUT;
wire [35:0] M;
DSP DUT(A_tb,B_tb,C_tb,D_tb,CARRYIN_tb,M,P,CARRYOUT,CARRYOUTF,CLK_tb,OPMODE_tb,CEA_tb,CEB_tb,CECARRYIN_tb,CEC_tb,CED_tb,CEM_tb,CEOPMODE_tb
,CEP_tb,RSTA_tb,RSTB_tb,RSTC_tb,RSTCARRYIN_tb,RSTD_tb,RSTM_tb,RSTP_tb,RSTOPMODE_tb,BCOUT,PCIN_tb,BCIN_tb,PCOUT);
integer i;
initial begin
CLK_tb=0;
forever
#4 CLK_tb=~CLK_tb;
end

initial begin
CEA_tb=1;CEB_tb=1;CECARRYIN_tb=1; CEC_tb=1;CED_tb=1;CEM_tb=1;CEOPMODE_tb=1;CEP_tb=1;
RSTA_tb=0;RSTB_tb=0;RSTC_tb=0;RSTCARRYIN_tb=0;RSTD_tb=0;RSTM_tb=0;RSTP_tb=0;RSTOPMODE_tb=0;

/* (D+B)*A+C+CIN */ /* 23 */
A_tb=2; B_tb=3; C_tb=4; D_tb=6; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
OPMODE_tb[1]=0; OPMODE_tb[0]=1; OPMODE_tb[3]=1; OPMODE_tb[2]=1; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
for(i=0;i<4;i=i+1)
@(negedge CLK_tb);

/* (D+B)*A+CIN */ /* 10 */
A_tb=3; B_tb=1; C_tb=5; D_tb=2; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
OPMODE_tb[1]=0; OPMODE_tb[0]=1; OPMODE_tb[3]=0; OPMODE_tb[2]=0; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
for(i=0;i<4;i=i+1)
@(negedge CLK_tb);
```

Figure 7: Testbench Part1

```
36
37  /* (D-B)*A+CIN*/ /* 57 */
38  A_tb=4; B_tb=1; C_tb=6; D_tb=15; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
39  OPMODE_tb[1]=0; OPMODE_tb[0]=1; OPMODE_tb[3]=0; OPMODE_tb[2]=0; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=1; OPMODE_tb[7]=0;
40  for(i=0;i<4;i=i+1)
41  @(negedge CLK_tb);
42
43  /* (D-B)*A+C+CIN */ /* 268 */
44  A_tb=5; B_tb=8; C_tb=7; D_tb=60; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
45  OPMODE_tb[1]=0; OPMODE_tb[0]=1; OPMODE_tb[3]=1; OPMODE_tb[2]=1; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=1; OPMODE_tb[7]=0;
46  for(i=0;i<4;i=i+1)
47  @(negedge CLK_tb);
48
49  /* B*A+CIN*/ /* 10 */
50  A_tb=1; B_tb=9; C_tb=1; D_tb=5; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
51  OPMODE_tb[1]=0; OPMODE_tb[0]=1; OPMODE_tb[3]=0; OPMODE_tb[2]=0; OPMODE_tb[4]=0; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
52  for(i=0;i<4;i=i+1)
53  @(negedge CLK_tb);
54
55  /* (B*A)+C+CIN */ /* 7 */
56  A_tb=4; B_tb=1; C_tb=2; D_tb=1; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
57  OPMODE_tb[1]=0; OPMODE_tb[0]=1; OPMODE_tb[3]=1; OPMODE_tb[2]=1; OPMODE_tb[4]=0; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
58  for(i=0;i<4;i=i+1)
59  @(negedge CLK_tb);
60
61  /* C+CIN*/ /* 5 */
62  A_tb=1; B_tb=3; C_tb=4; D_tb=2; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
63  OPMODE_tb[1]=0; OPMODE_tb[0]=0; OPMODE_tb[3]=1; OPMODE_tb[2]=1; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
64  for(i=0;i<4;i=i+1)
65  @(negedge CLK_tb);
66
67  /* CIN */ /* 1 */
68  A_tb=2; B_tb=10; C_tb=5; D_tb=4; PCIN_tb=1; CARRYIN_tb=1; BCIN_tb=0;
69  OPMODE_tb[1]=0; OPMODE_tb[0]=0; OPMODE_tb[3]=0; OPMODE_tb[2]=0; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
70  for(i=0;i<4;i=i+1)
```

Figure 8: Testbench Part2

```
71  @(negedge CLK_tb);
72
73  /* PCIN+CIN */ /* 5 */
74  A_tb=7; B_tb=3; C_tb=4; D_tb=1; PCIN_tb=4; CARRYIN_tb=1; BCIN_tb=0;
75  OPMODE_tb[1]=0; OPMODE_tb[0]=0; OPMODE_tb[3]=0; OPMODE_tb[2]=1; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
76  for(i=0;i<4;i=i+1)
77  @(negedge CLK_tb);
78
79  /* P+CIN */ /* 6 ,7 , 8, 9  */
80  A_tb=2; B_tb=3; C_tb=2; D_tb=6; PCIN_tb=2; CARRYIN_tb=1; BCIN_tb=0;
81  OPMODE_tb[1]=1; OPMODE_tb[0]=0; OPMODE_tb[3]=0; OPMODE_tb[2]=0; OPMODE_tb[4]=1; OPMODE_tb[5]=1; OPMODE_tb[6]=0; OPMODE_tb[7]=0;
82  for(i=0;i<4;i=i+1)
83  @(negedge CLK_tb);
84
85  $stop;
86  end
87
88  endmodule
```

Figure 9: Testbench Part3

3 Do File

```
vlib work
vlog DSP.v DSP_tb.v
vsim -voptargs=+acc work.DSP_tb
add wave *
run -all
```

Figure 10: Do file

4 Waveform

4.1 Waveform for input – output ports

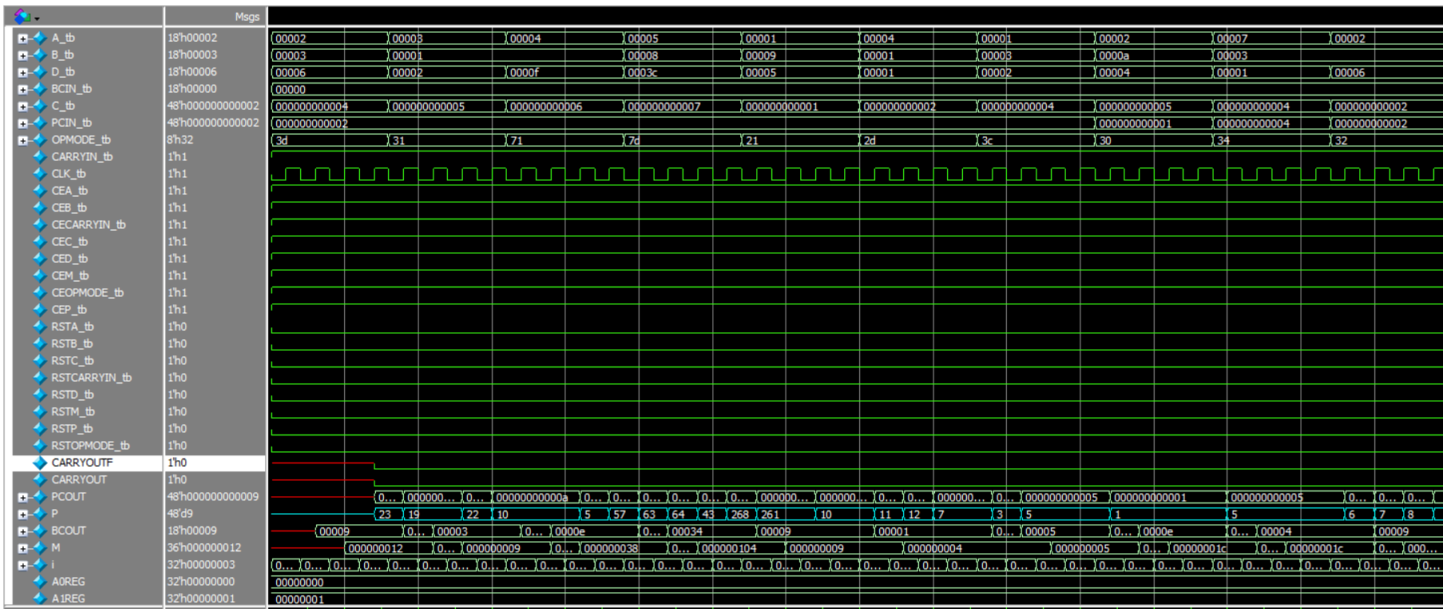

Figure 11: Waveform of input- Output Port

4.2 Waveform for internal signals

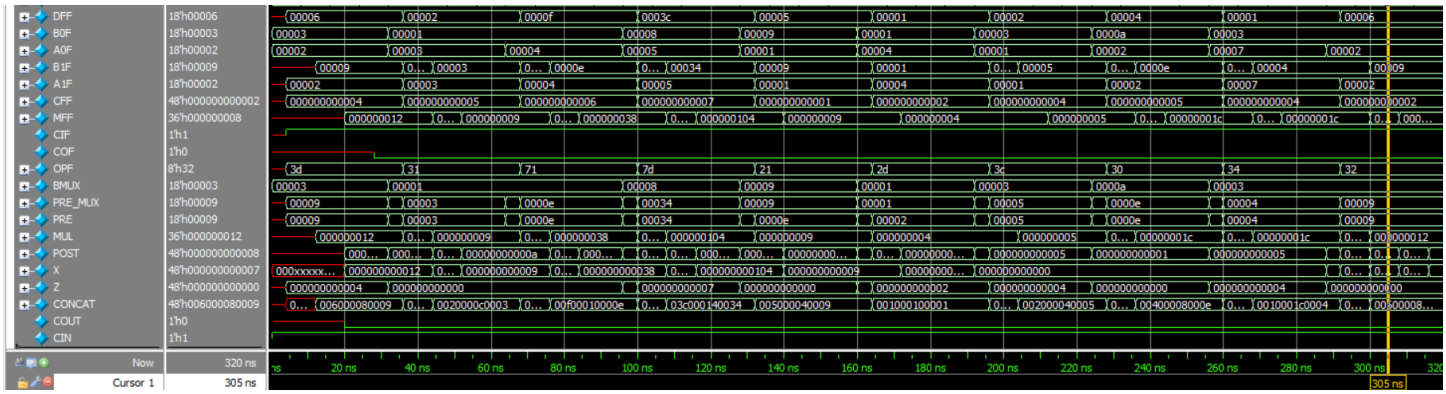

Figure 12: Waveform of internal Signals in the Design

5 Vivado Design Flow

5.1 Elaboration

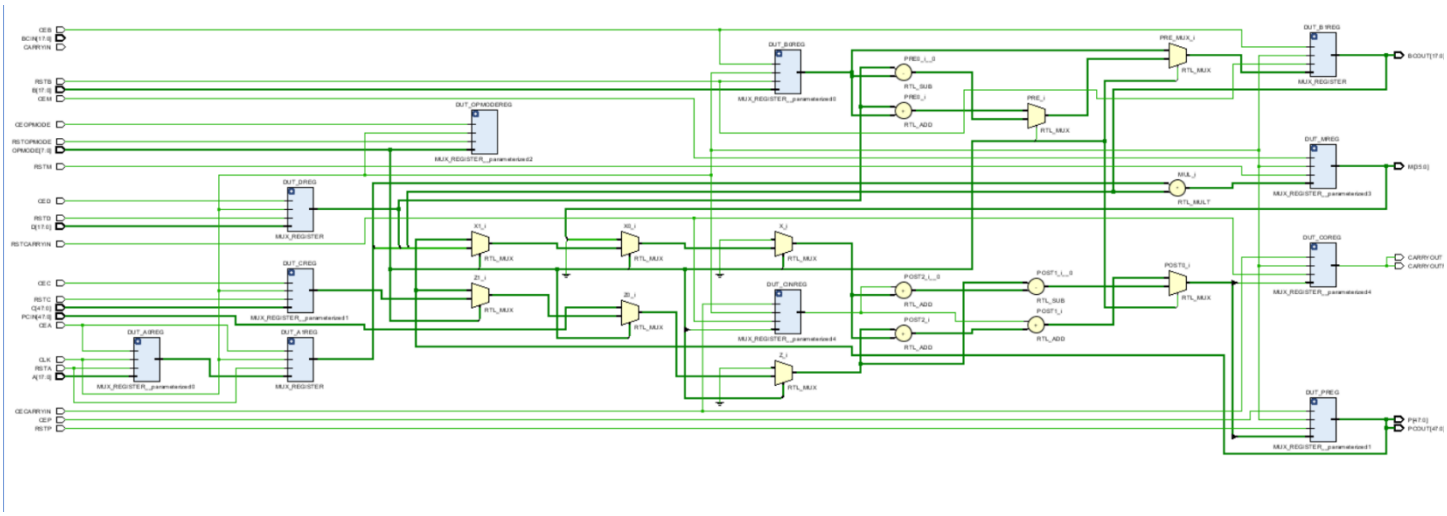

Figure 13: Elaborated Design Schematic

5.2 Time constraints

```
## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports CLK]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports CLK]
```

Figure 14: Time constraints File

5.3 Synthesis

5.3.1 Synthesis Schematic

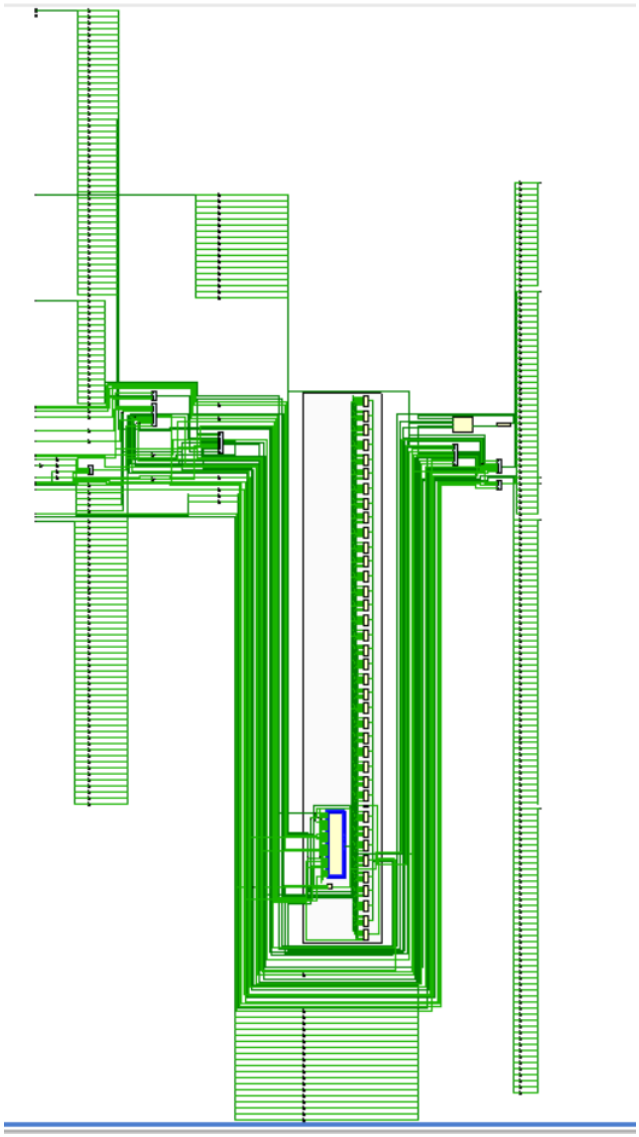

Figure 15: Synthesis Schematic

5.3.2 Detailed Schematic

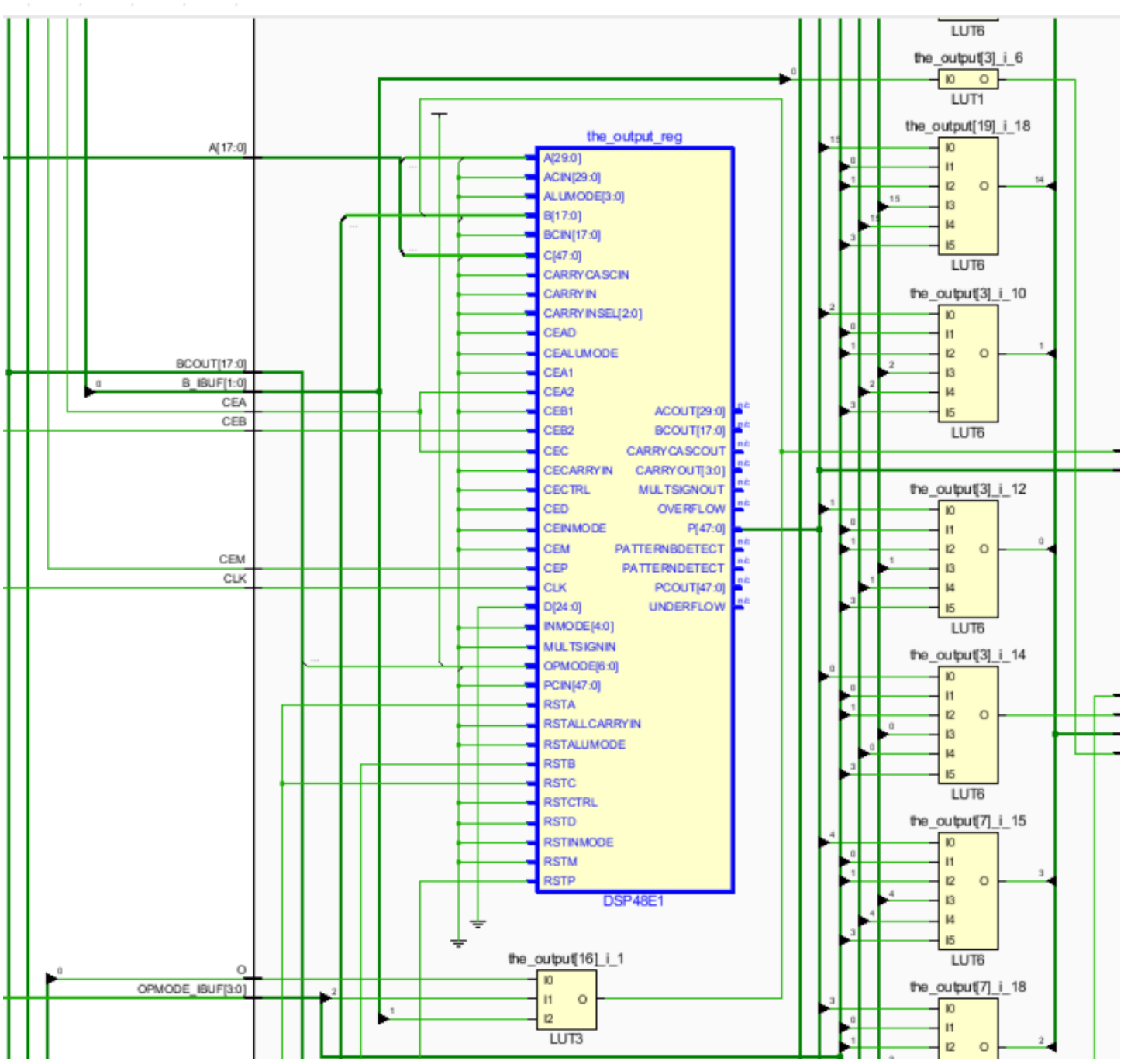

Figure 16: DSP48E1 block in FPGA used to Synthesis the Design

5.3.3 Synthesis Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.259 ns	Worst Hold Slack (WHS):	0.341 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	86	Total Number of Endpoints:	86	Total Number of Endpoints:	154

All user specified timing constraints are met.

Figure 17: Timing report in synthesis stage

5.3.4 Synthesis Utilization Report

Name 1	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP	229	152	1	325	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0
DUT_A1REG (MUX_R...	0	18	0	0	0
DUT_B1REG (MUX_R...	1	18	0	0	0
DUT_CINREG (MUX_...	0	1	0	0	0
DUT_COREG (MUX_R...	0	1	0	0	0
DUT_CREG (MUX_RE...	96	48	0	0	0
DUT_DREG (MUX_RE...	46	18	0	0	0
DUT_MREG (MUX_RE...	39	0	1	0	0
DUT_PREG (MUX_RE...	47	48	0	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0

Figure 18: Utilization report in synthesis stage

5.4 Implementation

5.4.1 Implementation Device

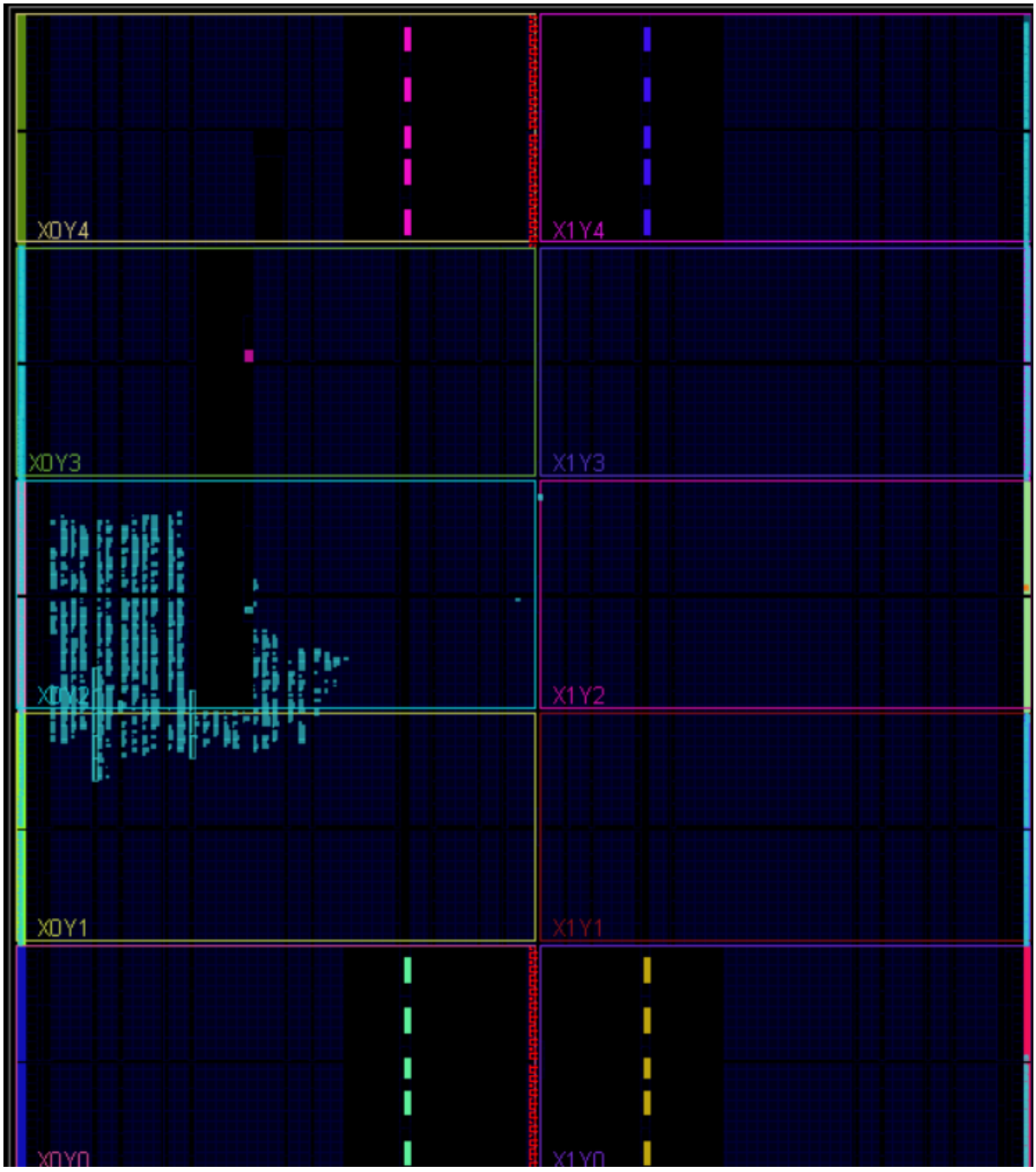

Figure 19: Design implemented on FPGA

5.4.2 Implementation Timing Report

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.895 ns	Worst Hold Slack (WHS):	0.057 ns	Worst Pulse Width Slack (WPWS):	3.950 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	7672	Total Number of Endpoints:	7656	Total Number of Endpoints:	4881

All user specified timing constraints are met.

Figure 20: Timing report in implementation stage

5.4.3 Implementation Utilization Report

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCANE2 (4)
N DSP	2547	4018	96	7	1228	2099	448	1474	8	1	325	2	1
dbg_hub (dbg_hub)	475	727	0	0	233	451	24	314	0	0	0	1	1
DUT_A1REG (MUX_R...	0	18	0	0	8	0	0	0	0	0	0	0	0
DUT_B1REG (MUX_R...	1	18	0	0	7	1	0	1	0	0	0	0	0
DUT_CINREG (MUX_...	0	1	0	0	1	0	0	0	0	0	0	0	0
DUT_COREG (MUX_R...	0	2	0	0	2	0	0	0	0	0	0	0	0
DUT_CREG (MUX_RE...	96	48	0	0	31	96	0	0	0	0	0	0	0
DUT_DREG (MUX_RE...	29	18	0	0	13	29	0	0	0	0	0	0	0
DUT_MREG (MUX_RE...	54	0	0	0	23	54	0	0	0	1	0	0	0
DUT_PREG (MUX_RE...	48	48	0	0	27	48	0	0	0	0	0	0	0
u_ila_0 (u_ila_0)	1843	3138	96	7	936	1419	424	1101	8	0	0	0	0

Figure 21: Utilization report in implementation stage

6 Message Tab

6.1 Message Tab for elaborated design

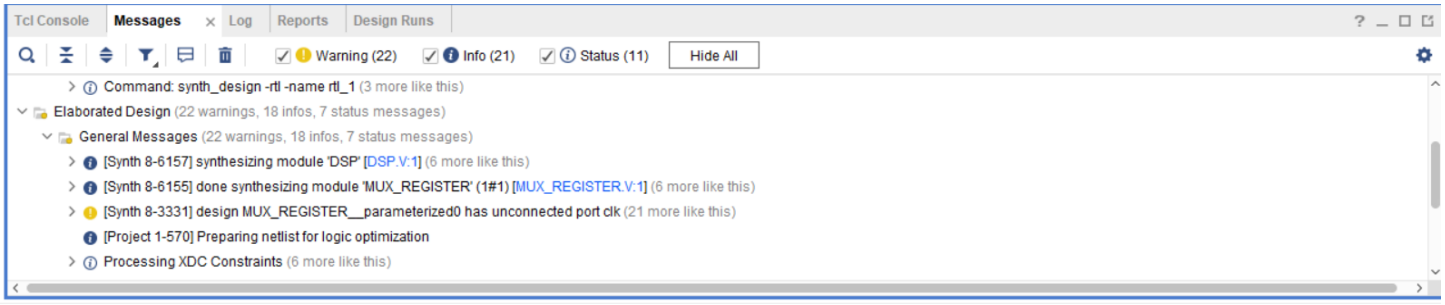

Figure 22: Message Tab for elaborated design

6.2 Message Tab for Synthesized design

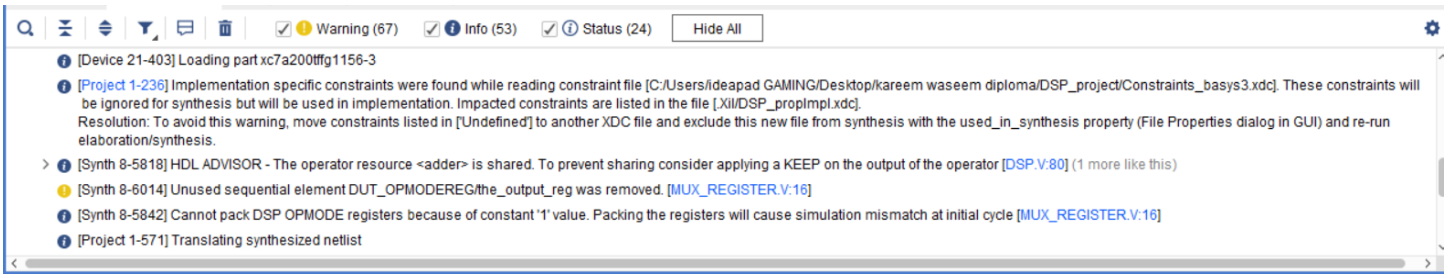

Figure 23 : Message Tab for Synthesized design

6.3 Message Tab for implemented design

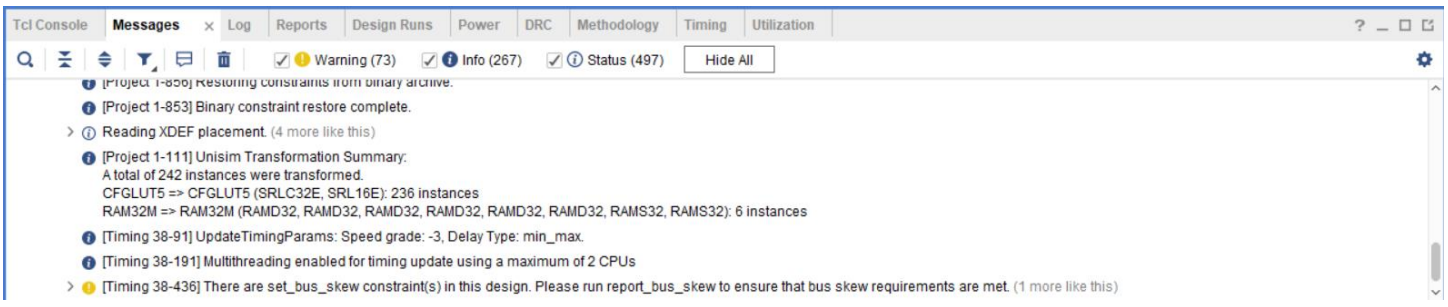

Figure 24: Message Tab for implemented design