Verilog
Lab2

Note: ***Follow the instructions to reach the best clean code.***

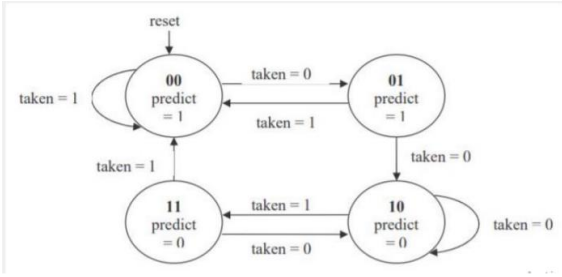
1-Write Verilog code to convert from binary to gray, write testbensh to test your design

Decimal Equivalent	Binary			Gray Code		
	B2	B1	B0	G2	G1	G0
0	0	0	0	**0**	**0**	**0**
1	0	0	1	**0**	**0**	**1**
2	0	1	0	**0**	**1**	**1**
3	0	1	1	**0**	**1**	**0**
4	1	0	0	**1**	**1**	**0**
5	1	0	1	**1**	**1**	**1**
6	1	1	0	**1**	**0**	**1**
7	1	1	1	**1**	**0**	**0**

2-Implement a Verilog code for 4-bit PISO (parallel to serial), write Testbensh to check result.

3- Implement a Verilog code for 4-bit SIPO (serial to parallel), write Testbensh to check result.

4- Write a Verilog code that implements this state machine. Use the signal or register names and state assignments given on the below graph. Used Testbensh to verify your design.



5- Write code this sequence detector by 2 different methods code style and Used mealy. [Sequence = 10110101]

5- Write Clock divider by (2, 4, 8, 16) have 4 outputs.

6- Write Clock Divider by 3 by two different methods.

7- Write Clock Divider by 6.

8- Write Synchronous FIFO have (data_width=32,Depth=8).

وَمَا أُوتِيتُم مِّنَ الْعِلْمِ إِلَّا قَلِيلًا