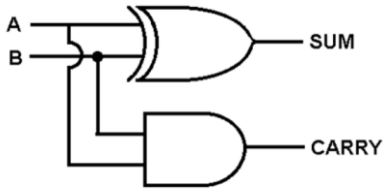
Verilog
Lab1

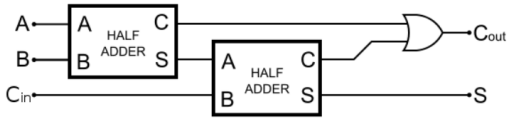
Note: ***Follow the instructions to reach the best clean code.***

1-Design [Half Adder] then design [Full Adder]
depend on Half-Adder as “sub module” by structure.

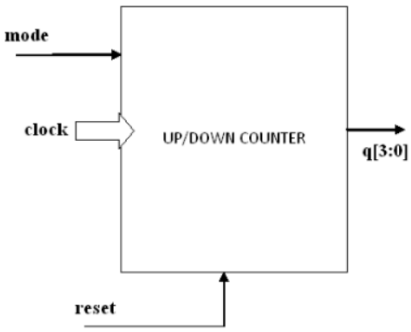
Half Adder



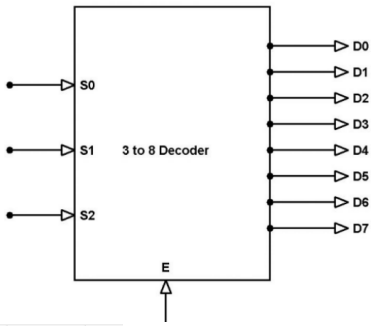
Full Adder



2- Write a Verilog model for a 4-bit up-down counter
with a parameter to define the output width.
Additionally, write a simple testbench to verify
the counter's functionality.
Use parameter override to test an 8-bit counter.



3- Write Verilog code to model 3–8-
line decoder using Case statement,
used simple Testbensh to check result



S0	S1	S2	E	D0	D1	D2	D3	D4	D5	D6	D7
x	x	x	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

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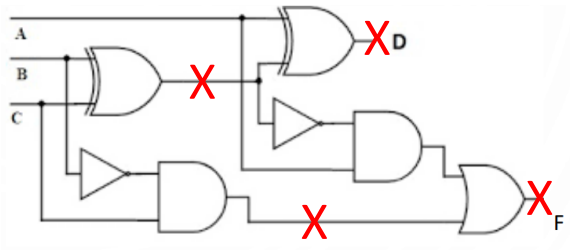
4- Write Verilog to model simple memory buffer:
-The input signals: clk, rst, en_w, en_r,Full_Flag ,Empty_Flag ,8-bit data_in.
-The output signals: 8-bit data_out, address size =3bit.
-Write testbensh to initialize memory and read it.

5- Seq1=1011 and Seq2=0011, access only the first 2 leftmost bits from Seq1 and the last 2 bits from Seq2. Perform an AND operation between these parts of Seq1 and Seq2, and concatenate the result with Seq3=1010. Finally, extend the MSB to achieve a final output with a width of 8 bits.
NOTE: ***[MSB:LSB] vector***

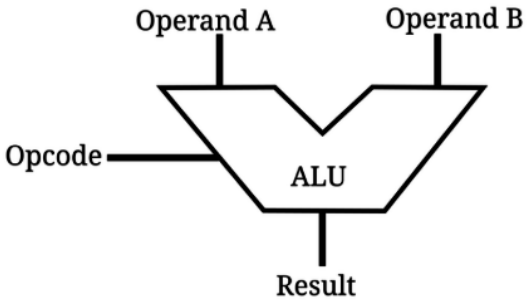
6- Write Verilog code for a combinational circuit, inserting a flip-flop at location X.
Compare the netlist and simulation results with and without the flip-flop.



7- Design an ALU to support various operations, including:

- **Arithmetic:** addition, subtraction, multiplication
- **Bitwise:** AND, OR, XOR, NAND, NOR, XNOR
- **Shift operations:** shift left, shift right
- **Concatenation:** between A and B

Consider the sizes of A and B to be 3 bits each, and operations are synchronized with the clock signal. Use a testbench to verify your design.



وَمَا أُوتِيتُم مِّنَ الْعِلْمِ إِلَّا قَلِيلًا