



# **Single-Cycle RISC-V Processor With One Level Cache Memory**

# Introduction

RISC V is RISC Processor

RISC V Operates on 32- bit Data

RISC V has 32-bit 32 register in register file

# RISC V Processor Microarchitecture

## **Processor Design Includes Main Modules:**

**Data Path**

**Control Unit**

Then integrate it with Cache System

## **-Our Design Covers instructions:**

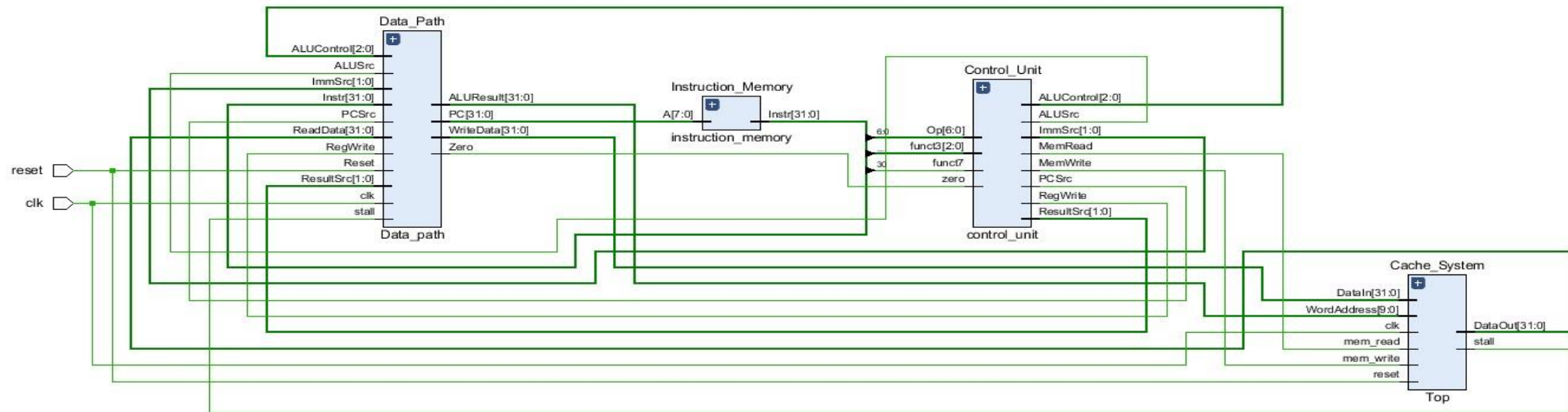
Lw , Sw

R-Type ,I-Type

Beq , jal



# RISC V Schematic

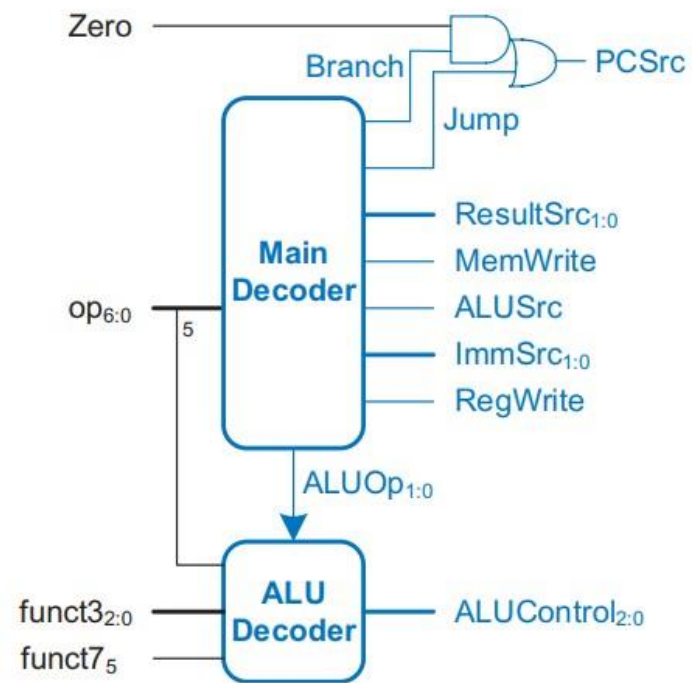


Activate Windows  
Go to Settings to activate Windows.

# RISC V Processor Microarchitecture

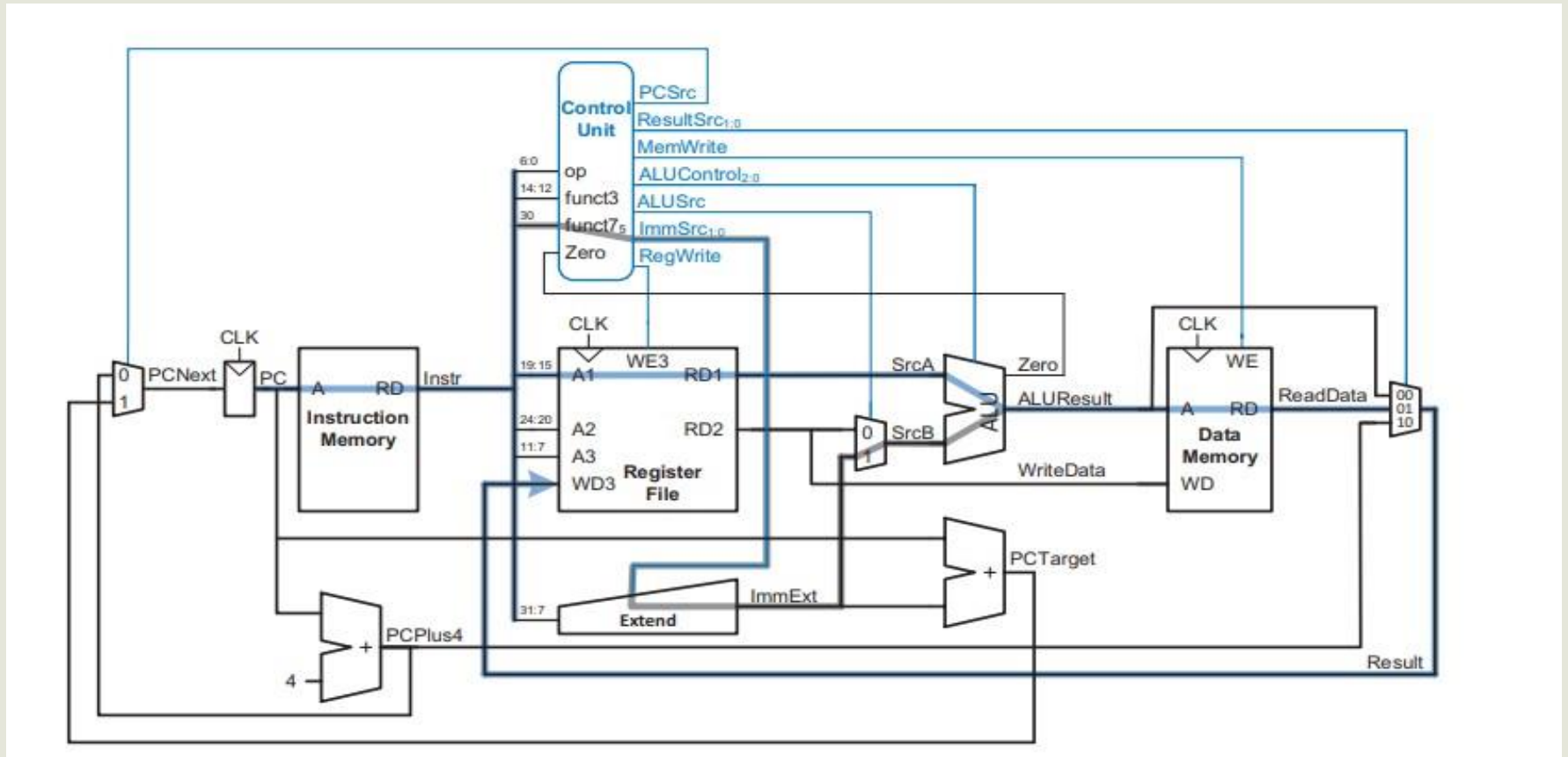
## Control Unit:

Generates Control Signals.



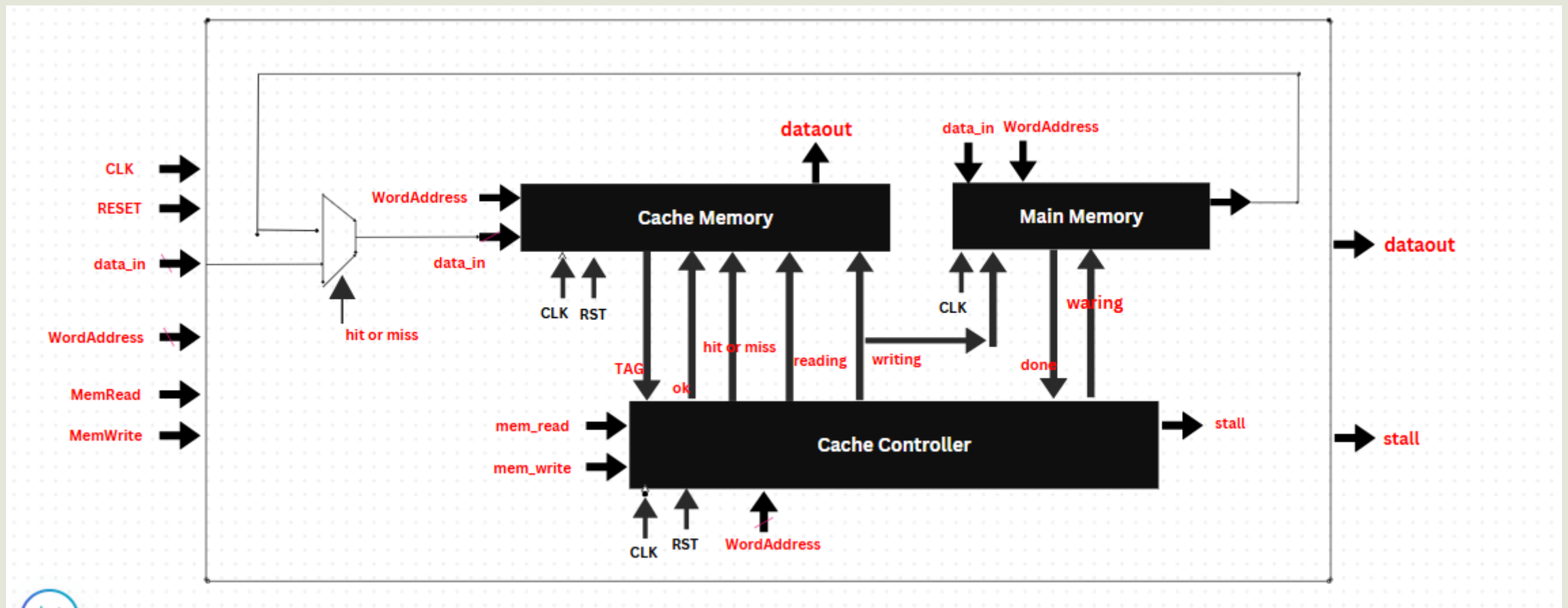
# RISC V Processor Microarchitecture

## Data Path:



# RISC V Processor Microarchitecture

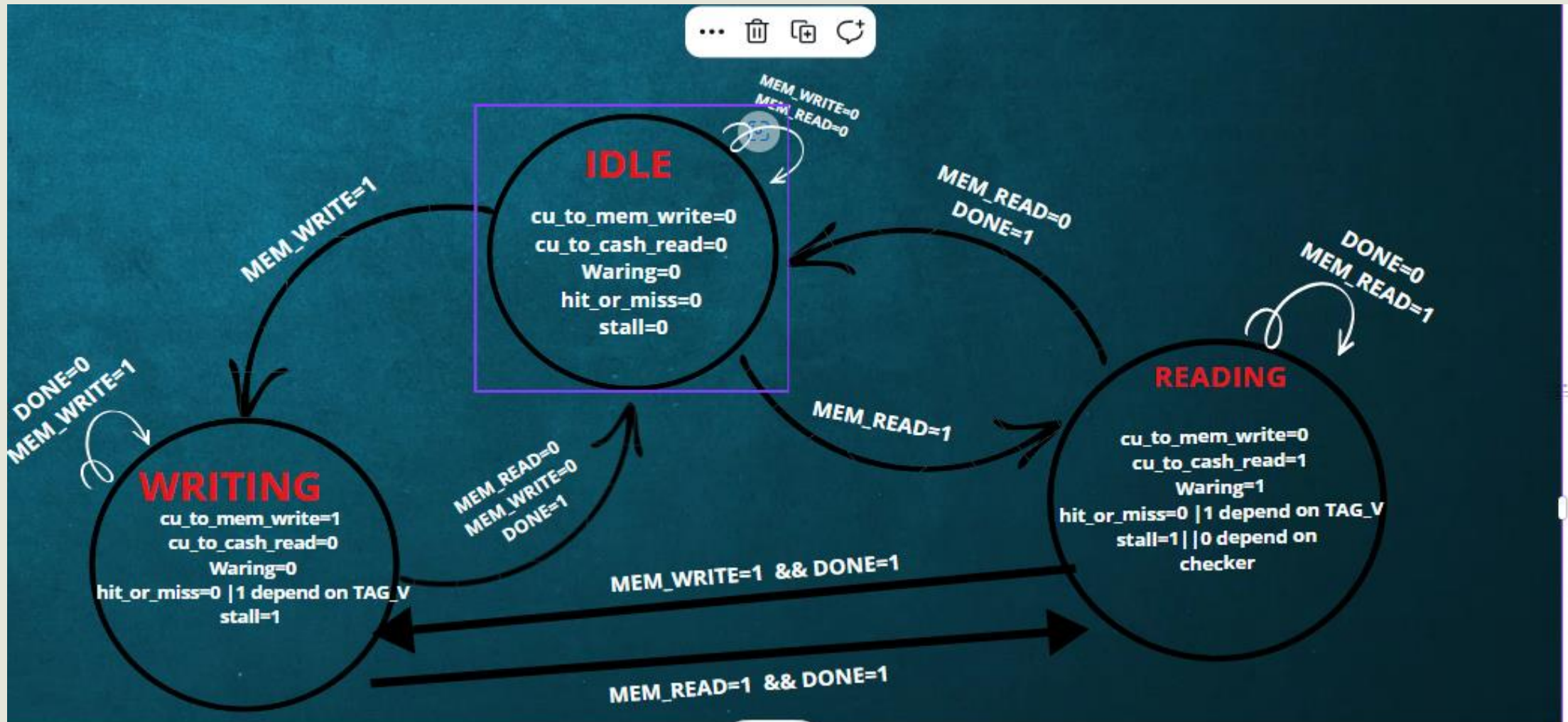
## Cache System:





# RISC V Processor Microarchitecture

## FSM





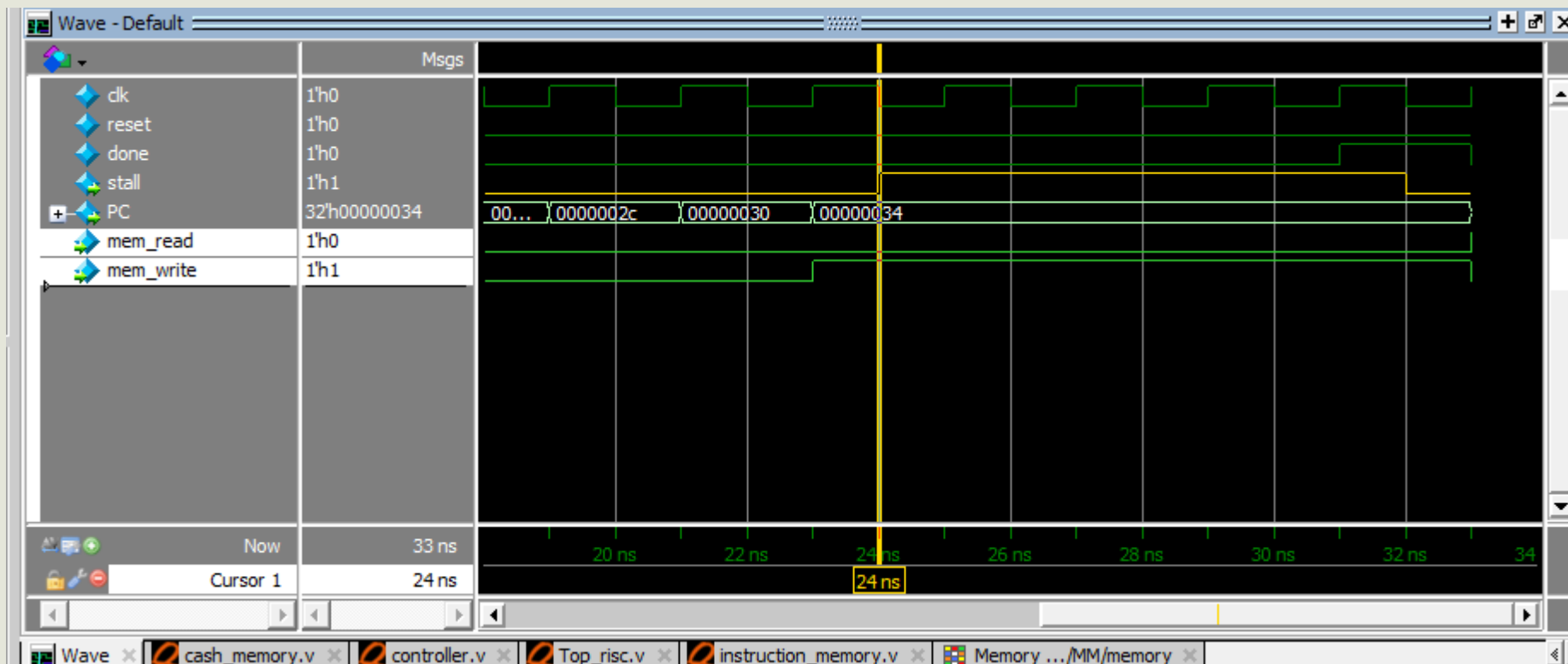
# RISC V Test Program

The Program writes the value 25 to address 100

# If successful, it should write the value 25 to address 100				
#	RISC-V Assembly	Description	Address	Machine Code
main:	addi x2, x0, 5	# x2 = 5	0	00500113
	addi x3, x0, 12	# x3 = 12	4	00C00193
	addi x7, x3, -9	# x7 = (12 - 9) = 3	8	FF718393
	or x4, x7, x2	# x4 = (3 OR 5) = 7	C	0023E233
	and x5, x3, x4	# x5 = (12 AND 7) = 4	10	0041F2B3
	add x5, x5, x4	# x5 = 4 + 7 = 11	14	004282B3
	beq x5, x7, end	# shouldn't be taken	18	02728863
	slt x4, x3, x4	# x4 = (12 < 7) = 0	1C	0041A233
	beq x4, x0, around	# should be taken	20	00020463
	addi x5, x0, 0	# shouldn't execute	24	00000293
around:	slt x4, x7, x2	# x4 = (3 < 5) = 1	28	0023A233
	add x7, x4, x5	# x7 = (1 + 11) = 12	2C	005203B3
	sub x7, x7, x2	# x7 = (12 - 5) = 7	30	402383B3
	sw x7, 84(x3)	# [96] = 7	34	0471AA23
	lw x2, 96(x0)	# x2 = [96] = 7	38	06002103
	add x9, x2, x5	# x9 = (7 + 11) = 18	3C	005104B3
	jal x3, end	# jump to end, x3 = 0x44	40	008001EF
	addi x2, x0, 1	# shouldn't execute	44	00100113
end:	add x2, x2, x9	# x2 = (7 + 18) = 25	48	00910133
	sw x2, 0x20(x3)	# [100] = 25	4C	0221A023
done:	beq x2, x2, done	# infinite loop	50	00210063

# Simulation Results

sw x7, 84(x3): Store 7 in location 96



# Simulation Results

sw x7, 84(x3) : Main Memory view

[illegible]

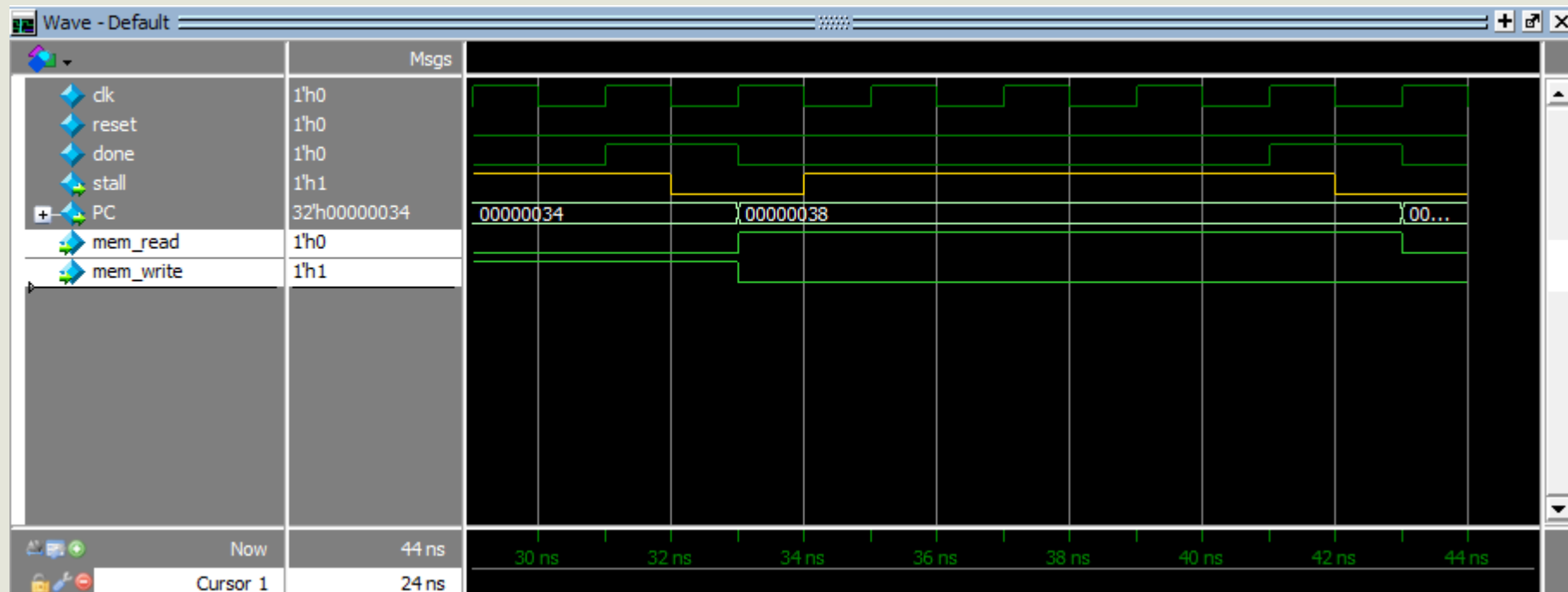


## sw x7, 84(x3) : Cache Memory View

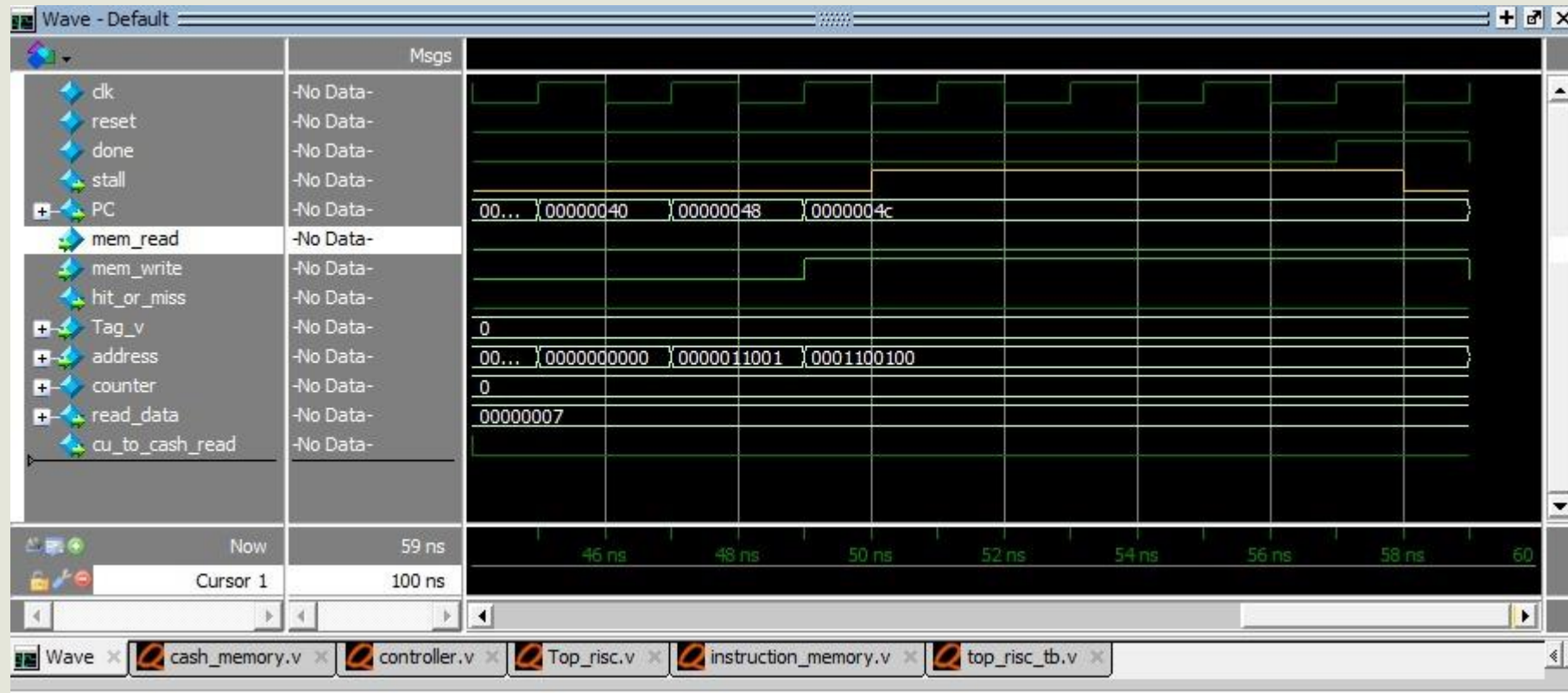
[illegible]

# Simulation Results

lw x2, 96(x0): load from location 96 to register x2



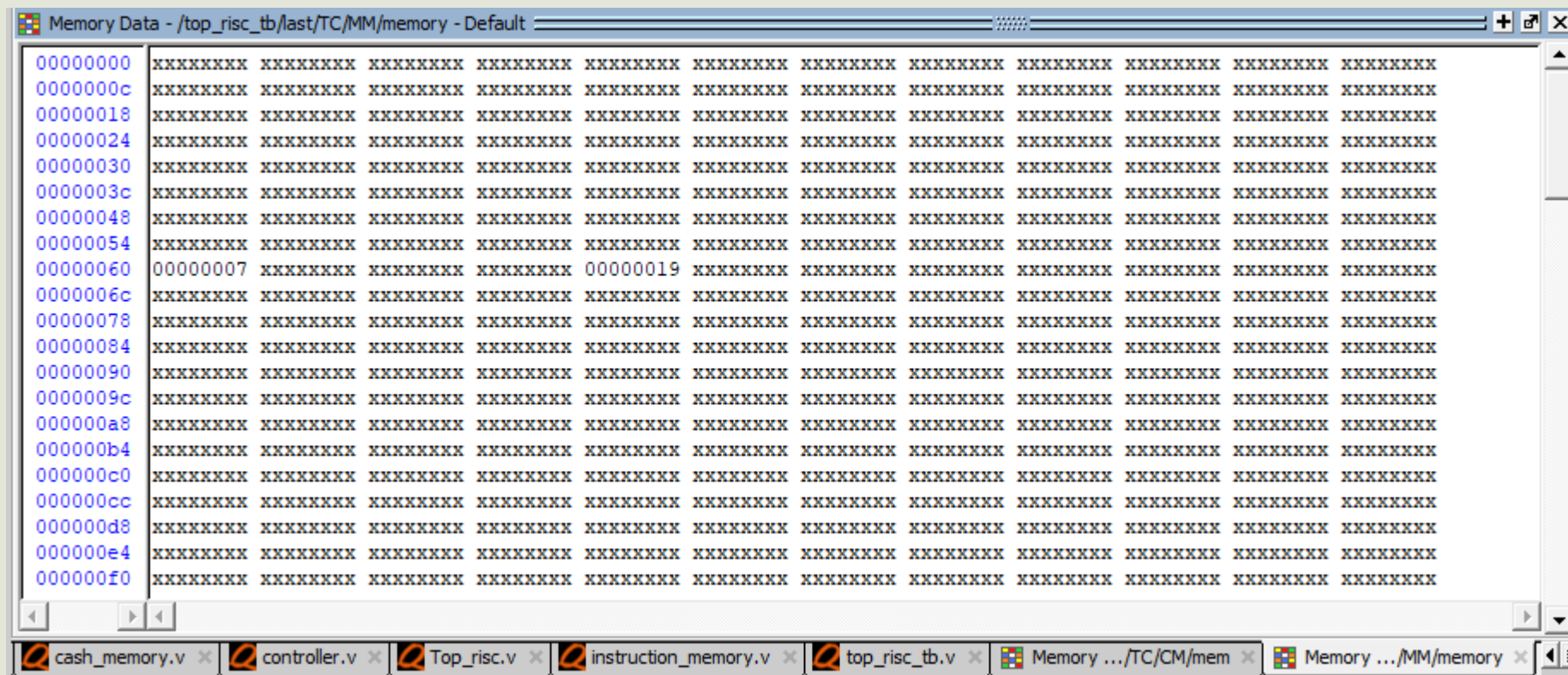
```
sw x2, 0x20(x3)
```





# Simulation Results

sw x2, 0x20(x3) : Main Memory view 0x19 Stored in in Location 0x64



```
Memory Data - /top_risc_tb/last/TC/MM/memory - Default
00000000 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
0000000c xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000018 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000024 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000030 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
0000003c xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000048 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000054 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000060 00000019 xxxxxxxx xxxxxxxx xxxxxxxx 00000019 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
0000006c xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000078 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000084 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
00000090 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
0000009c xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
000000a8 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
000000b4 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
000000c0 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
000000cc xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
000000d8 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
000000e4 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
000000f0 xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
```

cash\_memory.v controller.v Top\_risc.v instruction\_memory.v top\_risc\_tb.v Memory .../TC/CM/mem Memory .../MM/memory

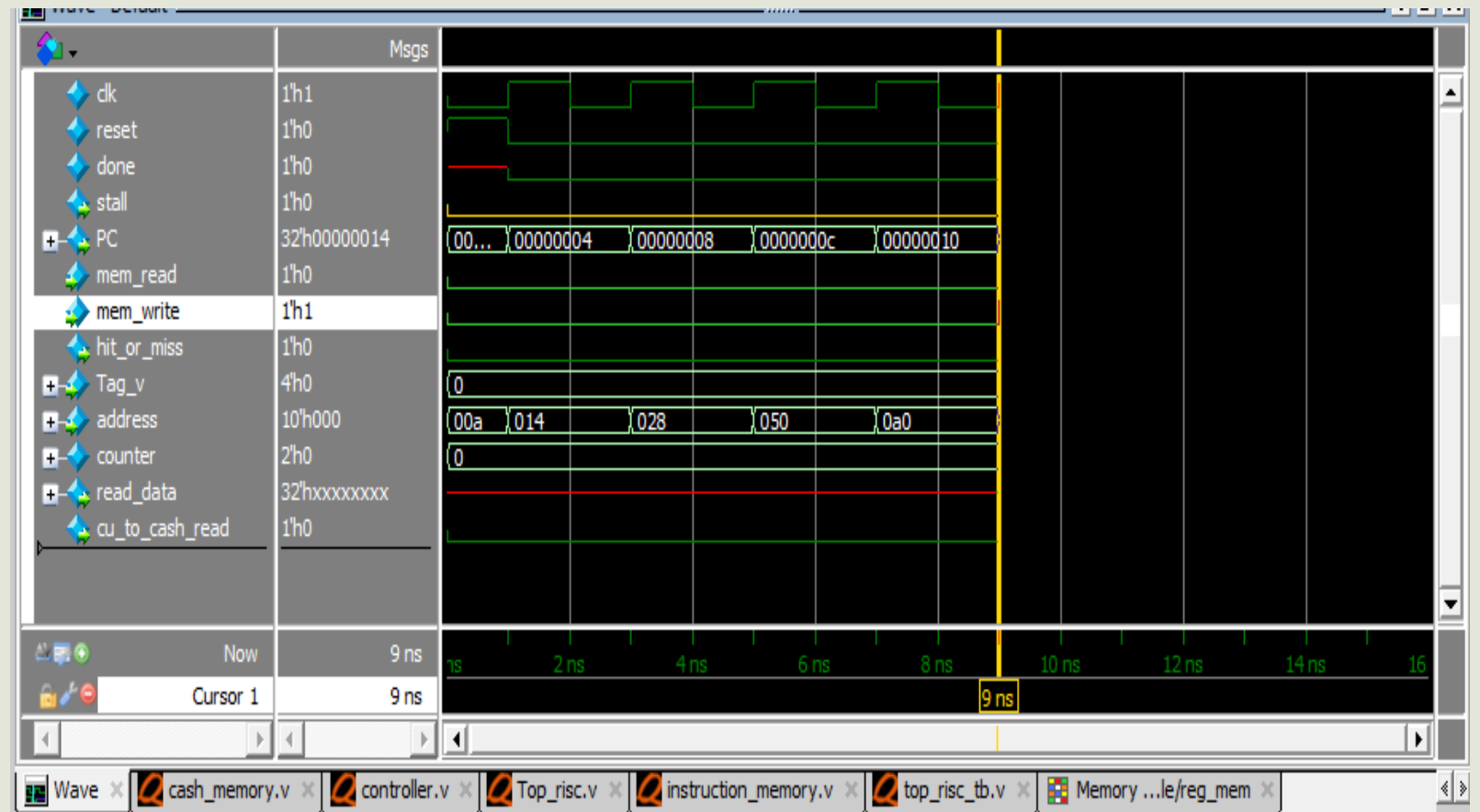
# Other Test Program

```
mem[0] = 32'b00000000101000000000000010010011; // addi x1, x0, 10
mem[1] = 32'b000000001010000000000000100010011; // addi x2, x0, 20
mem[2] = 32'b000000010100000000000000110010011; // addi x3, x0, 40
mem[3] = 32'b0000001010000000000000001000010011; // addi x4, x0, 80
mem[4] = 32'b0000010100000000000000001010010011; // addi x5, x0, 160
mem[5] = 32'b0000000000001000000010000000100011; // sw x1, 0(x0)
mem[6] = 32'b0000000000001000000010000010100011; // sw x1, 1(x0)
mem[7] = 32'b0000000000001000000010001000100011; // sw x2, 4(x0)
mem[8] = 32'b0000000000001100000010010000100011; // sw x3, 8(x0)
mem[9] = 32'b0000000000001000000010011000100011; // sw x4, 12(x0)
mem[10] = 32'b000000000010100000010011000100011; // sw x5, 12(x0)
mem[11] = 32'b0000000000000000000010010100000011; // lw x10, 0(x0)
mem[12] = 32'b0000000000100000000100101100000011; // lw x11, 4(x0)
mem[13] = 32'b0000000001000000000100110000000011; // lw x12, 8(x0)
mem[14] = 32'b0000000001100000000100110100000011; // lw x13, 12(x0)
mem[15] = 32'b0000000000100000000100101100000011; // lw x11, 4(x0)
mem[16] = 32'b000000000000100000010000100100011; // sw x1, 2(x0)
mem[17] = 32'b000000000001000000010010100000011; // lw x10, 0(x0)
```

```

addi x1, x0, 10
addi x2, x0, 20
addi x3, x0, 40
addi x4, x0, 80
addi x5, x0, 160

```





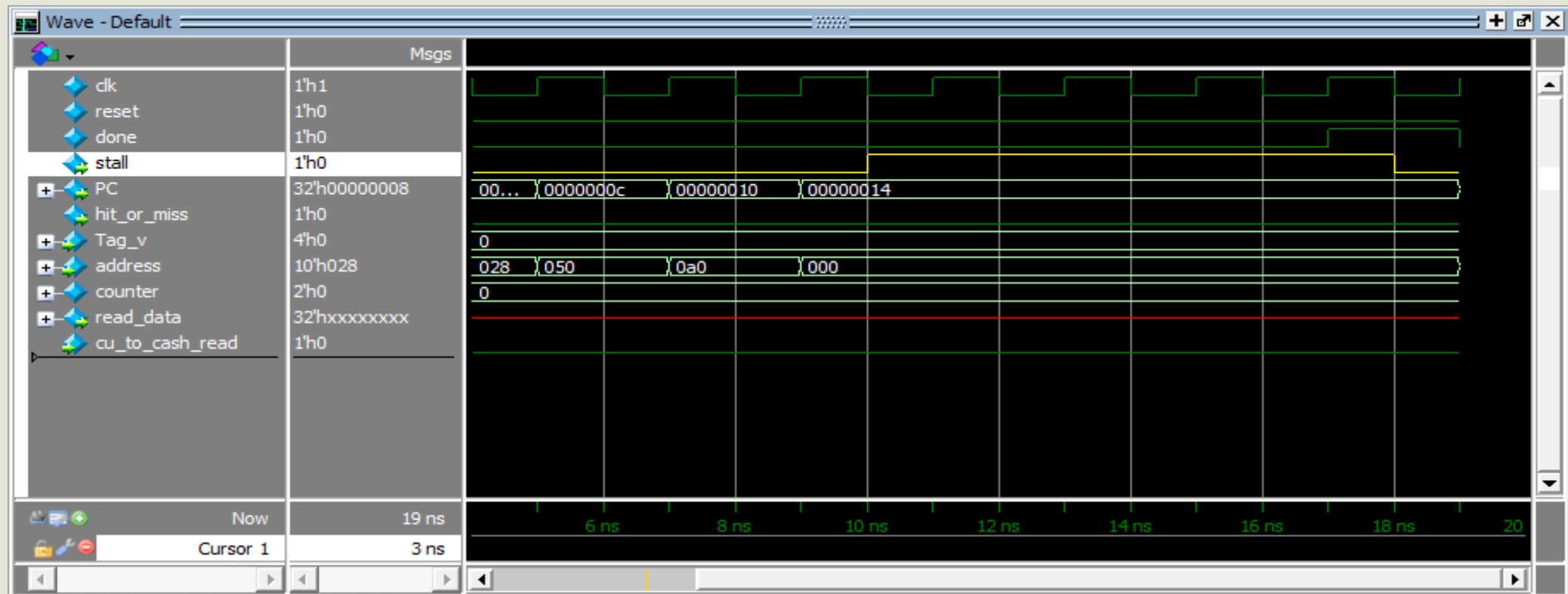
# Simulation Results

Store 10,20,40,80,160 in register file

[illegible]

# Simulation Results

sw x1, 0(x0)



# Simulation Results

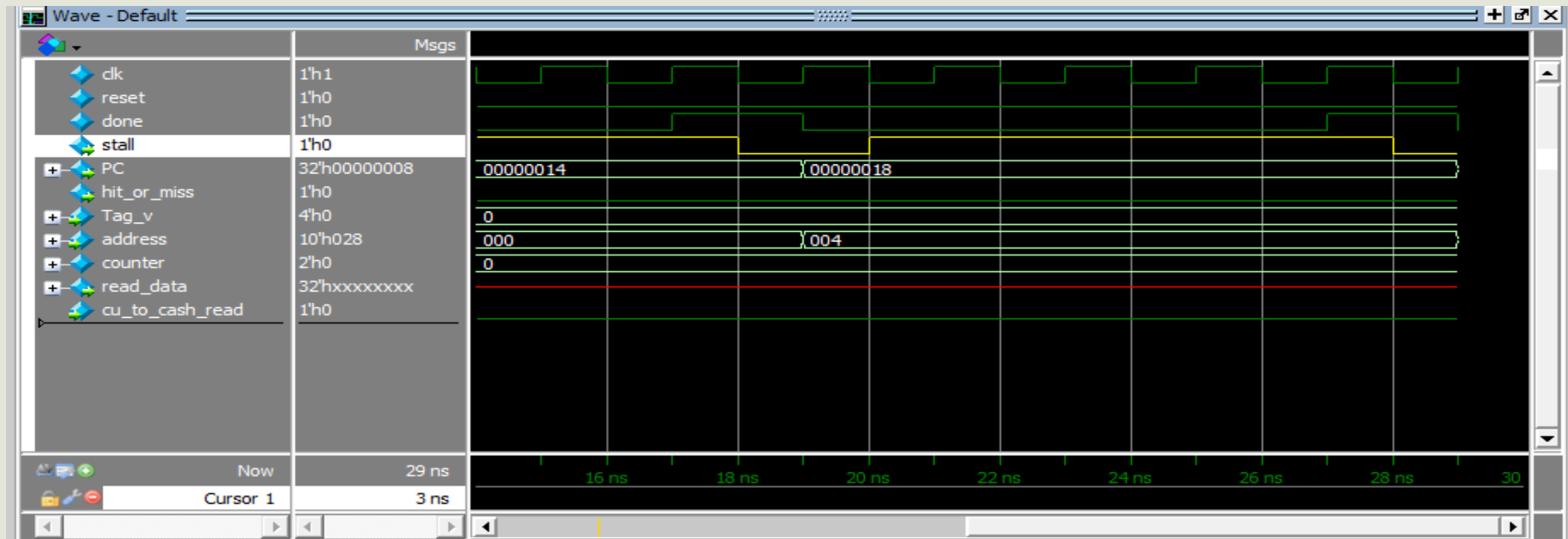
## Store 10 in location 0x00000000

[illegible]



# Simulation Results

sw x2, 4(x0)



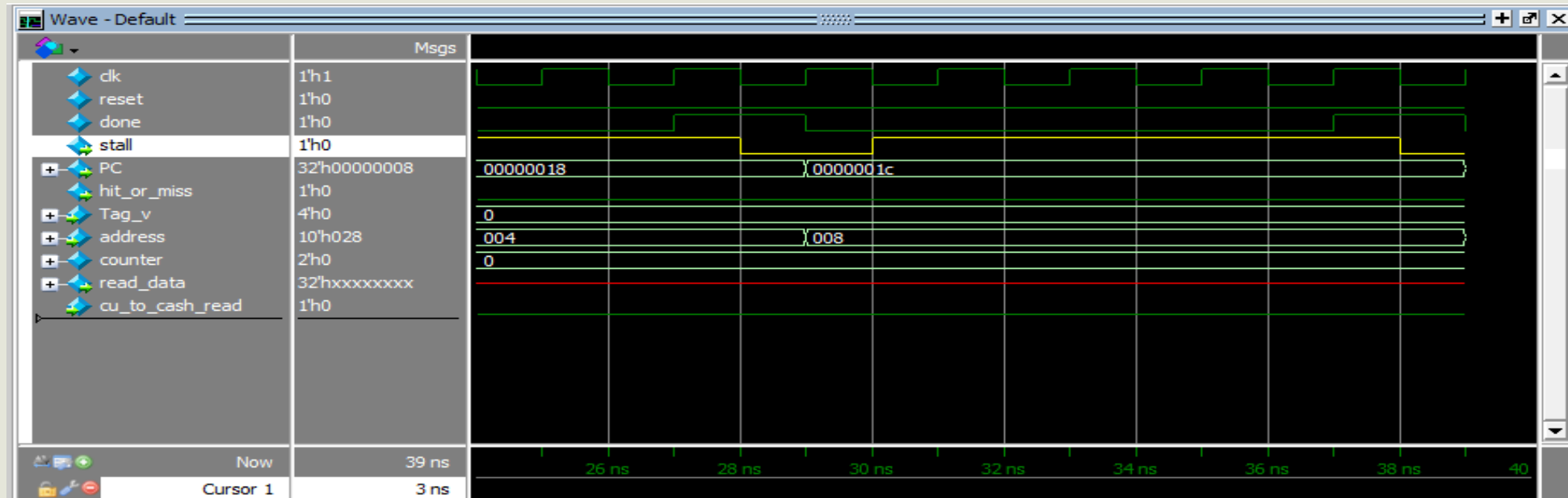
# Simulation Results

## Store 20 in location 0x00000004

[illegible]

# Simulation Results

sw x3, 8(x0)





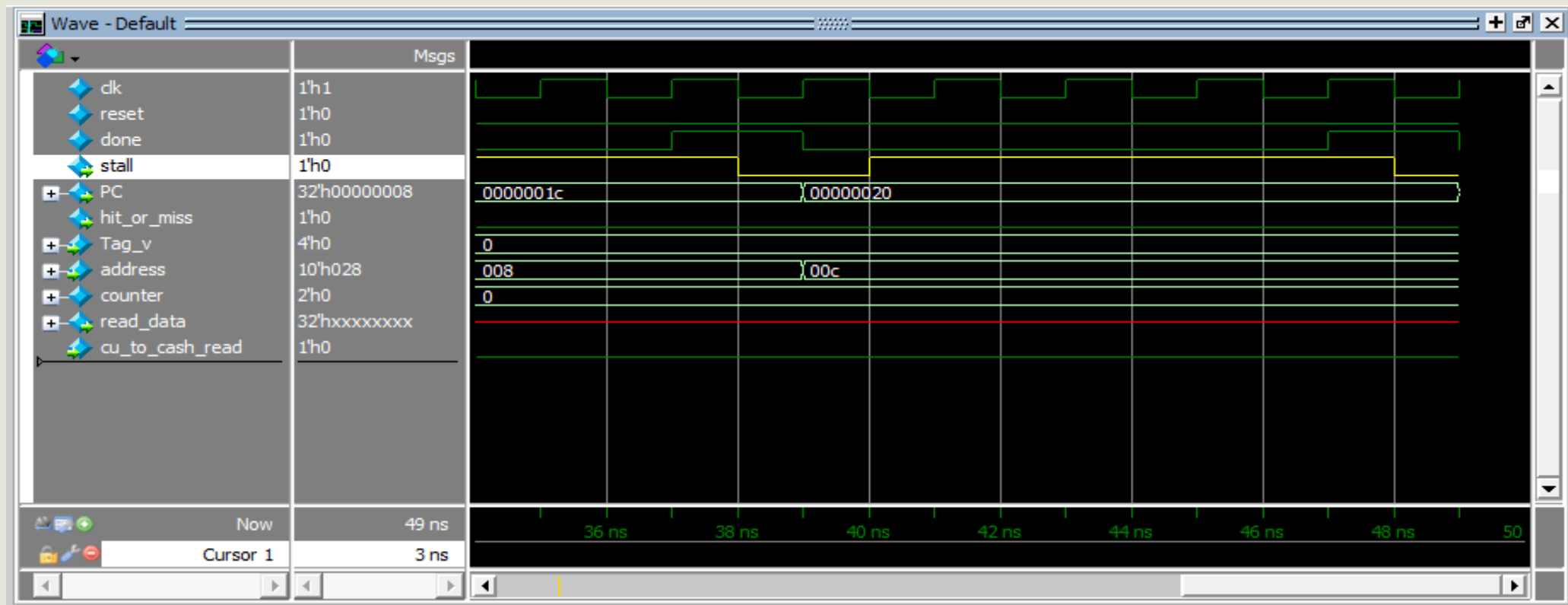
# Simulation Results

## Store 40 in location 0x00000008

[illegible]

# Simulation Results

sw x4, 12(x0)



# Simulation Results

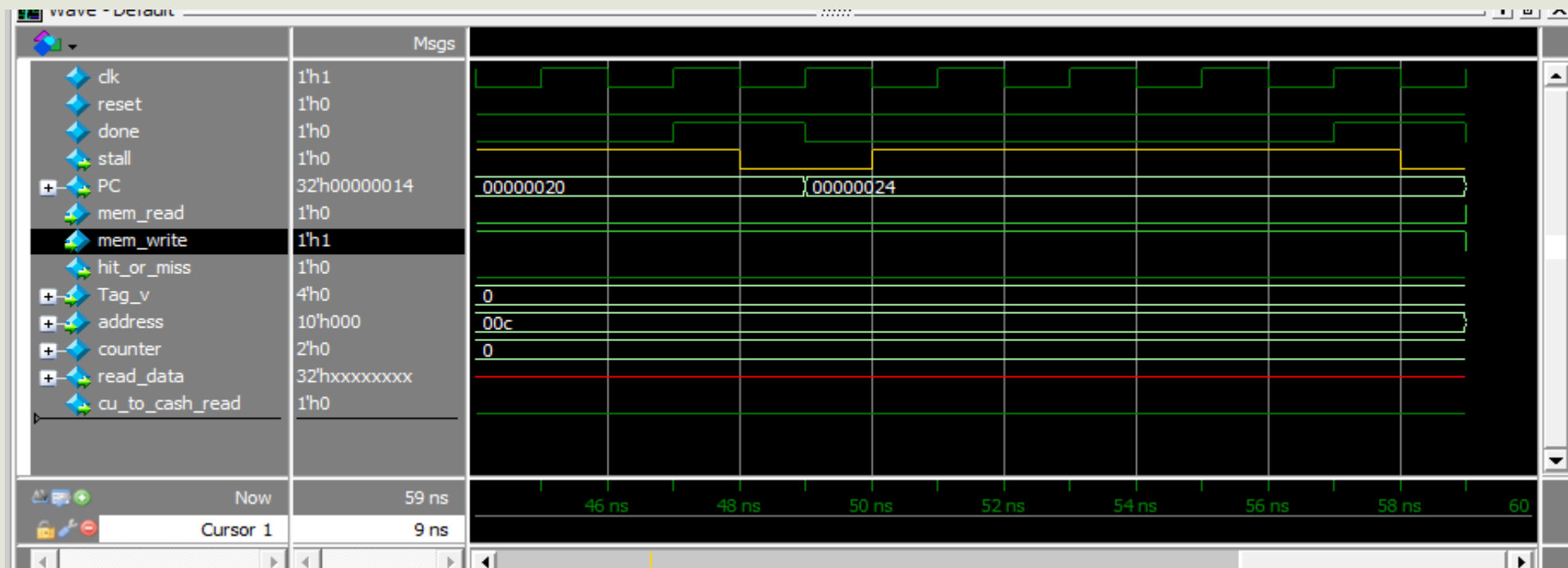
## Store 0x80 in location 0x0000000c

[illegible]



# Simulation Results

sw x5, 12(x0)



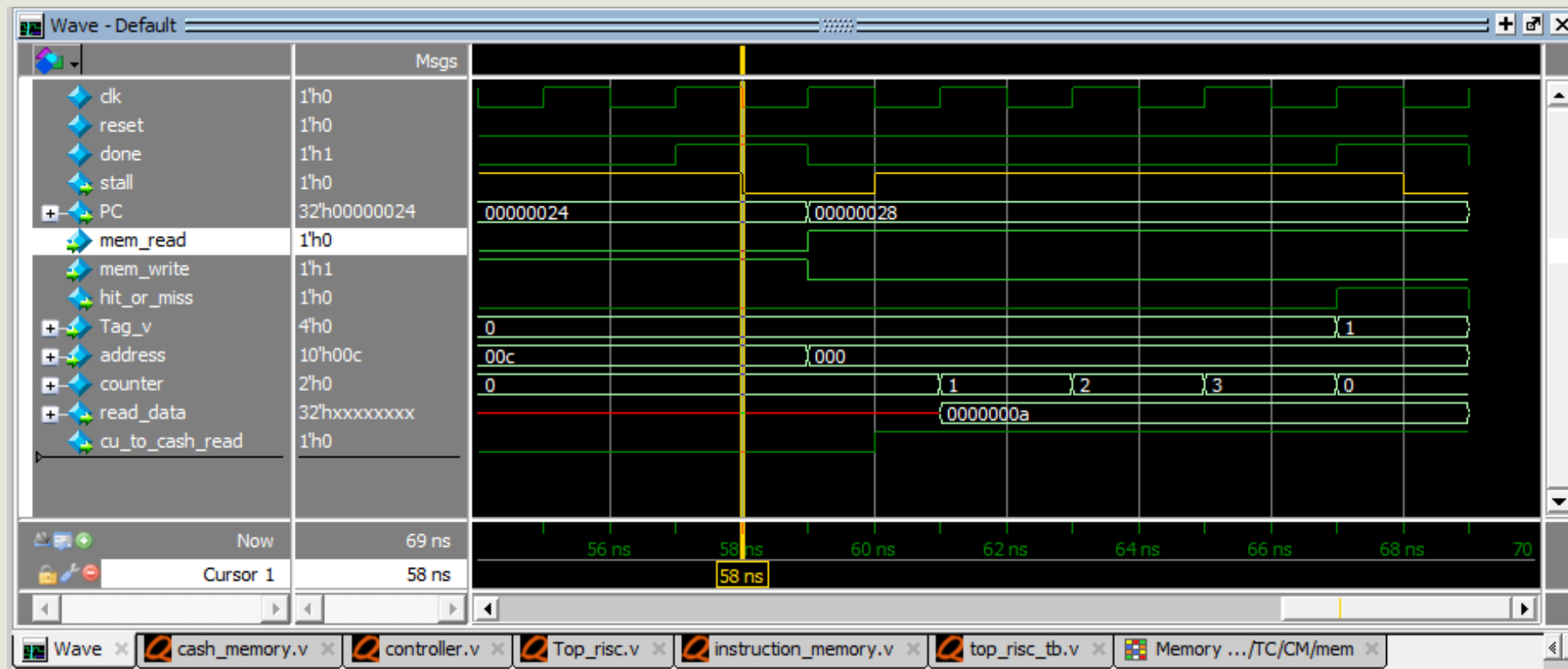
# Simulation Results

Store 0x160 in location 0x0000000c

[illegible]

# Simulation Results

lw x10, 0(x0)





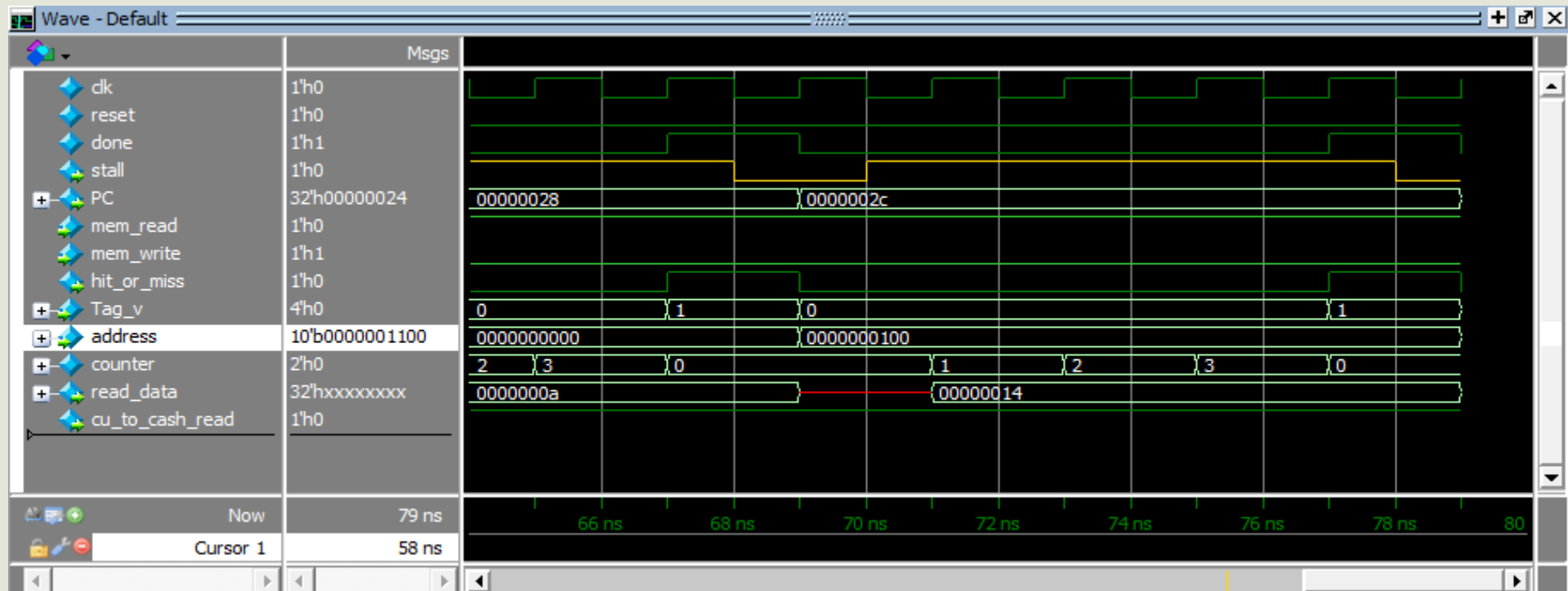
# Simulation Results

Store block 1 in cache memory then read the value 10

[illegible]

# Simulation Results

lw x11, 4(x0)



# Simulation Results

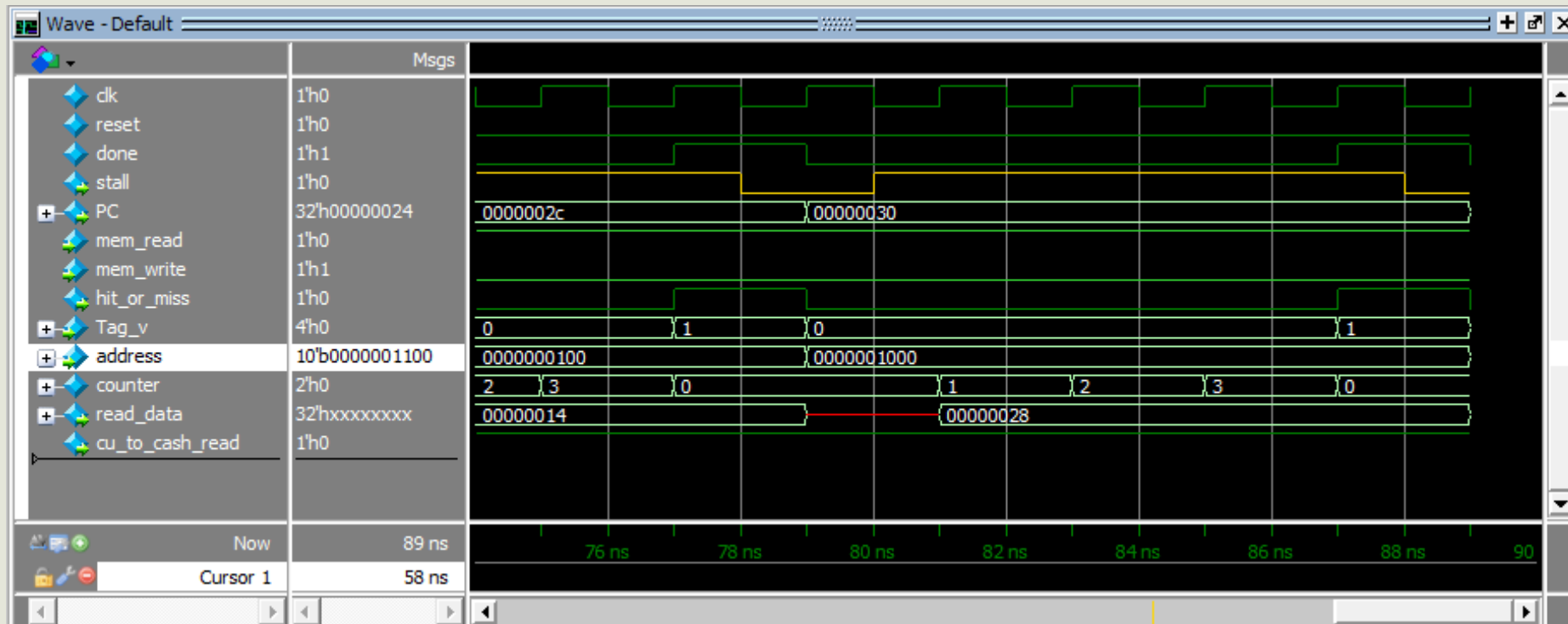
Store block 2 in cache memory then read the value 20

[illegible]



# Simulation Results

lw x12, 8(x0)



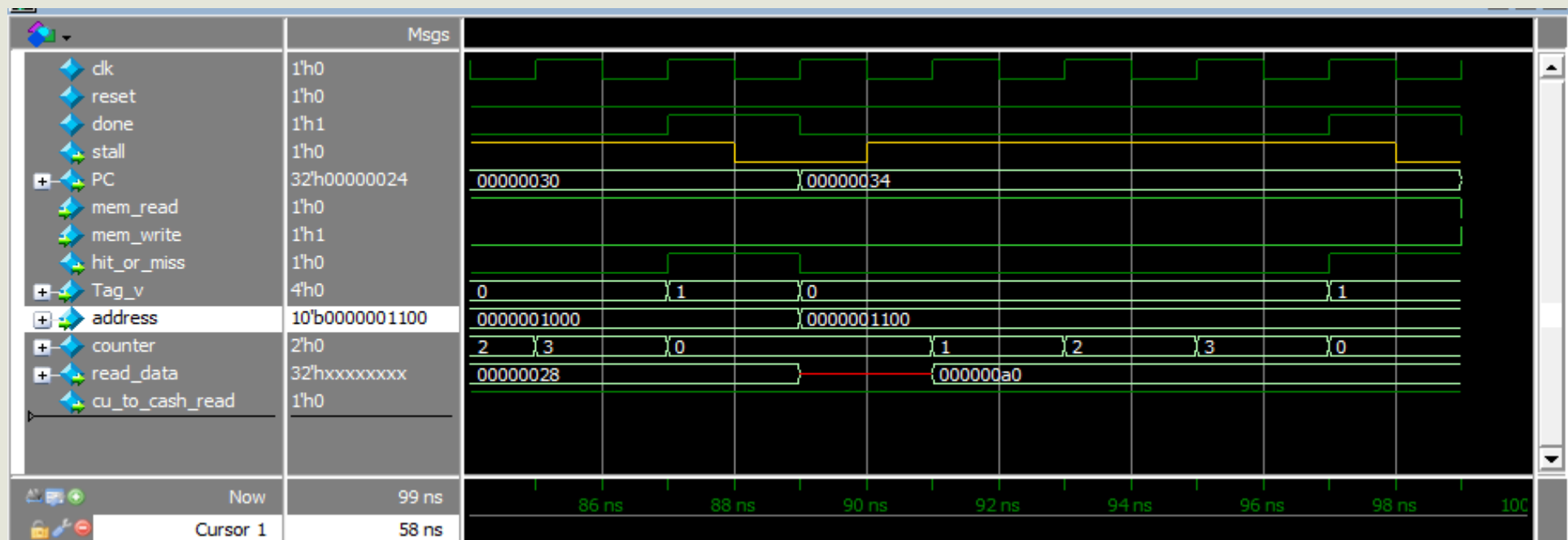
# Simulation Results

Store block 3 in cache memory then read the value 40

00000000	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000000a	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000014	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000028
00000003	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000006	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000009	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000000c	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000000f	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000012	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000015	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000018	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000001b	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000001e	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx

# Simulation Results

lw x13, 12(x0)



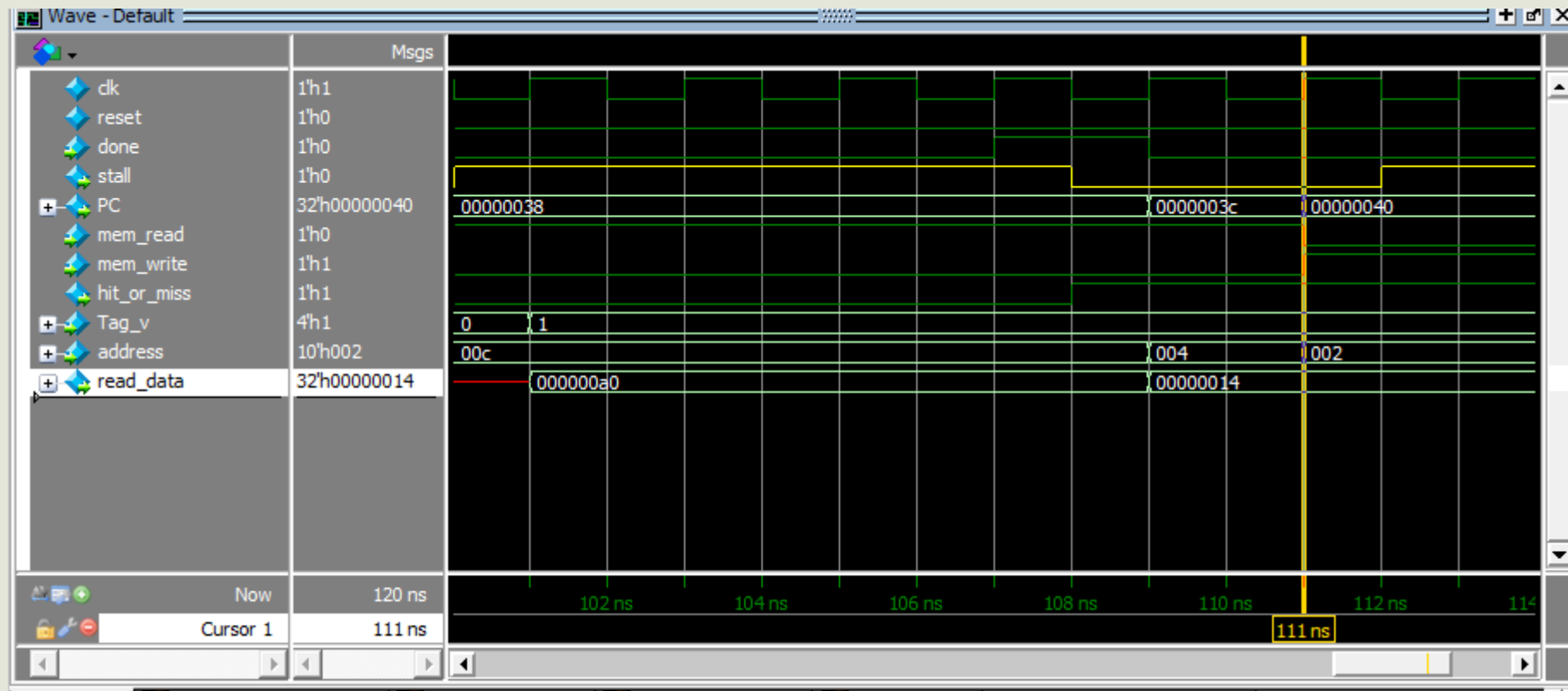


# Simulation Results

Store block 4 in cache memory then read the value 160

00000000	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000000a	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000014	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000028
00000003	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000a0	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000006	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000009	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000000c	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000000f	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000012	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000015	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000018	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000001b	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000001e	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xxxxxxxxxxxxxxxxxxxxxxxxxxxxx	

lw x11, 4(x0) here we read a value we reload to cache before so Hit

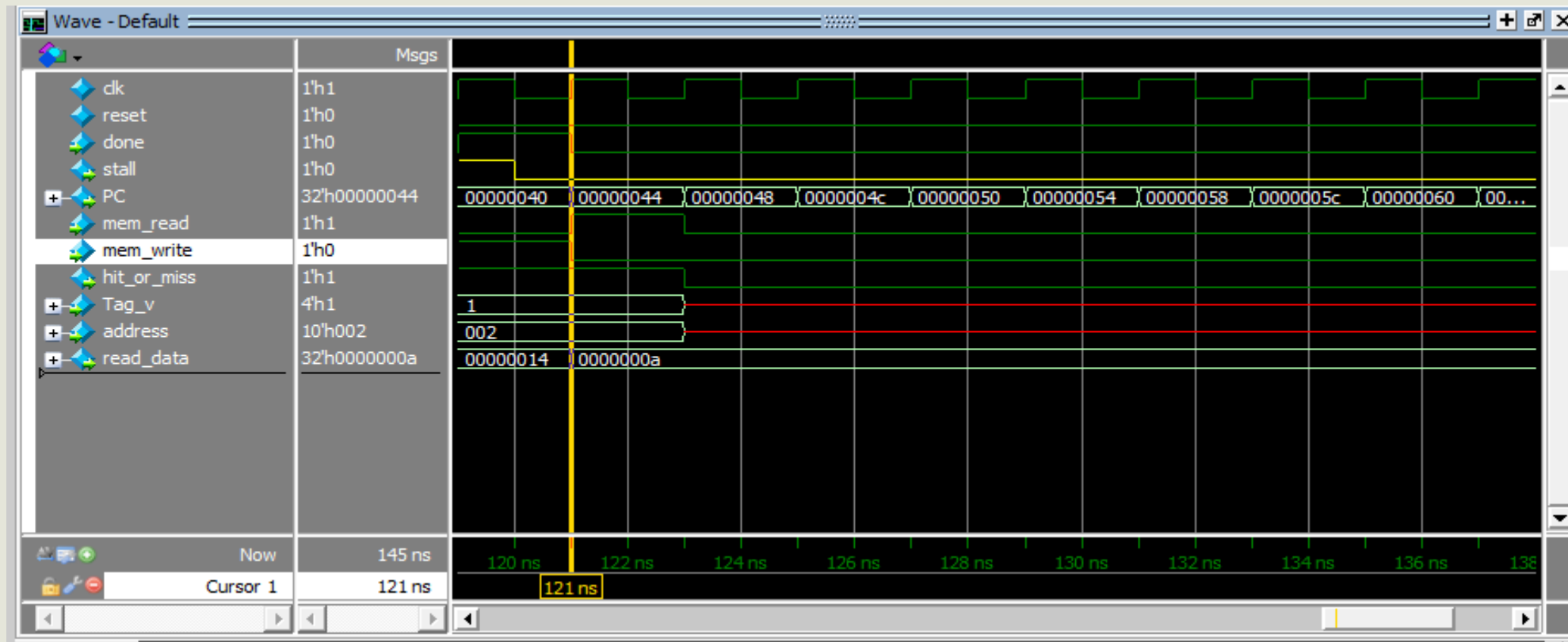


sw x1, 2(x0)

00000000	1xxxxxxxxx0000000a0000000a0000000a	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000014	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000028
00000003	1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000a0	0xx	0xx
00000006	0xx	0xx	0xx
00000009	0xx	0xx	0xx
0000000c	0xx	0xx	0xx
0000000f	0xx	0xx	0xx
00000012	0xx	0xx	0xx
00000015	0xx	0xx	0xx
00000018	0xx	0xx	0xx
0000001b	0xx	0xx	0xx
0000001e	0xx	0xx	0xx



lw x10, 0(x0) here we read a value we reload to cache before so Hit



Time's Up!!!

**Any Questions ?**

# Thank You

**Special Thanks to our instructors & Supervisor**

**.Eng Ahamed El-Gammal**

**.Eng Fayza Hamada**

