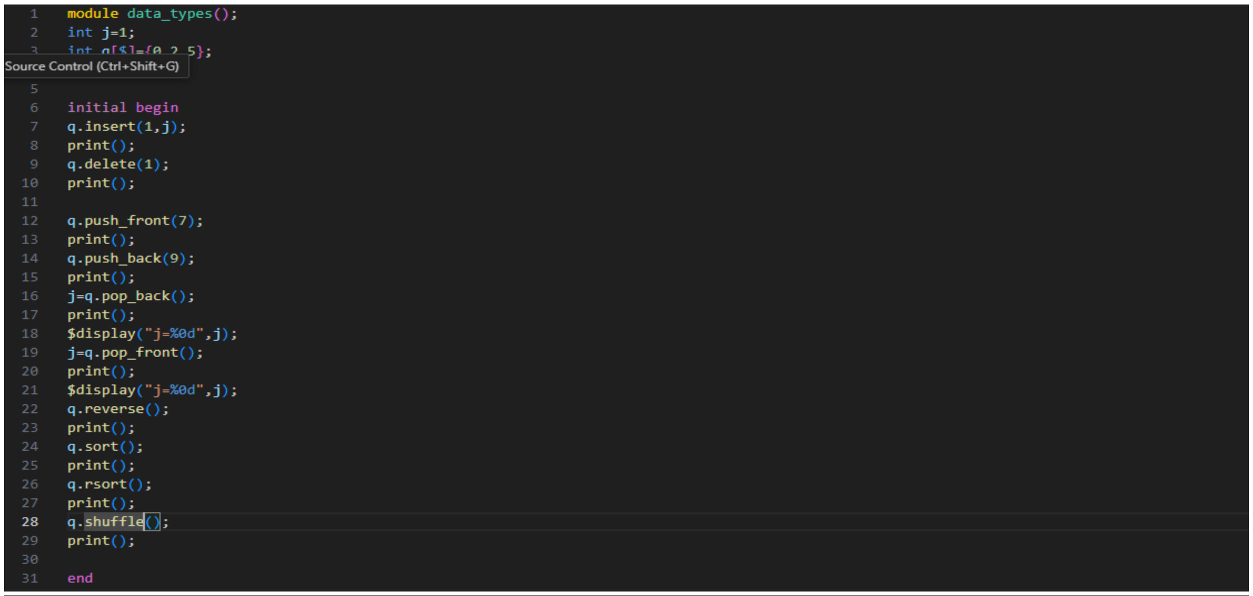
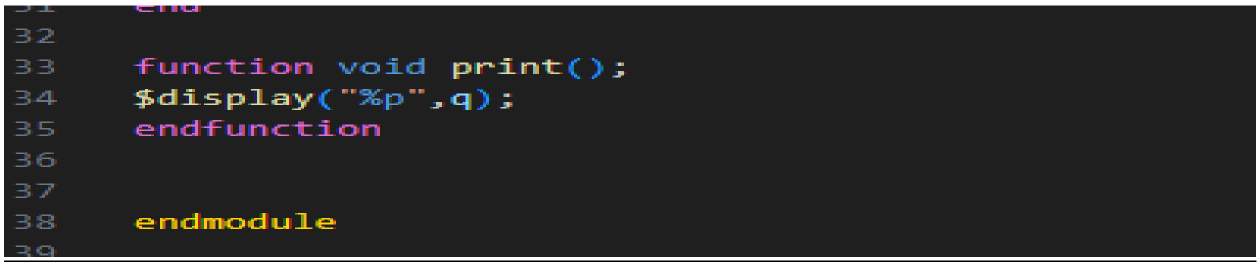
Assigment 3_extra

Queue project

Design

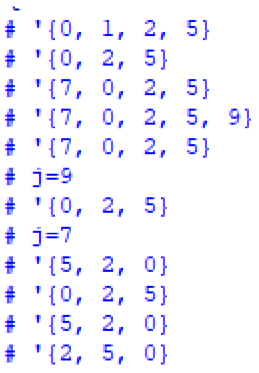


```
module data_types();
int j=1;
int q[$]={0,2,5};

initial begin
q.insert(1,j);
print();
q.delete(1);
print();

q.push_front(7);
print();
q.push_back(9);
print();
j=q.pop_back();
print();
$display("j=%0d",j);
j=q.pop_front();
print();
$display("j=%0d",j);
q.reverse();
print();
q.sort();
print();
q.rsort();
print();
q.shuffle();
print();

end
```



```

function void print();
$display("%p",q);
endfunction


endmodule
```

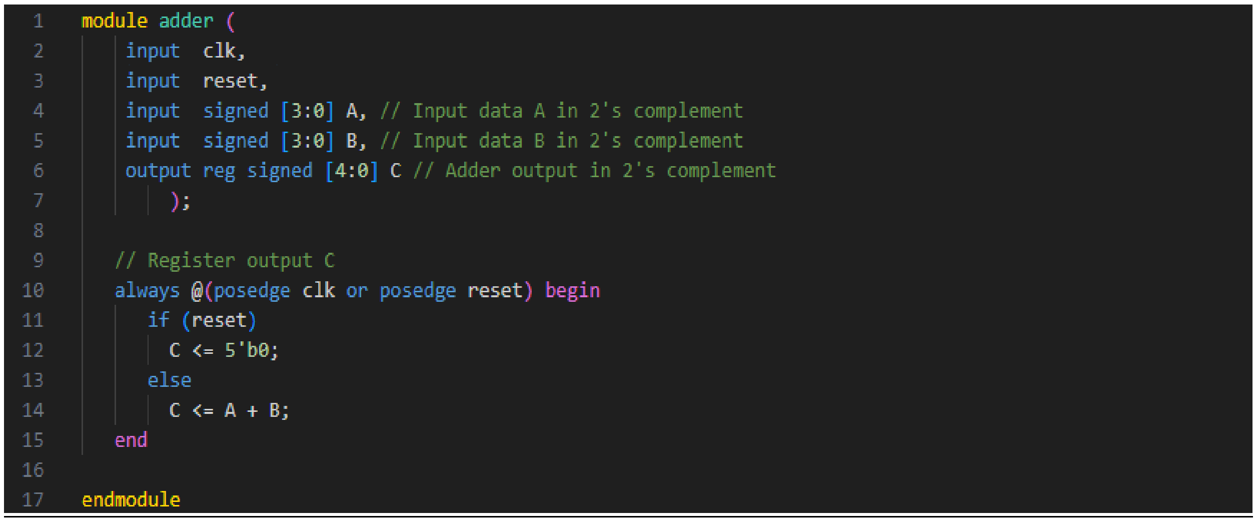
Result



```
# '{0, 1, 2, 5}
# '{0, 2, 5}
# '{7, 0, 2, 5}
# '{7, 0, 2, 5, 9}
# '{7, 0, 2, 5}
# j=9
# '{0, 2, 5}
# j=7
# '{5, 2, 0}
# '{0, 2, 5}
# '{5, 2, 0}
# '{2, 5, 0}
```

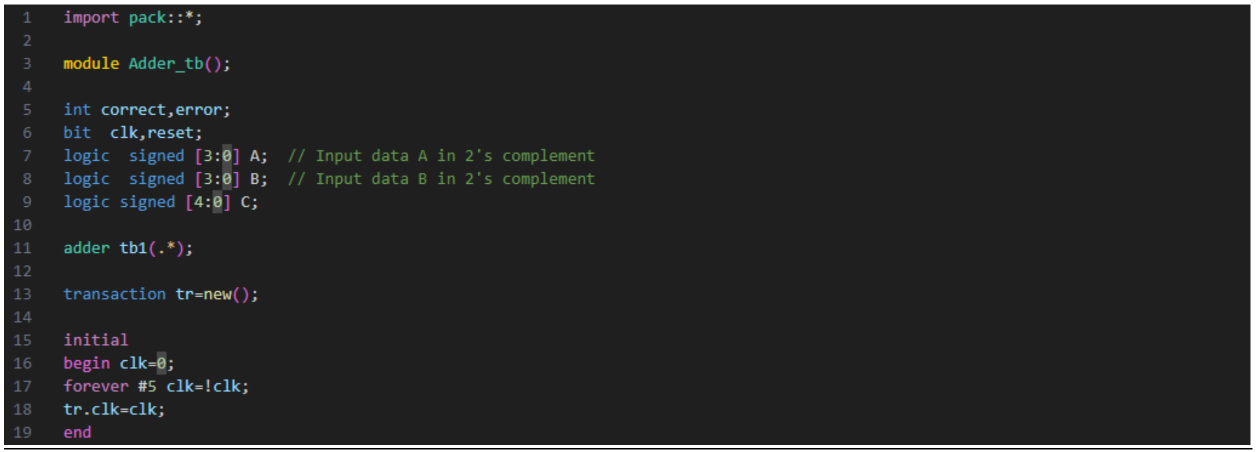
Adder project

Design

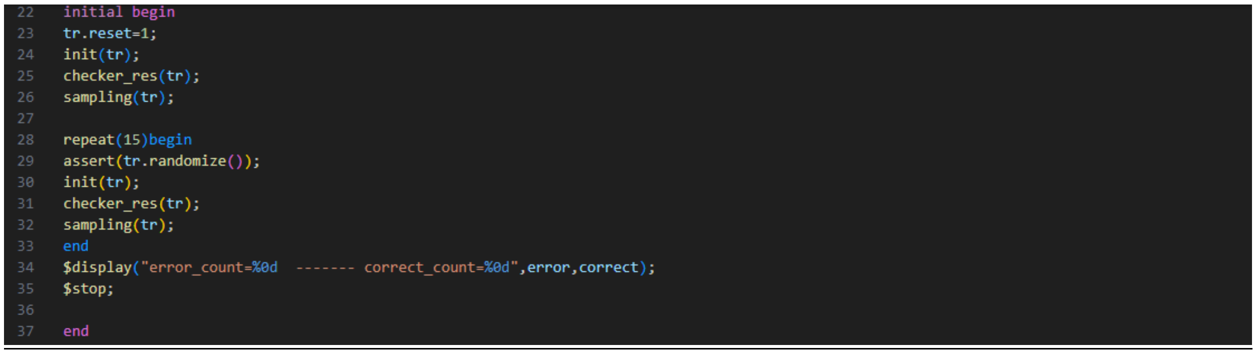


```
module adder (
    input  clk,
    input  reset,
    input  signed [3:0] A, // Input data A in 2's complement
    input  signed [3:0] B, // Input data B in 2's complement
    output reg signed [4:0] C // Adder output in 2's complement
        );

   // Register output C
   always @(posedge clk or posedge reset) begin
      if (reset)
        C <= 5'b0;
      else
        C <= A + B;
   end

endmodule
```

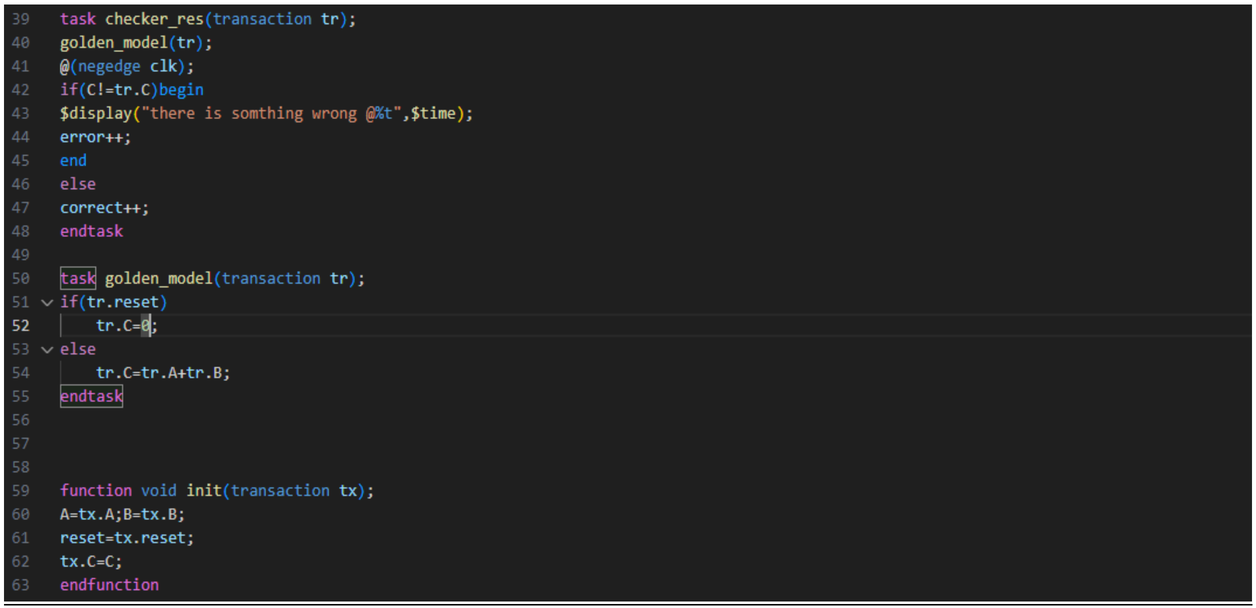
Tb



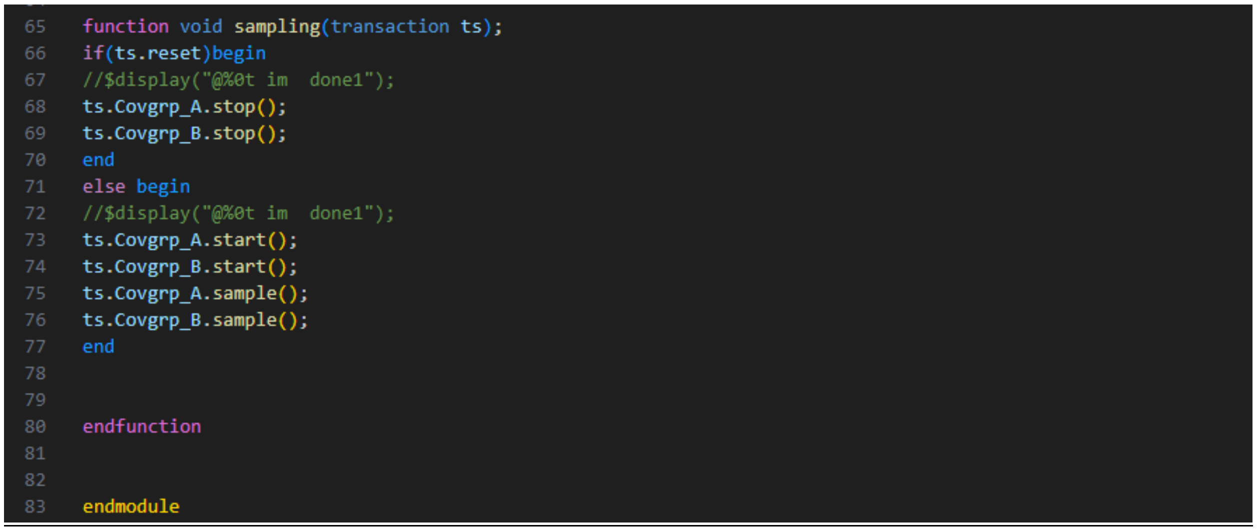
```
import pack::*;

module Adder_tb();

int correct,error;
bit  clk,reset;
logic  signed [3:0] A;  // Input data A in 2's complement
logic  signed [3:0] B;  // Input data B in 2's complement
logic signed [4:0] C;

adder tb1(.*);

transaction tr=new();

initial
begin clk=0;
forever #5 clk=!clk;
tr.clk=clk;
end
```



```
initial begin
tr.reset=1;
init(tr);
checker_res(tr);
sampling(tr);

repeat(15)begin
assert(tr.randomize());
init(tr);
checker_res(tr);
sampling(tr);
end
$display("error_count=%0d  ------- correct_count=%0d",error,correct);
$stop;

end
```

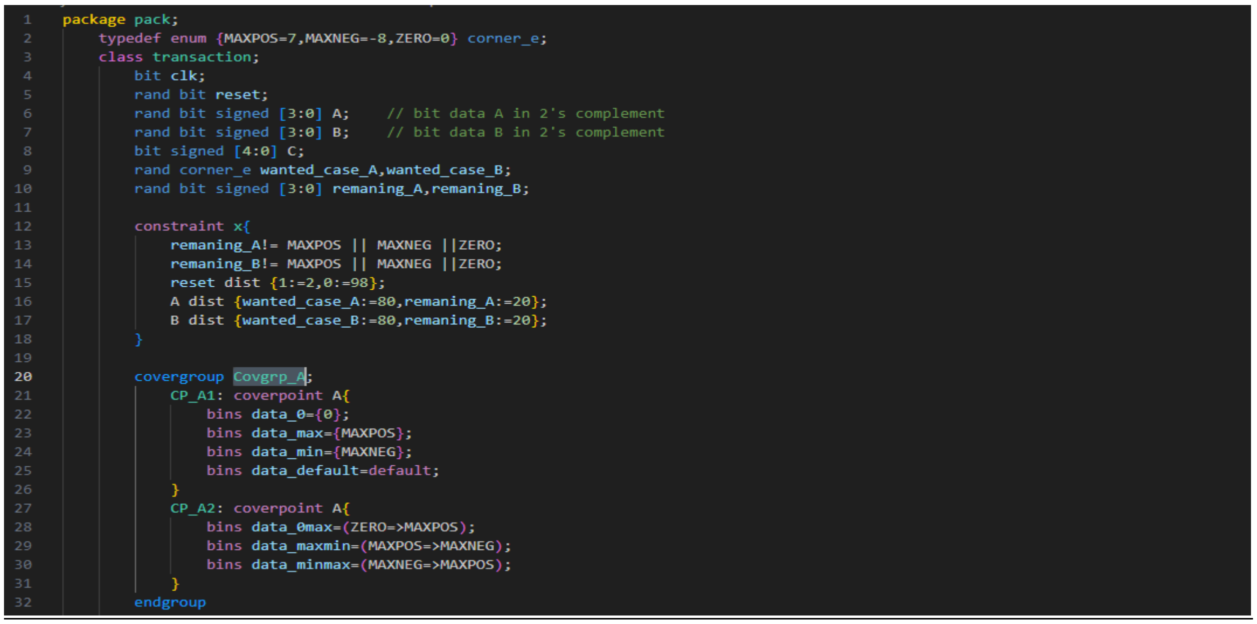


```
task checker_res(transaction tr);
golden_model(tr);
@(negedge clk);
if(C!=tr.C)begin
$display("there is somthing wrong @%t",$time);
error++;
end
else
correct++;
endtask

task golden_model(transaction tr);
if(tr.reset)
    tr.C=0;
else
    tr.C=tr.A+tr.B;
endtask



function void init(transaction tx);
A=tx.A;B=tx.B;
reset=tx.reset;
tx.C=C;
endfunction
```

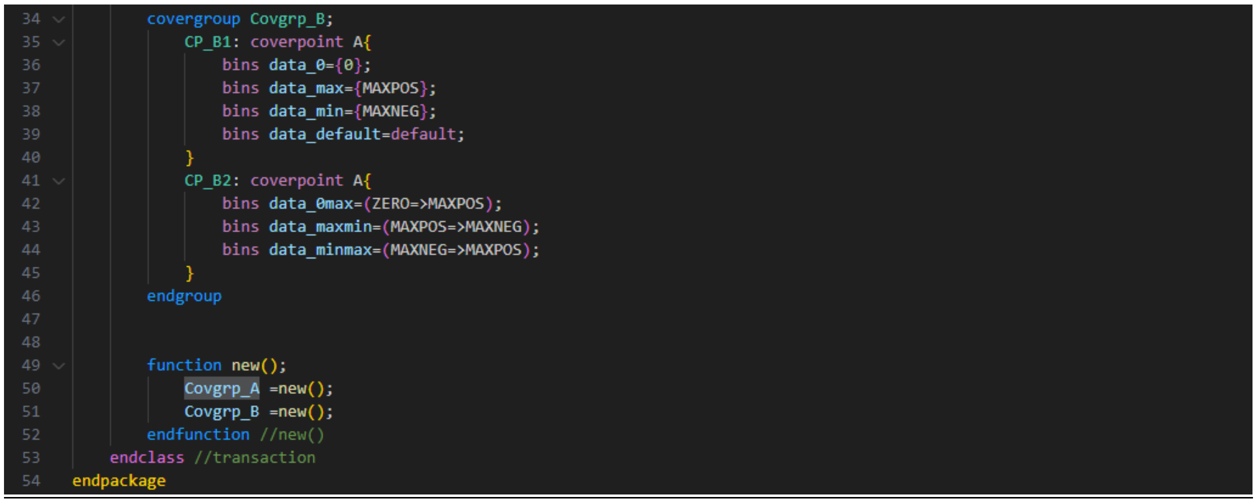


```
function void sampling(transaction ts);
if(ts.reset)begin
//$display("@%0t im  done1");
ts.Covgrp_A.stop();
ts.Covgrp_B.stop();
end
else begin
//$display("@%0t im  done1");
ts.Covgrp_A.start();
ts.Covgrp_B.start();
ts.Covgrp_A.sample();
ts.Covgrp_B.sample();
end


endfunction


endmodule
```

Package

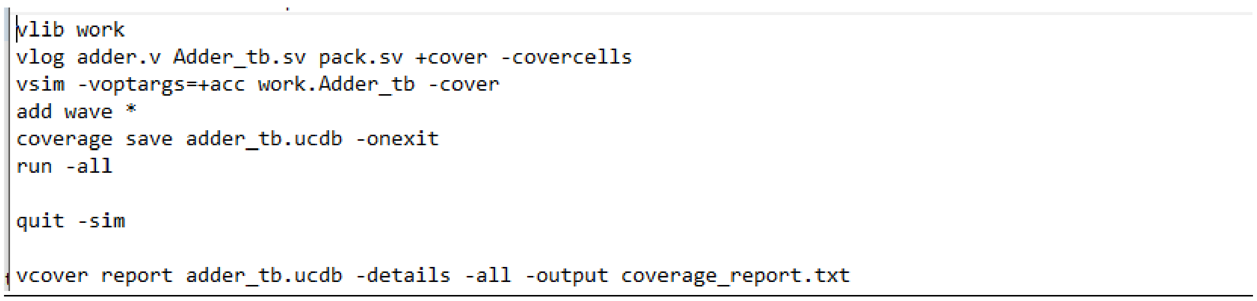


```
package pack;
    typedef enum {MAXPOS=7,MAXNEG=-8,ZERO=0} corner_e;
    class transaction;
        bit clk;
        rand bit reset;
        rand bit signed [3:0] A;    // bit data A in 2's complement
        rand bit signed [3:0] B;    // bit data B in 2's complement
        bit signed [4:0] C;
        rand corner_e wanted_case_A,wanted_case_B;
        rand bit signed [3:0] remaning_A,remaning_B;

        constraint x{
            remaning_A!= MAXPOS || MAXNEG ||ZERO;
            remaning_B!= MAXPOS || MAXNEG ||ZERO;
            reset dist {1:=2,0:=98};
            A dist {wanted_case_A:=80,remaning_A:=20};
            B dist {wanted_case_B:=80,remaning_B:=20};
        }

        covergroup Covgrp_A;
            CP_A1: coverpoint A{
                bins data_0={0};
                bins data_max={MAXPOS};
                bins data_min={MAXNEG};
                bins data_default=default;
            }
            CP_A2: coverpoint A{
                bins data_0max=(ZERO=>MAXPOS);
                bins data_maxmin=(MAXPOS=>MAXNEG);
                bins data_minmax=(MAXNEG=>MAXPOS);
            }
        endgroup
```



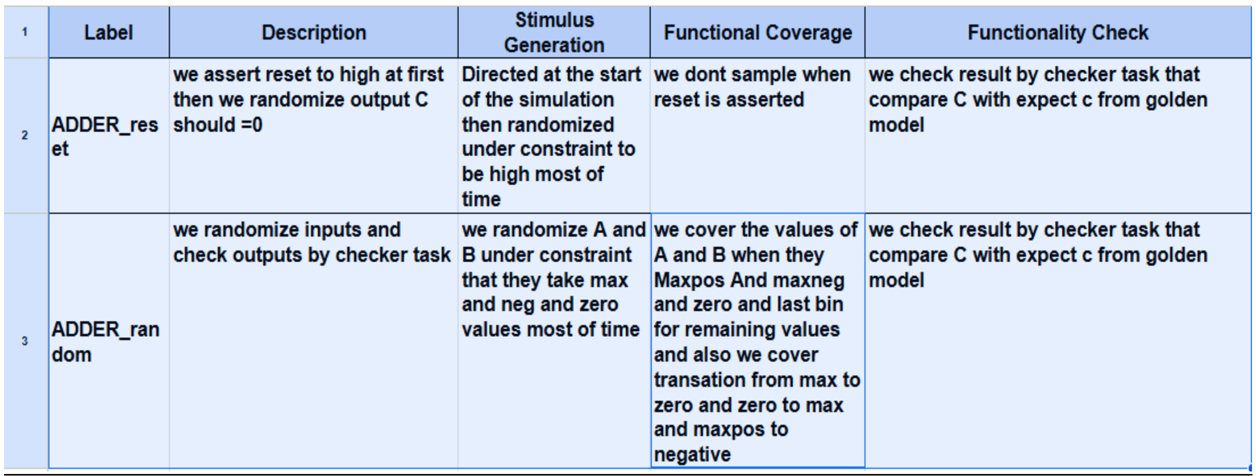
```
        covergroup Covgrp_B;
            CP_B1: coverpoint A{
                bins data_0={0};
                bins data_max={MAXPOS};
                bins data_min={MAXNEG};
                bins data_default=default;
            }
            CP_B2: coverpoint A{
                bins data_0max=(ZERO=>MAXPOS);
                bins data_maxmin=(MAXPOS=>MAXNEG);
                bins data_minmax=(MAXNEG=>MAXPOS);
            }
        endgroup


        function new();
            Covgrp_A =new();
            Covgrp_B =new();
        endfunction //new()
    endclass //transaction
endpackage
```

Do file



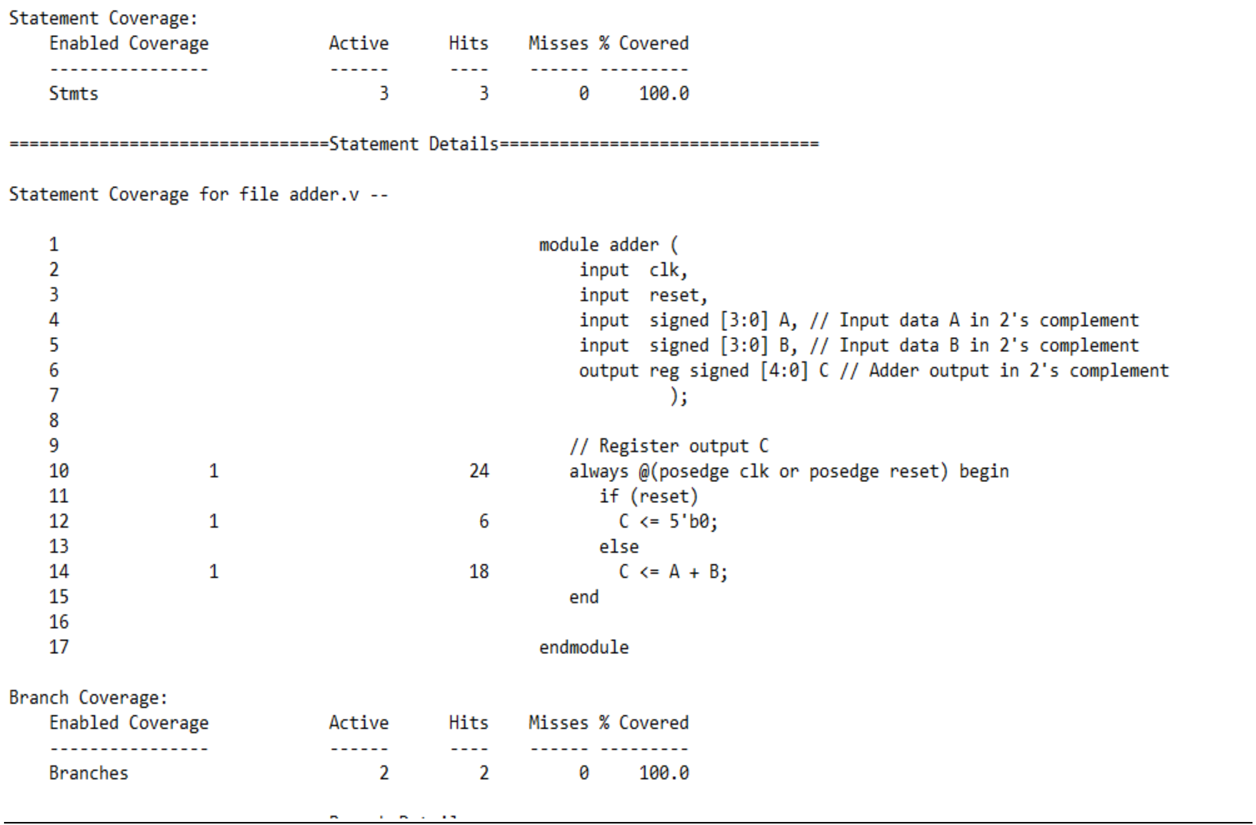
```
vlib work
vlog adder.v Adder_tb.sv pack.sv +cover -covercells
vsim -voptargs=+acc work.Adder_tb -cover
add wave *
coverage save adder_tb.ucdb -onexit
run -all

quit -sim

vcover report adder_tb.ucdb -details -all -output coverage_report.txt
```

Verification plan

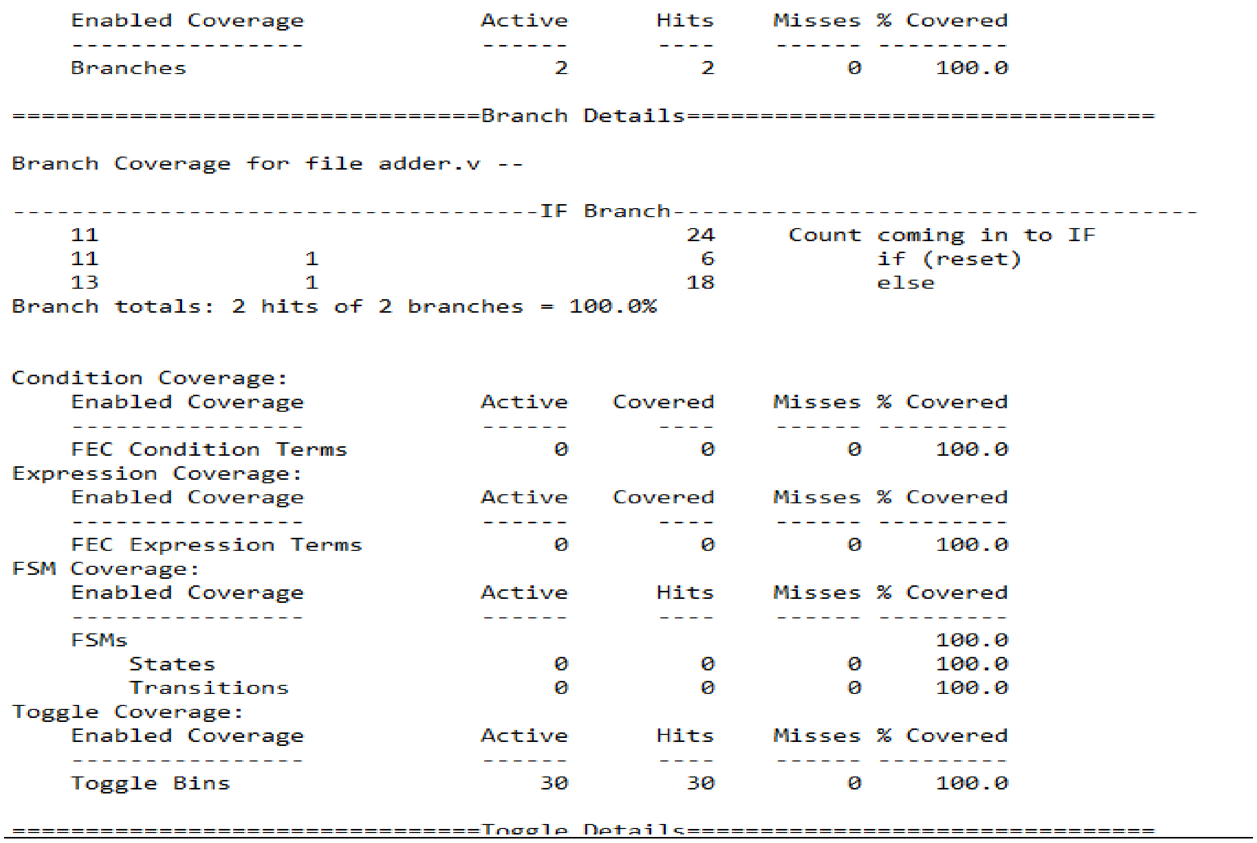


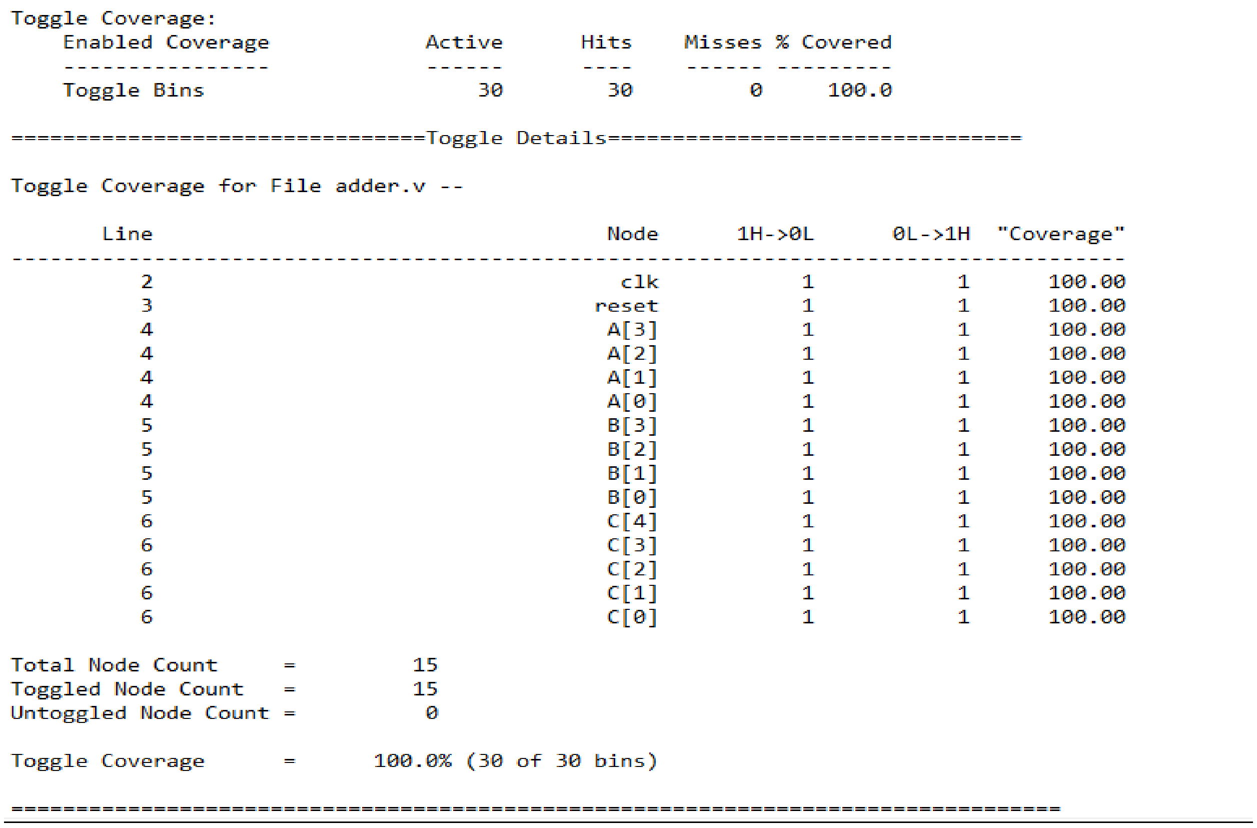
1	Label	Description	Stimulus Generation	Functional Coverage	Functionality Check
2	ADDER_reset	we assert reset to high at first then we randomize output C should =0	Directed at the start of the simulation then randomized under constraint to be high most of time	we dont sample when reset is asserted	we check result by checker task that compare C with expect c from golden model
3	ADDER_random	we randomize inputs and check outputs by checker task	we randomize A and B under constraint that they take max and neg and zero values most of time	we cover the values of A and B when they Maxpos And maxneg and zero and last bin for remaining values and also we cover transation from max to zero and zero to max and maxpos to negative	we check result by checker task that compare C with expect c from golden model

Code coverage

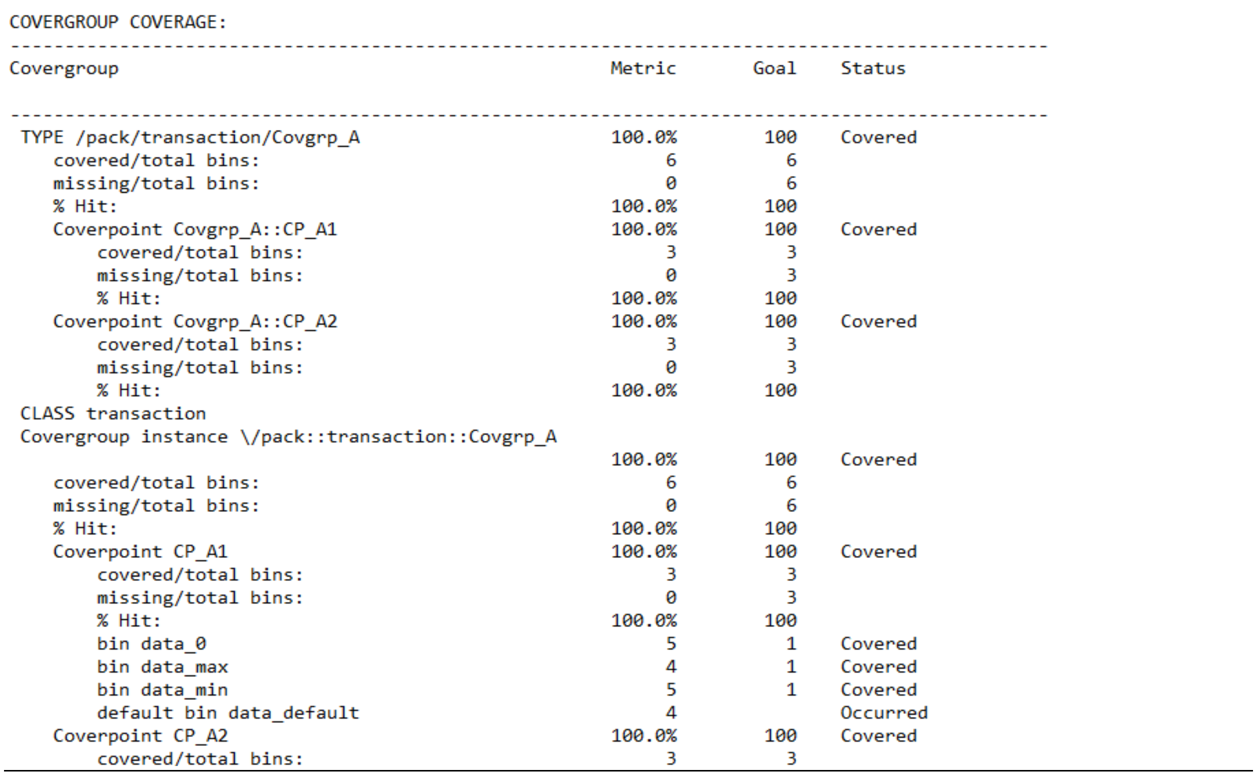


```
Statement Coverage:
    Enabled Coverage            Active      Hits    Misses % Covered
    ----------------            ------      ----    ------ ---------
    Stmts                            3         3         0     100.0

================================Statement Details================================

Statement Coverage for file adder.v --

    1                                                  module adder (
    2                                                      input  clk,
    3                                                      input  reset,
    4                                                      input  signed [3:0] A, // Input data A in 2's complement
    5                                                      input  signed [3:0] B, // Input data B in 2's complement
    6                                                      output reg signed [4:0] C // Adder output in 2's complement
    7                                                               );
    8
    9                                                     // Register output C
    10              1                           24        always @(posedge clk or posedge reset) begin
    11                                                       if (reset)
    12              1                            6             C <= 5'b0;
    13                                                       else
    14              1                           18             C <= A + B;
    15                                                    end
    16
    17                                                 endmodule

Branch Coverage:
    Enabled Coverage            Active      Hits    Misses % Covered
    ----------------            ------      ----    ------ ---------
    Branches                         2         2         0     100.0
```

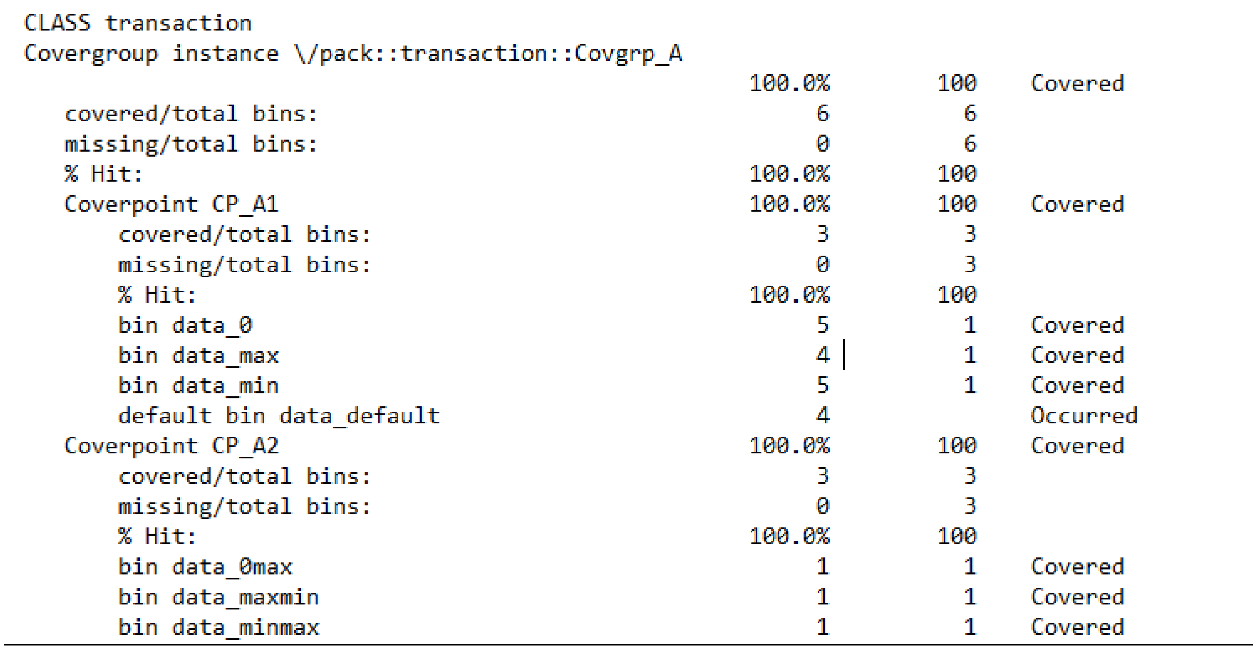

```
    Enabled Coverage            Active      Hits     Misses % Covered
    ----------------            ------      ----     ------ ---------
    Branches                         2         2          0     100.0

================================Branch Details================================

Branch Coverage for file adder.v --

-----------------------------------IF Branch-----------------------------------
    11                                        24      Count coming in to IF
    11              1                          6            if (reset)
    13              1                         18            else
Branch totals: 2 hits of 2 branches = 100.0%


Condition Coverage:
    Enabled Coverage            Active   Covered     Misses % Covered
    ----------------            ------      ----     ------ ---------
    FEC Condition Terms              0         0          0     100.0
Expression Coverage:
    Enabled Coverage            Active   Covered     Misses % Covered
    ----------------            ------      ----     ------ ---------
    FEC Expression Terms             0         0          0     100.0
FSM Coverage:
    Enabled Coverage            Active      Hits     Misses % Covered
    ----------------            ------      ----     ------ ---------
    FSMs                                                        100.0
        States                       0         0          0     100.0
        Transitions                  0         0          0     100.0
Toggle Coverage:
    Enabled Coverage            Active      Hits     Misses % Covered
    ----------------            ------      ----     ------ ---------
    Toggle Bins                     30        30          0     100.0

================================Toggle Details================================
```


```
Toggle Coverage:
    Enabled Coverage            Active      Hits     Misses % Covered
    ----------------            ------      ----     ------ ---------
    Toggle Bins                     30        30          0     100.0

================================Toggle Details================================

Toggle Coverage for File adder.v --

       Line                                 Node      1H->0L      0L->1H  "Coverage"
---------------------------------------------------------------------------------
          2                                  clk           1           1      100.00
          3                                reset           1           1      100.00
          4                                 A[3]           1           1      100.00
          4                                 A[2]           1           1      100.00
          4                                 A[1]           1           1      100.00
          4                                 A[0]           1           1      100.00
          5                                 B[3]           1           1      100.00
          5                                 B[2]           1           1      100.00
          5                                 B[1]           1           1      100.00
          5                                 B[0]           1           1      100.00
          6                                 C[4]           1           1      100.00
          6                                 C[3]           1           1      100.00
          6                                 C[2]           1           1      100.00
          6                                 C[1]           1           1      100.00
          6                                 C[0]           1           1      100.00

Total Node Count     =         15
Toggled Node Count   =         15
Untoggled Node Count =          0

Toggle Coverage      =      100.0% (30 of 30 bins)

=============================================================================
```

Functional coverage



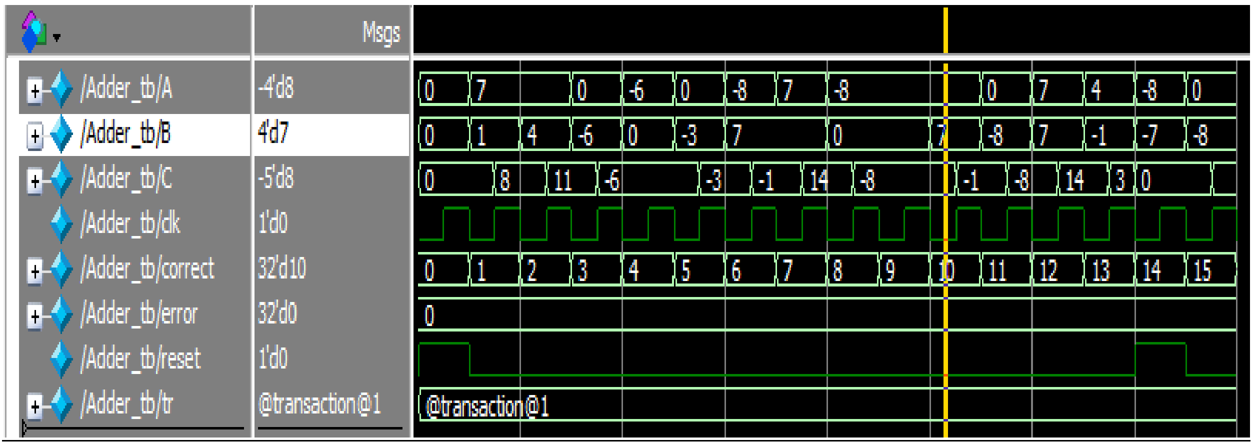
```
COVERGROUP COVERAGE:
-----------------------------------------------------------------------------------------------
Covergroup                                             Metric       Goal    Status

-----------------------------------------------------------------------------------------------
 TYPE /pack/transaction/Covgrp_A                       100.0%        100    Covered
    covered/total bins:                                     6          6
    missing/total bins:                                     0          6
    % Hit:                                             100.0%        100
    Coverpoint Covgrp_A::CP_A1                         100.0%        100    Covered
        covered/total bins:                                 3          3
        missing/total bins:                                 0          3
        % Hit:                                         100.0%        100
    Coverpoint Covgrp_A::CP_A2                         100.0%        100    Covered
        covered/total bins:                                 3          3
        missing/total bins:                                 0          3
        % Hit:                                         100.0%        100
 CLASS transaction
 Covergroup instance \/pack::transaction::Covgrp_A
                                                       100.0%        100    Covered
    covered/total bins:                                     6          6
    missing/total bins:                                     0          6
    % Hit:                                             100.0%        100
    Coverpoint CP_A1                                   100.0%        100    Covered
        covered/total bins:                                 3          3
        missing/total bins:                                 0          3
        % Hit:                                         100.0%        100
        bin data_0                                          5          1    Covered
        bin data_max                                        4          1    Covered
        bin data_min                                        5          1    Covered
        default bin data_default                            4               Occurred
    Coverpoint CP_A2                                   100.0%        100    Covered
        covered/total bins:                                 3          3
```



```
 CLASS transaction
 Covergroup instance \/pack::transaction::Covgrp_A
                                                       100.0%        100    Covered
    covered/total bins:                                     6          6
    missing/total bins:                                     0          6
    % Hit:                                             100.0%        100
    Coverpoint CP_A1                                   100.0%        100    Covered
        covered/total bins:                                 3          3
        missing/total bins:                                 0          3
        % Hit:                                         100.0%        100
        bin data_0                                          5          1    Covered
        bin data_max                                        4          1    Covered
        bin data_min                                        5          1    Covered
        default bin data_default                            4               Occurred
    Coverpoint CP_A2                                   100.0%        100    Covered
        covered/total bins:                                 3          3
        missing/total bins:                                 0          3
        % Hit:                                         100.0%        100
        bin data_0max                                       1          1    Covered
        bin data_maxmin                                     1          1    Covered
        bin data_minmax                                     1          1    Covered
```

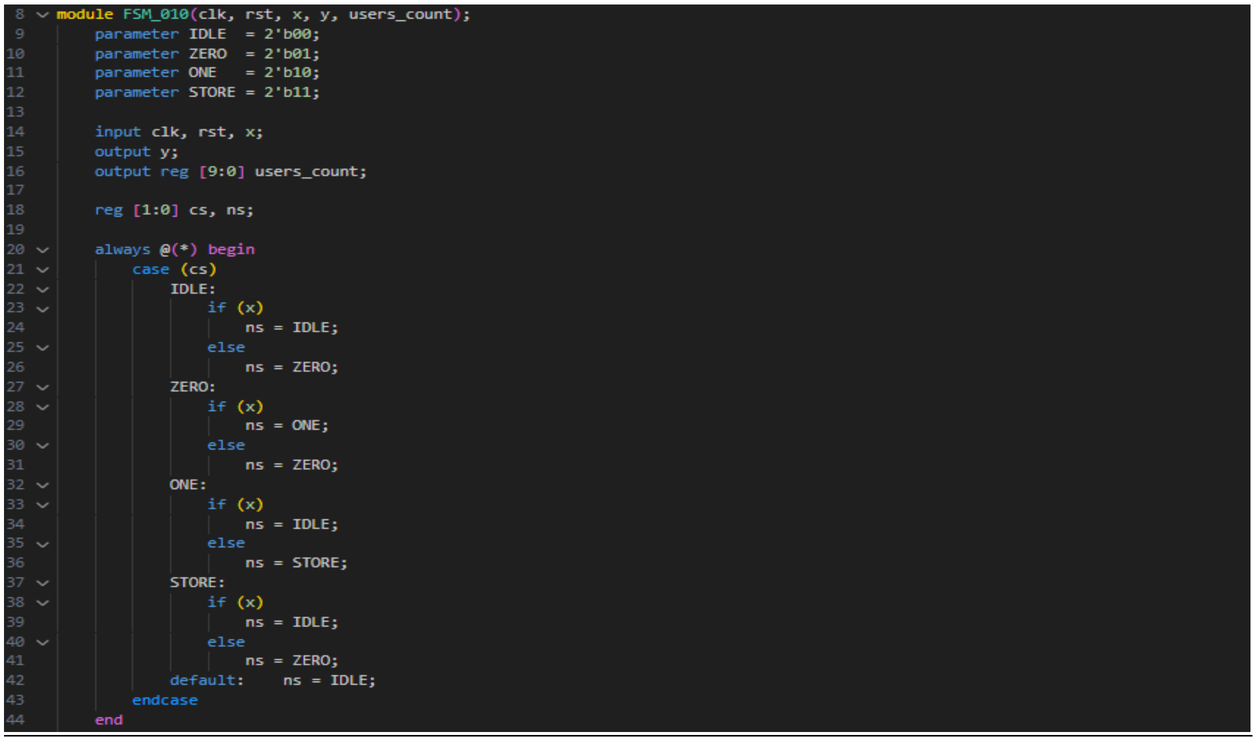
```
CLASS transaction
Covergroup instance \/pack::transaction::Covgrp_B
                                                    100.0%        100    Covered
   covered/total bins:                                   6          6
   missing/total bins:                                   0          6
   % Hit:                                           100.0%        100
   Coverpoint CP_B1                                 100.0%        100    Covered
       covered/total bins:                               3          3
       missing/total bins:                               0          3
       % Hit:                                       100.0%        100
       bin data_0                                        5          1    Covered
       bin data_max                                      4          1    Covered
       bin data_min                                      5          1    Covered
       default bin data_default                          4               Occurred
   Coverpoint CP_B2                                 100.0%        100    Covered
       covered/total bins:                               3          3
       missing/total bins:                               0          3
       % Hit:                                       100.0%        100
       bin data_0max                                     1          1    Covered
       bin data_maxmin                                   1          1    Covered
       bin data_minmax                                   1          1    Covered

TOTAL COVERGROUP COVERAGE: 100.0%  COVERGROUP TYPES: 2
```

Simulation

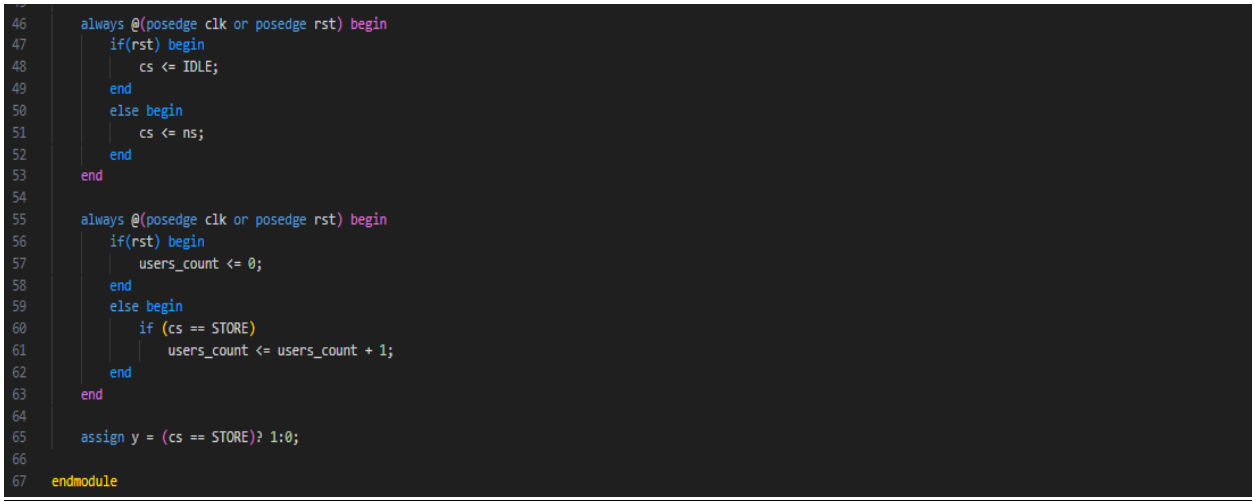


Fsm project

Design

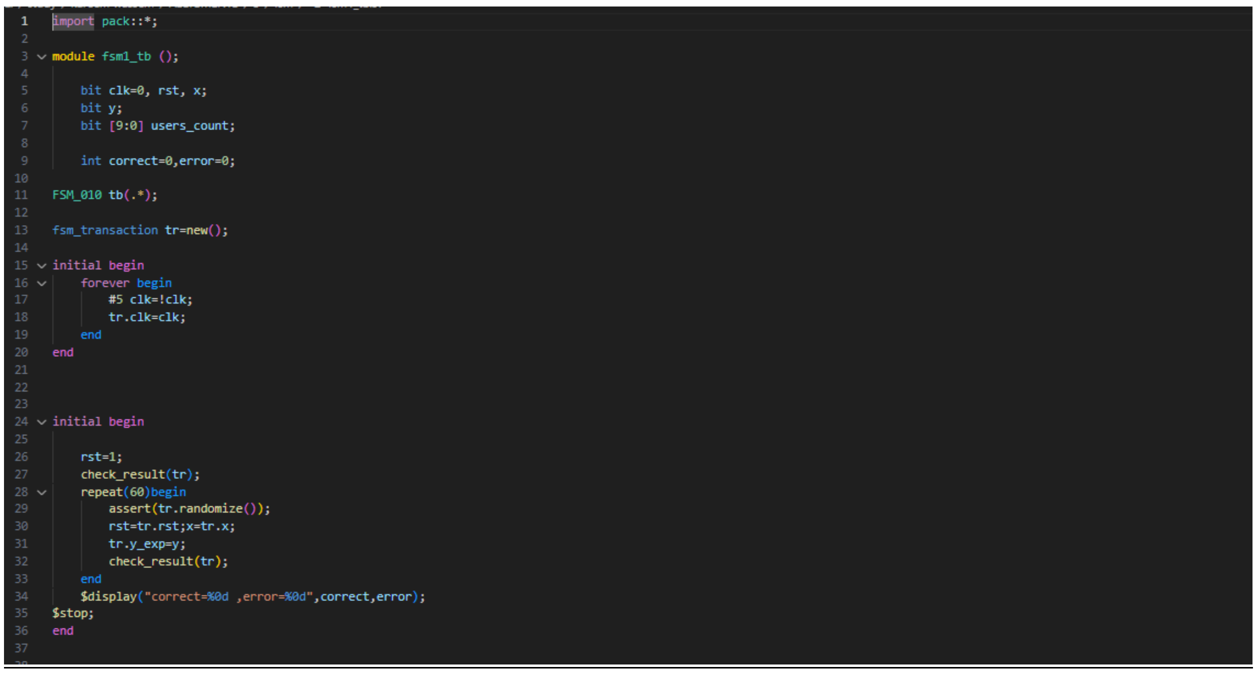


```verilog
module FSM_010(clk, rst, x, y, users_count);
    parameter IDLE  = 2'b00;
    parameter ZERO  = 2'b01;
    parameter ONE   = 2'b10;
    parameter STORE = 2'b11;

    input clk, rst, x;
    output y;
    output reg [9:0] users_count;

    reg [1:0] cs, ns;

    always @(*) begin
        case (cs)
            IDLE:
                if (x)
                    ns = IDLE;
                else
                    ns = ZERO;
            ZERO:
                if (x)
                    ns = ONE;
                else
                    ns = ZERO;
            ONE:
                if (x)
                    ns = IDLE;
                else
                    ns = STORE;
            STORE:
                if (x)
                    ns = IDLE;
                else
                    ns = ZERO;
            default:    ns = IDLE;
        endcase
    end
```

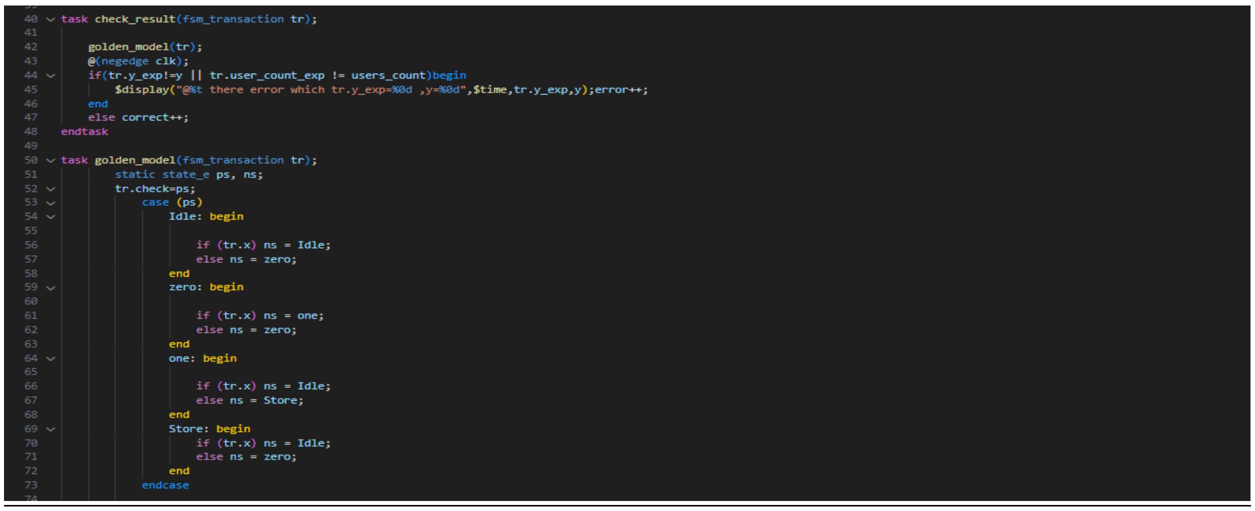


```verilog
    always @(posedge clk or posedge rst) begin
        if(rst) begin
            cs <= IDLE;
        end
        else begin
            cs <= ns;
        end
    end

    always @(posedge clk or posedge rst) begin
        if(rst) begin
            users_count <= 0;
        end
        else begin
            if (cs == STORE)
                users_count <= users_count + 1;
        end
    end

    assign y = (cs == STORE)? 1:0;

endmodule
```

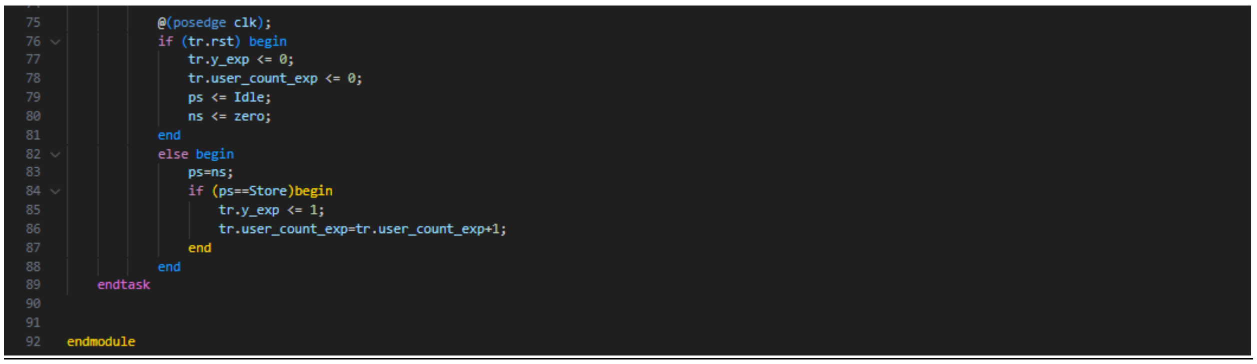
<u>Tb</u>



```
import pack::*;

module fsm1_tb ();

    bit clk=0, rst, x;
    bit y;
    bit [9:0] users_count;

    int correct=0,error=0;

FSM_010 tb(.*);

fsm_transaction tr=new();

initial begin
    forever begin
        #5 clk=!clk;
        tr.clk=clk;
    end
end



initial begin

    rst=1;
    check_result(tr);
    repeat(60)begin
        assert(tr.randomize());
        rst=tr.rst;x=tr.x;
        tr.y_exp=y;
        check_result(tr);
    end
    $display("correct=%0d ,error=%0d",correct,error);
$stop;
end

```

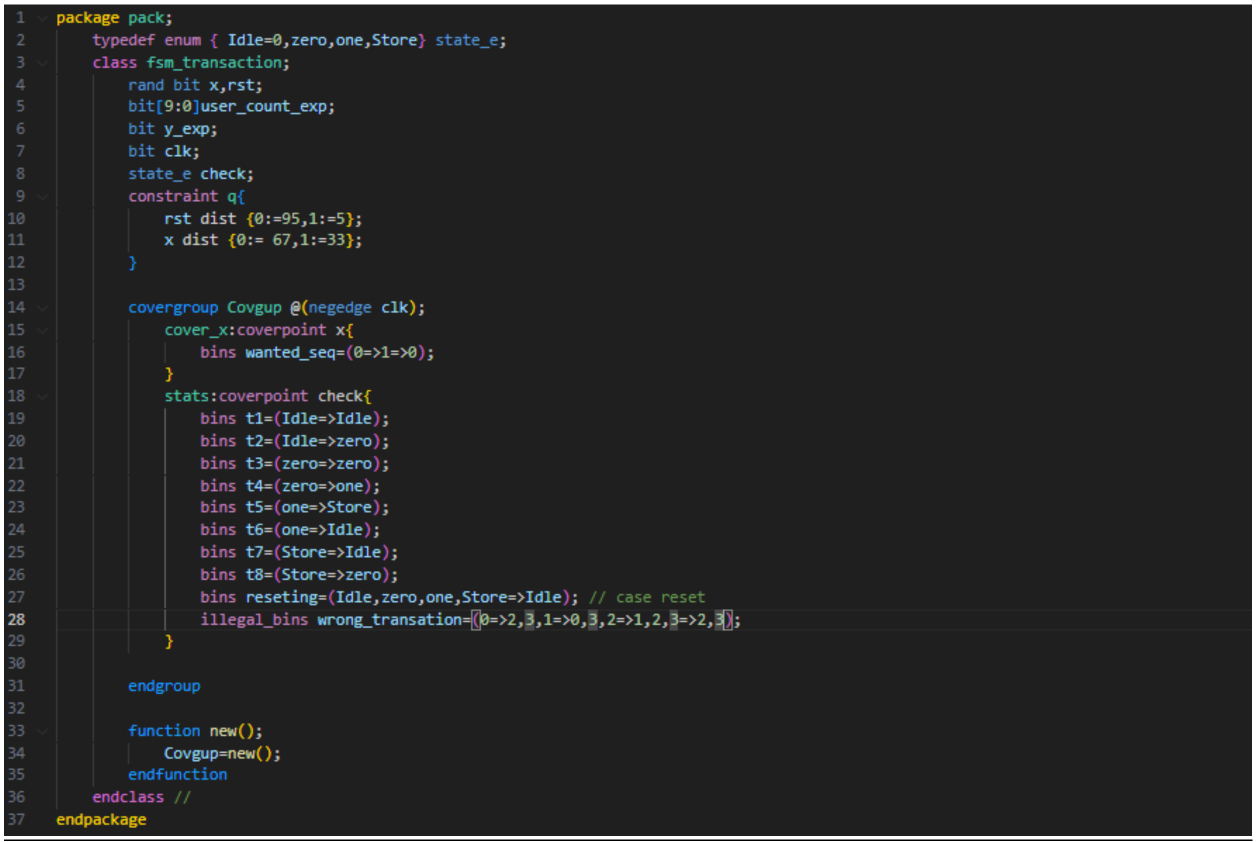


```
task check_result(fsm_transaction tr);

    golden_model(tr);
    @(negedge clk);
    if(tr.y_exp!=y || tr.user_count_exp != users_count)begin
        $display("@%t there error which tr.y_exp=%0d ,y=%0d",$time,tr.y_exp,y);error++;
    end
    else correct++;
endtask

task golden_model(fsm_transaction tr);
        static state_e ps, ns;
        tr.check=ps;
            case (ps)
                Idle: begin

                    if (tr.x) ns = Idle;
                    else ns = zero;
                end
                zero: begin

                    if (tr.x) ns = one;
                    else ns = zero;
                end
                one: begin

                    if (tr.x) ns = Idle;
                    else ns = Store;
                end
                Store: begin
                    if (tr.x) ns = Idle;
                    else ns = zero;
                end
            endcase
```



```
            @(posedge clk);
            if (tr.rst) begin
                tr.y_exp <= 0;
                tr.user_count_exp <= 0;
                ps <= Idle;
                ns <= zero;
            end
            else begin
                ps=ns;
                if (ps==Store)begin
                    tr.y_exp <= 1;
                    tr.user_count_exp=tr.user_count_exp+1;
                end
            end
    endtask


endmodule
```

Package



```
package pack;
    typedef enum { Idle=0,zero,one,Store} state_e;
    class fsm_transaction;
        rand bit x,rst;
        bit[9:0]user_count_exp;
        bit y_exp;
        bit clk;
        state_e check;
        constraint q{
            rst dist {0:=95,1:=5};
            x dist {0:= 67,1:=33};
        }

        covergroup Covgup @(negedge clk);
            cover_x:coverpoint x{
                bins wanted_seq=(0=>1=>0);
            }
            stats:coverpoint check{
                bins t1=(Idle=>Idle);
                bins t2=(Idle=>zero);
                bins t3=(zero=>zero);
                bins t4=(zero=>one);
                bins t5=(one=>Store);
                bins t6=(one=>Idle);
                bins t7=(Store=>Idle);
                bins t8=(Store=>zero);
                bins reseting=(Idle,zero,one,Store=>Idle); // case reset
                illegal_bins wrong_transation=(0=>2,3,1=>0,3,2=>1,2,3=>2,3);
            }

        endgroup

        function new();
            Covgup=new();
        endfunction
    endclass //
endpackage
```

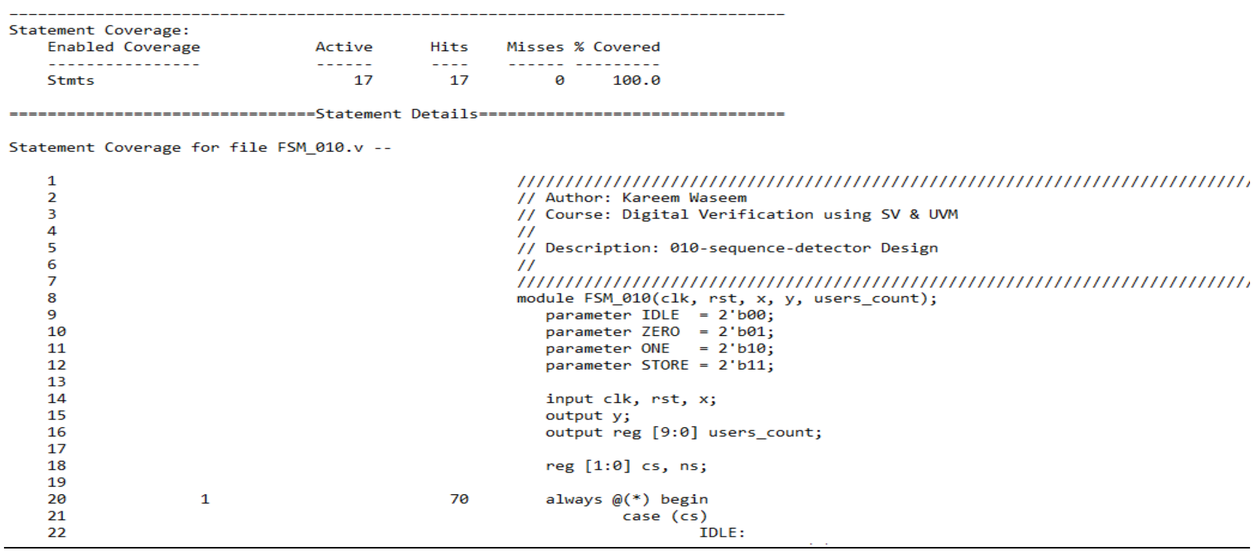
Do file

```
vlib work
vlog FSM_010.v fsm1_tb.sv pack.sv +cover -covercells
vsim -voptargs=+acc work.fsm1_tb -cover
add wave *
coverage save fsm_tb.ucdb -onexit
run -all

coverage exclude -du FSM_010 -togglenode {users_count[3]}
coverage exclude -du FSM_010 -togglenode {users_count[4]}
coverage exclude -du FSM_010 -togglenode {users_count[5]}
coverage exclude -du FSM_010 -togglenode {users_count[6]}
coverage exclude -du FSM_010 -togglenode {users_count[7]}
coverage exclude -du FSM_010 -togglenode {users_count[8]}
coverage exclude -du FSM_010 -togglenode {users_count[9]}

quit -sim


vcover report fsm_tb.ucdb -details -all -output coverage_report.txt
```

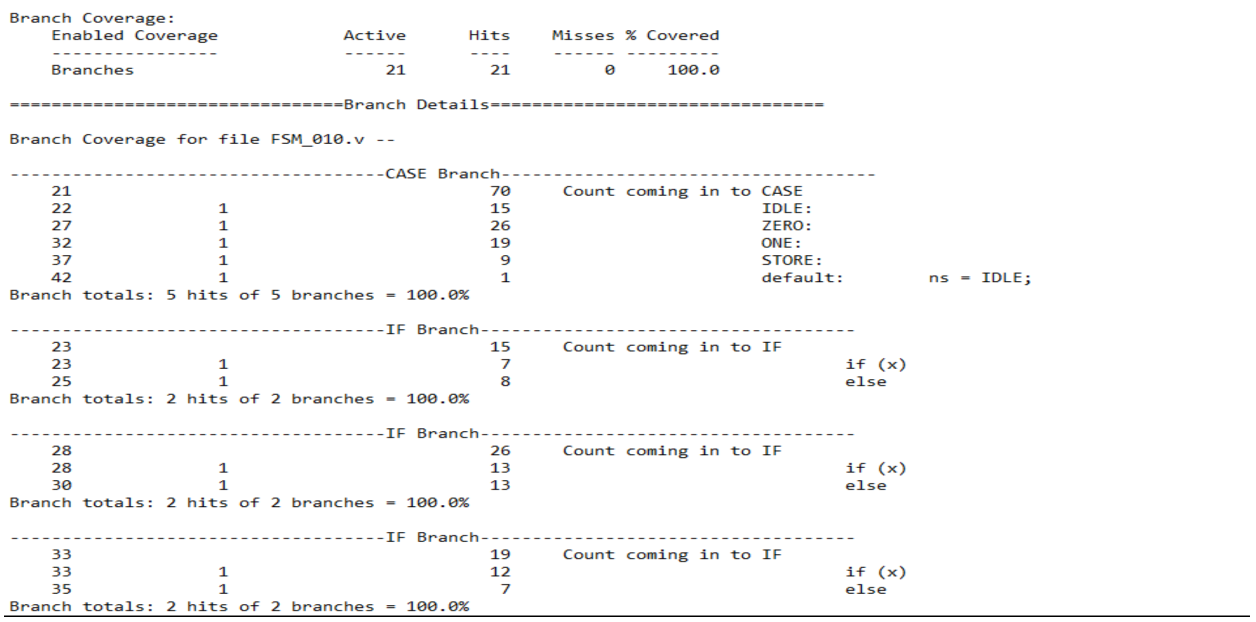
Verification plan

Label	Description	Stimulus Generation	Functionality Check	functionality coverage
FSM_reset	verify the output when rst is high	we directed at start of sinulation then we randomize under constraint that it will be off most of time	we check by send object to check result task and compare with output_expected from golden model task	-
FSM_INPUT	We verify output y and counter when input X generated	randomized under constraint that X is high for 67% of simulation time	we check by send object to check result task and compare with output_expected from golden model task	we cover transation from 0 to 1 to 0 to discover output y and we cover all possible transation in fsm and made unvalid transation in illegal bin

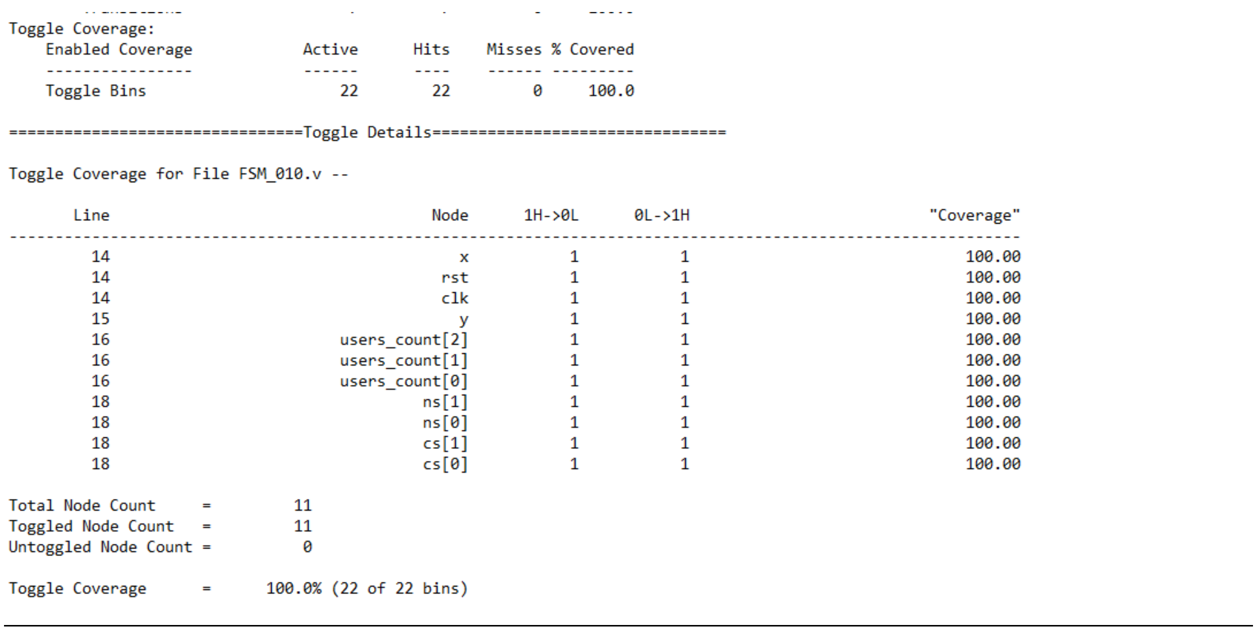
Code coverage



```
---------------------------------------------------------------------------------
Statement Coverage:
    Enabled Coverage            Active      Hits    Misses % Covered
    ----------------            ------      ----    ------ ---------
    Stmts                           17        17         0     100.0

================================Statement Details================================

Statement Coverage for file FSM_010.v --

    1                                                   /////////////////////////////////////////////////////////////////////////////
    2                                                   // Author: Kareem Waseem
    3                                                   // Course: Digital Verification using SV & UVM
    4                                                   //
    5                                                   // Description: 010-sequence-detector Design
    6                                                   //
    7                                                   /////////////////////////////////////////////////////////////////////////////
    8                                                   module FSM_010(clk, rst, x, y, users_count);
    9                                                      parameter IDLE  = 2'b00;
    10                                                     parameter ZERO  = 2'b01;
    11                                                     parameter ONE   = 2'b10;
    12                                                     parameter STORE = 2'b11;
    13
    14                                                     input clk, rst, x;
    15                                                     output y;
    16                                                     output reg [9:0] users_count;
    17
    18                                                     reg [1:0] cs, ns;
    19
    20               1                          70         always @(*) begin
    21                                                             case (cs)
    22                                                                     IDLE:
```

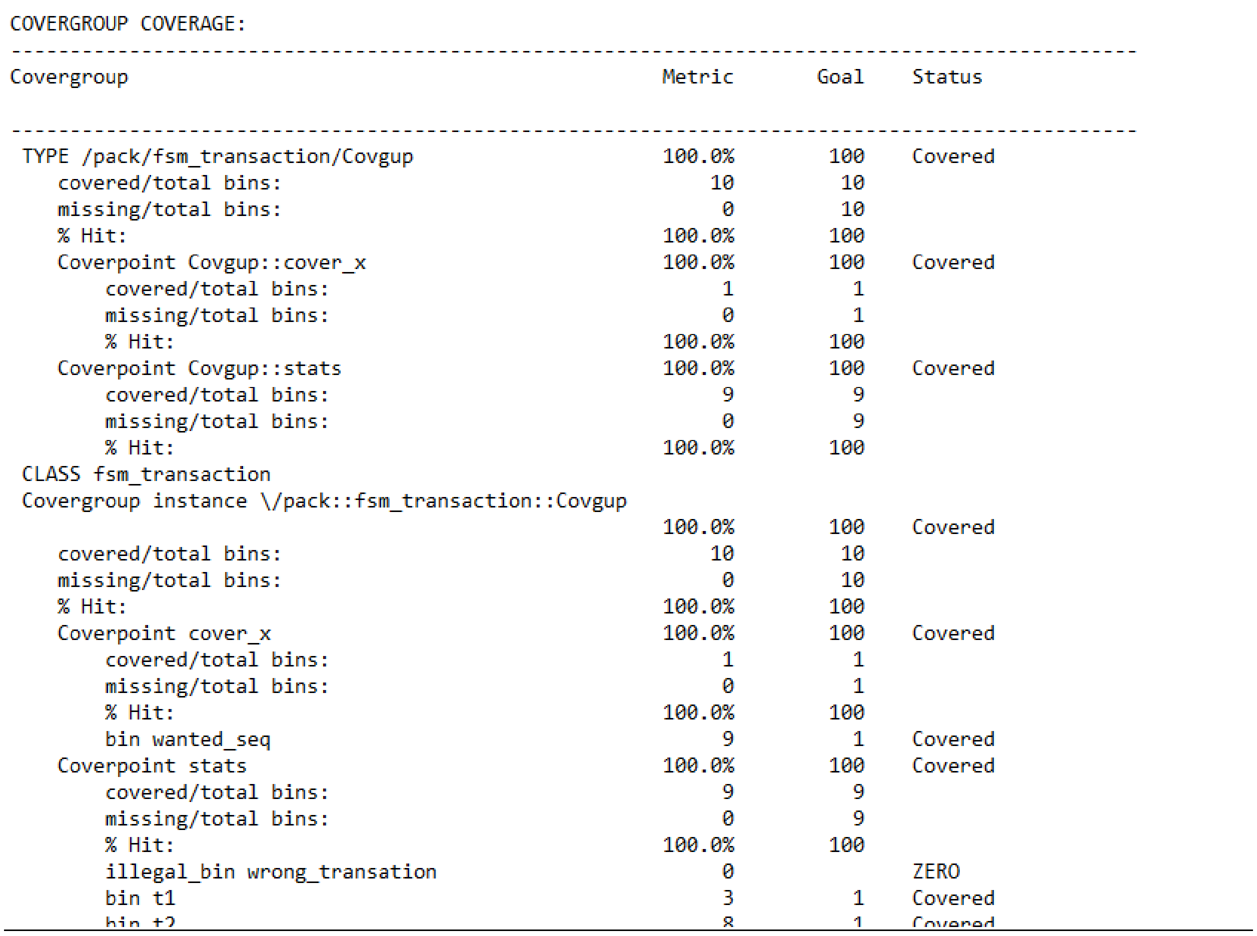


```
Branch Coverage:
    Enabled Coverage            Active      Hits    Misses % Covered
    ----------------            ------      ----    ------ ---------
    Branches                        21        21         0     100.0

================================Branch Details================================

Branch Coverage for file FSM_010.v --

------------------------------------CASE Branch------------------------------------
    21                                        70     Count coming in to CASE
    22              1                         15                        IDLE:
    27              1                         26                        ZERO:
    32              1                         19                        ONE:
    37              1                          9                        STORE:
    42              1                          1                        default:        ns = IDLE;
Branch totals: 5 hits of 5 branches = 100.0%

------------------------------------IF Branch------------------------------------
    23                                        15     Count coming in to IF
    23              1                          7                                if (x)
    25              1                          8                                else
Branch totals: 2 hits of 2 branches = 100.0%

------------------------------------IF Branch------------------------------------
    28                                        26     Count coming in to IF
    28              1                         13                                if (x)
    30              1                         13                                else
Branch totals: 2 hits of 2 branches = 100.0%

------------------------------------IF Branch------------------------------------
    33                                        19     Count coming in to IF
    33              1                         12                                if (x)
    35              1                          7                                else
Branch totals: 2 hits of 2 branches = 100.0%
```



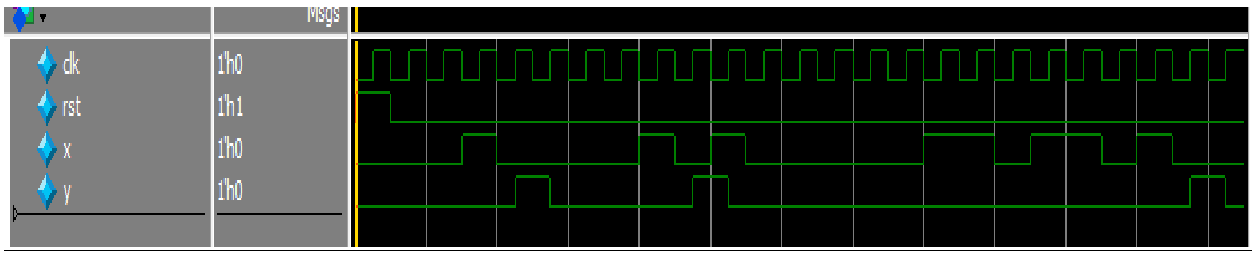
```
Toggle Coverage:
    Enabled Coverage             Active      Hits    Misses % Covered
    ----------------             ------      ----    ------ ---------
    Toggle Bins                      22        22         0     100.0

================================Toggle Details================================

Toggle Coverage for File FSM_010.v --

       Line                                   Node      1H->0L      0L->1H                          "Coverage"
--------------------------------------------------------------------------------------------------------------
         14                                      x           1           1                              100.00
         14                                    rst           1           1                              100.00
         14                                    clk           1           1                              100.00
         15                                      y           1           1                              100.00
         16                         users_count[2]           1           1                              100.00
         16                         users_count[1]           1           1                              100.00
         16                         users_count[0]           1           1                              100.00
         18                                  ns[1]           1           1                              100.00
         18                                  ns[0]           1           1                              100.00
         18                                  cs[1]           1           1                              100.00
         18                                  cs[0]           1           1                              100.00

Total Node Count     =         11
Toggled Node Count   =         11
Untoggled Node Count =          0

Toggle Coverage      =      100.0% (22 of 22 bins)
```

Functional coverage



```
COVERGROUP COVERAGE:
-----------------------------------------------------------------------------------
Covergroup                                            Metric       Goal    Status

-----------------------------------------------------------------------------------
 TYPE /pack/fsm_transaction/Covgup                    100.0%        100    Covered
    covered/total bins:                                   10         10
    missing/total bins:                                    0         10
    % Hit:                                            100.0%        100
    Coverpoint Covgup::cover_x                        100.0%        100    Covered
        covered/total bins:                                1          1
        missing/total bins:                                0          1
        % Hit:                                        100.0%        100
    Coverpoint Covgup::stats                          100.0%        100    Covered
        covered/total bins:                                9          9
        missing/total bins:                                0          9
        % Hit:                                        100.0%        100
 CLASS fsm_transaction
 Covergroup instance \/pack::fsm_transaction::Covgup
                                                      100.0%        100    Covered
    covered/total bins:                                   10         10
    missing/total bins:                                    0         10
    % Hit:                                            100.0%        100
    Coverpoint cover_x                                100.0%        100    Covered
        covered/total bins:                                1          1
        missing/total bins:                                0          1
        % Hit:                                        100.0%        100
        bin wanted_seq                                     9          1    Covered
    Coverpoint stats                                  100.0%        100    Covered
        covered/total bins:                                9          9
        missing/total bins:                                0          9
        % Hit:                                        100.0%        100
        illegal_bin wrong_transation                       0               ZERO
        bin t1                                             3          1    Covered
        bin t2                                             8          1    Covered
    missing/total bins:                                      0         10
    % Hit:                                              100.0%        100
    Coverpoint cover_x                                  100.0%        100     Covered
        covered/total bins:                                  1          1
        missing/total bins:                                  0          1
        % Hit:                                          100.0%        100
        bin wanted_seq                                       9          1     Covered
    Coverpoint stats                                    100.0%        100     Covered
        covered/total bins:                                  9          9
        missing/total bins:                                  0          9
        % Hit:                                          100.0%        100
        illegal_bin wrong_transation                         0                ZERO
        bin t1                                               3          1     Covered
        bin t2                                               8          1     Covered
        bin t3                                              19          1     Covered
        bin t4                                              11          1     Covered
        bin t5                                               7          1     Covered
        bin t6                                               4          1     Covered
        bin t7                                               2          1     Covered
        bin t8                                               5          1     Covered
        bin reseting                                        10          1     Covered

TOTAL COVERGROUP COVERAGE: 100.0%  COVERGROUP TYPES: 1
```

Simulation


Msgs
clk
rst
x
y
1'h0
1'h1
1'h0
1'h0