E.S concepts
Notes

IMT Diploma
IEE Task

Computing system: is a system that consists of three main components which are processor, memory, and I/O peripherals.

What is an Embedded system: An embedded system is a computing system that has a dedicated functions within larger mechanical or electrical system. It is embedded as a part of a complete device often including electrical, electronic and mechanical system.

Computing system components:

1 Processor:

- Processor is the heart of an embedded system.
- It's responsible for performing instructions.

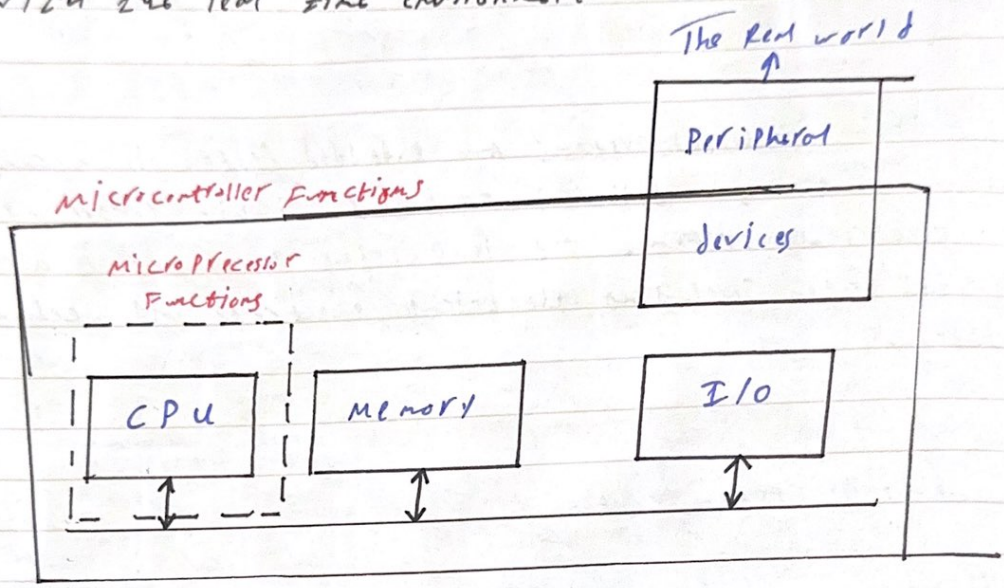
2 Memory:

- The main function is to store program and the useful data until they are needed

- Embedded system programming instructions are stored on a read-only-memory (ROM) or Flash memory chips.

3 Input/output Peripherals:

- The main function of I/O peripherals is interacting with the real time environment



Embedded system Implementation techniques:

- There's two ways to implement an embedded system:-

1 SB (system on board):

- used for development phase because it has the ability to be modified

2 SOC (system on chip):

- It's used in production phase because it can't be modified.

* The First world coulter used 18,000 tubes, covering an area of 170 m^2 weighing 30 tons and consumed 150 Kw.

Processor components: The processor has three main Functions to do

- Processor Fetch: Retrieves an instruction From memory.
- Processor decode: Determines what the instruction is.
- Processor Execute: carry out an instruction.

Instruction set Architecture (ISA):

- Instruction set is a table which has some numbers to recognize the instruction operation, every processor has its own ISA that could be processes and executed by the processor.

- Every instruction set has its own unique binary representation which is called "op code"

-Types:

1- Conplex instruction set Architecture (CISC)
2- Reduced instruction set Architecture (RISC)
3- one Instruction set architecture (OISC)
4- Zero instruction set architecture (ZISC)

RISC:

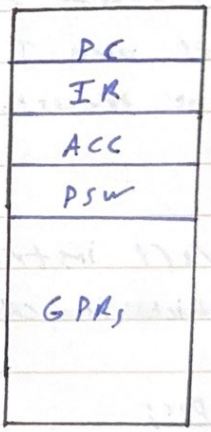
- In this ISA the instruction set has a few instructions and few hardware circuits to handle operations.

CISC:

- In this ISA the instruction set has many instructions and many complex hardware circuits.

Processor register bank:

- Special Purpose registers:-
  - Program counter (PC):
    - This register saves the pointer value pointing to flash addresses.
    - The value of PC is incremented by one automatically after fetching the recent instruction.
  - Instruction register (IR):
    - This register is used to stored the fetched instruction before decoding.
  - Accumulator register (ACC):
    - This register stores the output of the last operation executed in the ALU.
  - Process status word (PSW):
    - This register has some flags which express some information about the last operation occured.



- General purpose registers (GPRs):
  - These registers are used for wide purposes, such as storing high-speed accessing variable that is defined by "register" key word by the user.

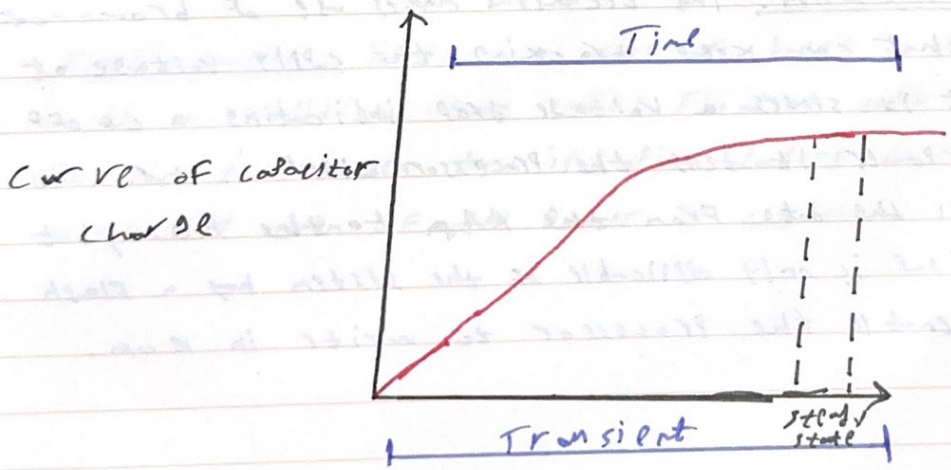
memory

Types:

- Volatile memory :- The volatile type of memory which loses its data when the applied voltage is removed like (RAM).

-Dynamic memory (DRAM):

- This type of RAM is made of capacitors
- The main disadvantage of this type that the capacitors take a long time to be fully charged and refreshing circuit is necessary need to keep data away from losing.



-Static RAM (SRAM):

- This ~~mode~~ type of RAM is made of transistors.
- The main disadvantage of this type is that transistors have high cost, but main advantage is that they are very fast because there's no need to recharge.
- Non-volatile memory: The non-volatile memory is a type of memory which keeps the data even if the applied voltage is removed.

- Non-Volatile RAM (NVRAM):-

  - Hardware NVRAM: This technique depends on an external power source to enable RAM to keep its data when the external power source is cut off, simply by connecting the RAM to a battery.
  - Software NVRAM: This technique makes use of brown-out detector that can keep tracking the supply voltage at the moment it senses a voltage drop indicating a cut off of system power it tells the processor which in turn will transfer all the data from the RAM to the ROM, but this technique is only applicable of the system has a Flash driver to enable the processor to write in ROM.

- Read only memory (ROM):

  - MaskedROM: it's the first memory has been manufactured, this memory is programmed by the Factor only, and of course it's the cheaper type.

  - one Time Programmable ROM (OTP ROM): This type can be Programmed by the user, but only for one time.

  - Erasable programmable ROM (EPROM): This type can be Programed several times, but its data is erased by ultra-violet rays (UV).

    * what happened to some missiles that Egypt imported during the wars of 6th october may they live always as heroes in the heaven.

  - Electrically Erasable Programmable Rom (EEPROM): This type can be programmed several times and its data can be erased by electric signals.

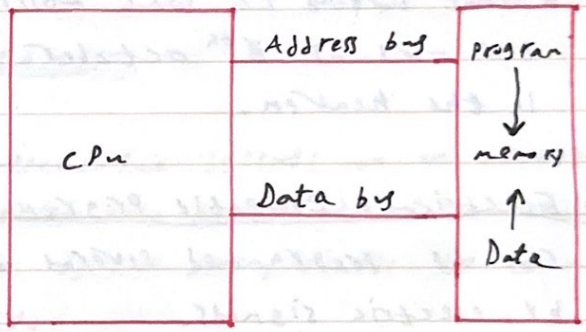
- Flash memories: Flash memories are based on MOSFET transistors with an additional gate called Floating gate. This gate is positioned between two isulation layers that enable it to store electrons even if the power is cut-off.

Memory cycle

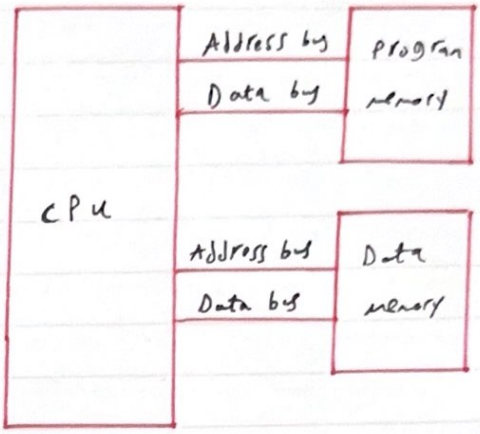
- At first processor sends a control dictator (what) sorry a control signal (0 → write, 1 → read) on the control bus, then it sends the address - stored in PC register of the instruction to be fetched on the address bus, then the data at this address will be transfered to IR via the data bus then passed to ID (Instruction decoder) to translate the fetched data.

Architecture

- Von-neumann architecture:
  It's an architecture that uses common buses for all memory system, meaning that there is one control bus, data bus and address bus for RAM, ROM and I/O memory, so any cycle starts the system will wait for it be finished before starting another one.



- Harvard architecture:-



Harvard system or architecture uses separate buses for all the memory system meaning that there is control bus, Data bus, and address bus for RAM and another control bus, address bus, and Data bus for ROM and another copy of the three buses, but for the I/O memory, so if any cycle starts the system can start another without waiting for the first one to finish.

Pipe Lining

- In computer science instruction pipe lining is a technique for Implementing Instruction level parallelism with a single processor.

Pipelining attempts to keep every part of the processor busy with some instruction by dividing incoming instructions into a series of sequential steps like a pipe.

Fetch → Decode → Execute

↓

Fetch → Decode → Execute