Faculty of Computers and Artificial Intelligence

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OOP

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Assignment 1 Task 4,5

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Vole Machine Simulator

This document provides a detailed design and testing report for the Vole Machine Simulator project, The simulator interprets and executes instructions on a virtual machine with simulated registers and

memory.

Design Section

Class Overview

The main class in this project is VoleMachine, which handles all operations for simulating the Vole machine. The main

attributes include:

- registers: array of 16-bit registers R0 to R15
- memory: 16x16 matrix simulating memory
- programCounter: points to the current instruction
- instructionRegister: holds the current instruction being executed

Attributes and Methods

Attributes:

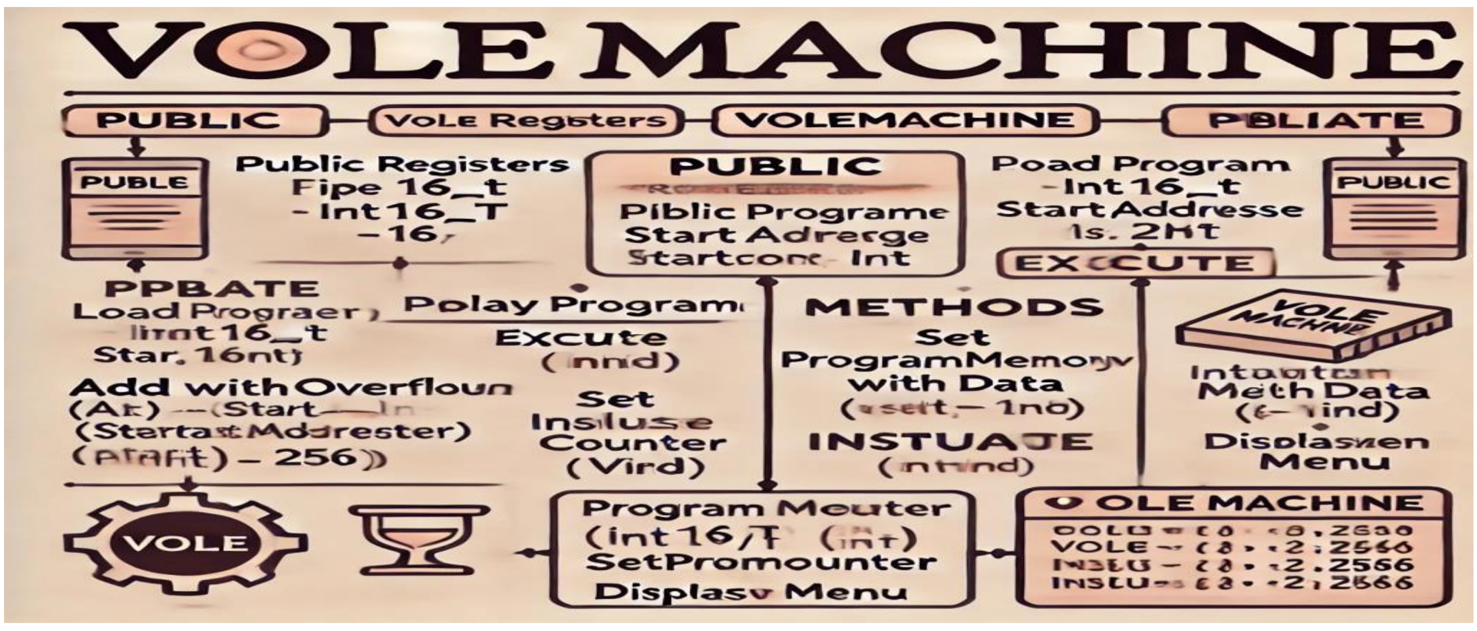
- registers: Array<int16_t, 16> - Represents 16 registers.
- memory: Array<int16_t, 256> - Simulates 256 memory cells.
- programCounter: int - Tracks the current instruction location.

Methods:

- loadProgram(filename, address): Loads a file into memory starting from a given address.
- execute(): Executes instructions one by one based on programCounter.
- displayStatus(): Shows registers, memory, and program counter status.

UML Overview

A simplified UML diagram representing the VoleMachine class and its primary interactions is included in this design. The class contains attributes for memory, registers, and program control, as well as methods for loading and executing instructions.



Opcode Logic

Each opcode is mapped to a specific operation. For instance, LOAD (opcode 1) transfers a memory value to a register, while STORE (opcode 3) places register data into memory. Other opcodes support arithmetic, logical, and control flow instructions. This logic enables effective simulation of program flow and arithmetic operations.

Testing Section

Test Plan

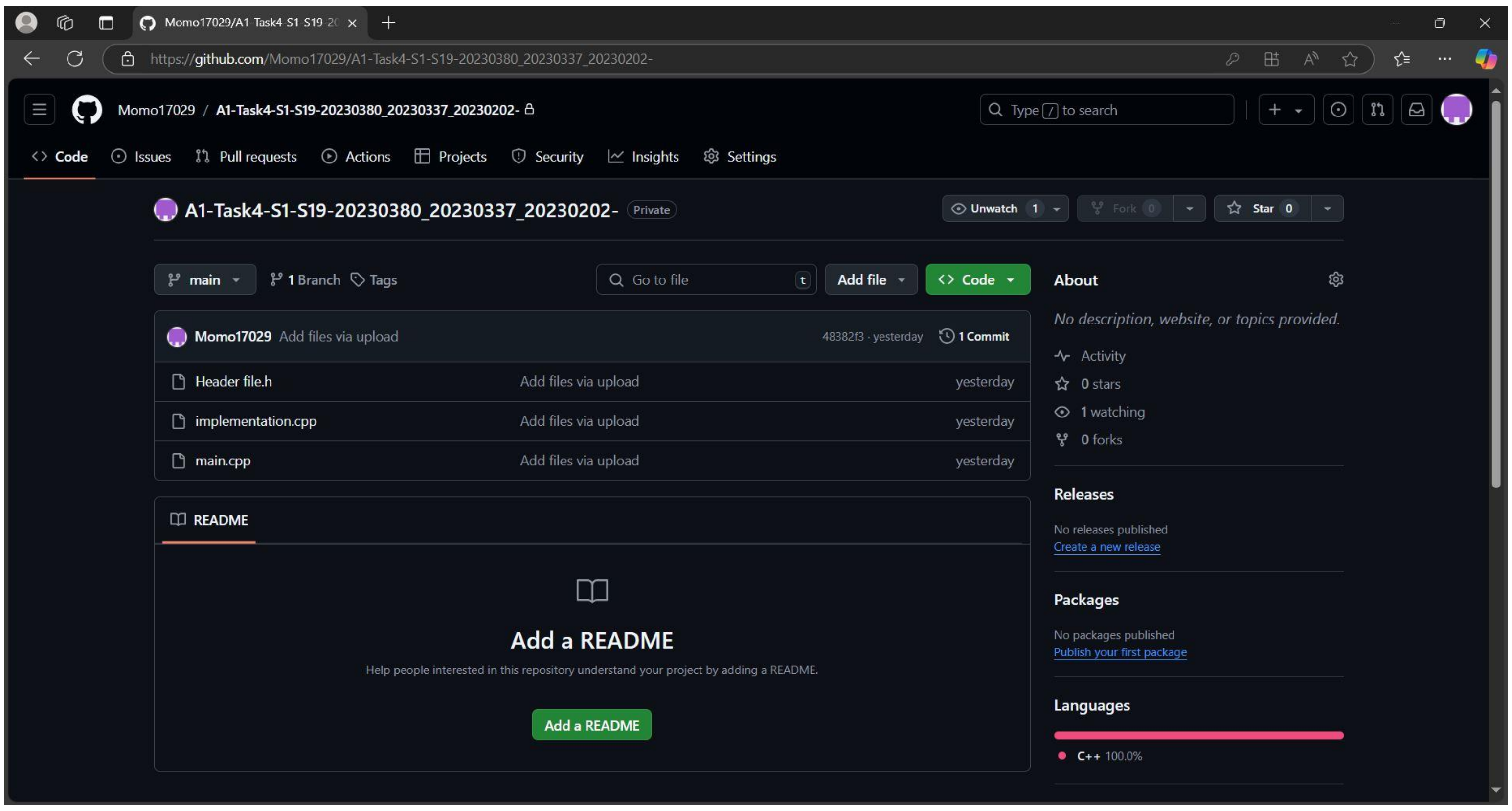
The testing plan includes loading, executing, and verifying memory, register, and program counter statuses. Specific cases are tested for each opcode to ensure accurate results.

Sample Test Cases

- Test Load Program: Verifies program loading into memory from a file.

- Test Execution: Confirms correct operation of each opcode.

- Test Invalid Opcode Handling: Tests that invalid instructions halt execution appropriately.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