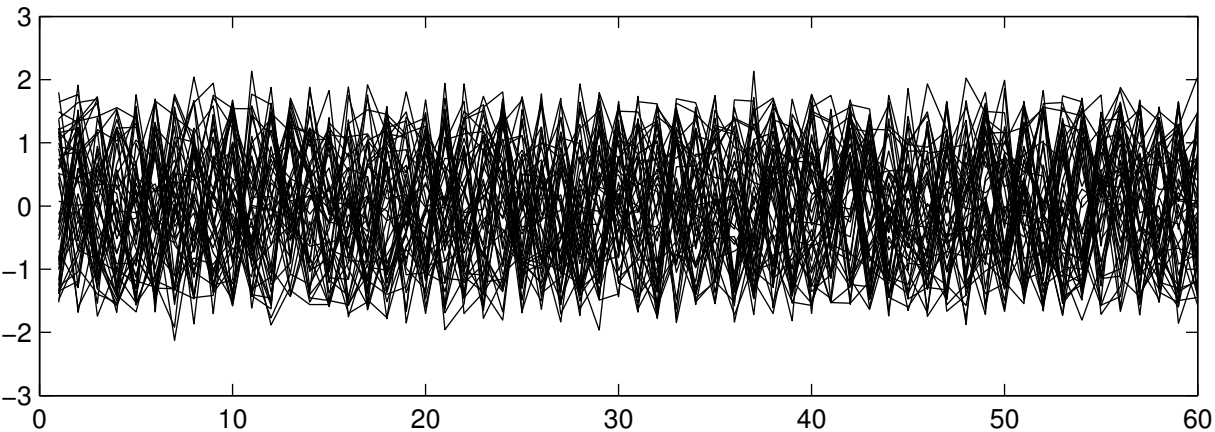


TRN synthetic_control class: 1 count: 50



TST synthetic_control class: 1 count: 50

