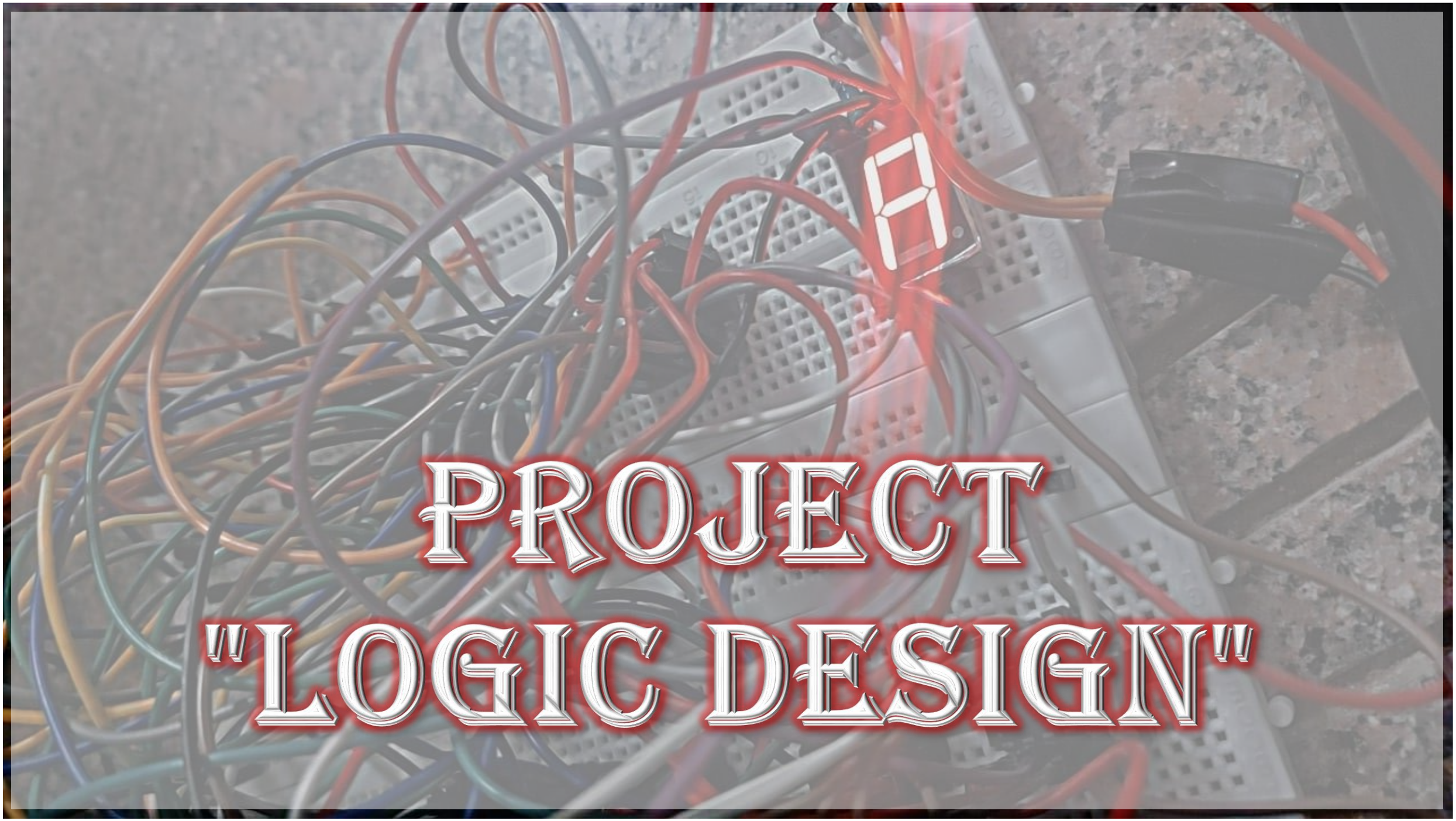
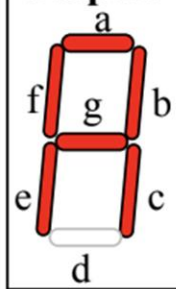
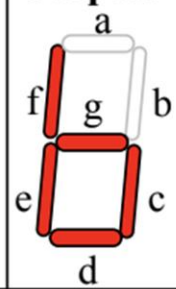
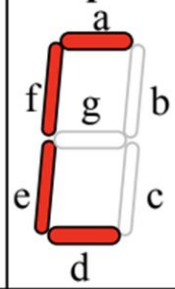
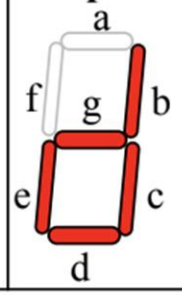
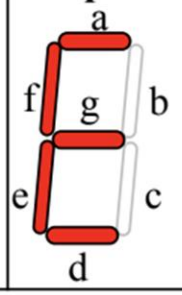
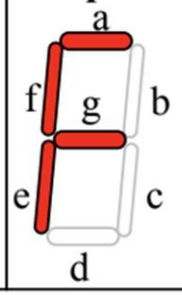
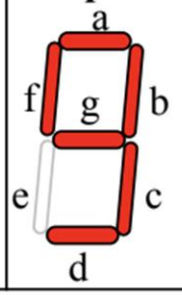
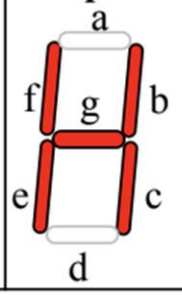
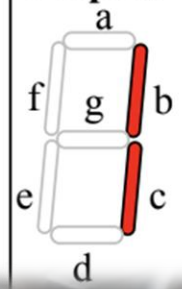
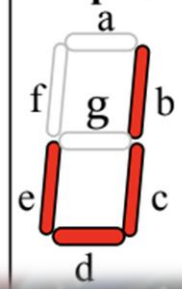

PROJECT
"LOGIC DESIGN"

Project 4: A to J with 7-Segments (common **Cathode**) using (AND-OR-NOT) only

You should do the following:

1- Write the Truth Table and use don't care inputs from 10 to 15
2- Simplify the output functions using K-Map and write the equations
3- Design the circuit and draw the logic diagram
4- Implement your Project virtual on **TINKERCAD.COM or Electronic Workbench**
5- Implement your Project on real board

Input: 0000 **Output:** 	**Input: 0001** **Output:** 	**Input: 0010** **Output:** 	**Input: 0011** **Output:** 	**Input: 0100** **Output:** 	**Input: 0101** **Output:** 	**Input: 0110** **Output:** 	**Input: 0111** **Output:** 
Input: 1000 **Output:** 	**Input: 1001** **Output:** 						

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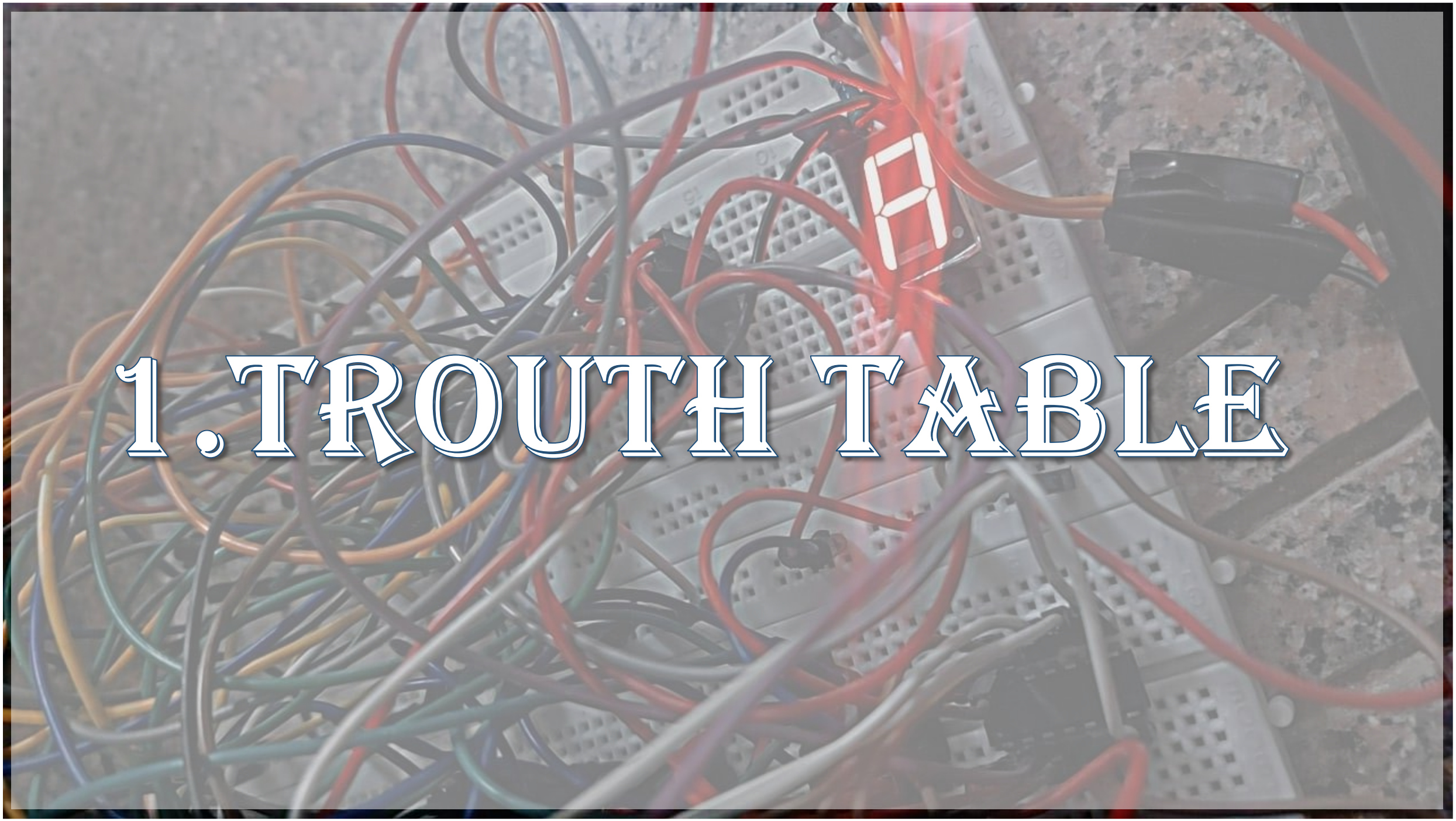
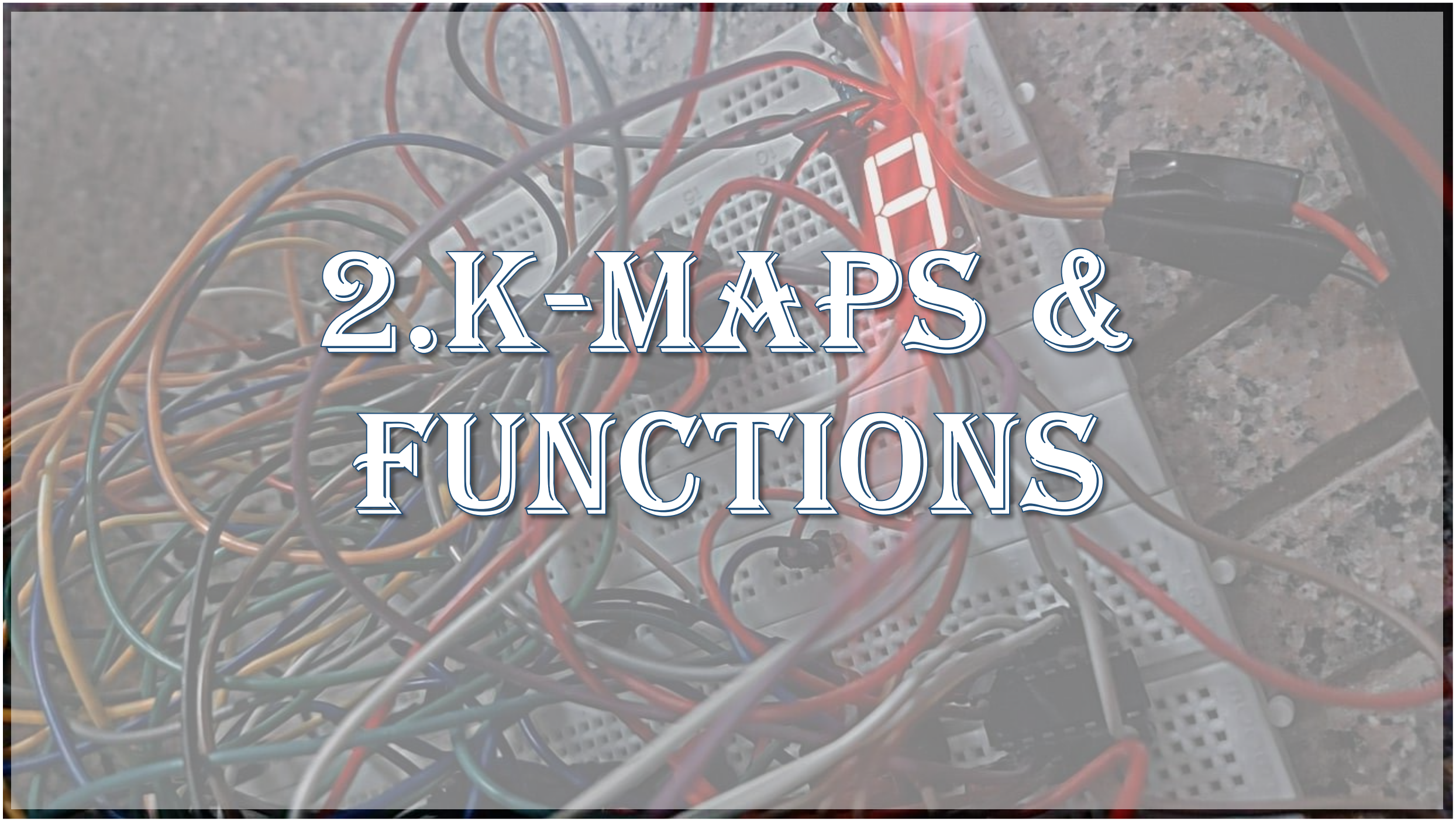
- Esraa walid
- Haneen Mahmoud Sayed


1.TROUTH TABLE

	W	X	Y	Z	A	B	C	D	E	F	G
A	0	0	0	0	1	1	1	0	1	1	1
B	0	0	0	1	0	0	1	1	1	1	1
C	0	0	1	0	1	0	0	1	1	1	0
D	0	0	1	1	0	1	1	1	1	0	1
E	0	1	0	0	1	0	0	1	1	1	1
F	0	1	0	1	1	0	0	0	1	1	1
G	0	1	1	0	1	1	1	1	0	1	1
H	0	1	1	1	0	1	1	0	1	1	1
I	1	0	0	0	0	1	1	0	0	0	0
J	1	0	0	1	0	1	1	1	1	0	0
	1	0	1	0	X	X	X	X	X	X	X
	1	0	1	1	X	X	X	X	X	X	X
	1	1	0	0	X	X	X	X	X	X	X
	1	1	0	1	X	X	X	X	X	X	X
	1	1	1	0	X	X	X	X	X	X	X
	1	1	1	1	X	X	X	X	X	X	X


2.K-MAPS &
FUNCTIONS

1.FOR 'A' FUN. :

	y'		y		
W'	1	0	0	1	X'
	1	1	0	1	x
w	x	x	x	X	
	0	0	x	x	X'
	Z'	z		Z'	

$$a = xy' + w'z'$$

1.FOR ‘B’ FUN. :

	y’		y		
W’	1	0	1	0	X’
	0	0	1	1	x
w	x	x	x	X	
	1	1	x	x	X’
	Z’	z		Z’	

$$b = x'y'z' + yz + xy + w$$

$$b = x'y'z' + y(z + x) + w$$

1.FOR 'C' FUN. :

	y'		y		
W'	1	1	1	0	X'
	0	0	1	1	x
w	x	x	x	X	
	1	1	x	x	X'
	Z'	z		Z'	

$$C = xy + yz + x'y'$$

$$C = y(x+z) + x'y'$$

1.FOR 'D' FUN. :

	y'		y		
W'	0	1	1	1	X'
	1	0	0	1	x
w	X	x	x	X	
	0	1	x	x	X'
	Z'	z		Z'	

$$d = yz' + x'z + xz'$$

1.FOR 'E' FUN. :

	y'		y		
W'	1	1	1	1	X'
	1	1	1	0	x
w	x	x	x	X	
	0	1	x	x	X'
	Z'	z		Z'	

$$e = z + w'x' + w'y'$$

$$e = z + w'(x' + y')$$

1.FOR 'F' FUN. :

	y'		y		
W'	1	1	0	1	X'
	1	1	1	1	x
w	X	x	x	X	
	0	0	x	x	X'
	Z'	z		Z'	

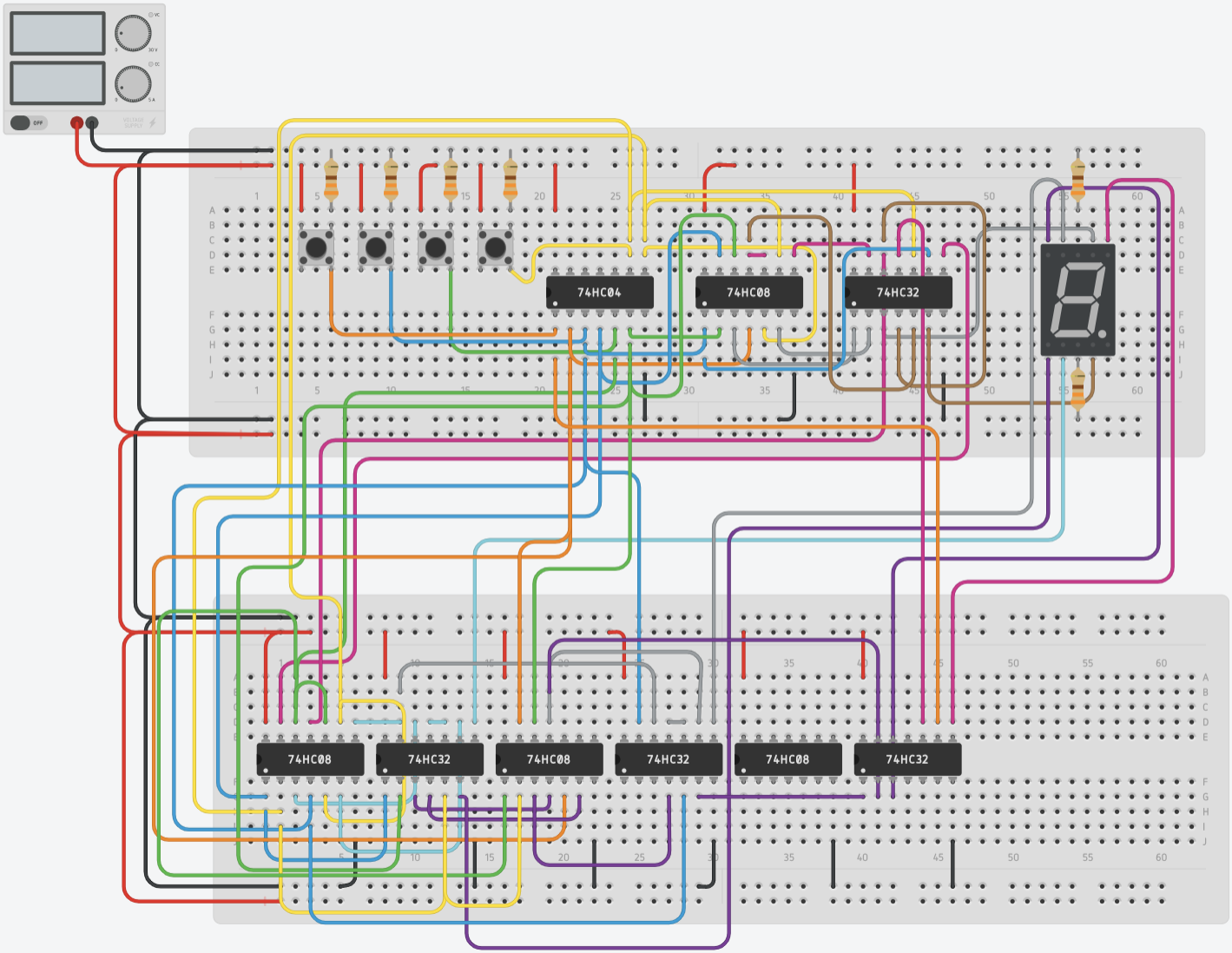
$$f = x + yz' + w'y'$$

1.FOR ‘G’ FUN. :

	y’		y		
W’	1	1	1	0	X’
	1	1	1	1	x
w	X	x	x	X	
	0	0	x	x	X’
	Z’	z		Z’	

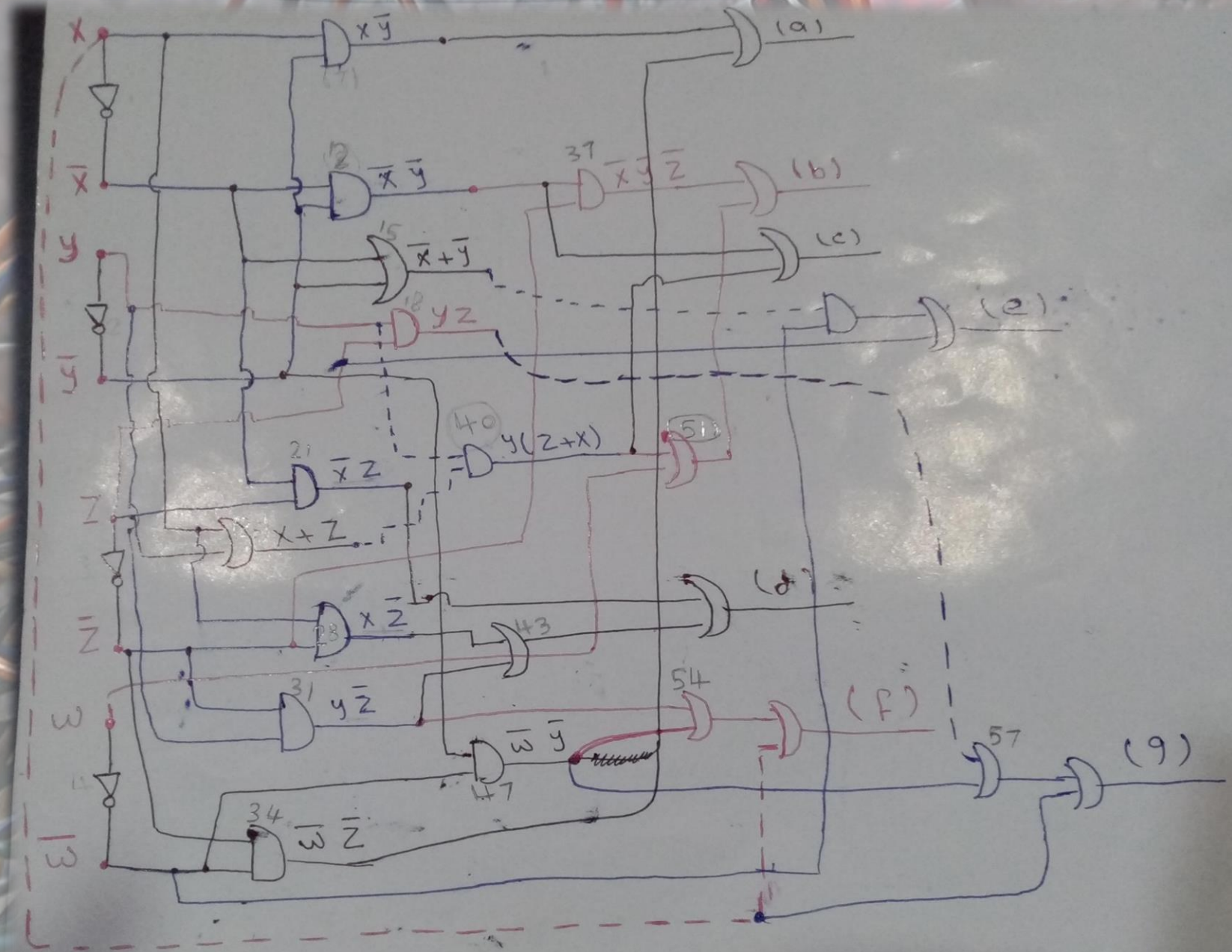
$$g = x+yz+w'y'$$

3.DESIGN OF THE CIRCUIT



https://www.tinkercad.com/things/8kvkgPYrrEN-copy-of-project-logic-the-final-copy-/editel?sharecode=zwXd_pUMFxwfGcbiy3NkKGBqFpwfjk62cFesOA1iEac

4.LOGIC DIGRAM


x
x̄
y
ȳ
z
z̄
ω
ω̄
xȳ
x̄ ȳ
x̄+ȳ
yz
ȳ z̄
x̄ z
x+z
x z̄
y z̄
ω̄ ȳ
ω̄ z̄
y(z+x)
(a)
(b)
(c)
(d)
(e)
(f)
(g)
37
15
18
40
51
21
28
43
31
54
47
34
57

5.ON A REEL BORD