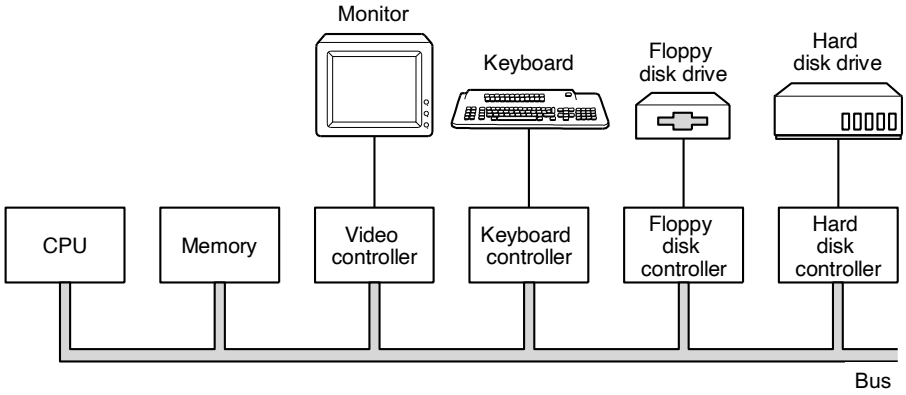
Computer Architecture basics
Period and Frequency
History review

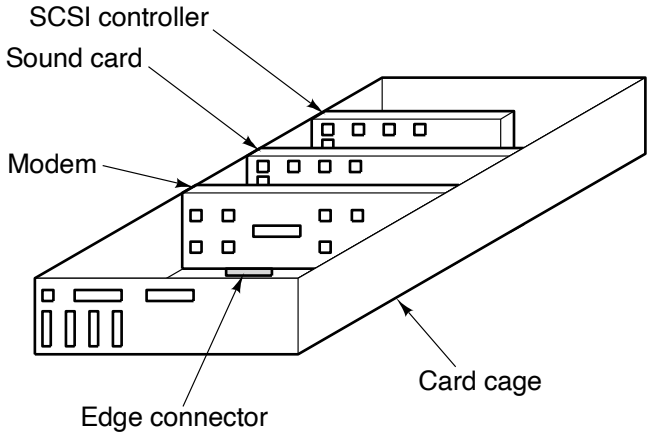
1

Classical architecture of microcomputers



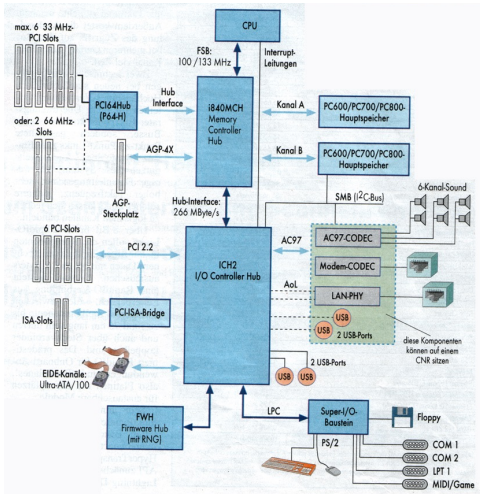
2

Classical idea of a modular computer system



3

A complete classical single processor system



4

A complete classical single processor system

- The usual chipset is divided into the north and south bridges.
- However, a physical separation into two building blocks is not absolutely necessary.
- The north bridge (host) regulates the data flows between the processor, cache and main memory.
- In **modern systems**, the AGP is also connected there.
- The PCI-to-ISA bridge is connected to the host bridge.
- In between is the PCI bus with 3 to 5 slots.
- The South Bridge takes care of the interfaces that are connected to the chipset and are available in the computer system.
- This includes EIDE and USB, as well as the serial and parallel interfaces.
- Depending on the version, the keyboard controller and the real-time clock are integrated.

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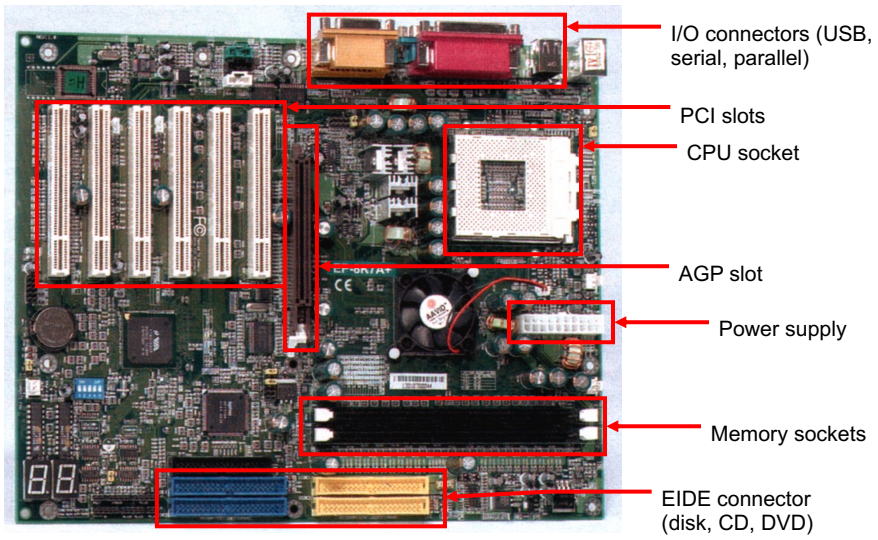

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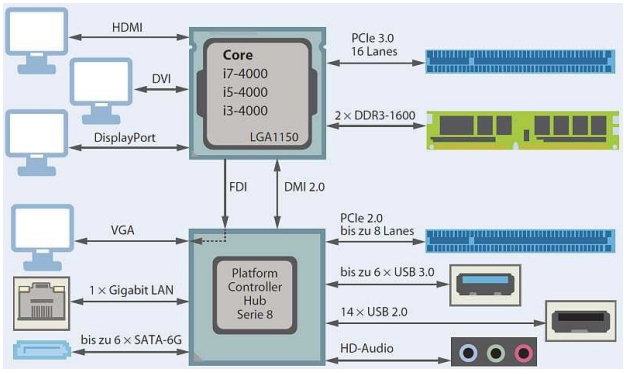
PC Architectures continued



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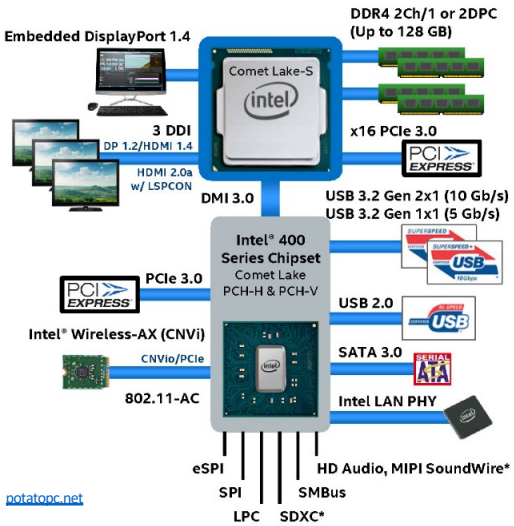
PC Architectures continued



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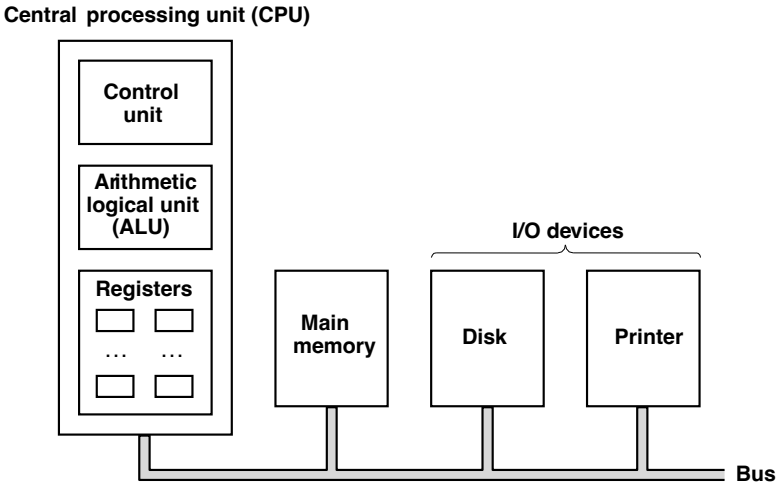
Back to a simple single processor system



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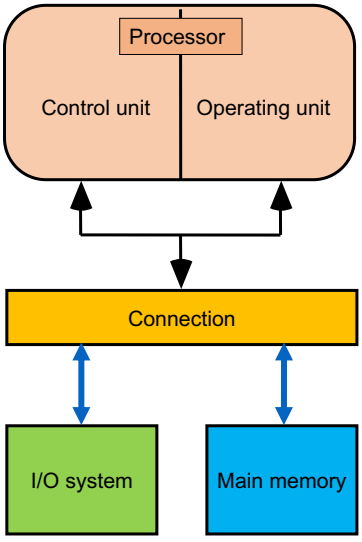
The von Neumann Architecture

- The von Neumann architecture forms the basis of many hardware architectures presented in this course.
- The architecture comprises the following main components
  - Central processing unit
    - Control unit
    - ALU / Operating unit
  - Memory
  - Input/Output units
  - Interconnection



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The von Neumann architecture

- **Central control** of the computer
- A computer consists of **several functional units** (central processing unit, memory, input/output unit, connection)
- The computer is **not tailored to a single problem** but a general-purpose machine. In order to solve a problem a program is stored in the memory ("program controlled universal computer") – yes, today this sounds so simple…

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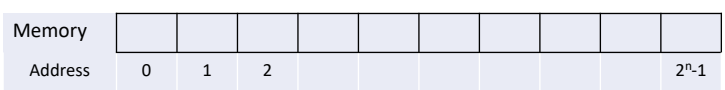
IMPORTANT

- Instructions (the program) and data (input and output values) are stored in the same memory.
- The memory consists of memory cells with a fixed length, each cell can be addressed individually.



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The von Neumann architecture

- **Processor, central unit** (CPU: "central processing unit")
  - Controls the flow and execution of all instructions
- **Control unit**
  - Interprets the CPU instructions
  - Generates all control commands for other components
- **Arithmetic Logical Unit (ALU)**
  - Executes all instructions (I/O and memory instructions with the help of these units)
- **Input/Output system**
  - Interface to the outside world
  - Input and output of program and data
- **Memory**
  - Storage of data and program as sequence of bits
- **Interconnection**

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Principle of Operation of a Computer

- At any time, the CPU executes only a **single instruction**.
- This instruction can only manipulate a **single operand**.
  - Traditionally, this is called **SISD** (Single Instruction Single Data).
- **Code and data** are stored in the **same memory** without any distinction. There are no memory protection mechanisms – programs can destroy each other; programs can access arbitrary data.
- **Memory is unstructured** and is addressed linearly. Interpretation of memory content depends on the context of the current program only.

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Principle of Operation of a Computer

- **Two phase principle** of instruction processing:
  - During the interpretation phase the content of a memory cell is fetched based on a **program counter**. This content is then interpreted as an instruction (note: this is a pure interpretation!).
  - During the execution phase the content of a memory cell is fetched based on the address contained in the instruction. This content is then interpreted as data.
- The instruction flow follows a strict sequential order.

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The von Neumann architecture

- Advantages
  - Principle of minimal hardware requirements
  - Principle of minimal memory requirements
- Disadvantages
  - The main interconnection (memory ↔ CPU) is the central bottleneck: the "**von Neumann bottleneck**"
  - Programs must consider the sequential data flow across the von Neumann bottleneck
    → Influences on higher programming languages ("intellectual bottleneck")
  - Low structuring of data (a long sequence of bits…)
  - The instruction determines the **operand type**
  - No memory protection

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Harvard Architecture

- Classical definition of the Harvard architecture
  - Separation of data and program memory
- Most processors with microarchitecture
  - von Neumann from the outside
  - Harvard from the inside
- Reason
  - Different time scales and locality when caching data and instructions

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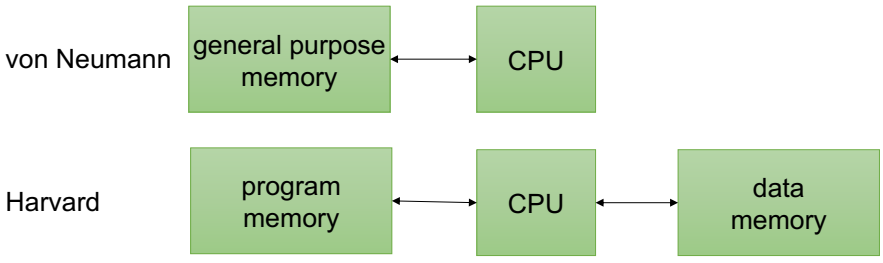
Comparision



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VON NEUMANN ARCHITECTURE	HARVARD ARCHITECTURE
It is ancient computer architecture based on stored program computer concept.	It is modern computer architecture based on Harvard Mark I relay based model.
Same physical memory address is used for instructions and data.	Separate physical memory address is used for instructions and data.
There is common bus for data and instruction transfer.	Separate buses are used for transferring data and instruction.
Two clock cycles are required to execute single instruction.	An instruction is executed in a single cycle.
It is cheaper in cost.	It is costly than Von Neumann Architecture.
CPU can not access instructions and read/write at the same time.	CPU can access instructions and read/write at the same time.
It is used in personal computers and small computers.	It is used in micro controllers (most of them).

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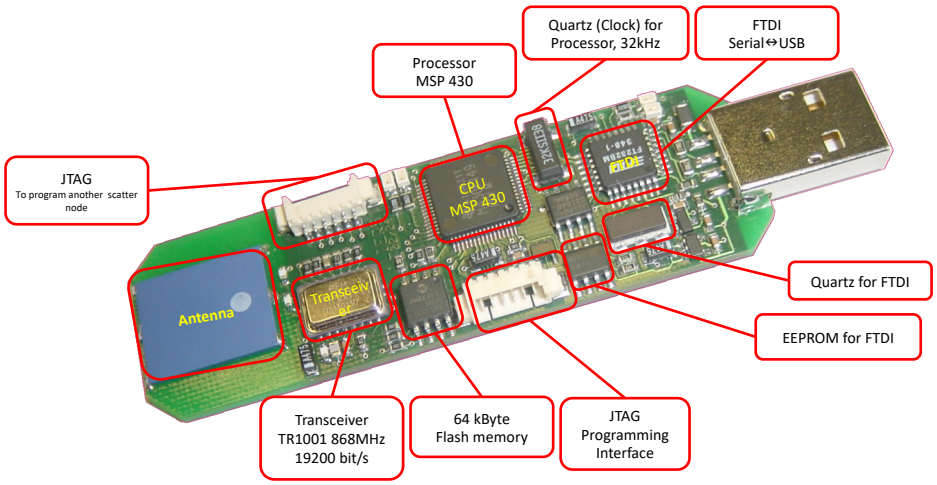
Micro processors



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Definition of a Micro computer system

- Micro processor system:
  - Digital system, using a micro processor as central control and/or arithmetic unit
- Micro computer:
  - includes a micro processor that communicates with memory, controllers and interfaces for external devices using the system bus.
- Special cases of microcomputers:
  - Single-chip microcomputer
    - All components of the microcomputer are located on one chip.
  - Single-circuit microcomputer (dt. Ein-Platinen-Mikrocomputer)
    - All components of the microcomputer are on one circuit board.
- Microcomputer system:
  - Microcomputer with connected **external devices**
  - Can be small – think of the Internet of Things!

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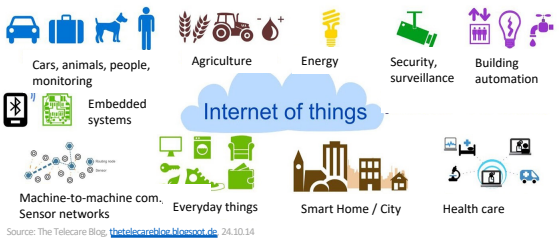
Internet of Things



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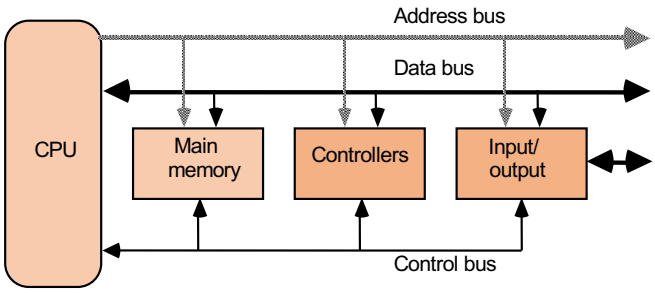
Basic concept of a micro computer

- The IBM PC is a modified von Neumann architecture and was introduced by IBM fall 1981.
- The interconnection structure was realized by a **bus**.
  - The bus connects the CPU with the main memory, several controllers and the input/output system.



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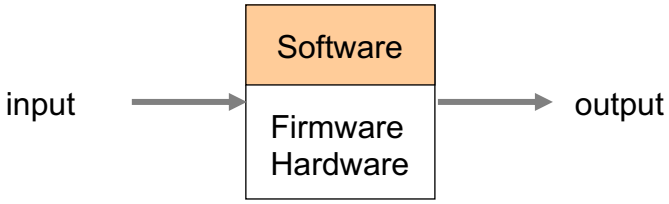
Components of a Computer

- **Hardware**: all mechanical and electronic components
- **Software**: all programms running on the computer
- **Firmware**: micro-programs stored in ROM, somewhere in-between SW and HW



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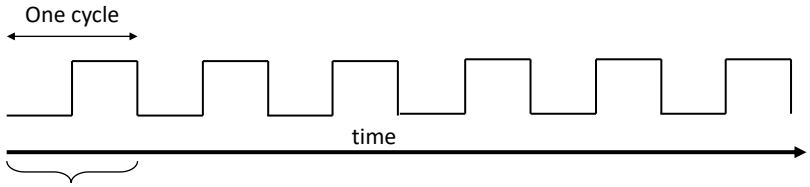
Physical review



Period: Time for one cycle
Unit: Seconds (s)
Symbol: T

Frequency: Number of cycles in one second
Unit: Cycles per second (Hz)
Symbol: F

$$F=\frac{1}{T} \qquad T=\frac{1}{F}$$

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SI multiples of hertz (Hz)

Submultiples				Multiples		
Value	SI symbol	Name		Value	SI symbol	Name
10^{-1} Hz	dHz	decihertz		10^{1} Hz	daHz	decahertz
10^{-2} Hz	cHz	centihertz		10^{2} Hz	hHz	hectohertz
10^{-3} Hz	mHz	millihertz		10^{3} Hz	**kHz**	**kilohertz**
10^{-6} Hz	µHz	microhertz		10^{6} Hz	**MHz**	**megahertz**
10^{-9} Hz	nHz	nanohertz		10^{9} Hz	**GHz**	**gigahertz**
10^{-12} Hz	pHz	picohertz		10^{12} Hz	**THz**	**terahertz**
10^{-15} Hz	fHz	femtohertz		10^{15} Hz	PHz	petahertz
10^{-18} Hz	aHz	attohertz		10^{18} Hz	EHz	exahertz
10^{-21} Hz	zHz	zeptohertz		10^{21} Hz	ZHz	zettahertz
10^{-24} Hz	yHz	yoctohertz		10^{24} Hz	YHz	yottahertz

Common prefixed units are in bold face.

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Units of period and frequency

Unit	*Equivalent*	*Unit*	*Equivalent*
Seconds (s)	1 s	Hertz (Hz)	1 Hz
Milliseconds (ms)	10^{-3} s	Kilohertz (kHz)	10^{3} Hz
Microseconds (μs)	10^{-6} s	Megahertz (MHz)	10^{6} Hz
Nanoseconds (ns)	10^{-9} s	Gigahertz (GHz)	10^{9} Hz
Picoseconds (ps)	10^{-12} s	Terahertz (THz)	10^{12} Hz

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Math\Digital review

- Base 10
  - Combinations = $10^{Number\ of\ symbols}$
  - Example: 2 symbols
  - Combinations = 10^{2} = 100 (combinations from 00 to 99)
- Base 2
  - Combinations = $2^{Number\ of\ symbols}$
  - Example: 4 symbols
  - Combinations = 2^{4} = 16 (combinations from 0000 to 1111)

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History review

Until 16 bits

Date	CPU	Number of Transistors	Clock (MHz)	Address space	Notes
Abr-71	4004	2300	0.108	640 B	First CPU in a single chip
Abr-72	8008	3 500	0.108	16KB	First 8 bits CPU
Abr-74	8080	6 000	2	64KB	First commercial success CPU
Jun-78	8086	29 000	10	1MB	First 16 bits CPU
Jun-79	8088	29 000	8	1MB	Used in the famous IBM PC
Jan-82	80186	100 000	12	1MB	
Jan-82	80188	100 000	12	1MB	Used until few years ago as micro controller
Fev-82	**286**	134 000	12	16MB	**First protected mode implementation**

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History review

The 32 bits Architecture

Date	CPU	Number of Transistors	Clock (MHz)	Address space	Notes
Out-85	386DX	275 000	16	4GB	First 32 bits CPU
Jul-88	386SX	375 000	20	4GB	External is a 16 bits CPU
Abr-89	486	1 200 000	25	4GB	Join coprocessor and 8K cache
Jun-91	486	1 200 000	50	4GB	

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History review

The power of parallel processing

Date	CPU	Number of Transistors	Clock (MHz)	Address space	Notes
Mar-93	Pentium	3 100 000	60	4GB	**2 Pipelines**

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History review

The power of parallel processing

Date	CPU	Number of Transistors	Clock (MHz)	Address space	Notes
Mar-93	**Pentium**	**3 100 000**	**60**	**4GB**	**2 Pipelines**
Mar-95	Pentium Pro	5 500 000	120	4GB	2 levels of cache
Mai-97	Pentium II	7 500 000	300	64GB	Pentium Pro + MMX
Ago-99	Pentium III	9 500 000	600	64GB	10 states for Pipeline; SSE
Mar-00	Pentium III	28 000 000	1000	64GB	
Nov-00	Pentium 4	42 000 000	1500	64GB	20 states for Pipeline; SSE2
Jan-02	Pentium 4	42 000 000	2200	64GB	
Nov-02	Pentium 4	55 000 000	3000	64GB	

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History review

Finally, the 64 bits CPU

Date	CPU	Number of Transistors	Clock (MHz)	Address space	Notes
Abr-05	Pentium D	125 000 000	3200	1TB	EM64T; 12 pipeline states 2*1M L2 cache SSE3
Jul-06	Core 2 Duo	410 000 000	2930	1TB	4M L2 cache; SSE4, SSE3
Nov-08	Core I7	781.000.000	3300	1TB	
02-10	Itanium Tukwila	2.000.000.000	1600	(1TB)	
2012	62-Core Xeon Phi	5.000.000.000	1200	(1TB)	
2016	Xeon Broadwell-E5	7,200.000.000	2200	(1TB)	
2017	32-core AMD Epyc	19,200.000.000	2200	4TB	

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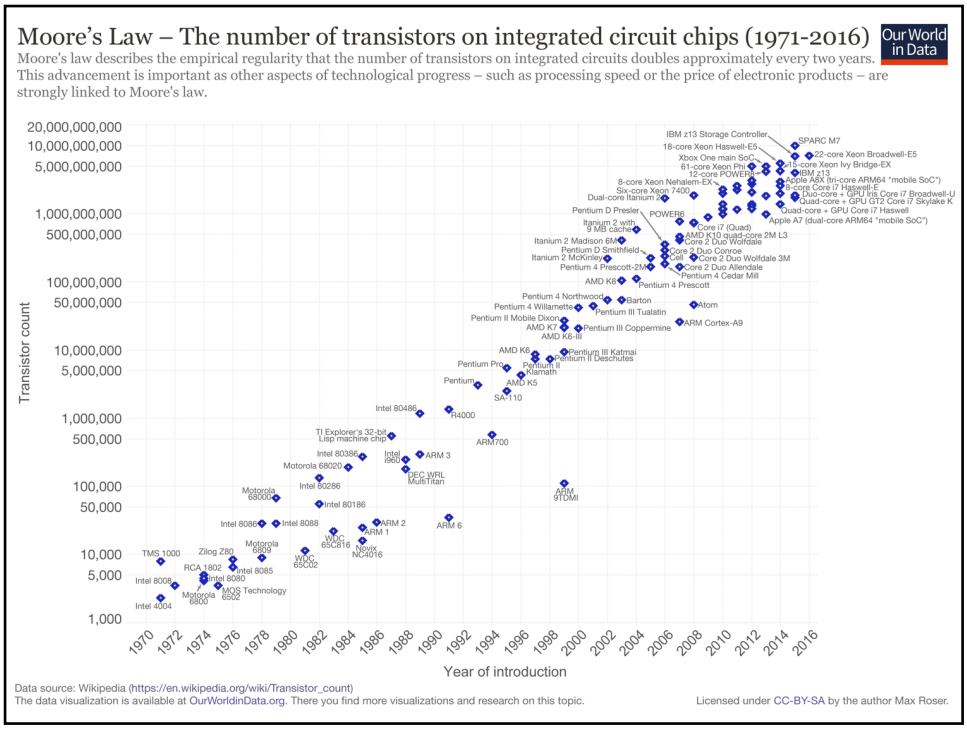

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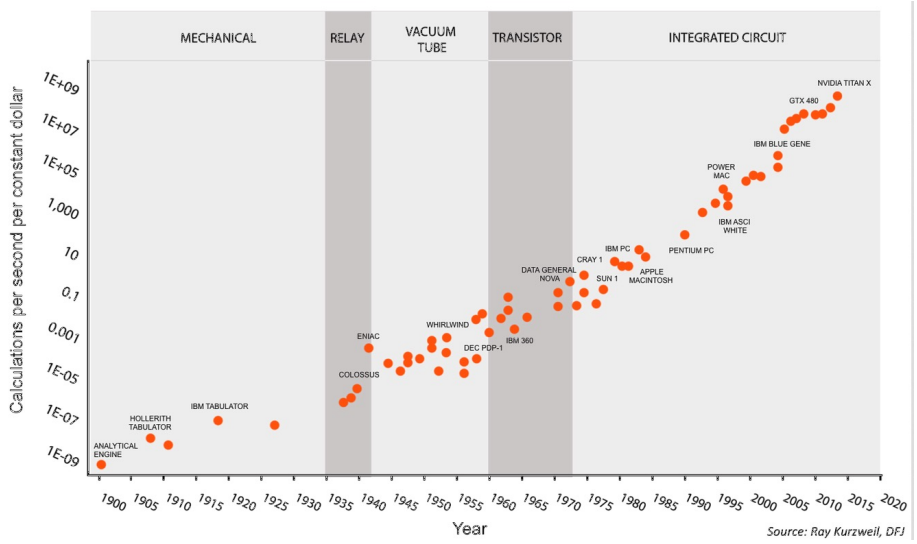
Moore's Law



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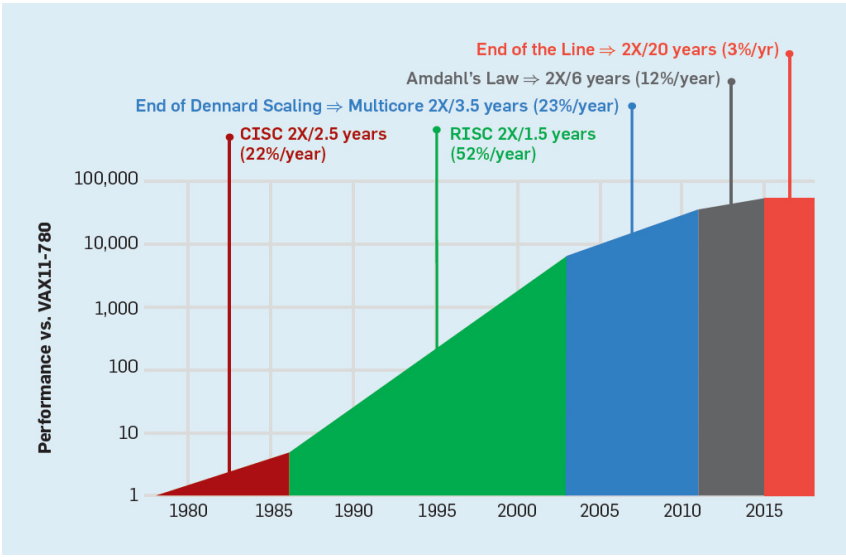
Moore's Law



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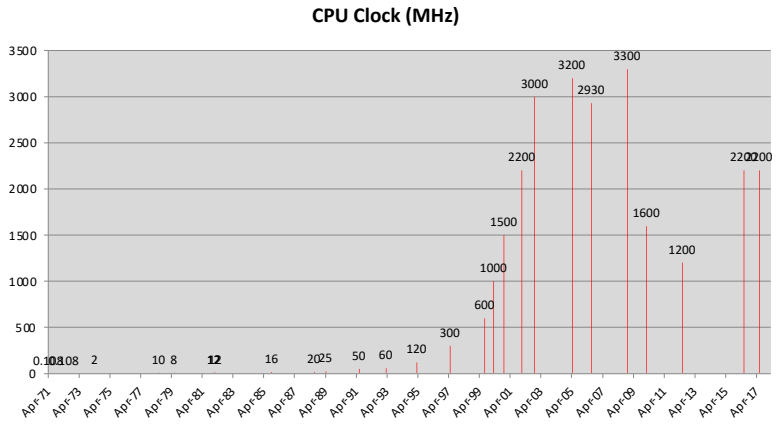
CPU CLOCK EVOLUTION



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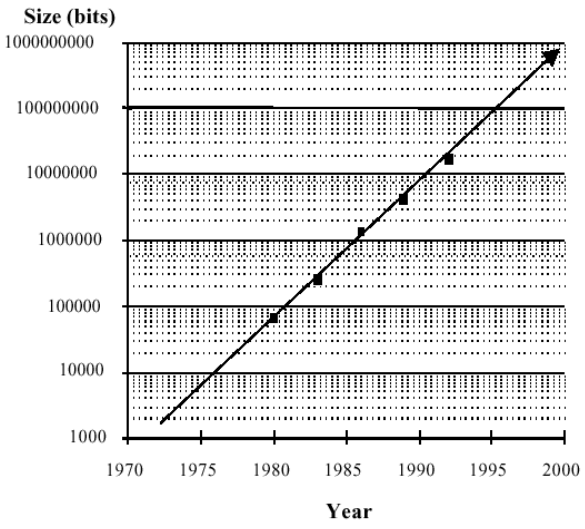
RAM Evolution



Year	Size(Mbit)
1980	0.0625
1983	0.25
1986	1
1989	4
1992	16
1996	64
2000	256

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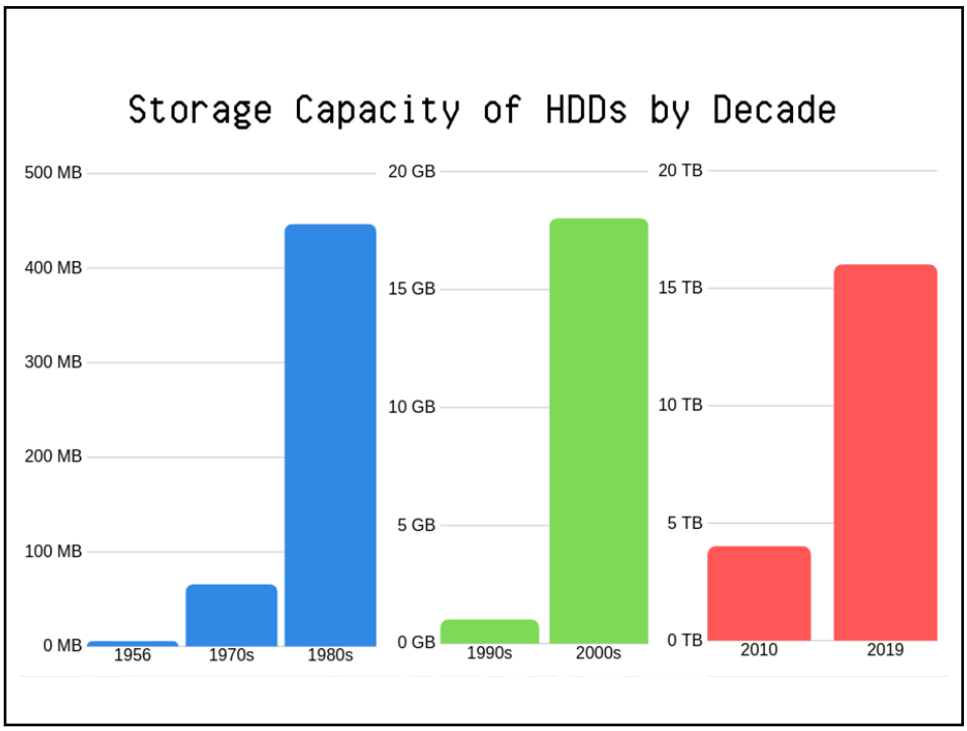
Storage Capacity of HDDs by Decade
500 MB
400 MB
300 MB
200 MB
100 MB
0 MB
1956
1970s
1980s
20 GB
15 GB
10 GB
5 GB
0 GB
1990s
2000s
20 TB
15 TB
10 TB
5 TB
0 TB
2010
2019

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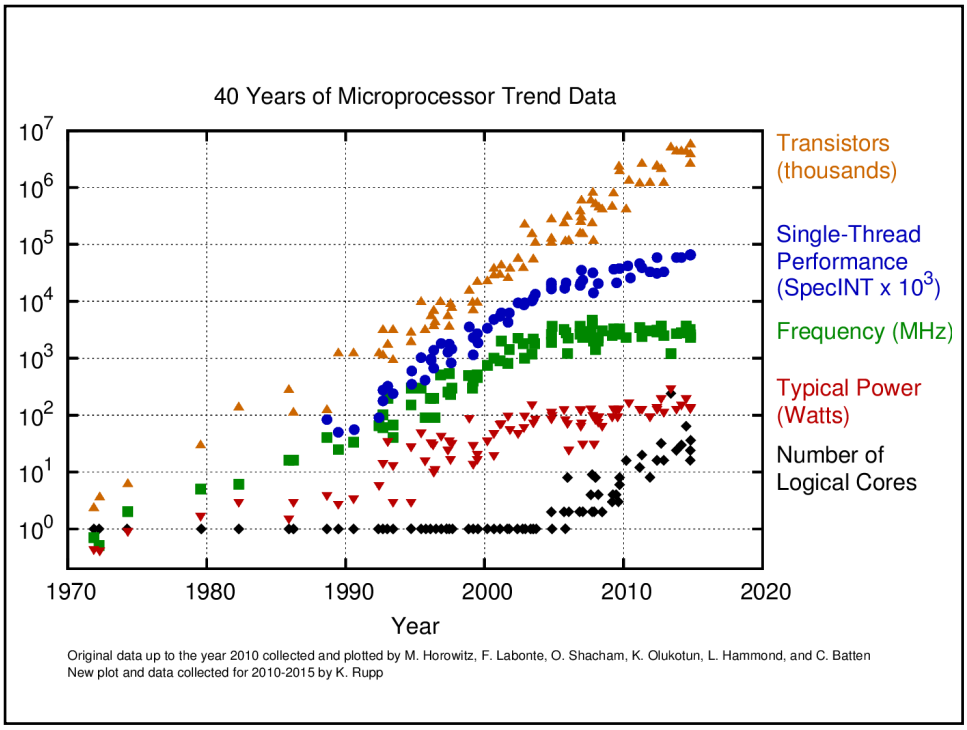
40 Years of Microprocessor Trend Data
10^7
10^6
10^5
10^4
10^3
10^2
10^1
10^0
1970
1980
1990
2000
2010
2020
Year
Transistors (thousands)
Single-Thread Performance (SpecINT x 10^3)
Frequency (MHz)
Typical Power (Watts)
Number of Logical Cores
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp

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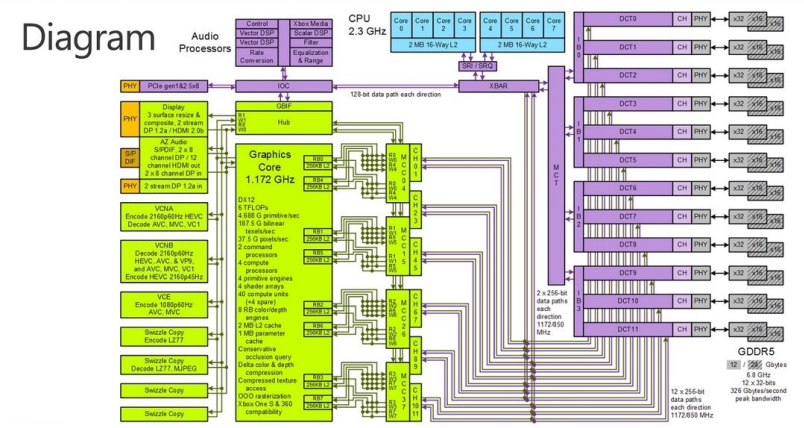
Xbox one X



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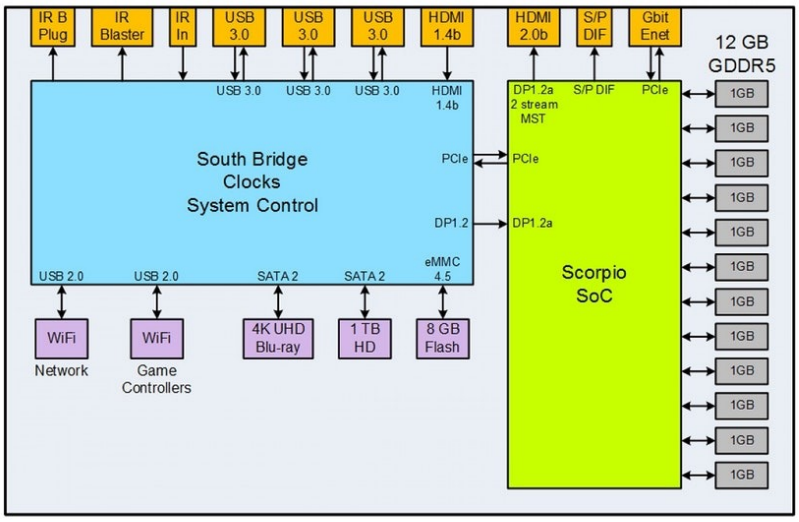
Many interfaces!!!



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What is computer architecture? Should be Computer Architectures

- Different opinions exist
  - Hardware structure, components, interfaces
  - Basic operation principle, applications
  - Only external view
  - Internal and external view
- Computer architecture is NOT (only) the standard PC architecture!
  - The vast majority of computers are embedded systems, specialized solutions
  - One size does NOT fit it all

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Amdahl, Blaauw and Brooks 1967

- "Computer architecture is defined as the attributes and behavior of a computer as seen by a machine-language programmer. This definition includes the instruction set, instruction formats, operation codes, addressing modes, and all registers and memory locations that may be directly manipulated by a machine language programmer.
- Implementation is defined as the actual hardware structure, logic design, and data path organization of a particular embodiment of the architecture."

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Another view: processor architecture

- The processor architecture (Instruction Set Architecture) comprises the description of attributes and functions of a system as seen from a machine language programmer's point of view.
- The specification of the processor architecture comprises:
  - instruction set
  - instruction formats
  - addressing modes
  - interrupt handling
  - logical address space
  - Register/memory model (as far as a programmer can access it)
- The processor architecture does not describe details of the implementation or hardware – all internal operations and components are explicitly excluded.

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Processor micro architecture

- An **implementation** (micro architecture) describes the hardware structure, all data paths, the internal logic etc. of a certain realization of the processor architecture, thus a real microprocessor.
- The **micro architecture** defines:
  - Number and stages of pipelines
  - Usage of super scalar technology
  - Number of internal functional units (ALUs)
  - Organization of cache memory

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Processor micro architecture

- The definition of a **processor architecture** (ISA, instruction set architecture) enables the use of programs independent of a certain internal implementation of a microprocessor.
- All microprocessors following the same processor architecture specification are called "**binary compatible**" (i.e., the same binaries run on them).

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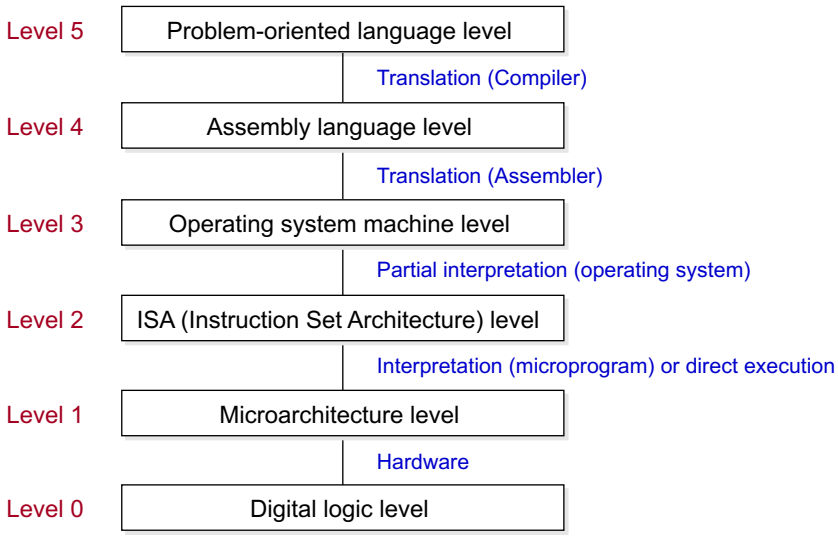
The Layered Computer Model



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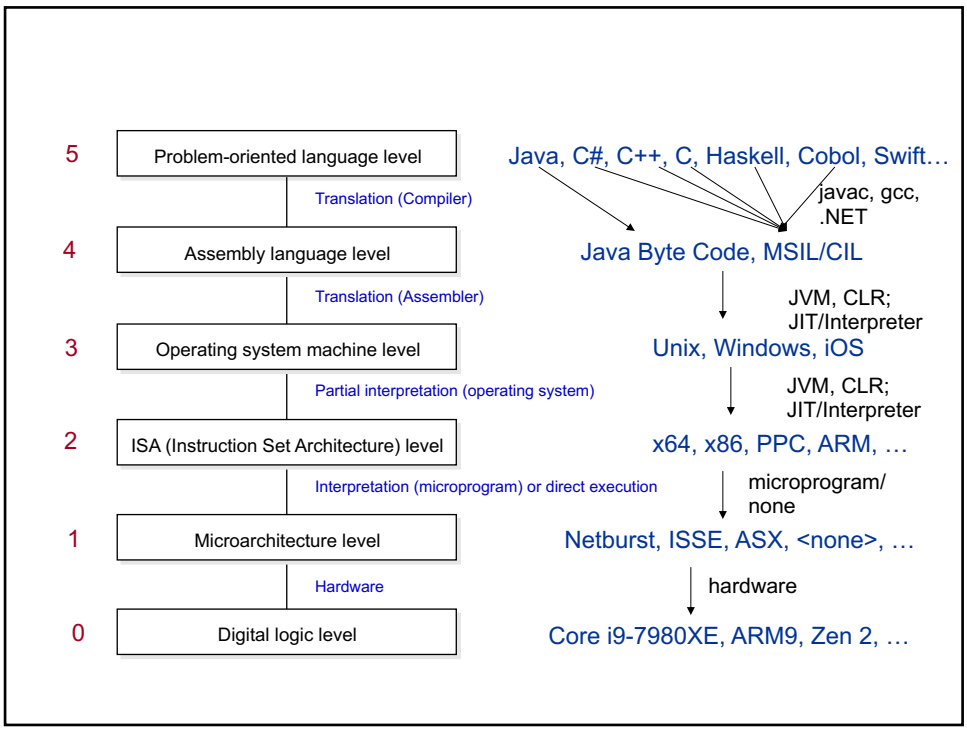
5
Problem-oriented language level
Translation (Compiler)
4
Assembly language level
Translation (Assembler)
3
Operating system machine level
Partial interpretation (operating system)
2
ISA (Instruction Set Architecture) level
Interpretation (microprogram) or direct execution
1
Microarchitecture level
Hardware
0
Digital logic level
Java, C#, C++, C, Haskell, Cobol, Swift…
javac, gcc, .NET
Java Byte Code, MSIL/CIL
JVM, CLR; JIT/Interpreter
Unix, Windows, iOS
JVM, CLR; JIT/Interpreter
x64, x86, PPC, ARM, …
microprogram/ none
Netburst, ISSE, ASX, <none>, …
hardware
Core i9-7980XE, ARM9, Zen 2, …

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