Electrical and Geometrical Circuit Performance Using an Advanced Sea-of-Gates Philosophy

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Abstract

A sea-of-gates array has been designed to optimally support random and regular logic, and analog circuits. Its philosophy is to promote wiring and communication instead of packing as many transistors as possible on the array. At the global level, thanks to the saved routing area, densities as good as those obtained with a standard cell design style are achieved. Some important results on circuit densities and electrical performance are presented and discussed in this paper, for the different circuit families. These results are compared with those obtained with other design styles. Finally, several suited CAD tools are presented.

1. Introduction - Sea-of-gates philosophy

Recent evolution of advanced masterslices has essentially consisted in an improvement of the apparent gate density, through a reduction of the basic device size and of the transistor pitch. This evolution and two new concepts, i.e. gate isolation and channelless layout, have lead to impressive packing capabilities (e. g. [2]). Design methodologies, however, did not evolve so much. Conventional semi-custom design styles still use fixed libraries of standard macros, align the cells in rows, and make intensive use of routing channels. This degrades flexibility, increases area consumption and average wire length, and finally limits the performance. Moreover, conventional arrays are usually random logic oriented, and can hardly be used for implementing regular arrays (RAM, PLA,..) or analog cells in an efficient way, except when reserving special areas for this purpose.

The new EPFL sea-of-gates array [1], later called SOG, has been primarily optimized to support mixed implementation of random logic, regular arrays, and analog circuits. Its underlying philosophy is to locally accept some reduction in transistor density (e. g. due to a larger transistor pitch), but to compensate this at the global level by suppressing most of the routing area. The channelless structure with gate isolation provides flexibility and stretching of the cells ; a ratio of 2 has been chosen for the N/P transistor count, for improving the density of regular arrays and analog circuits, without degrading the random logic packing density ; the transistor pitch, twice as large as the metal pitch, allows for vertical transparency ; and a very strict strategy in metal use gives transparency in both directions, and helps suppressing most of the routing channels. These features allow the application of advanced concepts, generally used in full-custom design only, such as cell abutment, regularity in the design, and hierarchy. In this way, the decrease of transistor density is not only compensated by a better use of the available devices, but the average wire length is reduced, leading to improved performance. An automatic procedure, converting a SOG layout into a topologically equivalent symbolic full-custom one, has also been defined. It allows the designer to easily convert a tested semi-custom prototype into a full performance, compact full custom circuit, more suited to mass production.

Using a standard double-metal two-microns CMOS technology, a wide variety of test circuits has been fabricated on the new SOG structure for an in-depth testing of circuit densities and electrical performance. These results are presented in sections 2 and 3. When appropriate, they are compared with standard cell or full-custom circuits generated in the same technology. The fourth section briefly reviews a set of CAD tools which take a particular advantage of the SOG structure capabilities.

2. Geometrical results

Figure 1 gives the area (in λ^2) of different cells or modules of increasing complexity, in comparison with other design styles such as standard cell, full-custom (generated from a

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CELL	Number of transistors	EPFL sea-of-gates	standard cells	symbolic full-custom	symb. gen. from s-o-g
LOGIC					
2 inputs nand	4	5'184	2'880	2'568	2'954
1 bit LIFO register	12	19'008	27'468	8'680	9'288
13 inputs AOI gate	26	29'380	43'602	10'456	12'560
1 bit full-adder	28	27'636	18'984	11'400	13'377
1x1 multiplier cell	34	36'278	23'902	18'796	20'112
4 bits CL adder	128	186'624	192'128	87'616	93'749
4 bits CL alu	294	430'122	390'432	-	-
16 bits adder	448	442'176	417'984	182'400	204'032
64 bit sync. counter	1'920	2'432'640	2'970'908	1'336'615	1'430'178
32 x 16 bits LIFO	6'144	9'732'096	17'161'655	4'444'160	4'755'456
REGULAR ARRAYS	Number of transistors	EPFL sea-of-gates	full-custom		
SRAM cell	6	5'184	828		
2 bits PLA cell	2	2'592	289		
ANALOG CIRCUITS					
OTA		95'680	51'800		

fig. 1 : Comparative areas for different design styles (in λ^2)

symbolic layout editor), and also full-custom automatically generated from the SOG layout with the procedure described in [1]. For random logic circuits, the area obtained with the SOG approach is generally comparable with standard cell area, and is about twice as large as the symbolically generated full-custom. The symbolic layout derived from SOG is generally 10-20% larger than the handcrafted symbolic layout. For regular circuits, density is comparable with random logic, but is of course much lower than the full custom density. This might limit the reasonable size of regular arrays implemented on the SOG structure to, say, 2K for the SRAM and 8K for the ROM. For the same order of electrical performance, the area of analog circuits built on the SOG structure is twice as large as the full-custom circuit area, which is quite acceptable.

Figure 2 displays the evolution of the density versus complexity (expressed in terms of a number of transistors) for

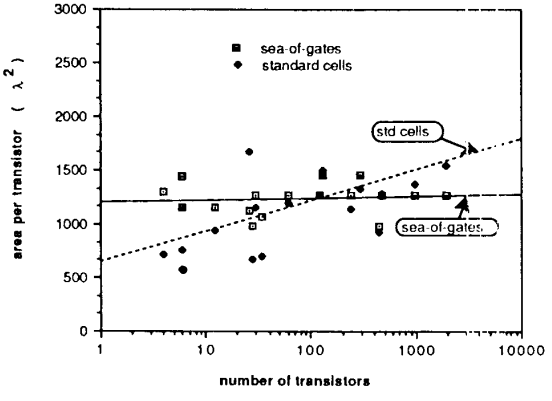

fig. 2 : Evolution of the area per transistor
Straight lines are first order approximations

both the SOG and standard cells design styles. As normally expected, individual standard cells are smaller than their equivalent SOG cells, but, because of the increase in routing area, standard cell layouts become generally larger beyond a certain complexity (about a few hundreds transistors), as indicated by the linear regression lines shown on the same figure.

A similar result is obtained from figure 3,where the standard cell over SOG area ratio is given as a function of the number of bits of a synchronous counter. The growth of the SOG layout is linear, which is not the case of the standard cell layout. The ratio becomes favorable to SOG for large sizes (from 8 or 16 bits).

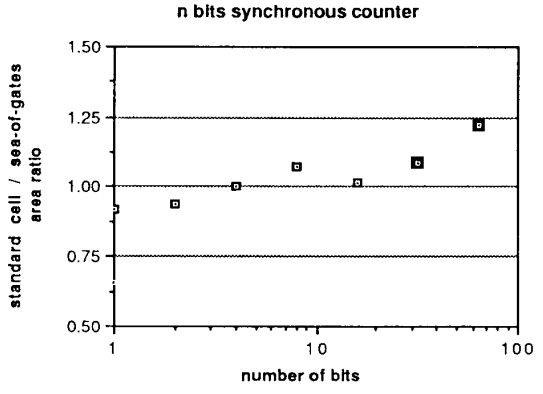

fig. 3 : Standard cell / Sea-of-gates area ratio for different sizes of a counter

As an example, figure 4 compares the layouts of the same 4 bits carry-lookahead ALU for the two design styles. In this case, the standard cell area is 90% of the SOG area, but the total routing wire length is 2.88 times larger for the standard cell approach, leading of course to worse electrical performance. It can be seen that the routing or unused area in the SOG layout is kept quite small (less than 20% of the total area), most of the routing being made of feed-through wires crossing the functional cells in both directions.

A complete 8 bits low-power A/D converter, based on a cyclic architecture [4] has also been designed. Its area is about 0.32 mm^2 for the analog part, and 1.04 mm^2 for the digital part (transistor utilization rates are respectively 86% and 85%). The needed capacitances were placed on I/O pad locations.

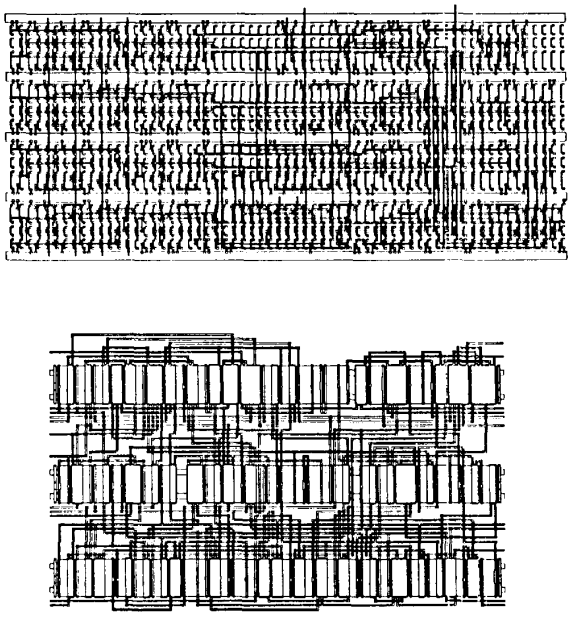

fig. 4 : Two implementations of the same module.
A 4 bits carry-lookahead ALU counting 300 transistors. SOG implementation is on the top, standard cell implementation is on the bottom.

3. Electrical performance

Some electrical performance obtained for circuits built on the SOG structure are summarized in figure 5. Most of these results come from measurements on the test chips. Some of them (marked by a 'S') come from simulations, which have been validated by measurements. Those results are compared with full-custom and standard cells in similar situations. Sea-of-gates random logic circuits behave generally better than the equivalent standard cells circuits, because the load capacitance is lower. For limited sizes, regular logic circuits also present speed performance comparable with full-custom. For higher sizes of course (beyond 4K for a RAM), full-custom circuits become faster. Large regular circuits are however not suitable for a SOG implementation, because of space wasting.

	unit	sea-of-gates	full-custom	standard cells
DIGITAL				
basic gate delay (ring oscillator)	ns	0.5	-	-
adder 1 bit addition time	ns	3.5	-	3.8 - 13.4 (S)
adder carry propagation time	ns	2.8	-	1.9 - 6.0 (S)
PLA max. frequency	MHz	50	-	-
4 bits sync. counter max frequency	MHz	75	-	70 (S)
RAM access time : 16 bits	ns	3.8	-	-
RAM access time : 2K bits	ns	22.0 (S)	-	-
ANALOG				
OTA transconductance	uA/V	108.1±4	96.5±3.9	-
OTA offset voltage	mV	4.4±3.1	2.1±1.3	-
OTA linear range	mV	103	100	-

fig. 5 : Electrical performance samples

The electrical characteristics of the analog circuits are comparable to full-custom ones, except the offset voltage, which is multiplied by a factor of 2. This value stays in an acceptable range for most applications, and could be further reduced, at the cost of a larger area.

4. CAD tools

Although the array architecture is compatible with classical place-and-route cell-based programs linked to a macro library, such systems would not take a full advantage of the possibilities of the structure. More suited CAD tools have therefore been designed.

A first category contains common tools which are familiar to full-custom designers : a symbolic editor with some additional functionalities, such as the on-line checking of the metallization rules, and several regular array generators for RAM, ROM and PLA. More advanced tools, such as data-path or state-machine compilers, can also be easily adapted to the SOG structure.

A second category consists of high-level design automation tools. The GRAPES module generator [3], which was originally dedicated to full-custom generation, is able to lay out random logic modules counting up to a few hundreds transistors, while taking a full advantage of the structure capabilities. The input consists of the boolean equations, and of some user-defined constraints like the aspect ratio, the side and order of the pins, and the load capacitance of the outputs.

The basic building block of the GRAPES system is called a cell, which can be either a general AOI gate, or some other special gate (e.g. xor gate). Any permutation of the inputs is allowed (as long as the inputs of a sub-gate are grouped), the cell can be stretched and crossed by feed-through wires, and transistors can be paralleled to yield larger sizes. Cells are arranged in rows like conventional macros, but, unlike most classical tools, placement and routing are produced simultaneously in a top-down fashion. No routing channel normally takes place between two rows, the cells being placed in order to allow horizontal and vertical abutment as much as possible. Furthermore, power nodes are merged whenever it is possible. Figure 6 shows an example of a 302 transistors module, laid out by GRAPES. For this example, only one routing channel was needed inside the module for

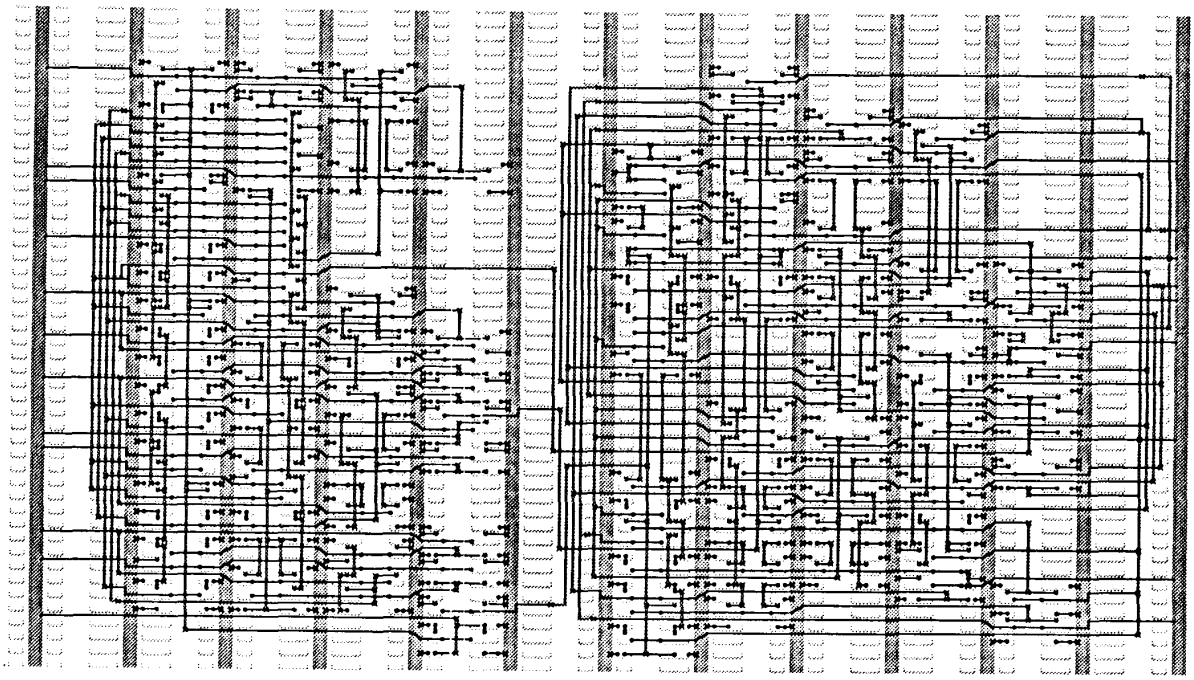

fig. 6 : The standard TTL-series 74885 8-bit magnitude comparator (302 transistor) laid out by Grapes.

the 9 cell rows.

5. Conclusion

Reducing the basic cell size is not the only way of getting high performance, high density semi-custom arrays. A careful optimization of the array architecture, making a trade-off between the gate density and the integration level, presents several advantages : possibility of abutting the cells in both directions, high level of cell integration and flexibility, suppression of most of the external routing, effective implementation of regular arrays and analog circuits on the core, and reduction of the average wire length.
On the basis of measurements made on the test circuits, the following results can be pointed out :
- the SOG random logic circuit density is comparable to (full-custom) standard cells density, and becomes even higher when complexity increases,
- the average wire length of SOG layouts is significantly lower than that of standard cells design,
- logic as well as analog circuits have electrical performance that compares well with standard cells or analog full-custom, thanks to a smaller load capacitance.

However, a very efficient SOG architecture is not sufficient to produce high quality circuits by itself. To take a full advantage of its potential performance, adapted CAD tools are needed. Until now, most of the researchers effort has consisted of adapting older conventional tools to some new aspects of arrays architecture. But the basic drawbacks (area, wire length) of these strategies stay. New design strategies and algorithms should be developed, in order to really use the full potential of the second-generation semi-custom arrays.

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