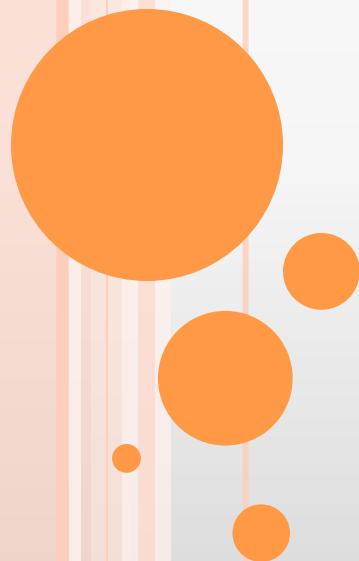
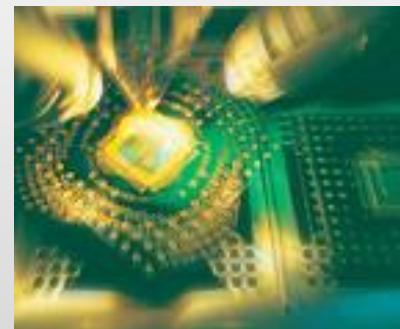


TECNICAS DE INTEGRACION



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II-2013



TENSION DE UMBRAL - RESUMEN

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

↑ ↑ ↑
Workfunction Surface Charge Implants
Difference Depletion Layer Charge

Body Effect Coefficient

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

with

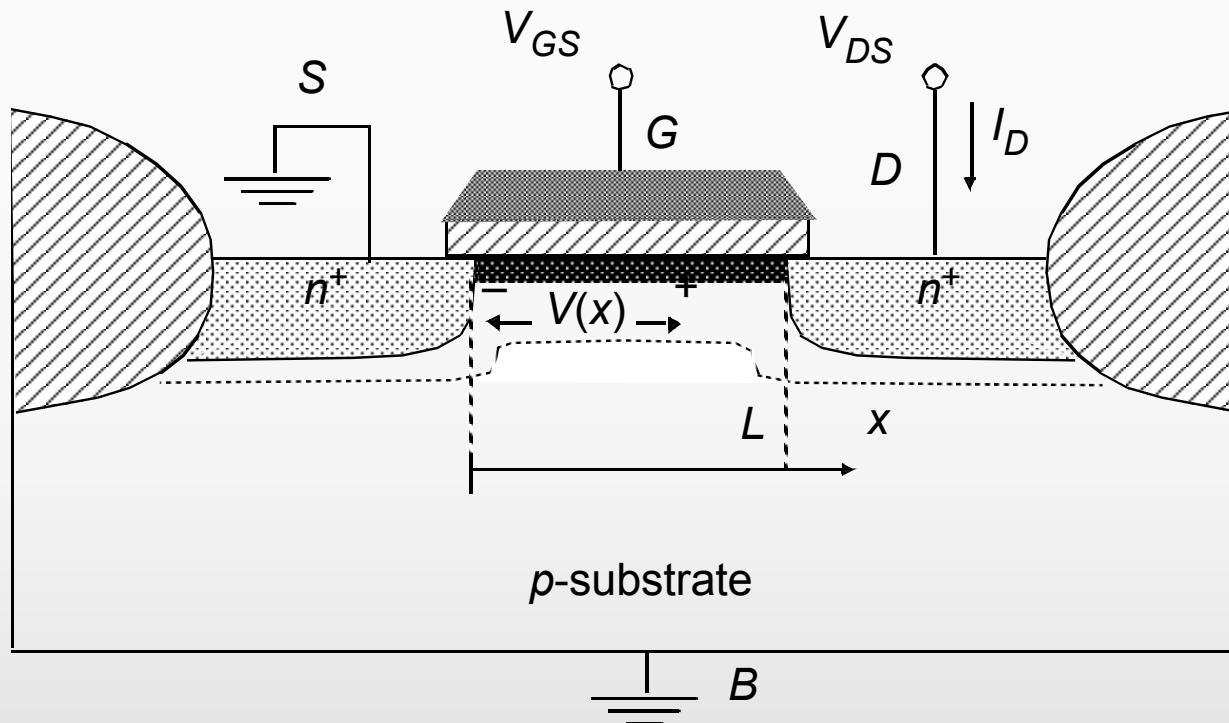
$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$$



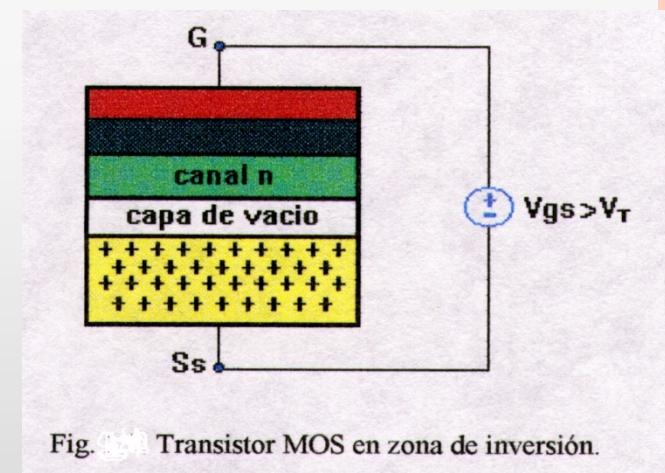
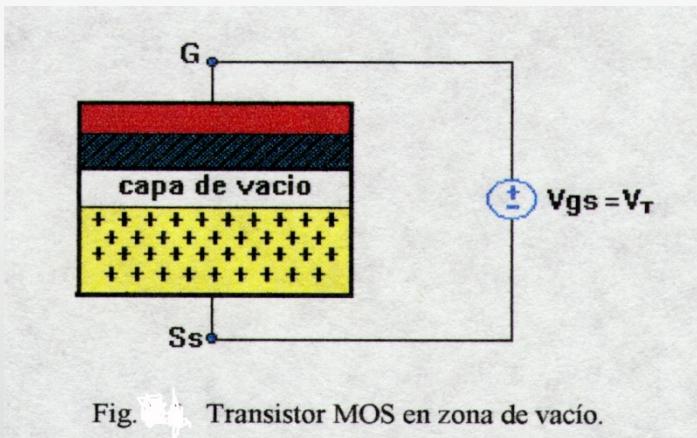
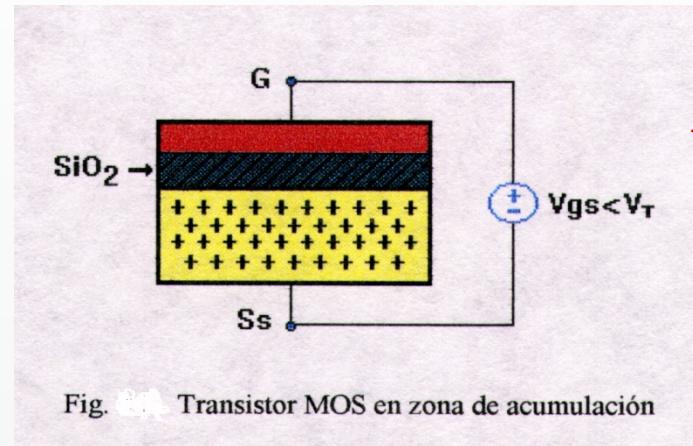
RELACIÓN TENSIÓN - CORRIENTE



MOS transistor and its bias conditions



ZONAS DE OPERACION



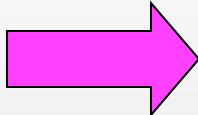
VACIO

INVERSION

ZONAS DE OPERACIÓN

$$I_{ds} = \frac{C_g \cdot \mu \cdot V_{ds}}{L^2} \cdot (V_{gs} - V_t)$$

Al aumentar V_{ds} se pierde linealidad


$$I_{ds} = \beta \cdot \left[(V_{gs} - V_t) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right], \quad 0 < V_{ds} < V_{gs} - V_t$$

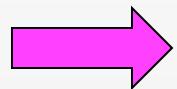
$$\beta = \frac{C_{ox} \cdot \mu \cdot W}{L} = \frac{\epsilon_{SiO_2} \cdot \mu}{T_{ox}} \cdot \frac{W}{L}$$

β es el factor de ganancia del transistor MOS

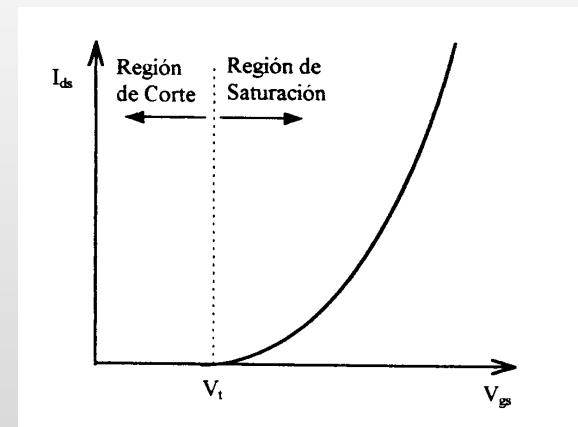
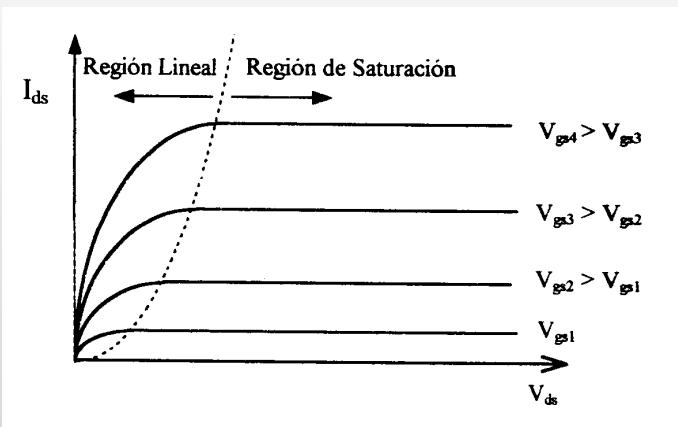


ZONAS DE OPERACIÓN

Región Saturación



$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2}, \quad 0 < V_{gs} - V_t < V_{ds}$$



ECUACIONES DE OPERACIÓN

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

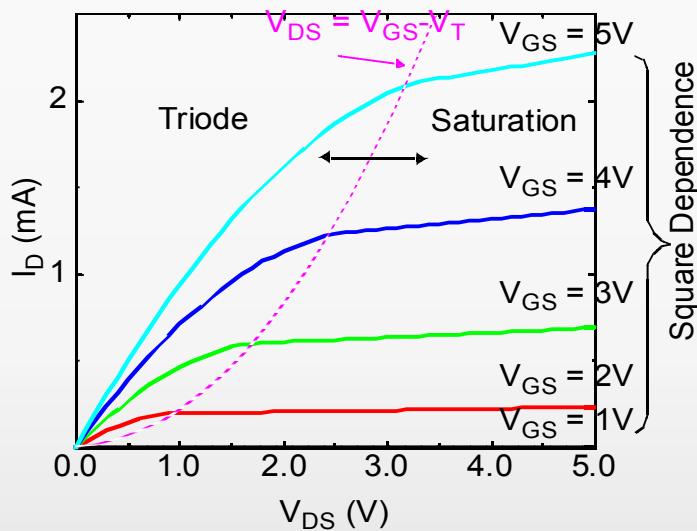
Process Transconductance
Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

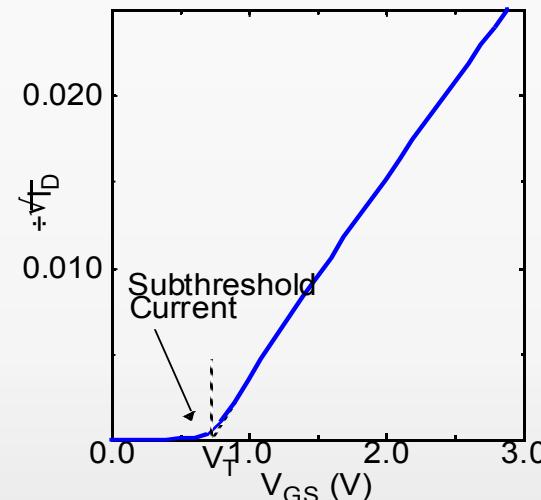
$$I_D = \frac{k'_n W}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

↖
Channel Length Modulation

Relación I-V



(a) I_D as a function of V_{DS}

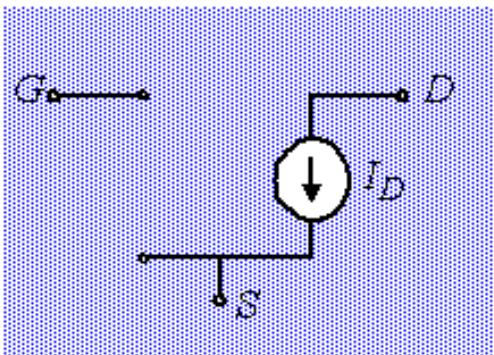


(b) $\sqrt{I_D}$ as a function of V_{GS}
(for $V_{DS} = 5V$)

NMOS Enhancement Transistor: $W = 100 \mu\text{m}$, $L = 20 \mu\text{m}$



MODELO DE ANÁLISIS



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'nW}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$



PARAMETROS DE CONSTRUCCION

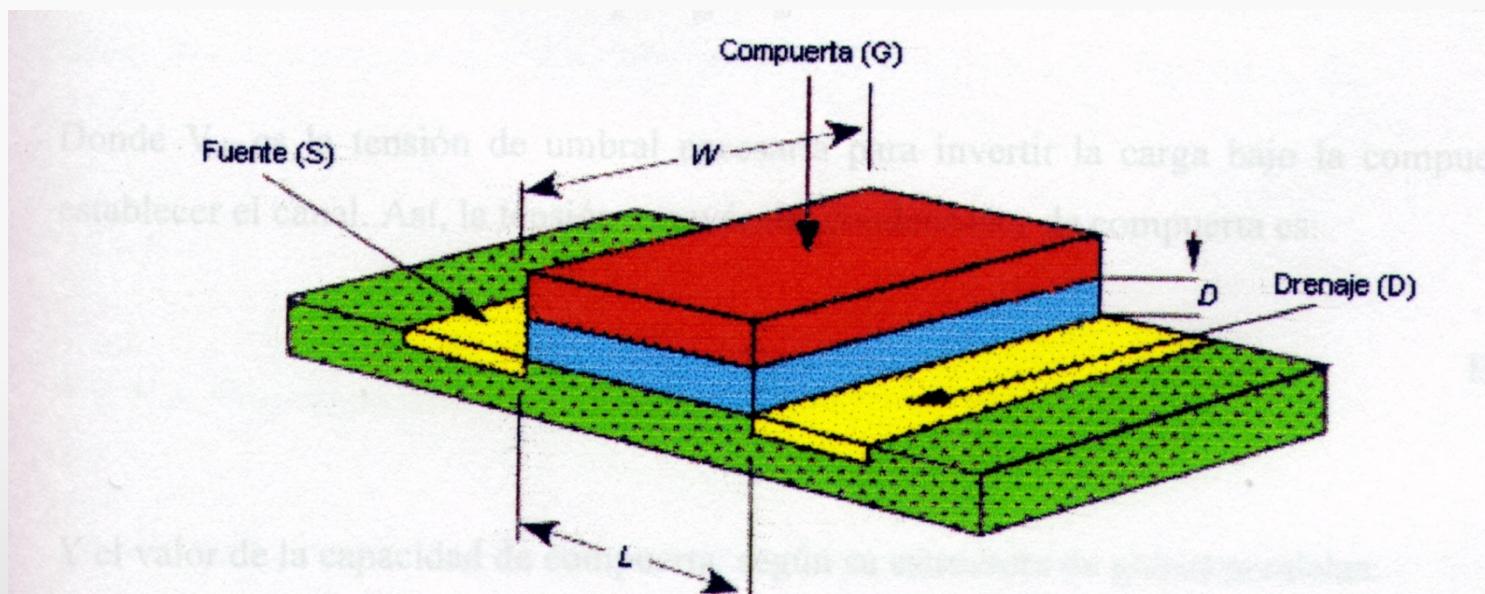


Figura ... Estructura de un MOSFET de enriquecimiento.

ESQUEMA DE OPERACION

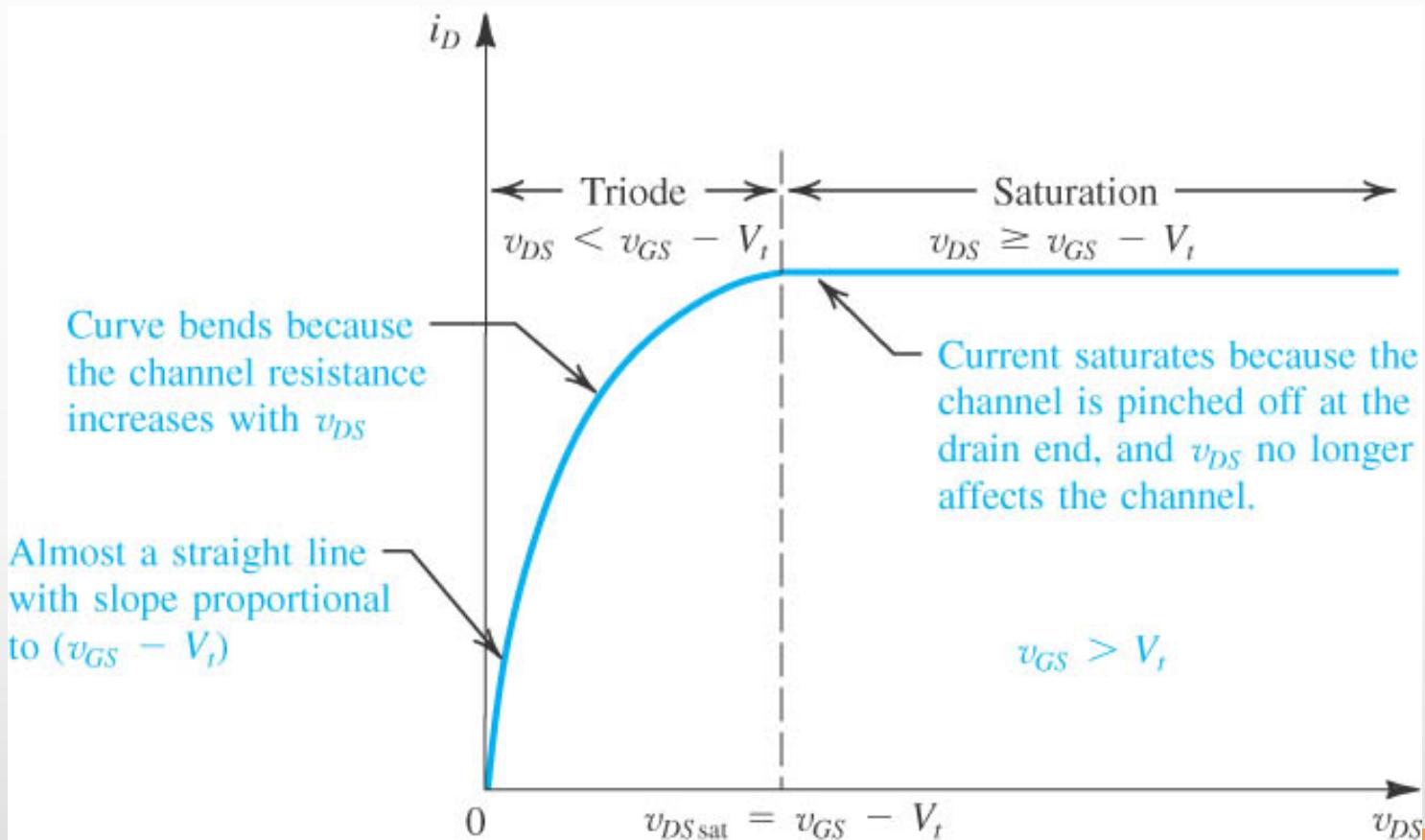
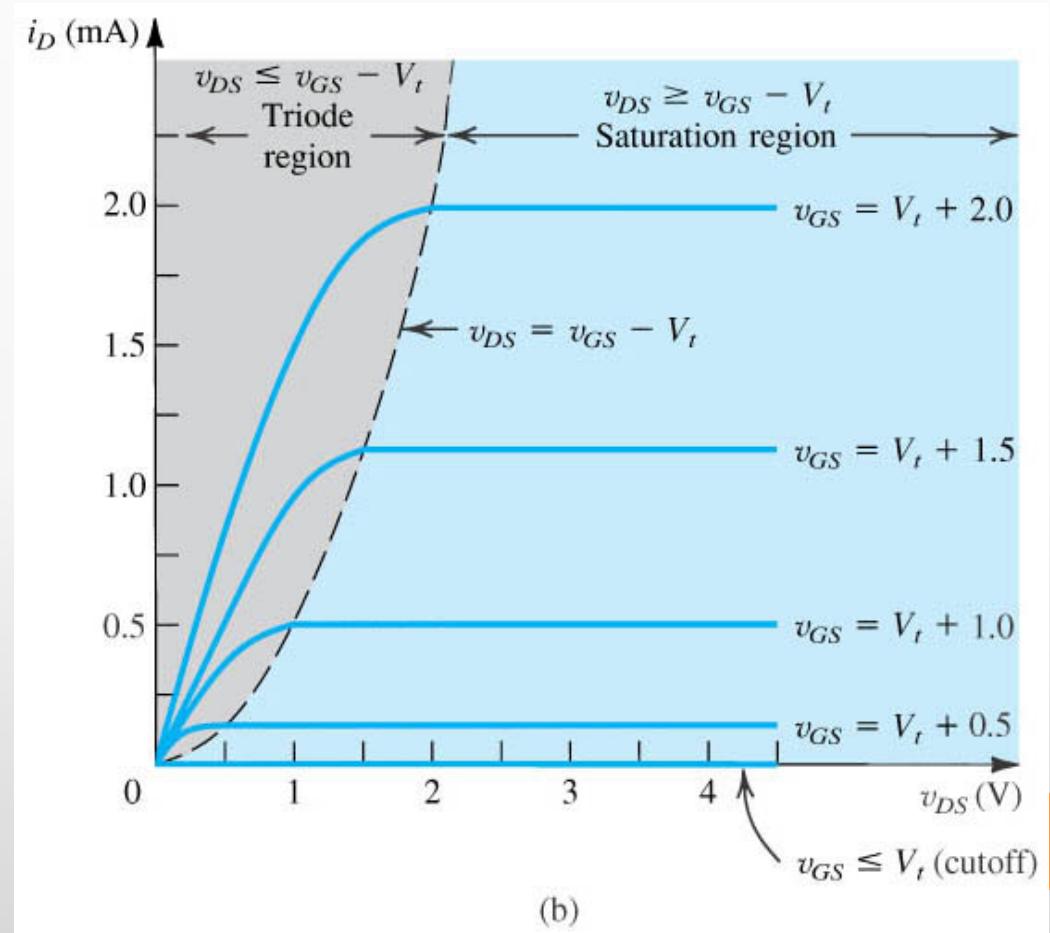
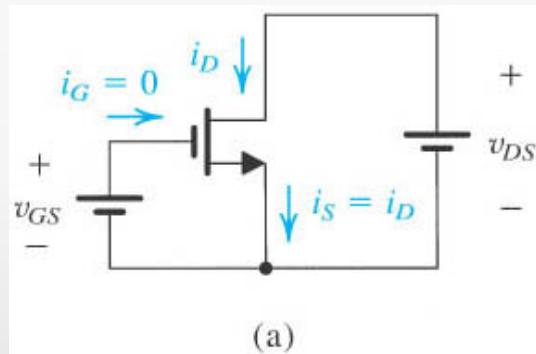


Figure 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

MOSFET CANAL N - MEJORADO



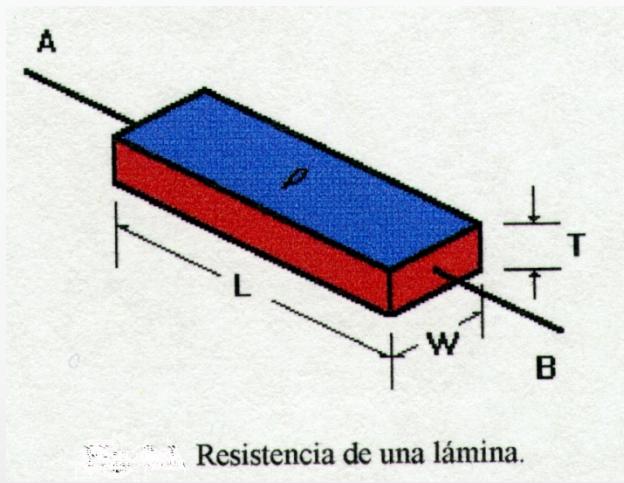
PARÁMETROS SPICE

Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E-14
Emission coefficient	n	N	-	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	sec	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	-	0.5
Junction potential	ϕ_0	VJ	V	1

First Order SPICE diode model parameters.

ELEMENTOS BASICOS

RESISTENCIA



ρ : Resistividad

T : Espesor

L : Longitud del conductor

W : Ancho del conductor

R_s : Resistencia laminar [$\Omega/$].

$$R = \frac{\rho}{T} \cdot \frac{L}{W}$$

$$R = R_s \cdot \frac{L}{W}$$

$$R_c = k \cdot \frac{L}{W} \quad k = \frac{1}{\mu \cdot C_o x (V_{gs} - V_t)}$$

VALORES TÍPICOS DE RESISTENCIA

CAPA	TECNOLOGIA 5 μ	TECNOLOGIA 2 μ	TECNOLOGIA 1,2 μ
METAL	0,03	0,04	0,04
DIFUSION	10 → 50	20 → 45	20 → 45
POLISILICIO	15 → 100	15 → 30	15 → 30
CANAL n	104	2×10^4	2×10^4
CANAL p	$2,5 \times 10^4$	$4,5 \times 10^4$	$4,5 \times 10^4$

Valores típicos de resistencia laminar para diferentes capas de fabricación.

ELEMENTOS BASICOS(1)

CAPACITANCIA

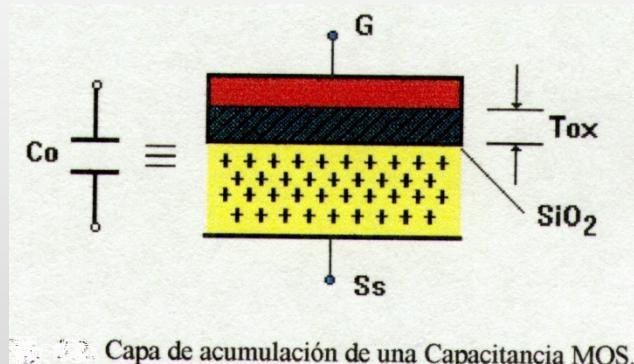
$$C_o = \epsilon_{SiO_2} \frac{2 \cdot \epsilon_0}{T_{ox}} A$$

ZONA ACUMULACION

A : Area de Gate

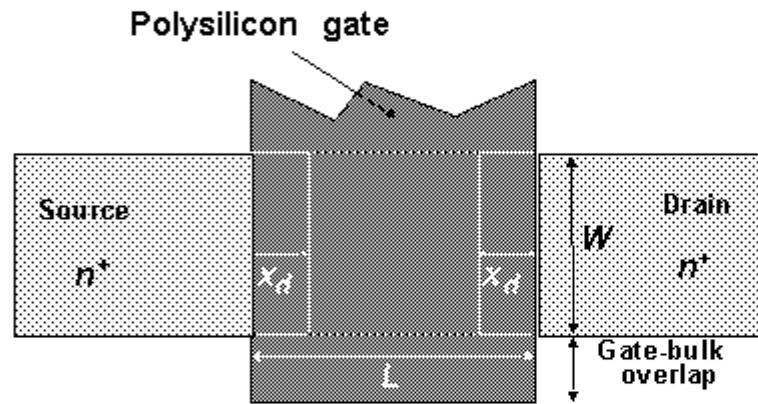
ϵ_{SiO_2} : Constante dieléctrica del SiO₂

ϵ_0 : Permitividad del vacío

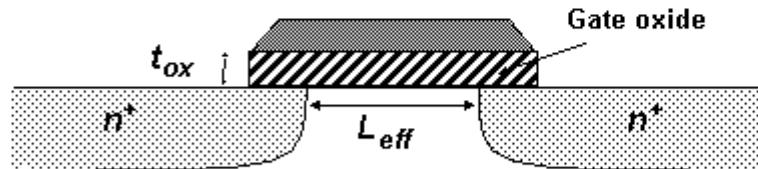


CAPACITANCIA DE COMPUERTA

(a) Top view.



(b) Cross-section



$$C_{gate} = \frac{\epsilon_{ox}}{t_{ox}} WL$$

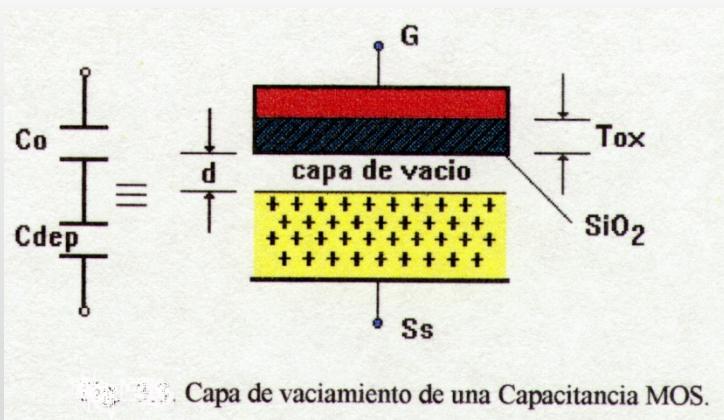


CAPACITANCIA - ZONA DE VACIAMIENTO

$$C_{\text{dep}} = \frac{\epsilon_0 \cdot \epsilon_{\text{Si}}}{d} A$$

d : Profundidad de la capa de vaciamiento

ϵ_{Si} : Constante dieléctrica del silicio



$$C_{\text{gb}} = \frac{C_o \cdot C_{\text{dep}}}{C_o + C_{\text{dep}}}$$

CAPACITANCIA -ZONA DE INVERSIÓN

baja frecuencia ($f < 100$ Hz)

$$C_{gb} = C_o$$

$$C_{gb} = \frac{C_o \cdot C_{dep}}{C_o + C_{dep}}$$

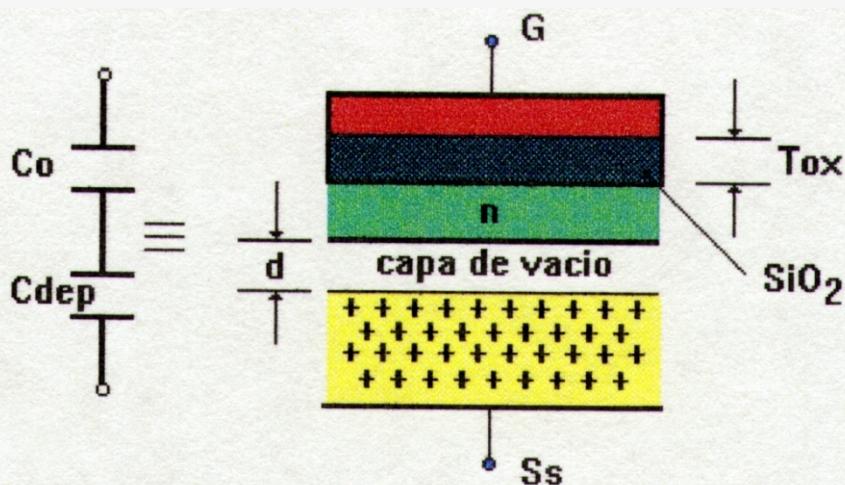
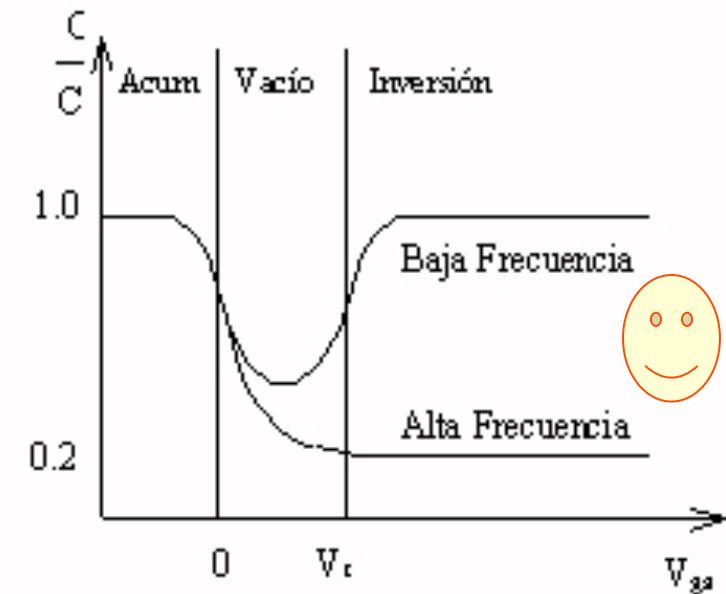


Fig. 1.1 Capa de inversión de una Capacitancia MOS.

alta frecuencia



CAPACITANCIAS EN EL MOSFET

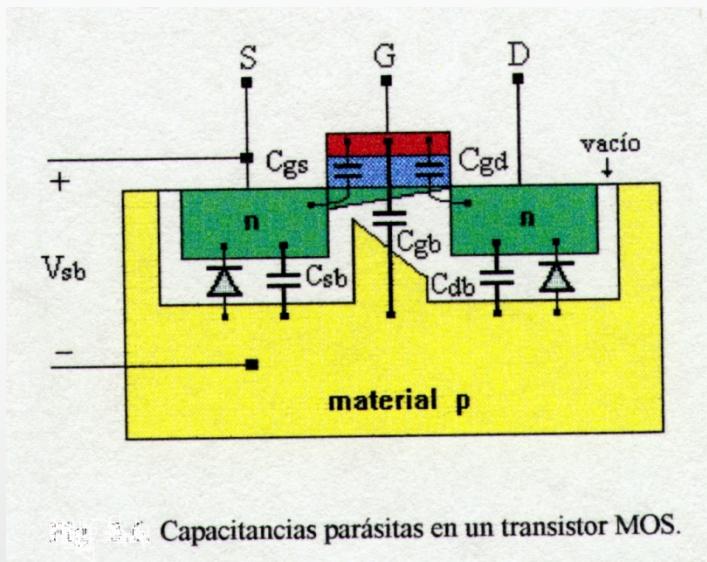
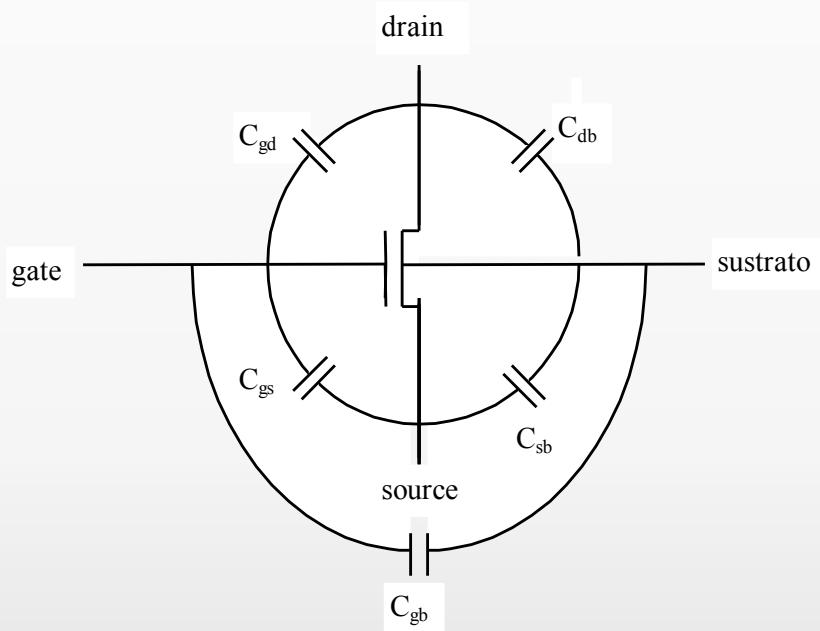


FIG. 3.1 Capacitancias parásitas en un transistor MOS.



$$C_g = C_{gb} + C_{gs} + C_{gd}$$

REGION DE CORTE

V_{gs}<V_t

$$C_{gs} = C_{gd} = 0$$

$$C_{gb} = \frac{Co \cdot C_{dep}}{Co + C_{dep}}$$

REGION NO SATURADA

$$V_{gs} - V_t > V_{ds}$$

$$C_{gd} = C_{gs} = \frac{1}{2} \cdot \frac{\varepsilon_0 \cdot \varepsilon_{SiO2}}{T_{ox}} \cdot A$$

$$C_{gb}=0$$

REGION SATURADA

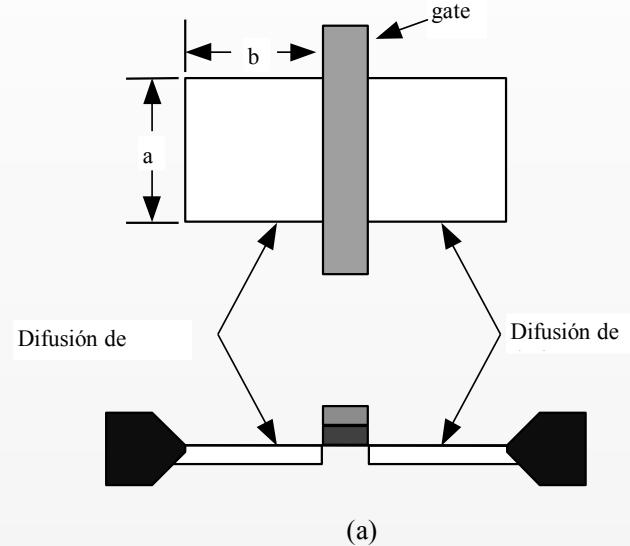
$$V_{gs} - V_t < V_{ds}$$

$$C_{gs} = \frac{2}{3} \cdot \frac{\varepsilon_0 \cdot \varepsilon_{SiO2}}{t_{ox}} \cdot A$$



CAPACITANCIAS DE DIFUSION

$$C_d = C_{ja} \cdot a \cdot b + C_{jp} \cdot (2a + 2b)$$

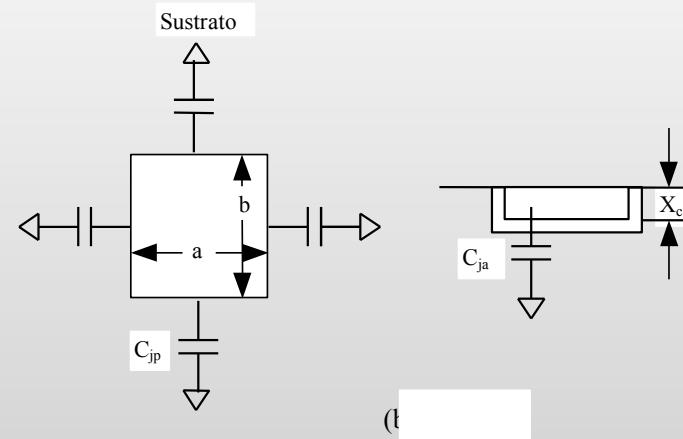


C_{ja} : Capacitancia de juntura por μm^2

C_{jp} : Capacitancia periférica por μm

a : Ancho de la región de difusión [μm]

b : Longitud de la región de difusión [μm]

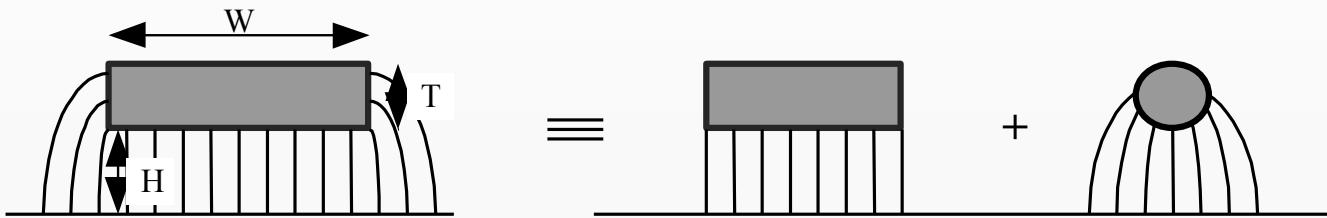


RESUMEN - CAPACITANCIAS

CAPACITANCIAS			
Parámetro	Corte	Lineal	Saturado
C_{gb}	$\frac{\epsilon \cdot A}{T_{ox}}$	0	0
C_{gs}	0	$\frac{e \cdot A}{2 T_{ox}}$	$\frac{2e \cdot A}{3 T_{ox}}$
C_{gd}	0	$\frac{e \cdot A}{2 T_{ox}}$	0 (finita para dispositivos de canal corto)
$C_g = C_{gb} + C_{gs} + C_{gd}$	$\frac{e \cdot A}{T_{ox}}$	$\frac{e \cdot A}{T_{ox}}$	$\frac{2e \cdot A}{3 T_{ox}} \rightarrow \frac{0.9e \cdot A}{3 T_{ox}}$



CAPACITANCIAS DE LINEA



$$C = \epsilon \cdot \left[\frac{W \cdot \frac{T}{2}}{H} + \frac{2 \cdot p}{\ln \left(1 + \frac{2 \cdot H}{T} + \sqrt{\frac{2 \cdot H}{T} \left[\frac{2 \cdot H}{T} + 2 \right]} \right)} \right]$$

W : Ancho del conductor

H : Espesor del aislante

T : Espesor del conductor

ϵ : Permitividad del aislante

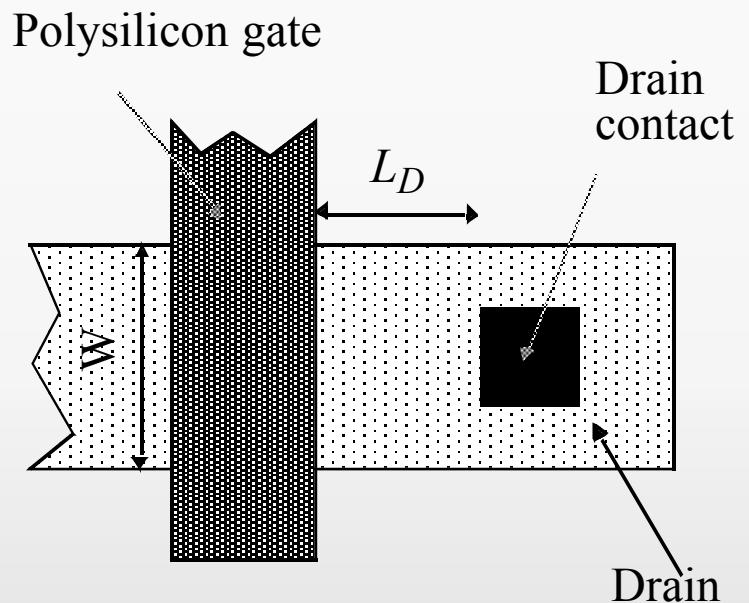
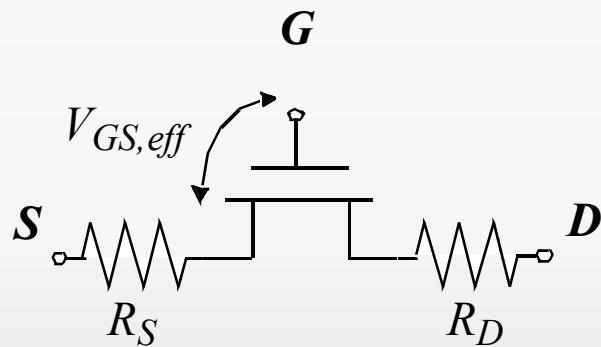


VALORES TÍPICOS DE CAPACITANCIA

CAPAS	C
GATE-SUSTRATO	860 $\mu\text{F}/\text{m}^2$
POLISILICIO-SUSTRATO	36 $\mu\text{F}/\text{m}^2$
METAL-SUSTRATO	19 $\mu\text{F}/\text{m}^2$
METAL-n ⁺	30 $\mu\text{F}/\text{m}^2$
METAL-p ⁺	33 $\mu\text{F}/\text{m}^2$
METAL-POLISILICIO	35 $\mu\text{F}/\text{m}^2$
METAL2-SUSTRATO	17 $\mu\text{F}/\text{m}^2$
METAL2-n ⁺	17 $\mu\text{F}/\text{m}^2$
METAL2-p ⁺	17 $\mu\text{F}/\text{m}^2$
METAL2-POLISILICIO	18 $\mu\text{F}/\text{m}^2$
METAL2-METAL1	36 $\mu\text{F}/\text{m}^2$

Capacitancias típicas de transistores MOS.

RESISTENCIA PARÁSITAS



SPICE MODELS

Level 1: Long Channel Equations - Very Simple

Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations

Level 3: Semi-Emperical - Based on curve fitting to measured devices

Level 4 (BSIM): Emperical - Simple and Popular



PRINCIPALES PARAMETROS SPICE PARA EL MOSFET

Parameter Name	Symbol	SPICE Name	Units	Default Value
SPICE Model Index		LEVEL	-	1
Zero-Bias Threshold Voltage	VT0	VT0	V	0
Process Transconductance	k'	KP	A/V ²	2.E-5
Body-Bias Parameter	g	GAMMA	V0.5	0
Channel Modulation	l	LAMBDA	1/V	0
Oxide Thickness	tox	TOX	m	1.0E-7
Lateral Diffusion	xd	LD	m	0
Metallurgical Junction Depth	xj	XJ	m	0
Surface Inversion Potential	2 ff	PHI	V	0.6
Substrate Doping	NA,ND	NSUB	cm ⁻³	0
Surface State Density	Qss/q	NSS	cm ⁻³	0
Fast Surface State Density		NFS	cm ⁻³	0
Total Channel Charge Coefficient		NEFF	-	1
Type of Gate Material		TPG	-	1
Surface Mobility	m0	U0	cm ² /V·sec	600
Maximum Drift Velocity	umax	VMAX	m/s	0
Mobility Critical Field	xcrit	UCRIT	V/cm	1.0E4
Critical Field Exponent in Mobility Degradation		UEXP	-	0
Transverse Field Exponent (mobility)		UTRA	-	0



SPICE PARÁMETROS PARÁSITOS

Parameter Name	Symbol	SPICE Name	Units	Default Value
Source resistance	R_S	RS	Ω	0
Drain resistance	R_D	RD	Ω	0
Sheet resistance (Source/Drain)	R_o	RSH	Ω/\circ	0
Zero Bias Bulk Junction Cap	C_{j0}	CJ	F/m^2	0
Bulk Junction Grading Coeff.	m	MJ	-	0.5
Zero Bias Side Wall Junction Cap	C_{jsw0}	CJSW	F/m	0
Side Wall Grading Coeff.	m_{sw}	MJSW	-	0.3
Gate-Bulk Overlap Capacitance	C_{gb0}	CGBO	F/m	0
Gate-Source Overlap Capacitance	C_{gs0}	CGSO	F/m	0
Gate-Drain Overlap Capacitance	C_{gd0}	CGDO	F/m	0
Bulk Junction Leakage Current	I_S	IS	A	0
Bulk Junction Leakage Current Density	J_S	JS	A/m^2	1E-8
Bulk Junction Potential	ϕ_0	PB	V	0.8

SPICE PARAMETROS DEL TRANSISTOR

Parameter Name	Symbol	SPICE Name	Units	Default Value
Drawn Length	L	L	m	-
Effective Width	W	W	m	-
Source Area	AREA	AS	m ²	0
Drain Area	AREA	AD	m ²	0
Source Perimeter	PERIM	PS	m	0
Drain Perimeter	PERIM	PD	m	0
Squares of Source Diffusion		NRS	-	1
Squares of Drain Diffusion		NRD	-	1



EVOLUCIÓN DE LA TECNOLOGÍA

Year of Introduction	1994	1997	2000	2003	2006	2009
Channel length (μm)	0.4	0.3	0.25	0.18	0.13	0.1
Gate oxide (nm)	12	7	6	4.5	4	4
V_{DD} (V)	3.3	2.2	2.2	1.5	1.5	1.5
V_T (V)	0.7	0.7	0.7	0.6	0.6	0.6
NMOS I_{Dsat} (mA/ μm) (@ $V_{GS} = V_{DD}$)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{Dsat} (mA/ μm) (@ $V_{GS} = V_{DD}$)	0.16	0.11	0.14	0.09	0.13	0.16

TEMA DE TRABAJO

- PROBLEMAS DE CIRCUITOS
MICROELECTRONICOS – SEDRA/
SMITH
 - Cuarta Edición
- CAP 5: 9,10 y 11



TEMA DE TRABAJO

- MODELOS DEL MOSFET
 - NIVEL 1
 - NIVEL 2
 - NIVEL 3
 - BSIM

