A HIGHLY FLEXIBLE SEA-OF-GATES STRUCTURE FOR DIGITAL AND ANALOG APPLICATIONS

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Abstract

This paper describes a new sea of gates structure, usable for digital random logic, regular arrays, and analog cells. A dedicated design procedure features a full cell-abutment capability, together with channelless routing. Design results are presented for several macroblocs, and compared with other semi-custom approaches .
A set of rules is finally presented, which allows an automatic transformation of the sea of gates layout into a topologically equivalent full custom layout, converting semi-custom prototypes to full performance circuits.

1. Introduction

Gate arrays, including sea of gates, covers roughly 50% of the ASIC's market. The key of this success holds in their ability to fulfill two basic requirements for prototypes and small series, i.e. fast turn-over time and low cost. However, this design style suffers from severe limitations. It is usually inapplicable when digital modules (registers, ALU,...), repetitive circuits (RAM, PLA, ...) and analog cells (amplifiers, A/D or D/A converters,..) should be mixed on the same chip. Moreover, it is hardly suited to a mass production where high density, full performance circuits are required.
Reducing the gap between those conflicting requirements is the objective of the sea of gates structure and the layout philosophy presented in this paper.

2. Basic philosophy at the origin of the new structure

Besides the basic limitations of classical gate arrays described hereabove, its advantages of short delay and low cost are generally obtained at the expense of poor performance in speed and area. To deal with those problems, the following objectives have been defined for the development of the new array :

-high packing density for random digital circuits, based on the following means : suppression of routing channels, cell abutment, and use of arbitrary complex cells, dynamically generated from functional specifications. The use of a static standard cell library is prohibited.
-efficient implementation of regular circuits (RAM, PLA,...), through the definition of an optimized array
-use of the same array for analog circuits, by respecting a high level of symmetry, together with other special features described hereafter
-compatibility with existing layout generation algorithms, providing easy design automation.
-possibility to automatically transform a sea of gates layout into a full custom circuit by developing an appropriate set of rules. The resulting layout is, of course, much more compact and efficient. Moreover, its topological equivalence with the sea of gates layout guarantees its functional correctness (under the assumption that the sea of gates layout was tested and validated).

The target technology is a classical two metals CMOS technology.

3. Description of the sea of gates array

The micro-architecture is shown on figure 1. Its main characteristics are :

- absence of pre-defined channels (sea of gates concept [1]), because no routing channels will be needed
- use of the gate isolation technique [2], giving surface advantages and greater flexibility in the cell design
- the N versus P transistor numbers ratio is 2. This optimizes the density of repetitive circuits, without disturbing random logic density.
- the doubling of the gate contacts improves the internal routability
- the unalignment of transistor gates results from technological reasons (no metal 1 -metal 2 via is permitted over the gate)
- the P and N transistor size ratio equals the carriers mobility ratio.

Except for some regular circuits, the use of both levels of metal is rigorous and systematic. This helps achieving a full transparence of cells in both directions, which is a necessary condition for suppressing routing channels. Metal 1 is routed vertically (parallel to polysilicium) and metal 2 horizontally (parallel to diffusion). This choice minimizes the number of contacts as well as the area. Power supplies are distributed with the second level of metal.

4. Applications

4.1 Random logic

In the case of static CMOS logic, only one of the two N-diffusion strips is used, and the numbers of P and N devices become equal. The area of the unused diffusion strip is then available for routing. Dynamic logic can also be implemented : in this case the two N-diffusions can be used for surface reduction.

Cell abutment is possible because the four necessary conditions are fulfilled, i.e. : trough-cell routing in both directions, choice of the cell shape, choice of the connectors location, and stretching.

Horizontal through-cell routing is allowed by transparency of the cells. 11 horizontal tracks are supplied on one core cell height, which is enough in most cases. Vertical routing is also feasible. If a vertical track is already occupied, shifting the transistors one step to the right will free the track for routing. Concerning the shape, one can first design a cell with the minimum height, and later fold it like a S to make it higher and thinner. Finally, because of the total freedom of the routing, any internal node can be wired to any cell edge without difficulty. Cell stretching is obvious. The conclusion is that abutment makes no problem, and that very few channels are needed. In fact a channel is required only when the number of free horizontal tracks is too small. Experience has shown that it was quite rare. Big modules up to a few hundred transistors were designed without the need of routing channels.

Another interesting feature is the natural application of existing layout generation algorithms to the new structure. Two examples are the Uehara-Van Cleemput algorithm for complex gates layout [3], and the GRAPES module generator [4].

4.2 Regular circuits

The continuity of the structure and the difference between the N and P transistor count yield relatively high densities for the implementation of regular circuits (RAM, ROM, PLA, ...). As a matter of fact, for electrical reasons, the number of N transistors is usually greater than the number of P devices in these circuits. Unlike many gate-arrays [5], the same core cell is used for random logic and regular circuits. This suppresses all constraints on the type, size, and situation of these circuits.

Figure 2 presents a RAM cell layout. It should be noticed that occupation rate is optimum, all available transistors being used.

4.3 Analog cells

The array naturally presents a "comb" structure, the one most used in analog layouts. It also promotes a symmetrical layout design. Mirroring of successive core cells allows the gathering of two or four identical diffusions for the implementation of big structures, as differential pairs, on a restricted area. Programmable structures on the chip periphery can be transformed into digital output buffers, or into big analog transistors. Finally, polysilicium deposit under I/O pads provides capacitances under unused pads. Figure 3 shows an OTA (operational transconductance amplifier) layout designed on the sea of gates structure. As for random logic, the adaptation of an existing analog layout generator [6] is planned.

5. Sea of gates to full custom transformation

Decomposing the sea of gates layout into elementary components (transistors, contacts, wires) and applying to these the transformation rules given on figure 4, produces a single-metal symbolic full custom layout, topologically equivalent to the sea of gates layout. After compaction, the area is very close to a handcrafted layout.

6. Results

Table 1 gives comparative surfaces of different cells implemented with several full- and semi- custom design styles. Surface reference is the handcrafted full custom, fixed at 100 %. Figure 5 shows compared layouts of a 4-bits carry-lookahead adder.

One can see that the use of the sea of gates structure yields very small surfaces compared to classical gate arrays and standard cells. This is due to the suppression of routing channels, and the use of a lower number of more complex cells. The full custom layout derived from the sea of gates gives similar densities to those of handcrafted layouts.

7. Conclusion

A new sea of gates structure has been presented. Combined with the systematic use of the two levels of metal inside and outside the cells, it offers several advantages :

- high packing density for random logic, due to the suppression of routing channels and the use of complex cells
- easy implementation of repetitive circuits and analog cells
- design automation (compatibility with existing algorithms)
- possibility of transforming the sea of gates layout into a compact full custom layout

References

[1] A. HUI et al., "A 4.1K Gates Double Metal HCMOS Sea of Gates Array"
Proc. CICC 1985, Portland, May 1985, pp15-17

[2] I. OHKURA et al., "Gate Isolation - A Novel Basic Cell Configuration for CMOS Gate Arrays"
Proc. CICC 1982, May 1982, pp 307-310

[3] T. UEHARA, W. VAN CLEEMPUT, "Optimal Layout of CMOS Functional Arrays"
IEEE Trans. on computers, vol. C-30, No 5, 1981

[4] H. HEEB, W. FICHTNER, "GRAPES : A Module Generator Based on Graph Planarity"
Proc. ICCAD 1987, Santa Clara, Nov. 87, p 428

[5] T. CHAN et al., "Advanced Structured Arrays Combine High Density Memories with Channel-free Logic Array"
Proc. CICC 1987, May 1987, pp 39-43

[6] M. KAYAL, S. PIGUET, M. DECLERCQ, B. HOCHET, "SALIM : A Layout Generation Tool for Analog IC"
Proc. CICC 88, Rochester, May 1988

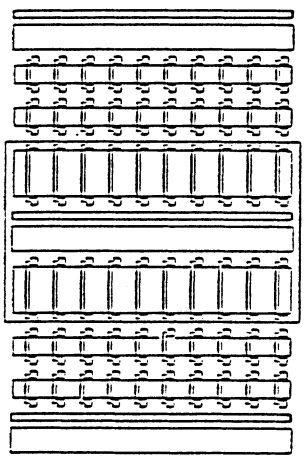

Fig. 1 : Basic cell layout

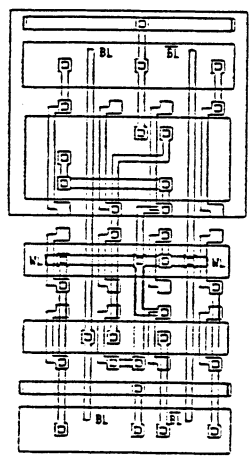

Fig. 2 : Static RAM cell layout

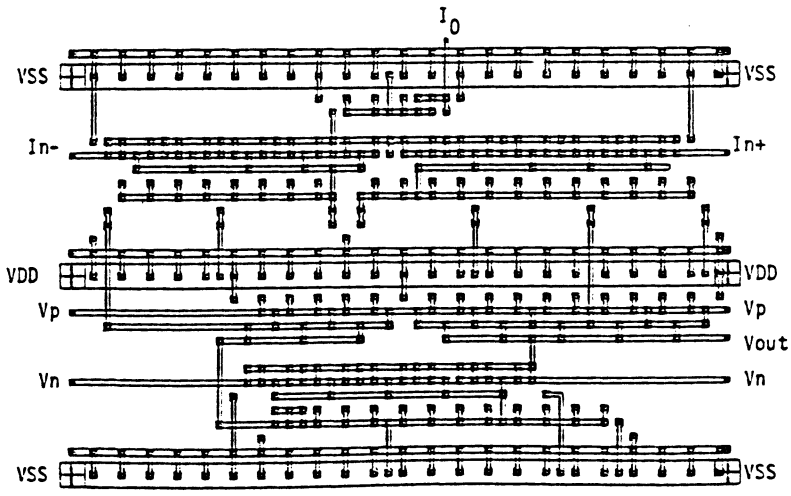

Fig. 3 : OTA layout (metal customization only)

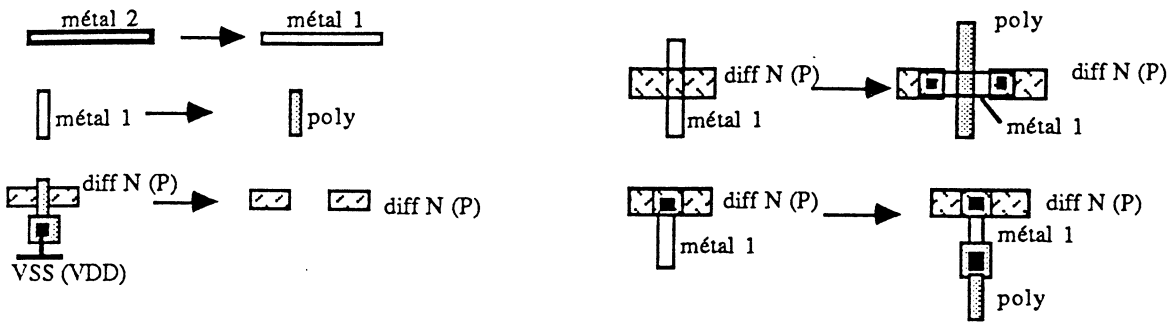

Fig. 4 : Sea of gates to full-custom transformation rules

	Full custom design	Sea of gates design	Gate Array design	Standard cell design	Full custom derived from sea of gates
Carry lookahead adder	100 %	213 %	261 %	249 %	107 %
Synchronous counter	100 %	182 %	258 %	229 %	119 %
Parallel multiplier	100 %	193 %	271 %	217 %	107 %
LIFO stack	100 %	219 %	-	243 %	111 %

Table 1 : Surface comparison for different methodologies

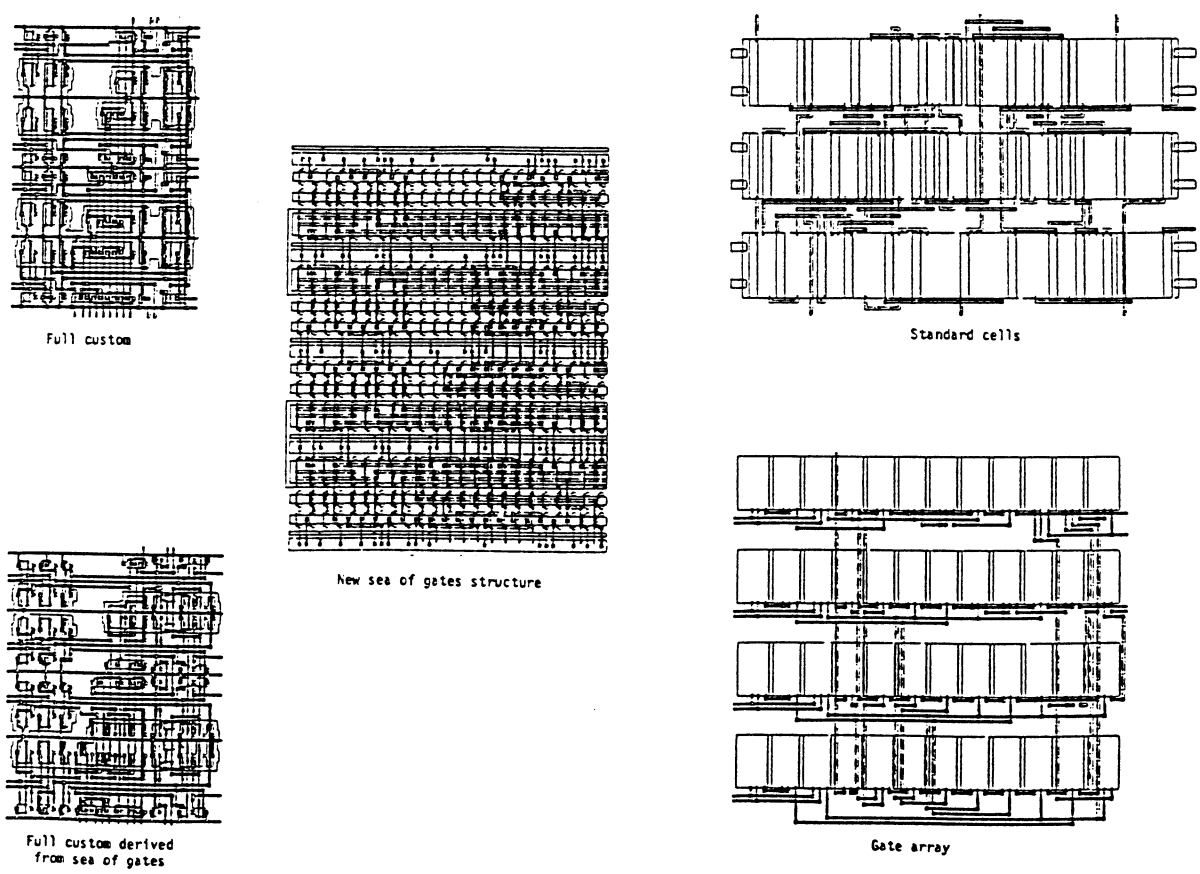

Fig. 5 : Compared layouts of a 4 bits carry-lookahead adder