10K GATE GaAs JFET SEA OF GATE

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ABSTRACT

The first GaAs 10K gate sea of gate has been successfully fabricated using JFETs with a gate length of 0.5μm. A basic cell is designed to constitute both DCFL 4-NOR circuit and SCFL inverter circuit with the identical enhancement-type JFET. Each input and output level is designed to be compatible to Si ECL, CMOS, and TTL logic levels. Unloaded and loaded DCFL gate delay are 21psec/gate and 180psec/gate with power consumption of 0.4mW/gate and 0.5mW/gate, respectively. The toggle frequency of T-type flip-flop is obtained to be 3.9GHz and 4.4GHz for DCFL and SCFL, respectively.

INTRODUCTION

GaAs integrated circuits have already been attained to large-scale integration and applied to ASICs (Application Specific Integrated Circuits). From the practical point of view,however, it is very important to realize large-scale and high-speed ASICs within the limit of realistic power consumption. Although some GaAs gate array have been reported [1]-[6], channel-less type gate array (sea of gate) using GaAs devices have not been reported yet. A sea of gate is advantageous to GaAs because chip size is smaller than a conventional gate array, which contributes to high yield and high-speed performance

In this paper, we will discuss the basic performance of 10K gate GaAs JFET sea of gate. The GaAs JFET has high driving capability, large logic swing capability, and large noise margins in DCFL circuit which is adequate for low-power consumption ICs. GaAs JFET sea of gate is demonstrated to be a high performance of GaAs ASIC.

FABRICATION

The sea of gate ICs were fabricated on a semi-insulating 3-inch undoped LEC GaAs substrate using conventional optical lithography. A p-layer was buried underneath the channel of the JFET by Mg+ implantation with 220KeV to surpress the short channel effects (BP-JFET) [7]. The n-channel and n+ ohmic contact region of the BP-JFET and resistors for DCFL and SCFL circuits were formed by Si ion implantation with subsequent capless annealing technique. The p+ gate was formed by a selective Zn diffusion at 600°C using the open-tube diffusion system with DEZ (Diethyl-Zinc). The threshold voltage for the JFET can be precisely determined by the diffusion time. A gate length of 0.5μm was delineated for the JFET by using a sidewall assisted technique. Transconductance of 400mS/mm was typically obtained at the threshold voltage of +0.2V.

Three levels interconnecting lines were used in the sea of gate.

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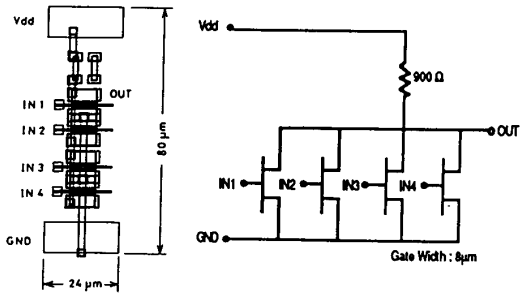
The minimum line/space width are 2μm/2μm. The minimum size of via-hole are 2μm square for the contact between ohmic metal and 1st interconnecting metal, and 1.5μm square for the contact among three level interconnecting metals.

CELL DESIGN AND LAYOUT

The basic cell is composed of 4 FETs with the gate width of 8μm, 2 different resistors, and power lines of Vdd and GND. The layout of DCFL 4-NOR gate and its equivalent schematic are shown in Fig.1(a) and Fig.1(b), respectively. The basic cell has an area of 24μm x 80μm. The load resistance for DCFL circuits is selected to be 900ohm in order to achieve a power consumption of less than 0.5mW/gate at Vdd of 1.0V and a noise margin of more than 150mV with the minimum gate delay. The layout of SCFL inverter gate and its equivalent schematic circuit are also shown in Fig.2(a) and Fig.2(b), respectively. SCFL circuit has power lines of Vss and Vcs, which are constructed on the basic cells, in addition to the established power lines. The SCFL inverter cell has an area of 96μm x 160μm. The load resistance for SCFL circuits is selected to be 750ohm.

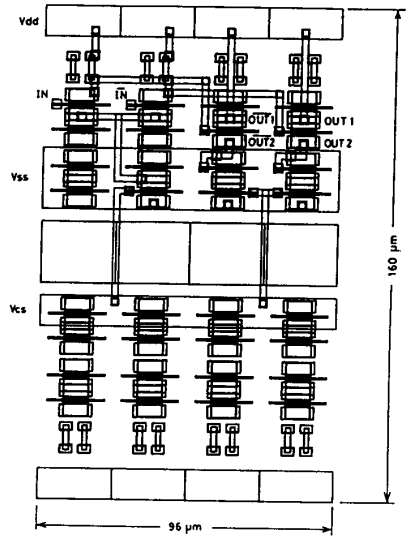
I/O DESIGN AND LAYOUT

The input and output buffers are designed to be compatible to Si ECL, CMOS, TTL, and internal GaAs JFET DCFL logic levels. Each input buffer is designed to operate with a single-phase signal. A source-follower circuit was adopted in the final stage of the output buffer for ECL level to drive the 50ohm line. Each input and output buffers which is allowed to use mixed I/O levels simultaneously can be established voluntarily at the periphery of the

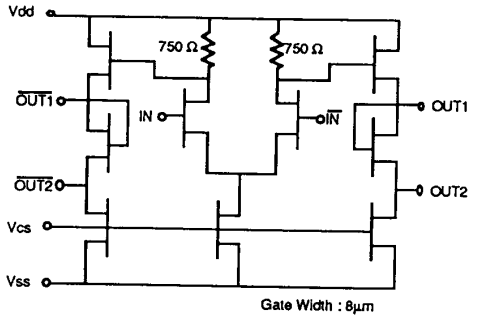


(a) (b)

Fig.1. (a) Layout and (b) Equivalent schematic circuit of DCFL 4-NOR gate



(a)



(b)

Fig.2. (a) Layout and (b) Equivalent schematic circuit of SCFL inverter gate

chip. The I/O buffers has dimensions of 240μm x 480μm.

CHIP CONSTRUCTION

Four different types of sea of gate ICs which are summarized in Table.1 are provided in order to correspond to the scale of circuit required. Fig.3 shows the microphotograph of the JFET 10K sea of gate, which consists of 11880 basic cells and 80 I/O cells. The chip size is acheived to be as small as 6.24mm x 6.24mm, which is effective to reduce the average wiring length and consequently to improve the maximum operating speed.

The standard voltage of power supply are 1.0V for Vdd for DCFL circuits. Both -4.0V for Vss and -3.0V for Vcs are needed for SCFL circuits and ECL I/O buffers. If either CMOS or TTL I/O is required, +5.0V supply has to be added. These power supply pads are placed at all the corners of the chip and power supply lines surround the internal array.

PERFORMANCE

The basic performance of an internal gate was evaluated with various kinds of ring oscillators arranged on the 10K gate chip and test element groups. The unloaded gate delay of the internal DCFL gate is 21psec/gate with power consumption of 0.4mW/gate. The delay time versus gate loading conditions are shown in Fig.4. Increase of the delay time on the fan-in and fan-out are 6.0psec/fan-in and 15.4psec/fan-out, respectively. Increase of the delay due to the load capacitance was 83psec/100fF. The loaded DCFL gate delay of 180psec/gate is obtained under the loading condition of fan-in/fan-out=3/3 and wiring length of 2mm, with consuming power of 0.5mW

Array Size	50	1K	3K	10K
Total Gate (DCFL)	60	1440	3600	11880
(SCFL)	6	180	450	1485
I/O Cells	6	28	44	80
Total Pads	36	80	112	192
Chip Size [mm x mm]	1.68x1.44	2.88x2.88	3.84x3.84	6.24x6.24

Table.1. Gate Array Statistics

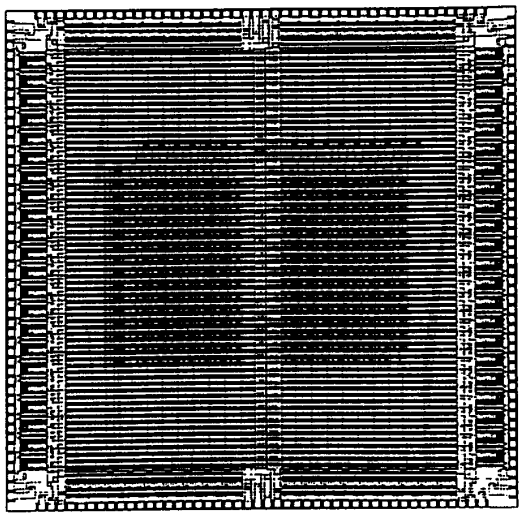


Fig.3. Microphotograph of GaAs JFET 10k sea of gate

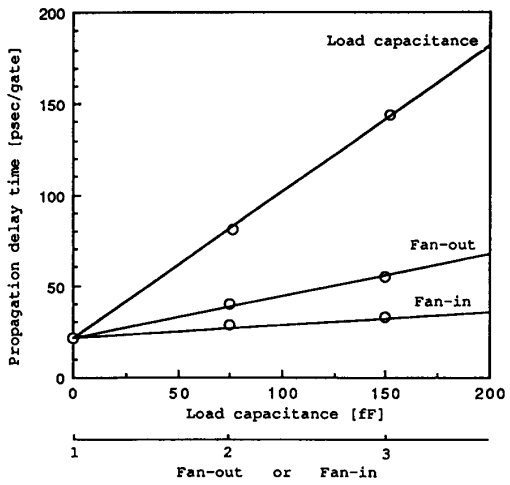


Fig.4. DCFL gate delay time versus gate loading condition

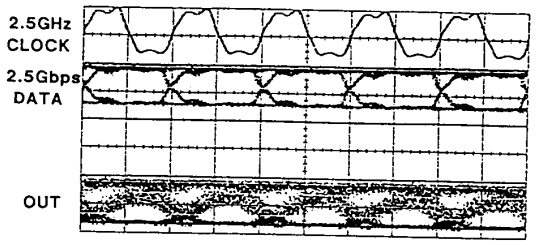


Fig.5. Input and output waveforms of SCFL D-type flip-flop at the input data rate of 2.5Gbps of 2^{23}-1 PRBS

/gate. The basic delay of the internal SCFL gate is 46psec/gate.

The maximum operating frequency for DCFL T-type flip-flop which has the DCFL input and output buffers was obtained to be 3.9GHz.

SCFL T-type flip-flop which has ECL input and output buffers was measured and operated at maximum operating frequency of 4.4GHz.

SCFL D-type flip-flop was also evaluated and operated in error free at the input data rate of 2.5Gbps of 2^{23}-1 PRBS. Fig.5 shows the input and output waveforms of the SCFL D-type flip-flop.

16x16-bit parallel multiplier was arranged on the 10K gate chip. The multiplier applies the carry-save-adder array algorithm and consists of 224 full-adder cells, 16 half-adder cells, and input resister blocks. The multiplication time was obtained to be 10.1nsec for the critical path of the multiplier.

CONCLUSION

The first GaAs 10K gate sea of gate with Si ECL, TTL, and CMOS compatible terminals has been fabricated using a JFET with a gate length of 0.5μm. The basic cell is designed to constitute both DCFL and SCFL circuits with the identical enhancement-type JFET. The loaded DCFL gate delay is obtained to be 180 psec/gate with the power consumption of 0.5mW/gate. The applicability of GaAs JFET and its technology to high speed and large scale integration is confirmed.

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