Advanced Analog Circuit Design on a Digital Sea-of-Gates Array

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Abstract

High performance analog circuits have been realised on a purely digital Sea-of-Gates Array: an 8 bit weighted current DA-converter (typical INL of 0.2 LSB) and a class AB Opamp that has a quiescent supply current of only 23 μA, and that can drive 3.4 V_{pp} into a 1 kΩ load with a THD < 0.1 % (5 V supply). Dedicated CAD tools have been developed for a fast and reliable layout of the analog circuitry on the SOG array.

I. Introduction

Gate Arrays provide an interesting alternative for full-custom designs, in case small to medium quantities of chips are required, or in case the time-to-market is critical. Most Gate Arrays require only four customized masks (two masks for the metal layers, one mask for the contacts and one mask for the vias). Consequently, the layout process will take less time and, together with the reduced mask costs, this may result in a considerable cost advantage over full-custom solutions. Usual Gate Array applications are in the field of digital circuitry, but in view of the clear economical advantages of Gate Arrays, there is a growing interest for the realisation of mixed-mode or even purely analog ICs on Gate Arrays.

Good analog circuit performance on Gate Arrays has already been reported [1,2], but the employed Gate Arrays all had special dedicated parts for analog design. For many applications, this means a loss of flexibility and an inefficient use of the available chip area. This paper discusses the design and implementation of analog circuits on a conventional digital Sea-of-Gates (SOG) array [3]. The SOG structure does not contain any special parts for analog applications. It will be shown that, in spite of this absence of dedicated analog parts, the realisation of high performance analog circuits is very well possible.

Section II gives a short overview of the employed SOG structure. The CAD tools that were developed for a fast and reliable layout of analog circuitry on the SOG array are discussed in section III. Section IV presents two advanced analog circuits that were succesfully implemented on the SOG array. The first circuit is a linear 8 bit weighted current DA-converter, that has an active area of 0.6 mm^2, an average supply current of 150 μA, and a settling time of 2 μs. The second circuit is a class AB Opamp with rail-to-rail output swing, that can operate at supply voltages of down to 2.0 V and that has a quiescent supply current of only 23 μA.

II. Sea-of-Gates structure

The employed SOG array has already been presented in [3]. The main features are:

- n/p transistor count ratio of 2
- transistor dimensions: W_p/L_p= 26μm/2μm; W_n/L_n=10μm/2μm
- 2 μm n-well CMOS technology with two metal layers and a single poly-silicon layer

Fig. 1 shows a small part of the SOG core. The total SOG core consists of 38 rows each containing 255 basic cells with 1 p-MOS and 2 n-MOS transistors.

A large variety in transistor dimensions, necessary for analog applications, can be obtained by connecting unit transistors in parallel and in series. Resistors are realized by chaining poly-silicon gates. The poly gate of 1 unit p-MOST represents about 450 Ω, the poly gate of 1 unit n-MOST about 200 Ω. Metal1/metal2 capacitors (46 pF/mm^2) are used in case small capacitances are needed. Electrical isolation between (sub)blocks is obtained using the gate isolation concept (the gates of adjacent unit transistors are connected to the appropriate power lines).

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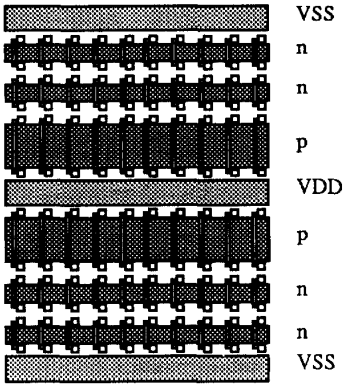

Fig. 1 Part of the SOG core

III. CAD tools : basic building block generators and verification procedures

Advanced analog circuits may require over 1000 unit transistors when implemented on the SOG array. Obviously, doing the layout of such a circuit by hand is a very time consuming and tedious job, and errors are almost inevitable. In order to speed up the layout process, generators for the following analog building blocks have been developed: compound transistors, current mirrors and differential pairs.

The input parameters for the generators can be subdivided into dimensional and architectural parameters. The dimensional parameters specify the compound transistor dimensions, the architectural parameters determine how many rows of either n or p transistors are to be used, and whether the building blocks should be isolated (gate isolation) from adjacent blocks.

Various layout architectures for current mirrors and differential pairs have been tested. The layout architecture chosen for the generators (Fig. 2) has good matching properties and can be implemented in a very efficient way without wasting gates due to isolation or routing. Each block in Fig. 2 represents a certain number n of unit transistors connected in series. The dark blocks form together one compound transistor of the current mirror or differential pair, the light blocks the other compound transistor. In Fig. 2 both compound transistors consist of five parallel branches of n unit transistors connected in series. The arrows indicate the direction of the current flow.

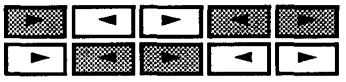

Fig. 2 Architecture of current mirrors and differential pairs

Layout verification is done at compound transistor level. The compound transistors are extracted from the layout and their dimensions are calculated and compared with the dimensions in the schematic. Distributed resistors, for example poly-silicon gate resistors, are reduced to lumped resistors and their values are calculated and compared with the schematic values. Isolation transistors and unconnected transistors are skipped from the layout before verification. Fig. 3 shows the complete verification procedure.

The Falcon Framework environment of Mentor Graphics [4] has been used for the implementation of the generators and the verification procedures.

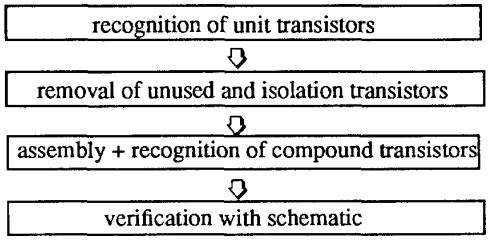

Fig. 3 Verification procedure

IV. High-performance analog circuits on the SOG array

Using the CAD Tools presented in the previous section, an analog cell library for the SOG array has been developed. The library consists of various conventional two stage CMOS Opamps (offset voltages < 3 mV, unity gain-bandwidth > 2 MHz), a folded cascode Opamp, fast comparators (100 ns response time), a relaxation oscillator, a bandgap voltage reference, an 8 bit weighted current DA-converter and a low power class AB Opamp with rail-to-rail output swing. The latter two circuits are presented hereafter.

IV.1 8 bit DA-converter

Fig. 4 shows the block diagram of the 8 bit binary weighted current DAC. In fact, the DAC simply consists of a (cascoded) current mirror with one input branch and

8 selectable binary weighted output branches. The converter was split into two submodules in order to limit the area and power consumption [5]. The currents of the 3 bit DAC-submodule are scaled down by an 8:1 current divider that is built from two cascoded current mirrors. Fig. 5 shows the schematics of the input branch and of the 3 bit DAC-submodule. Fig. 6 shows the bit selection circuit (bsc).

The nonlinearity of the weighted current DAC is determined by the mismatch among the various bit branches. Following the design methodology outlined in [6], the dimensions and biasing for the compound transistors that form the various bit branches were chosen. An effective L of 14 µm and an effective W of 10 µm were chosen for the lower compound transistor in the LSB branch. The MSB branch consists of 16 of these LSB branches connected in parallel. A bias current of 4.5 µA

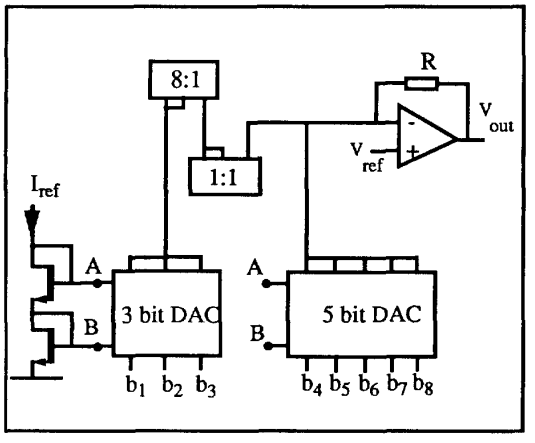

Fig. 4 8 bit binary weighted current DA-converter

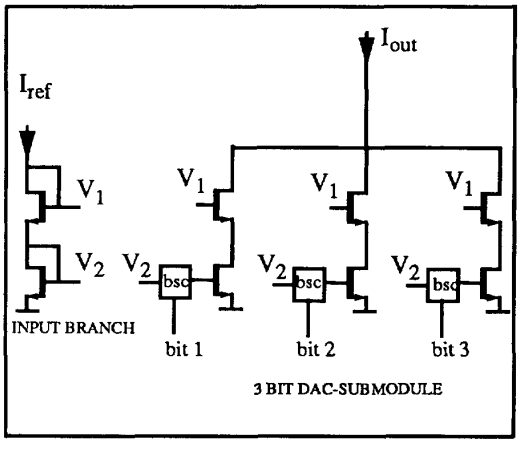

Fig. 5 Input branch and 3 bit DAC-submodule

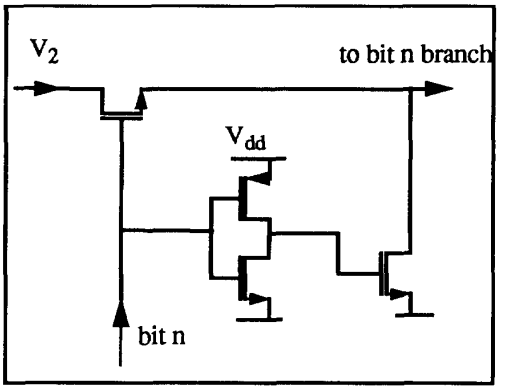

Fig. 6 Bit selection circuit

was chosen for the LSB branch. A typical integral nonlinearity (INL) of ± 0.2 LSB resulted. The good linearity of the DAC clearly demonstrates that the matching properties of the SOG structure are excellent (a linear 10 bit DAC seems possible). Table 1 shows the experimental results for the 8 bit DAC. The SOG implementation of the DAC required 576 unit transistors. Without output buffer, the cell area is only 0.4 mm^2. The settling time is mainly determined by the value of I_{ref} (36 µA). By enlarging I_{ref} (and the input branch) the settling time can be reduced.

Table 1: Measurement results 8 bit DAC

Supply voltage : 5 V
Integral nonlinearity (typical) : 0.2 LSB
Average supply current : 150 µA
Settling time : < 2 µs
Output voltage range : 1.9-3.8 V
Active layout area including output buffer : 0.6 mm^2

IV.2 Class AB Opamp with rail-to-rail output swing

Conventional two-stage CMOS Opamps are not suitable if large capacitive and/or resistive loads have to be handled, and a low standby current consumption is required. In that case an Opamp with a class AB output stage, preferably with rail-to-rail capability, is required. Such an Opamp, based on [7], was successfully realised on the SOG array.

Fig. 7 shows the schematic of the Opamp. In the output stage a complementary source-follower stage (transistors M3-M6) is combined with a so-called pseudo-source follower (PSF) stage. The latter stage consists of two complementary common source MOSTs, each driven by an error amplifier in a feedback loop. When the Opamp is operating in or near standby, the complementary source follower can provide the relatively small output currents. The PSF is inactive due to intentionally built-in offset voltages in the error amplifiers. The large output transistors M1 and M2 are turned off (zero current) and the quiescent current in the output stage is well controlled by transistors M3-M6. The PSF stage becomes active as soon as larger output currents are needed. The complementary source follower provides a direct feedforward path to the output, and consequently reduces the excess phase shift at higher frequencies caused by the slow PSF.

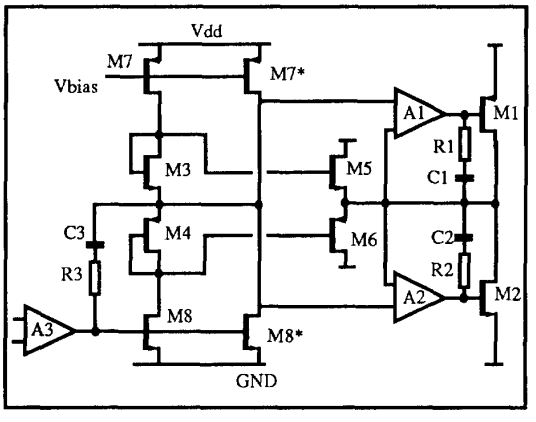

Fig.7 Class AB Opamp that was realised on the SOG array, after [7]

The amplifiers A1, A2 and A3 in the schematic of fig. 7 are all simple differential stages with a current mirror load. R_1-C_1, R_2-C_2 and R_3-C_3 are compensation networks needed for a stable operation of the three amplifiers.

In our case, the application of the Opamp dictated a very low quiescent current consumption (< 25 µA), in combination with a maximum output current of more than 1 mA. In order to ensure the stability of the Opamp in case of purely capacitive loads, the Beta of the source-follower transistors M5 and M6 had to be chosen large ($\approx$10 mA/V^2). In this way a reasonable g_m was obtained while the quiescent output current through M5 and M6 could be kept low. The compensation capacitors C_1 (2 pF), C_2 (2 pF) and C_3 (4 pF) were realised using metal1/metal2 capacitors. The layout (including verification) of this Opamp on the SOG array took not more than one day, owing to the use of the CAD tools presented in section III. An active layout area of 0.5 mm^2 resulted. Table 2 summarizes the measurement results of the class AB Opamp.

Table 2: Performance of the class AB Opamp. Unless otherwise specified, V_{supply} = 5 V, $C_L \approx$ 50 pF and R_L = infinite

DC open loop gain > 80 dB
Unity Gain-Bandwidth : 150 kHz
Supply current : 23 µA
Supply voltage > 2 V
Slew rate : rising 0.25 V/µs, falling 0.37 V/µs
Output swing (R_L = 1 kΩ) : 0.8 V - 4.2 V
THD (R_L = 1 kΩ, frequency = 1 kHz, closed loop gain of 2, output swing 0.8 V - 4.2 V) : < 0.1 %
Maximum output current (short circuit) : 12.5 mA
Phase margin (C_L = 50 pF, respectively 500 pF) : 76 degrees, respectively 27 degrees
CMRR at 10 Hz, respectively 1 kHz : 67 dB, 66 dB
PSSR(V_{dd}) at 10 Hz, respectively 1 kHz : 70 dB, 49 dB
PSSR(V_{ss}) at 10 Hz, respectively 1 kHz : 80 dB, 39 dB
Layout area : 0.5 mm^2

IV.3 Limitations for analog circuit implementation

During the design of the analog cell library it has been found that the present SOG array provides enough possibilities for the implementation of advanced analog circuits. In all cases it was possible to select a circuit schematic that could meet the desired specifications without requiring large resistance or capacitance values, and consequently the cell areas could be kept relatively small. Of course, compared to full-custom design, analog design on the SOG array has its limitations :

1) the source/drain area capacitances are rather large. The S/D area dimensions of a unit n-MOST are 14 µm x 10 µm resulting in a S/D capacitance of about

0.05 pF. The S/D area dimensions of a unit p-MOST are 14 μm x 26 μm resulting in a S/D capacitance of about 0.13 pF. Especially in those cases where transistors with large W's (i.e. several unit transistors in parallel) are required, this results in large parasitic capacitances. Consequently, the speed of SOG implementations of comparators and weighted current DACs will be lower than that of full-custom circuits. Moreover, the secondary poles of Opamps will become more important, causing a reduced phase margin.

2) it is difficult to avoid the occurence of the body effect in input differential pairs. Usually, the transistors of the input differential pair of an Opamp are placed in a seperate well. The well is tied to the sources of the input transistors, thus preventing the occurence of the body effect, which would reduce the common mode input voltage range and the gain of the Opamp. The p-MOSTs in the SOG core are positioned in rows having a large common n-well. Of course, this n-well could be tied to the sources of the two compound transistors forming the input differential pair, but this would introduce a very large parasitic capacitance to ground, causing a drastic reduction of the CMRR. Furthermore, the remaining transistors in the row would become useless.

3) realization of transistors with small W/L ratios is area-consuming, since the W/L ratios of the unit n-MOSTs and p-MOSTs are respectively 5 and 13. For instance, the realisation of a compound n-MOST with a W/L ratio of 0.1 would take 50 unit n-MOSTs in series.

4) it is not easy to realize a "clean" floating capacitor, i.e. a capacitor without a large parasitic capacitance to ground. Most multistage Opamps require a floating compensation capacitor to ensure the stability of the Opamp in case of capacitive loads. If the use of such a compensation capacitor introduces also a large capacitor to ground, this will partly cancel the stabilizing effect of the compensation capacitor. Metal1-metal2 capacitors have a parasitic capacitance to ground (substrate) that is approximately 50 % of the nominal capacitor value.

V. Conclusions

High performance analog circuits can be realised on a purely digital Sea-of-Gates Array. Two examples have been presented: an 8 bit weighted current DA-converter (typical INL of 0.2 LSB, supply current of 150 μA, 2 μs settling time), and a low power class AB Opamp (23 μA quiescent supply current, stable for purely capacitive loads of up to 500 pF, for a 1 kΩ load the output can reach the supply lines within 0.8 V, with a THD < 0.1 %). The circuit areas could be kept relatively small (0.6 mm^2, respectively 0.5 mm^2).

These results demonstrate that, for many applications, there is no need for special dedicated analog areas on a Gate Array; a conventional digital Sea-of-Gates Array, that offers the highest degree of flexibility and allows an optimal use of the available chip area, can be used.

For a fast and cost-effective layout of the analog circuits on the SOG array, dedicated CAD tools have been developed. These CAD tools are essential in order to retain one of the most important advantages of Gate Arrays, a short development time.

Acknowledgements

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