TECNICAS DE INTEGRACION

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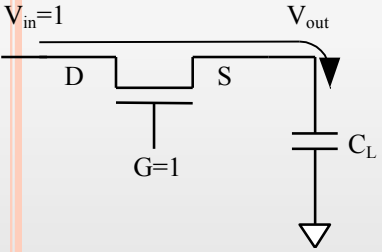
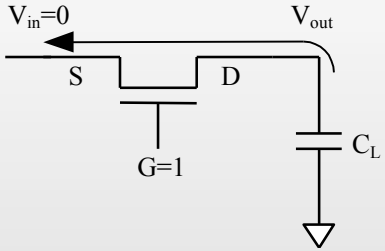
II-2013

Transistor MOS como Interruptor

nMOS

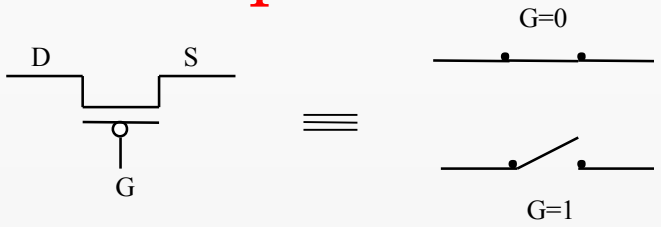


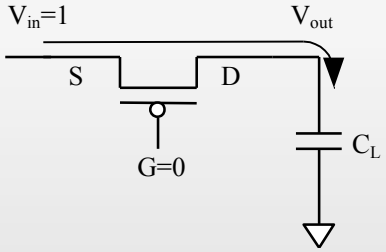
Transmisión de ‘1’



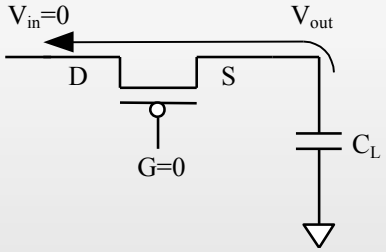
Transmisión de ‘0’

pMOS





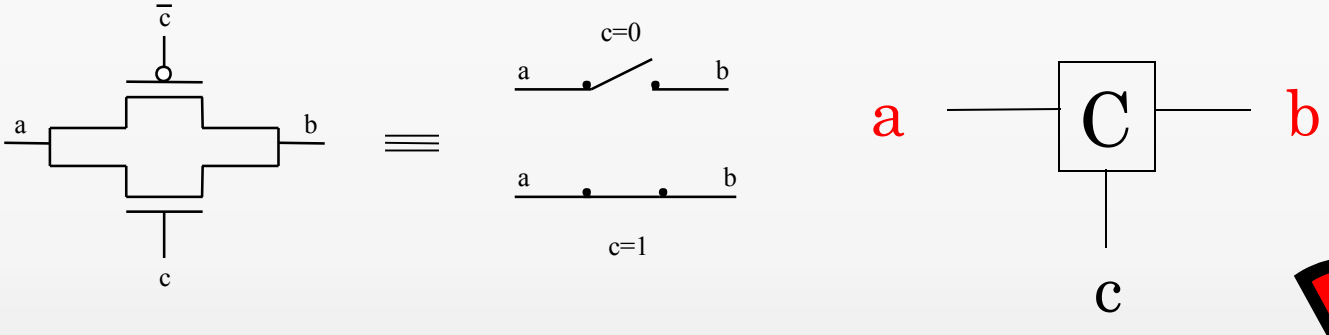
Transmisión de ‘1’



Transmisión de ‘0’

Compuerta de Transmisión

C --> NO DEGRADA NIVELES LOGICOS



nMOS DEGRADA '1' LOGICO

pMOS DEGRADA '0' LOGICO

INVERSOR CMOS

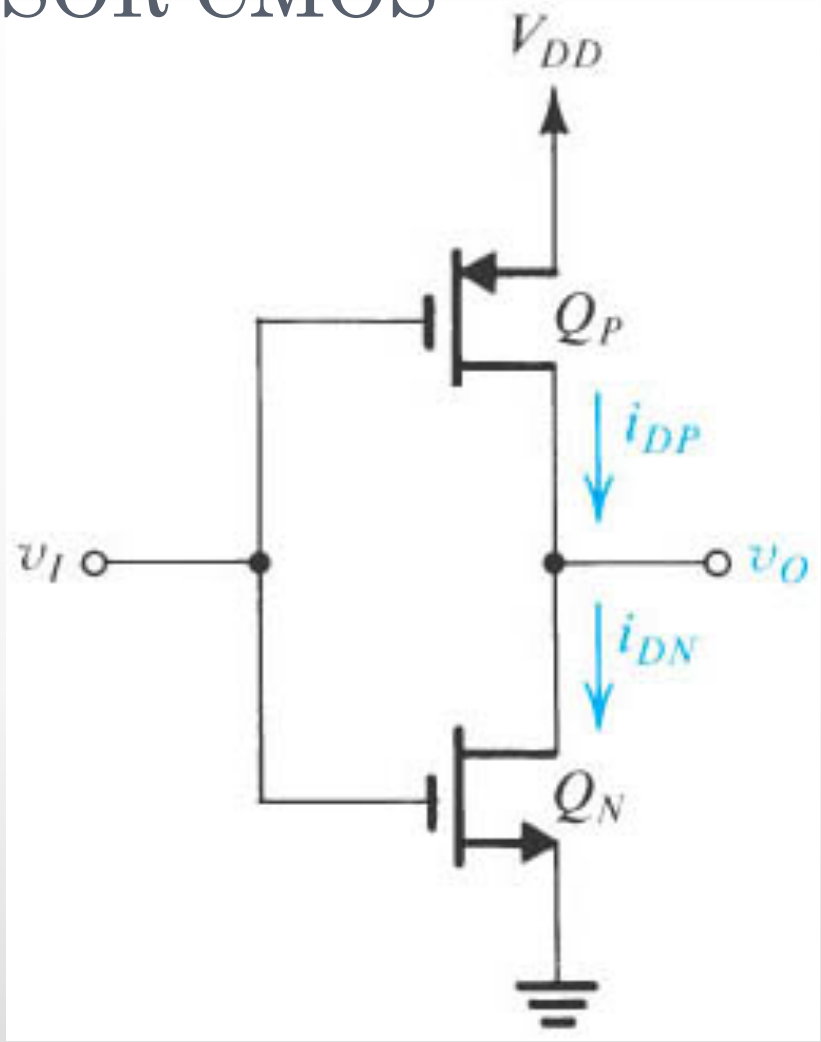
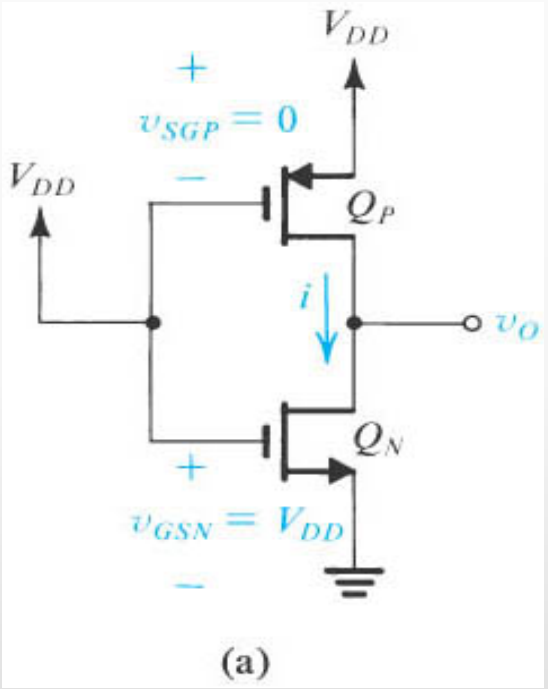
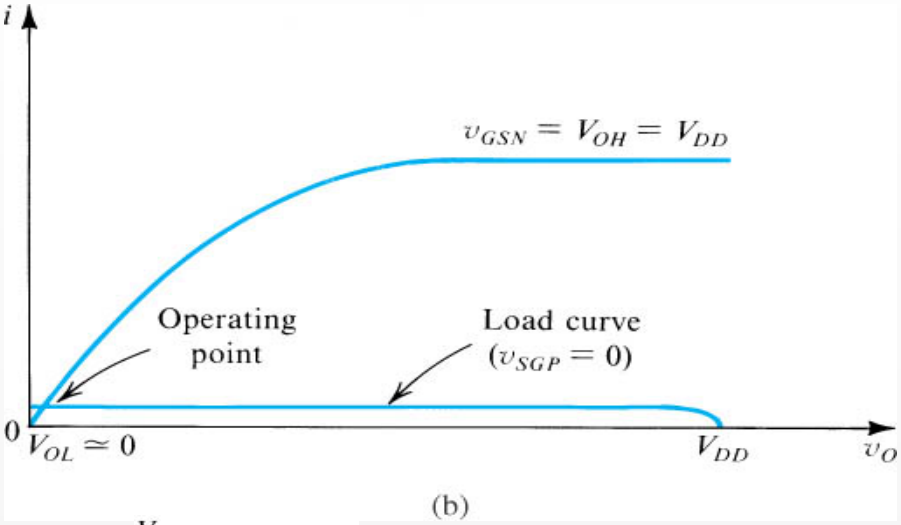


Figure 4.53 The CMOS inverter.

OPERACIÓN INVERSOR





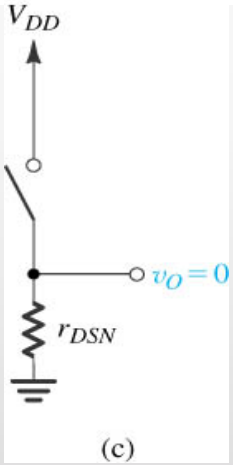
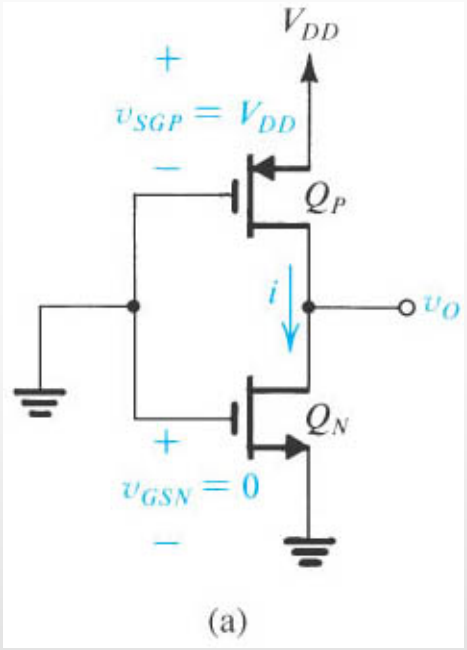
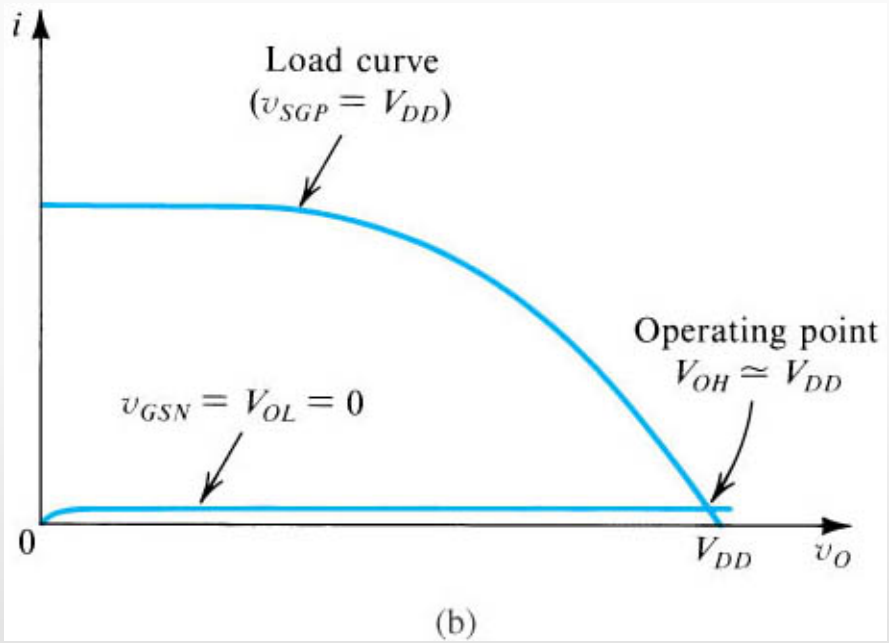


Figure 4.54 Operation of the CMOS inverter when v_I is high: **(a)** circuit with $v_I = V_{DD}$ (logic-1 level, or V_{OH}); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

OPERACIÓN INVERSOR





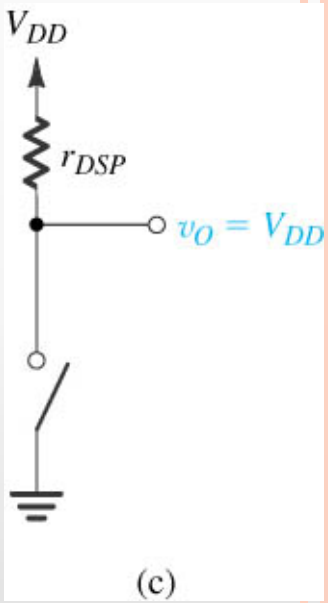


Figure 4.55 Operation of the CMOS inverter when v_I is low: **(a)** circuit with $v_I = 0$ V (logic-0 level, or V_{OL}); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

CARACTERISTICA V-I

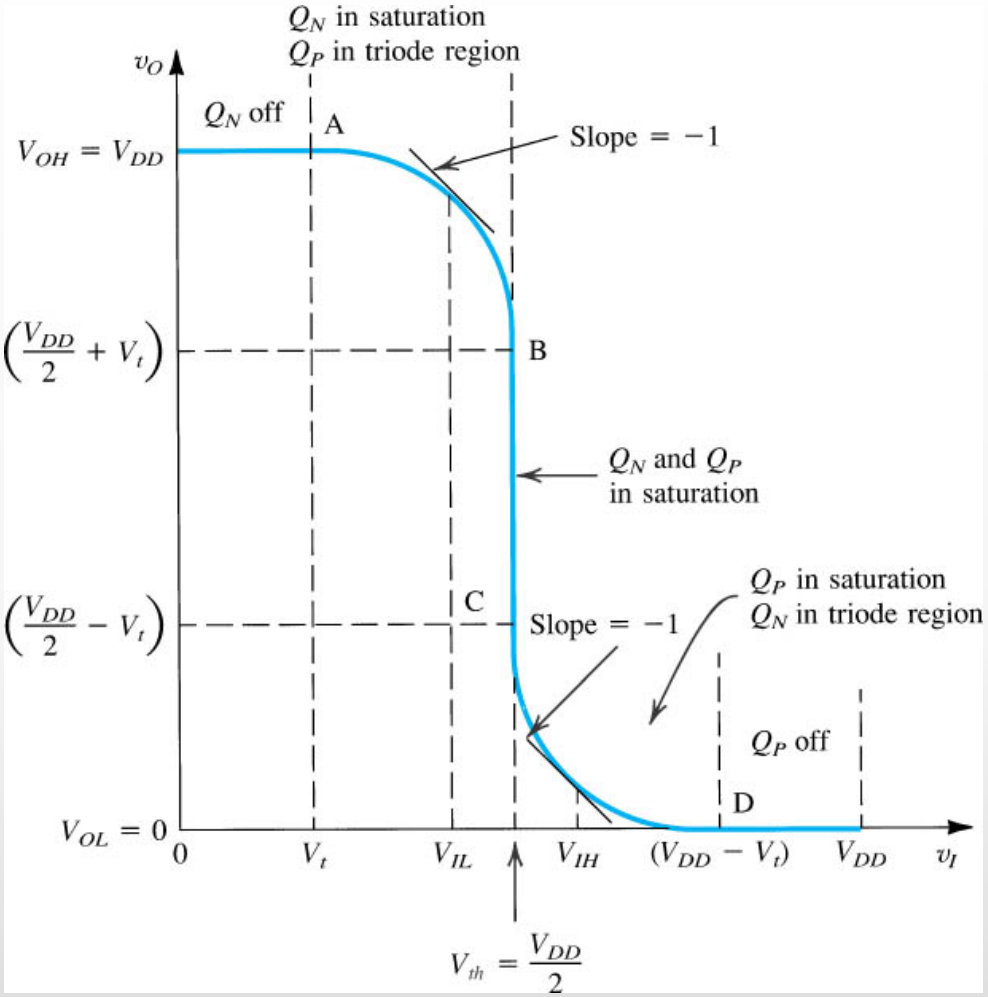


Figure 4.56 The voltage transfer characteristic of the CMOS inverter.

RESPUESTA INVERSOR

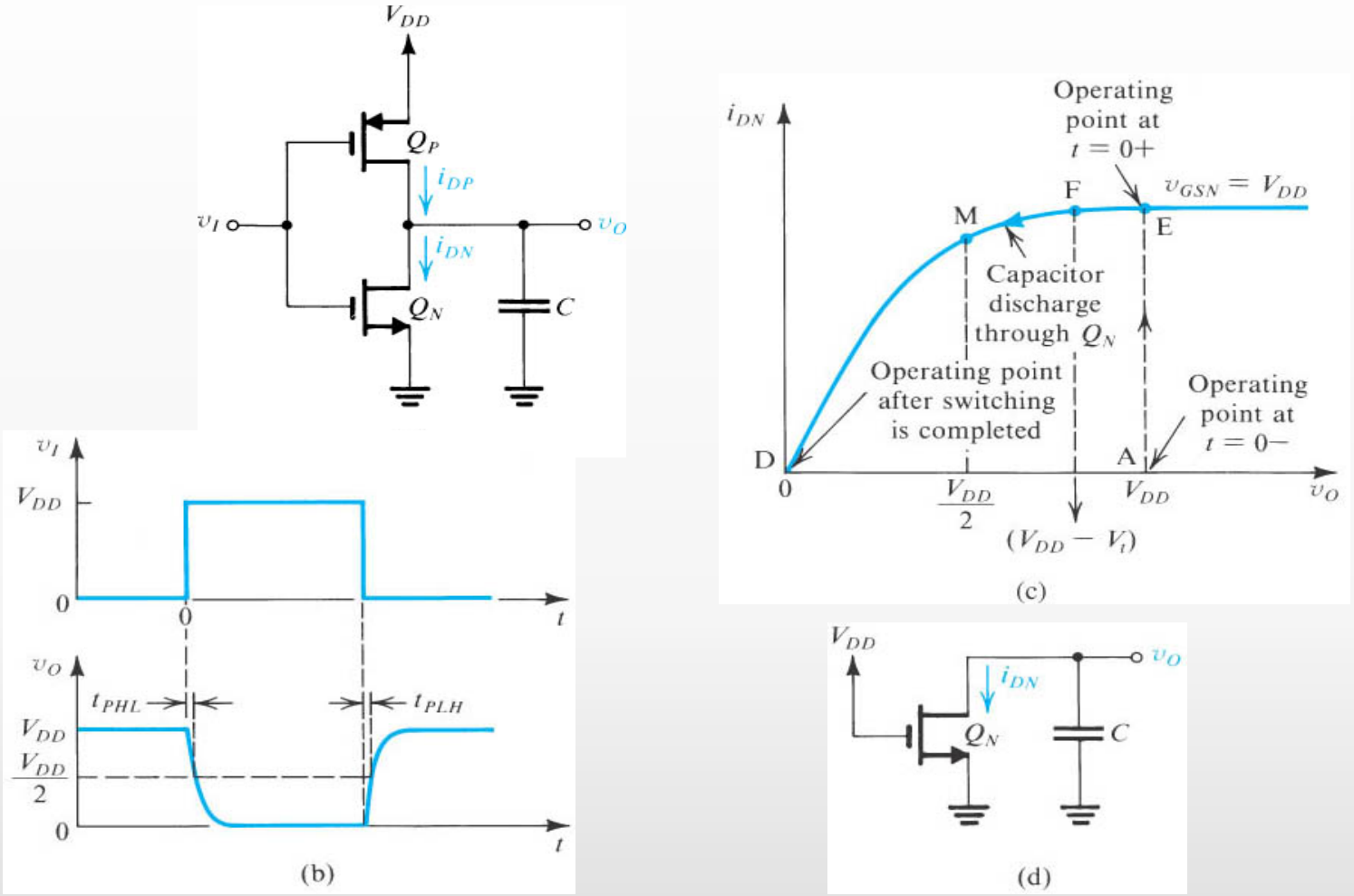
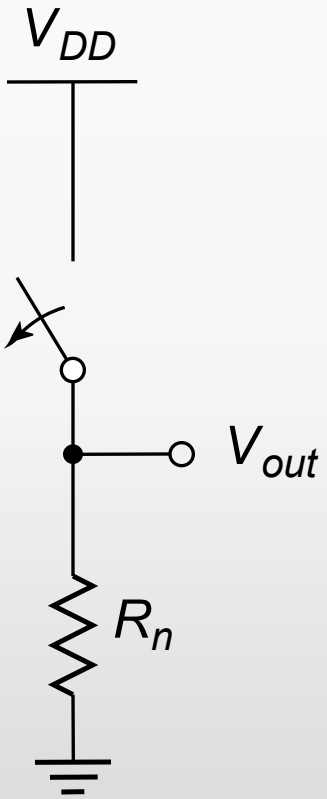
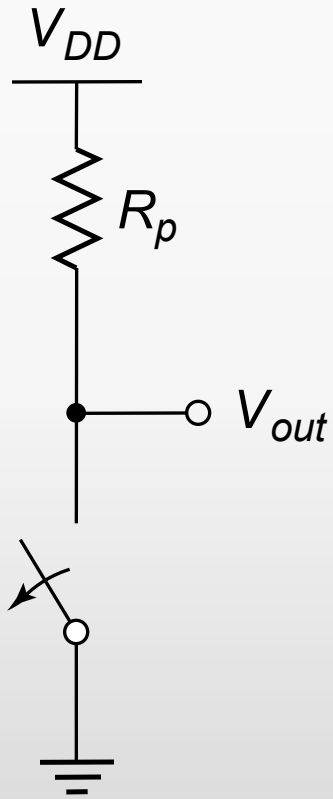


Figure 4.57 Dynamic operation of a capacitively loaded CMOS inverter: **(a)** circuit; **(b)** input and output waveforms; **(c)** trajectory of the operating point as the input goes high and C discharges through Q_N; **(d)** equivalent circuit during the capacitor discharge.

Inversor CMOS Modelo Primer Orden Análisis DC



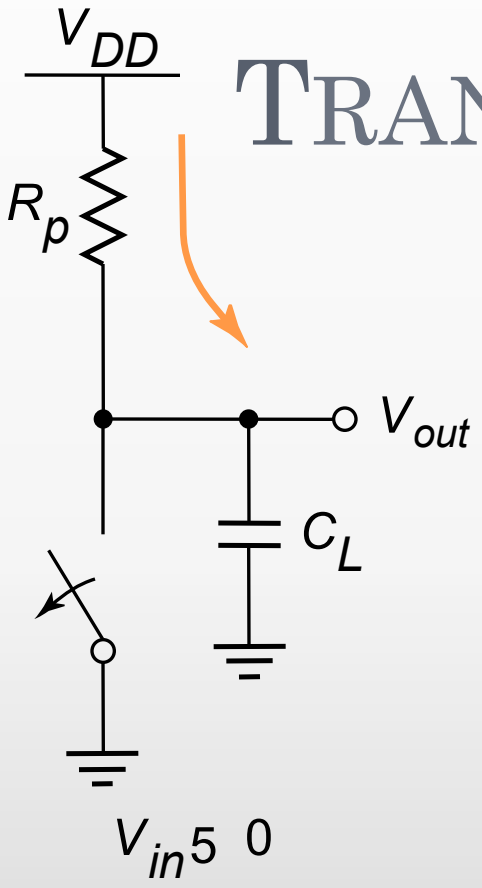
V_{in} 5 V_{DD}



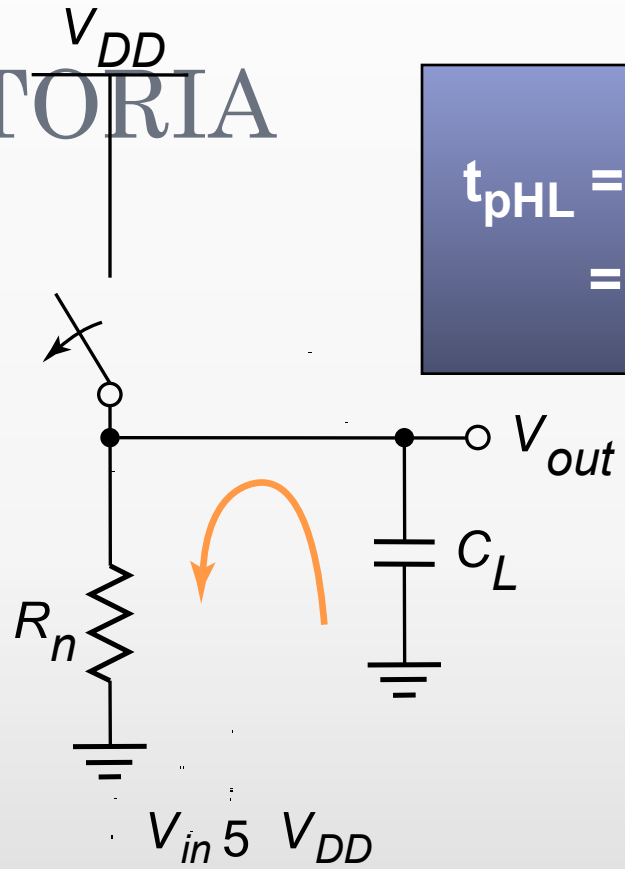
V_{in} 5 0

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

Inversor CMOS: Respuesta Transitoria



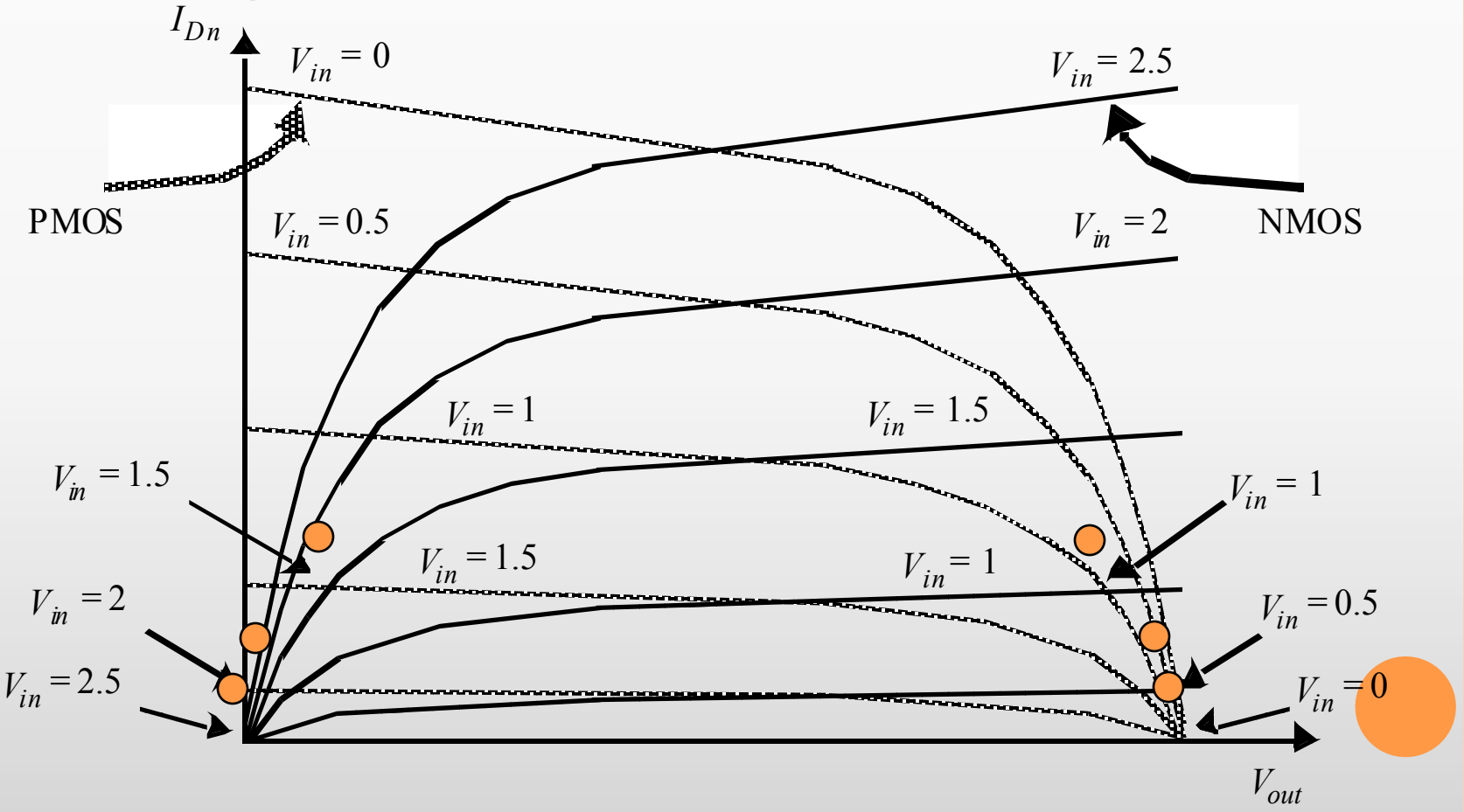
(a) Low-to-high



(b) High-to-low

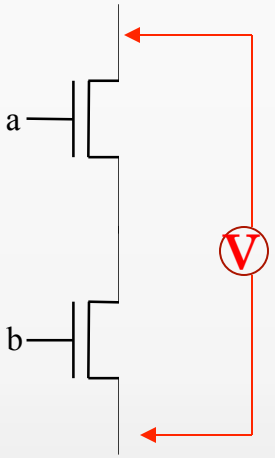
$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

Inversor CMOS Característica de Carga

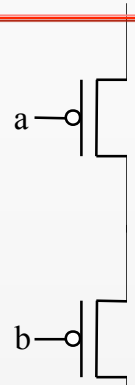


Lógica Combinatoria

TRANSISTORES EN SERIE

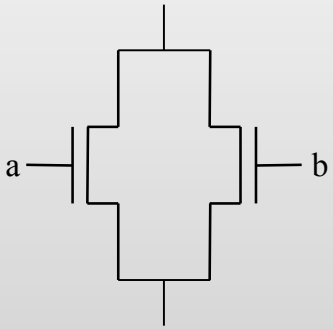


a	b	Interruptor
0	0	off
0	1	off
1	0	off
1	1	on

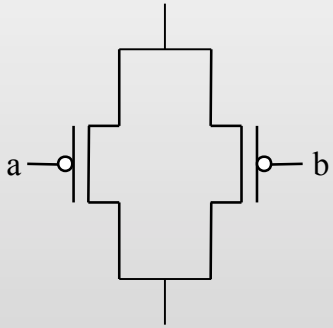


a	b	Interruptor
0	0	on
0	1	off
1	0	off
1	1	off

TRANSISTORES EN PARALELO

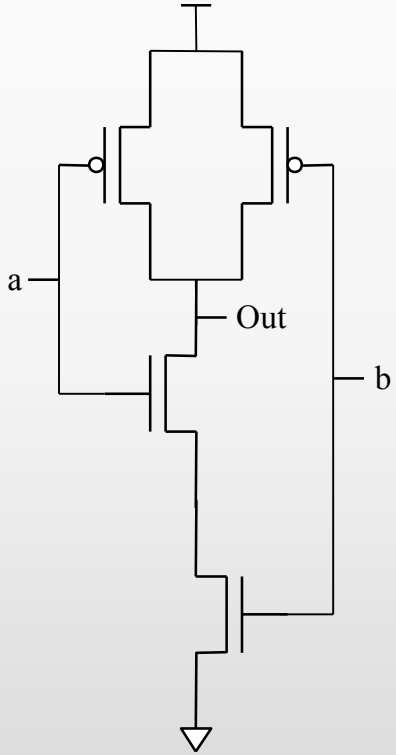


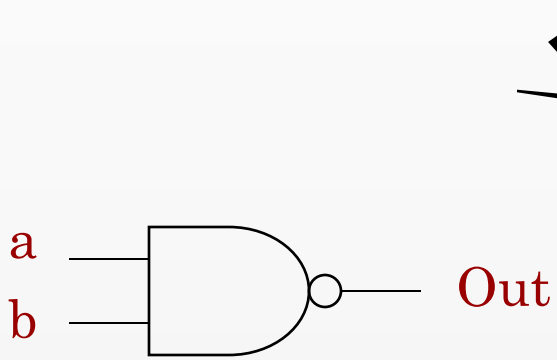
a	b	Interruptor
0	0	off
0	1	on
1	0	on
1	1	on

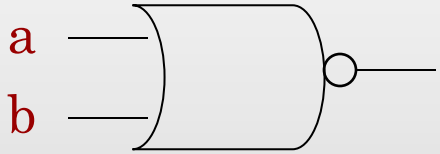


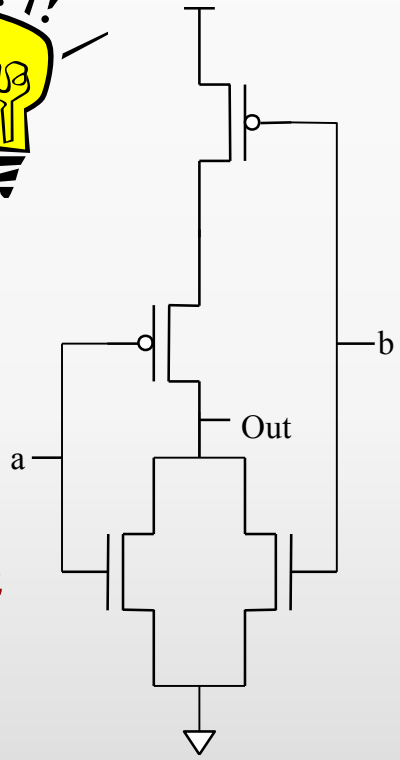
a	b	Interruptor
0	0	on
0	1	on
1	0	on
1	1	off

Compuertas Básicas









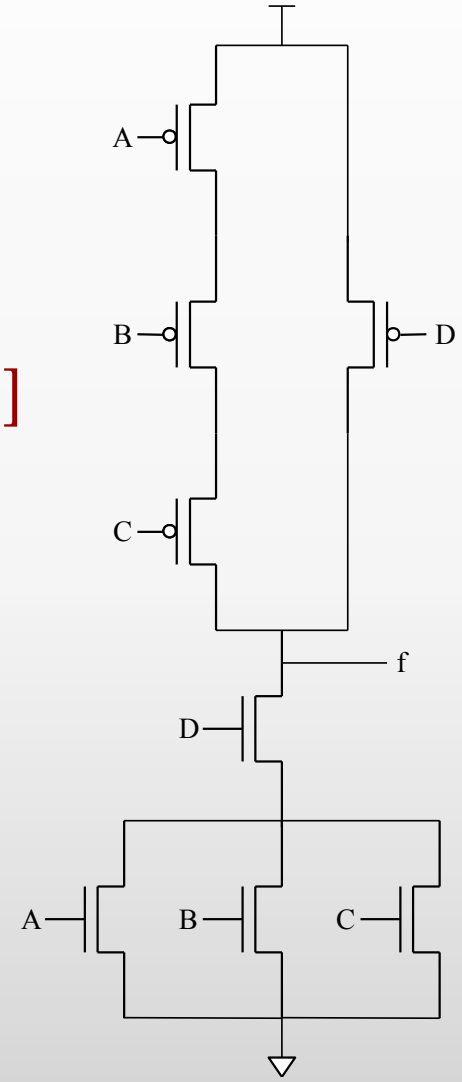
NAND 2 ENTRADAS

NOR 2 ENTRADAS

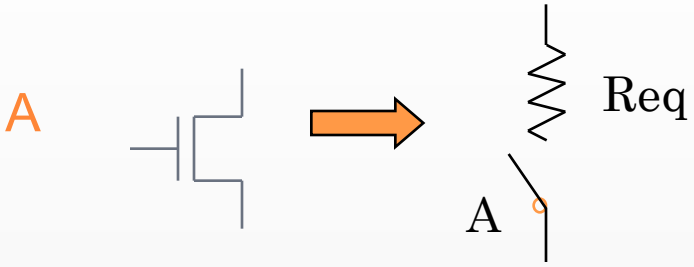
Función Ejemplo

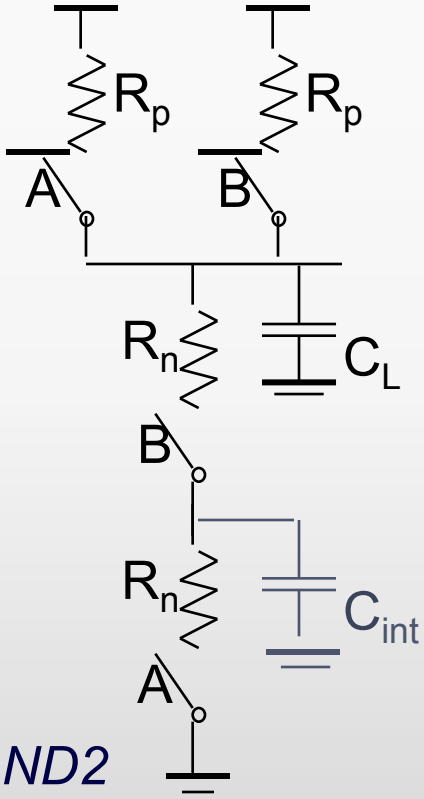
$$F=\overline{[[A+B+C].D]}$$

IMPLEMENTACION CON TRANSISTORES nMOS Y pMOS

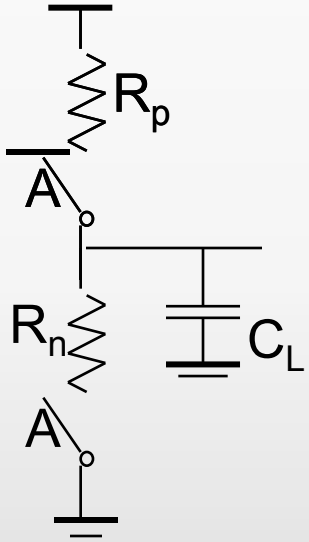


Modelo de Conmutación

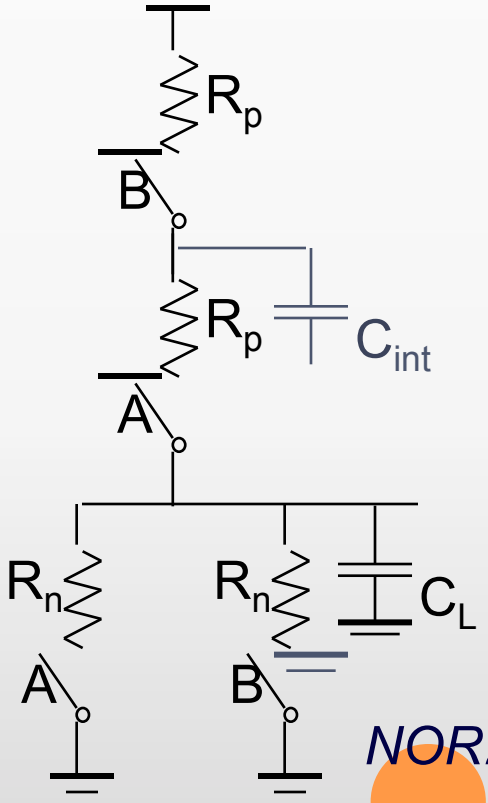




NAND2



INV



NOR2

TEMA DE TRABAJO

- PARA LOS MOSFET DE LA TECNOLOGIA CNM25 REALIZAR:
- BIBLIOTECA SPICE PARA TRANSISTOR N Y P
- IMPLEMENTAR COMPUERTA EXOR CMOS
- EFECTUAR SIMULACION DE LA COMPUERTA.