

Fig. 2: Estilos de layout para el inversor de la familia CMOS.

La Fig. 2 ilustra dos métodos para desollar a cabo una compuerta inversora. Cabe notar como las entradas y salidas de las celdas utilizan la segunda capa de metal, mientras que los conductores de alimentación y tierra se enrutan con una capa de metal diferente a la anterior.

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Operating Voltage	5, 12 V	
Substrate Material	P-Type, Bulk or EPI	
Drawn Transistor Length	0.6 μm	
Gate Oxide Thickness	13.5 nm	
Contact/Via Size	0.5 μm	
Contacted Gate Pitch	3.9 µm	
Top Metal Thickness	675 nm	
Contacted Metal Pitch		
Metal 1	1.5 μm	
Metal 2, 3	1.6 µm	
Metal Composition	TIN/AICu/TIN	

Fig. 3: Caracteristicas del proceso C5.

N-Channel	Typical Value	Unit
V <sub>t</sub>	0.7	V
I <sub>dsat</sub>	450	μ <b>A</b> /μm
P-Channel		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Vt	-0.9	V
Îdsat	-260	μ <b>A</b> /μm

Fig. 4: Características de los transistores estándar de la tecnología C5.

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Rule	Description		Lambda		
		SCMOS	SUBM	DEEP	
3.1	Minimum width	2	2	2	
3.2	Minimum spacing over field	2	3	3	
3.2.a	Minimum spacing over active	2	3	4	
3.3	Minimum gate extension of active	2	2	2.5	
3.4	Minimum active extension of poly	3	3	4	
3.5	Minimum field poly to active	1	1	1	

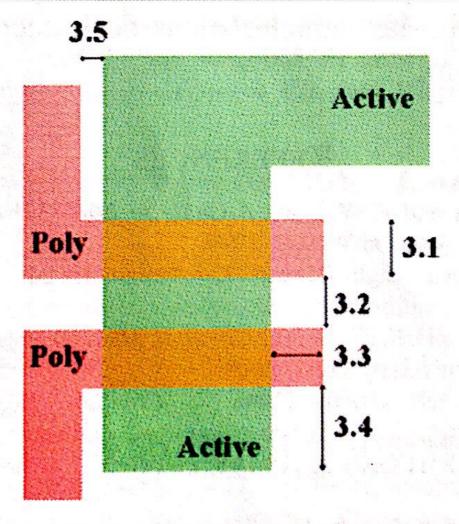


Fig. 5: Reglas de diseño MOSIS para la tecnología de proceso C5.

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Scale PROJECT Preferences	Categories	
The technology scale converts grid units to real spacing on the chin:		
bicmos (scale=1000.0 nanometers) bipolar (scale=2000.0 nanometers) cmos (scale=2000.0 nanometers) fpga (scale=2000.0 nanometers)	Carrier Display Carrier 1/0 Carrier Tools Carrier Display Carrier 1/0 Carrier	
mocmos (scale=300.0 nanometers) mocmosold (scale=1000.0 nanometers) mocmossub (scale=200.0 nanometers) mos (scale=2000.0 nanometers) ocb (scale=1270000.0 nanometers) cmos (scale=2000.0 nanometers) ft'(scale=5000.0 nanometers)	Technology Design Rules Scale Units Icon	
	Export Import	
	Reset Reset All  (Only resets USER Preference  Help Apply	

Fig. 6: Ventana del Programa donde se realizo el cambio del parámetro Lambda

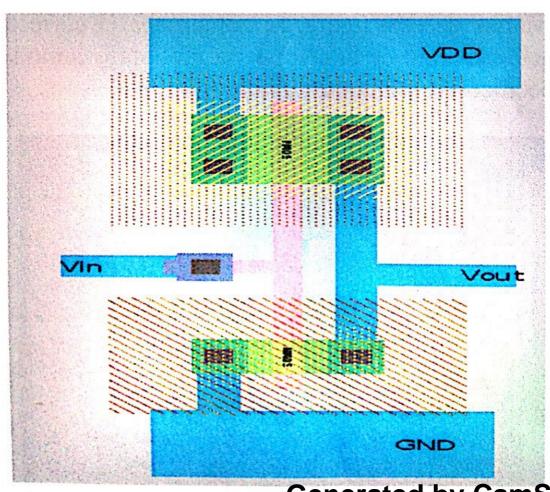


Fig. 7: Layout del inversor vista 2D

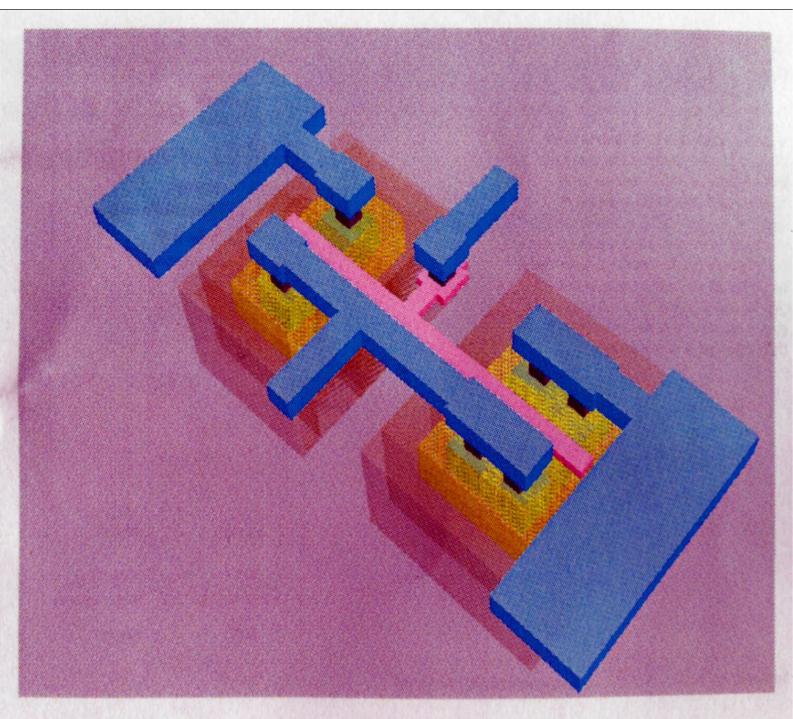


Fig. 8: Layout del inversor vista 3D