Digital CMOS Sea-of-Gates Core Cells and Master Images

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Abstract

New digital CMOS sea-of-gates architectures are being developed in order to increase the flexibility and density in generating micro-cells. The key feature of these sea-of-gates architectures is the absence of a row-oriented architecture. This paper presents two newly developed sea-of-gates arrays. In order to investigate the suitability of the developed arrays a multiplier circuit has been designed and a test chip has been realized. The measurement results of this test chip are presented.

Introduction

Sea-of-gates architectures that are to be used for the implementation of VLSI/ULSI application specific integrated circuits (ASICs) are being developed at a rapid pace. Basic idea is to provide full-custom performance of large systems while enjoying semi-custom advantages like for instance a short design-time cycle. These types of arrays do not only allow the implementation of a part of a system, but entire systems with gate counts in excess of 250K on a single-chip and are expected to exhibit excellent performances. Examples of single-chip systems are e.g. digital-signal and data-communication processors.

Sea-of-gates arrays are a type of gate array in which the core-cell area and the space required for routing purposes are the same. A core-cell is the repetitive unit of the sea-of-gates array. Unlike conventional gate arrays, no distinction is made between the areas in which micro-cells are constructed and that are used for routing. A micro-cell is a small logical function constructed from core-cells like e.g. a nand-gate, a flipflop or a fulladder.

The physical properties and application range identify some architectural features of sea-of-gates arrays. Micro-cell and global interconnections are located in the same physical area, imposing requirements on the architecture of the core-cell. The performance and density of the ASIC built with a sea-of-gates array must be full-custom like, requiring additional demands. The core-cell architecture must be optimally balanced between the interconnect possibilities, the performance and the density requirements.

With the increasing level of system integration more and more structured design approaches are used. Furthermore, VLSI systems also need distributed memory blocks like dual-port SRAMs. On-chip memory has significant advantages like higher performance and lower costs. Wide memory words can be used without I/O pin limitations. Sea-of-gates arrays used for the implementation of these VLSI systems must therefore provide an efficient and high density mapping of structured modules and memory blocks on these arrays.

After having identified some important architectural features, the architectures of existing sea-of-gates arrays have been investigated [1,2,3,4]. Most of these arrays have a conventional gate-array architecture where the routing channels have been filled up with core-cells. The resulting architecture is indeed a sea-of-gates architecture because no explicit routing areas are reserved. However, these sea-of-gates arrays face a row-oriented architecture because the core-cells are lined up in channels. This row-oriented architecture does impose restrictions on the design process and thereby on the final chip design. Our activities try to circumvent these problems and are concentrated on the development of two-dimensional architectures. Several two-dimensional architectures have been investigated. These two-dimensional architectures give a transparent master image with respect to the design process, while the flexibility of the design process is increased.

Development of two-dimensional core cells and architectures

In this section, two newly developed sea-of-gates arrays will be presented. The key feature of these sea-of-gates architectures is the absence of a row-oriented architecture. As a first attempt to achieve a more flexible and transparent sea-of-gates architecture a "chess-board"-like floorplan was used. Figure 1 shows the p-type and n-type core cells and figure 2 the resulting master image array. Every p-type core-cell is surrounded by four n-type core-cells and every n-type core-cell by four p-type core-cells. The x and y dimensions of the core-cells are equal, giving the optimum aspect ratio of one with respect to routing in a sea-of-gates environment. The small n-type transistors are used for SRAM and ROM implementations and share a common diffusion area with the large n-type transistors. This common diffusion area reduces the amount of needed intra-cell wiring. All large transistors are isolated among each other by means of oxide isolation. Table 1 depicts some of the characteristics of this sea-of-gates array.

The main advantage of this array is its flexibility in generating different shaped micro-cells without having restrictions imposed by the master image. In other words, the master image reflects a transparent architecture without preference directions.

During experiments with this array, some subjects of consideration were encountered. The use of oxide isolation between the transistors increases the amount of internal micro-cell wiring because no common source-drain areas exist. This reduces the transparency of the micro-cells considerably. Because of the alternation of p-type and n-type core cells it is relatively difficult to locate the power lines near to the p-type transistors and the ground lines to the n-type transistors.

Although micro-cells can be designed in a lot of different shapes, no rotation operations on micro-cells are possible because the lack of rotation symmetry in the n-type core-cells. This turned out to be a drawback during the placement of micro-cells as it decreased the overall flexibility.

To circumvent the encountered drawbacks, a more sophisticated array has been developed. Figure 3 shows the developed core cells and figure 4 the resulting master image. This image is called the "octagon" image because of the octagon shape of the core cells. Every p-type core-cell is surrounded diagonally by four n-type core-cells and every n-type core-cell by four p-type core cells. To, gain optimal flexibility in generating micro-cells, the core-cell architecture is rotation and mirror symmetrical and the aspect ratio of the core cells is designed to be one which is important for optimum routing results. The octagon core cells use a mix of oxide isolation and transistor isolation which resulted in more transparency and higher gate densities. Within every core-cell four clusters of four transistors with common source-drain areas can be identified. The octagon image has a good transistor density and efficient SRAM implementations are possible. This octagon image allows a flexible and efficient power and ground routing. Table 1 depicts some characteristics of the octagon array.

To show the efficiency of the octagon master image a ten-by-ten bit fully-pipelined multiplier has been designed with the octagon image. The placing of the multiplier is taken from an existing custom standard cell design [5]. The routing has been carried out by means of the GAS system [6]. The multiplier consists of 5.4 Kgates and consumes an area of 2.9 mm^2 which results in an usable gate density of 1900 gates/mm^2. Three interconnect layers were used.

During the implementation of the multiplier it appeared that the used CAD tools did not optimally support the possibilities of the two-dimensional image. In spite of that an efficient implementation could be realized. It is expected that with the use of CAD tools supporting the two-dimensional images even higher implementation densities can be achieved.

Test chip

A sea-of-gates array must not only allow efficient circuit implementations but also the performance of integrated circuits realized with sea-of-gates arrays is of major importance. Therefore, the research is also extended to actual silicon experiments to determine the performance characteristics of the two-dimensional sea-of-gates arrays. A test chip has been realized in the Philips 0.8 μm sea-of-gates process [5]. A microphotograph of the test chip is shown in figure 5. The test chip incorporates

fulladder and ringoscillator test circuits implemented with the chess-board array. Results of measurements are shown in table 2. The measurements have confirmed the expectation that the extended diffusion areas and the bended transistor gates slightly decrease the performance. The influence of the extended diffusion areas can be minimized by connecting these areas to Vdd and Vss. However, the influence of the bended transistor gates can not be reduced. Measurements on dedicated test structures have confirmed the decrease in performance due the bended transistor gates.

The test chip also incorporates several inverter chains with different transistor widths and loadings. These test chains are used to estimate the needed transistor width with respect to propagation delay and fanout.

Because of the test structures, characterization of the two-dimensional core-cells has been possible. Furthermore, during the design of the test chip a lot of circuit design experience has been collected with the two-dimensional images. This experience, together with the performance characteristics, will be used for future developments of the two-dimensional core-cells and master images.

Conclusions

New sea-of-gates array architectures have been developed. These architectures which are not row-oriented, have shown their suitability and good densities in conjunction with transparency can be achieved. The flexibility in the generation, adjustment and manipulation of micro-cells is very important to relieve the VLSI system design process of restrictions imposed by the master image. The optimum performance of these architectures is still a matter of some concern. Two-dimensional core cells are being developed with emphasis on good transistor performance and minimal diffusion areas without bended transistor gates.

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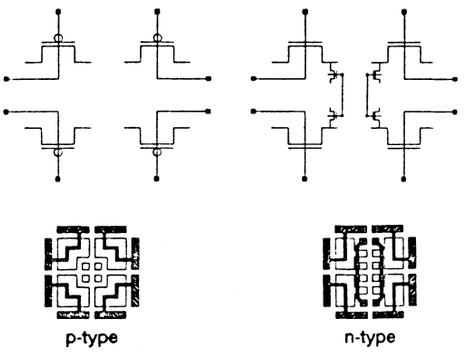

Figure 1. The chess-board core-cells.

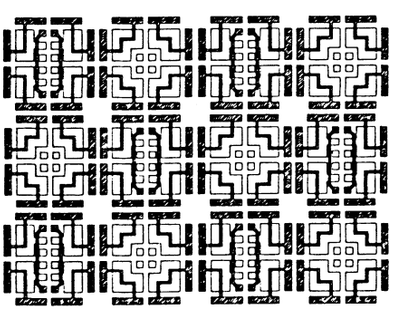

Figure 2. The chess-board image.

Table 1. Characteristics of the chess-board and octagon master image.

	chess-board	octagon
width large nmost:	9.2 μm	5.5 μm
width large pmost:	12.8 μm	12.0 μm
width small nmost:	2 μm	(not present)
raw transistor density:	4822 transistors/mm^2	12,597 transistors/mm^2
gate density: (2-input NAND equivalent)	1205 gates/mm^2	1900 gates/mm^2
SRAM density:	1205 bits/mm^2	1574 bits/mm^2
ROM density:	7230 bits/mm^2	9448 bits/mm^2
technology:	* 0.8 μm CMOS * 3 metal interconnect layers * metal pitch 3.6 μm for all layers	

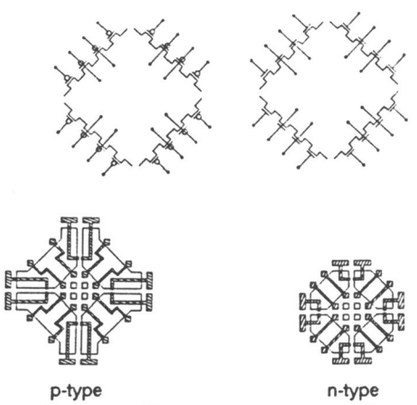

Figure 3. The octagon core-cells.

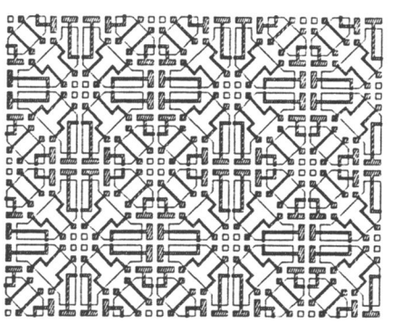

Figure 4. The octagon image.

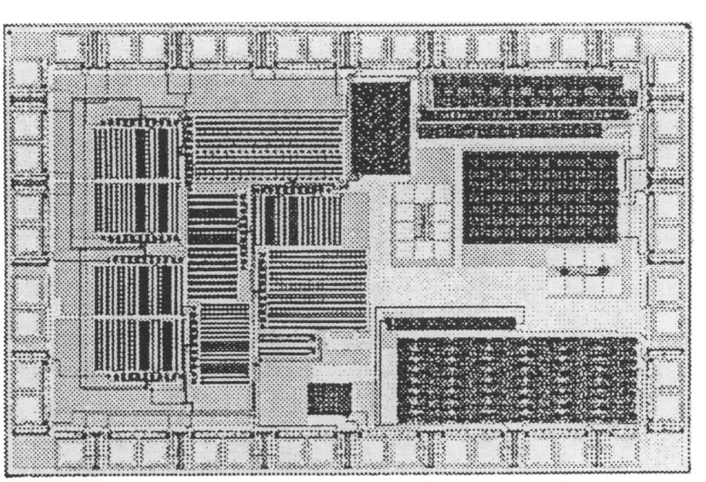

Figure 5. Microphotograph of the test chip.

Table 2. Measured propagation-delay values.

carry chain (delay per fulladder)	sum chain (delay per fulladder)	typical gate delay (2-input NAND, fanout 2)	ringoscillator (delay per inverter)
1.4 ns	2.0 ns	680 ps	190 ps