

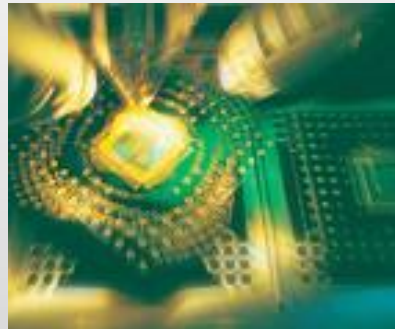
TECNICAS DE INTEGRACION

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II-2013



INVERTOR CMOS

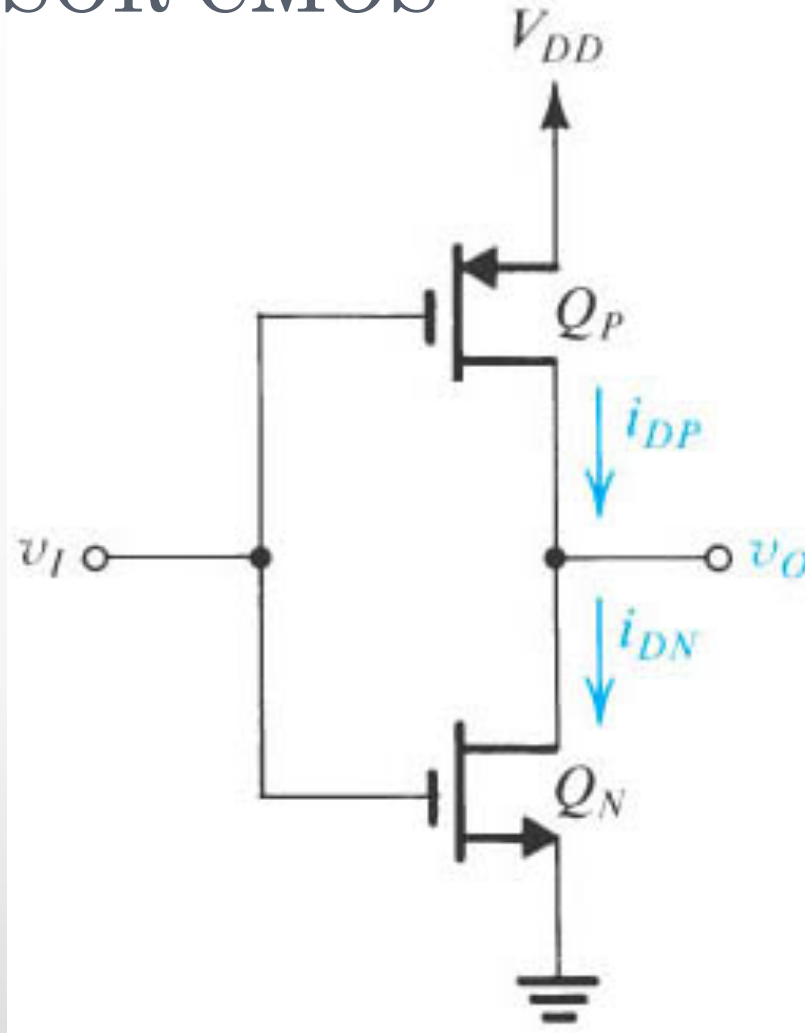


Figure 4.53 The CMOS inverter.

OPERACIÓN INVERSOR

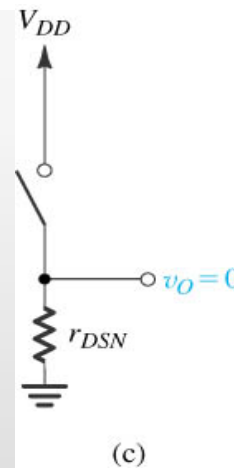
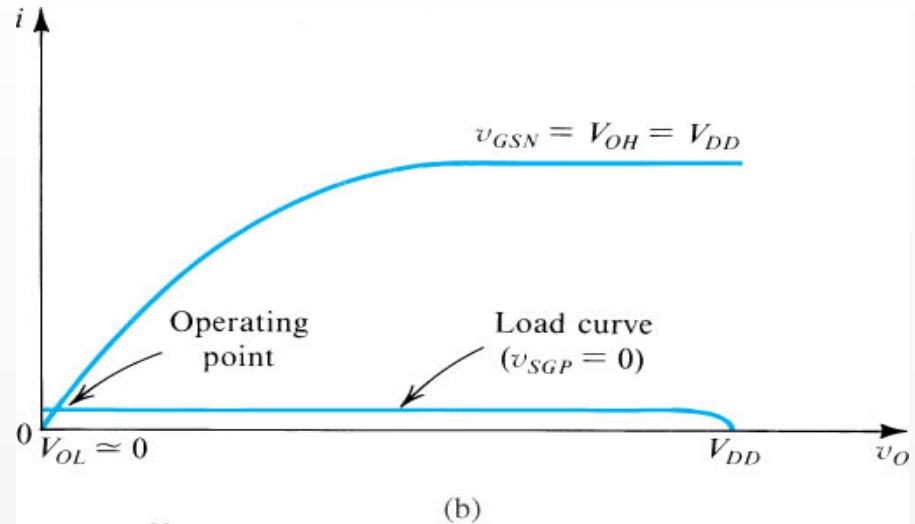
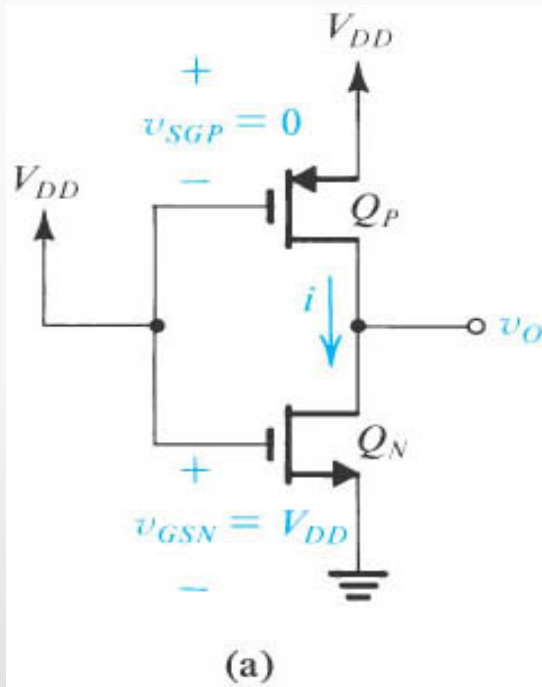


Figure 4.54 Operation of the CMOS inverter when v_I is high: (a) circuit with $v_I = V_{DD}$ (logic-1 level, or V_{OH}); (b) graphical construction to determine the operating point; (c) equivalent circuit.

OPERACIÓN INVERSOR

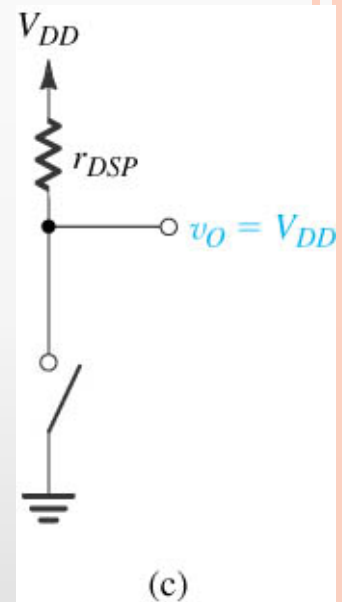
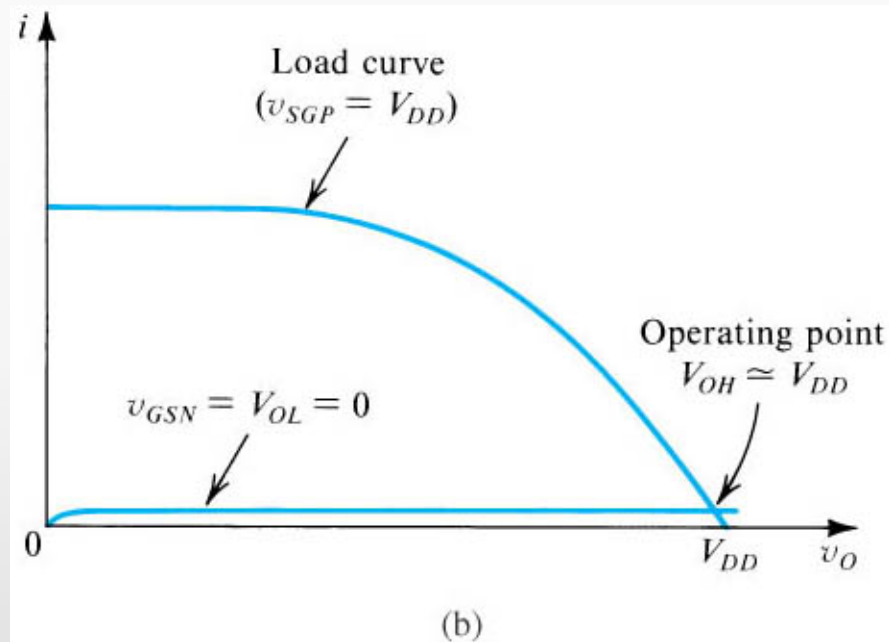
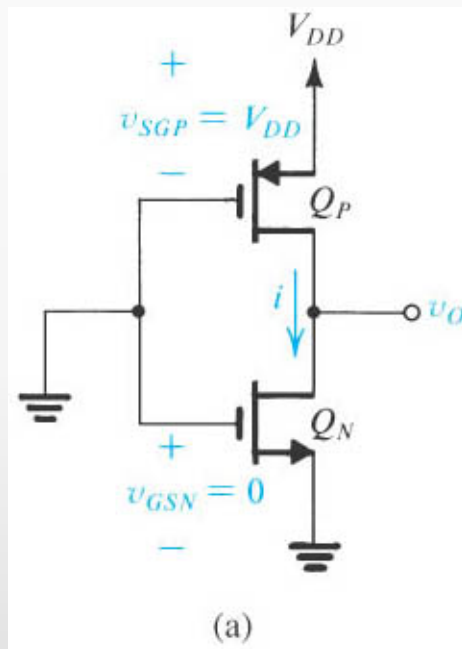


Figure 4.55 Operation of the CMOS inverter when v_I is low: **(a)** circuit with $v_I = 0$ V (logic-0 level, or V_{OL}); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

CARATTERISTICA V-I

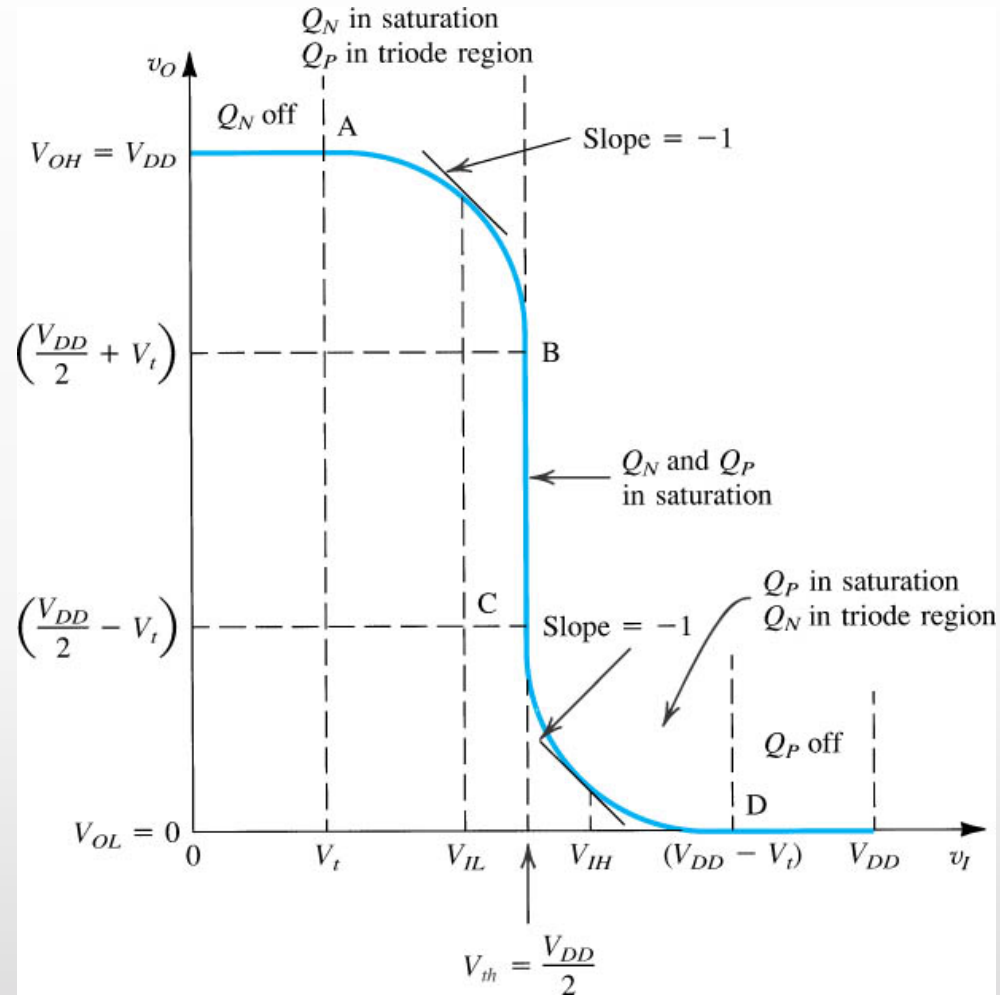


Figure 4.56 The voltage transfer characteristic of the CMOS inverter.

RESPUESTA INVERSOR

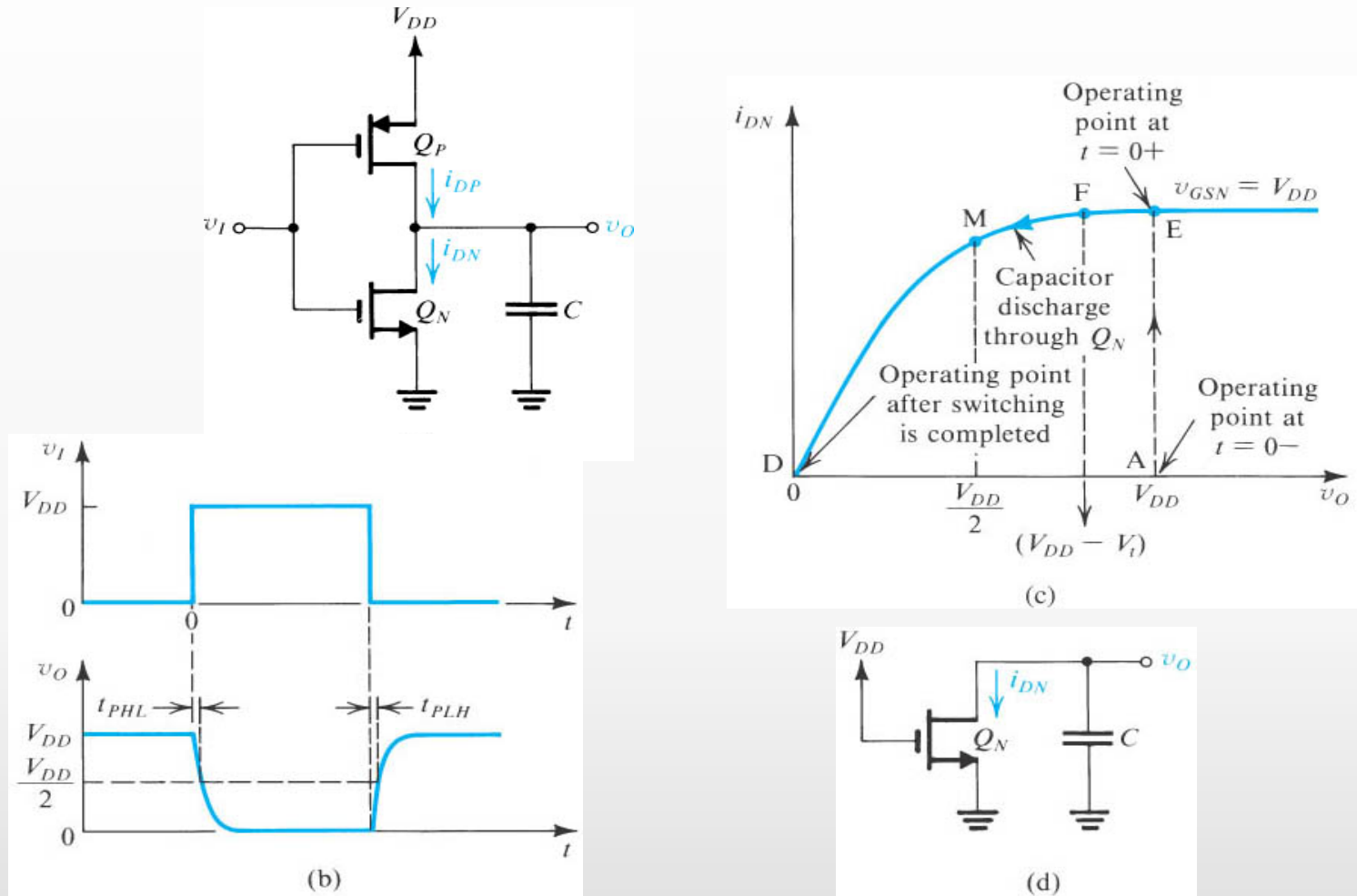
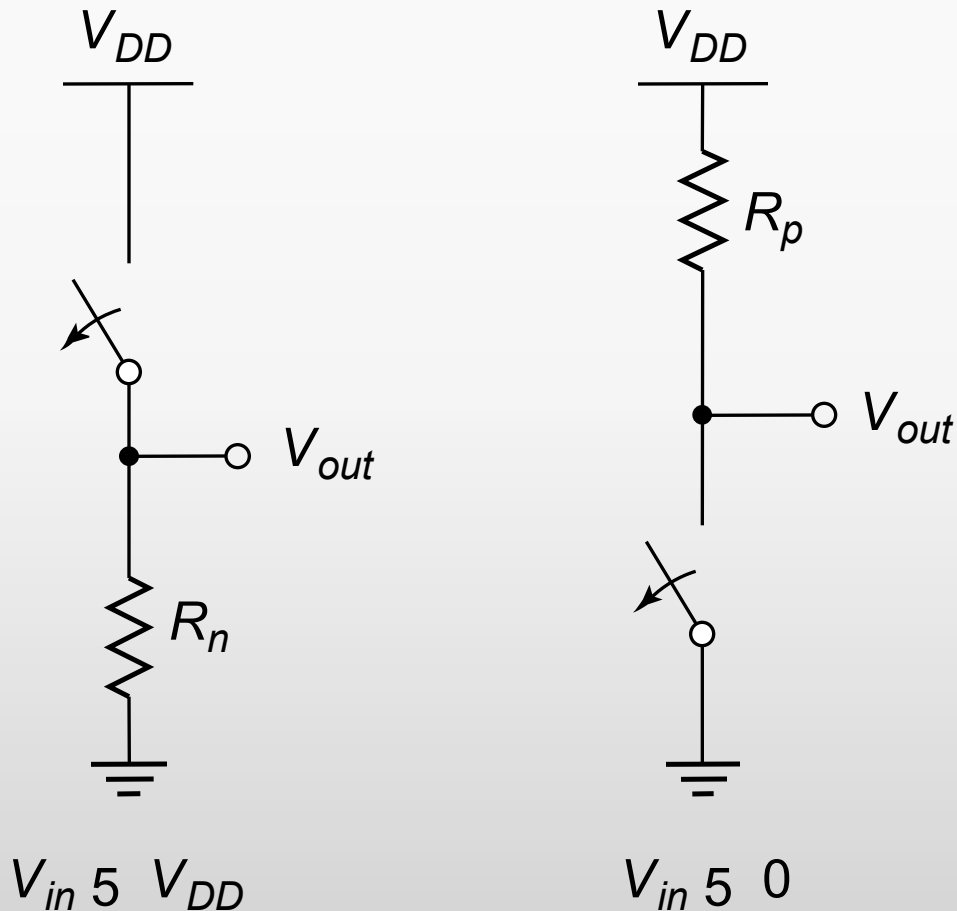


Figure 4.57 Dynamic operation of a capacitively loaded CMOS inverter: **(a)** circuit; **(b)** input and output waveforms; **(c)** trajectory of the operating point as the input goes high and C discharges through Q_N ; **(d)** equivalent circuit during the capacitor discharge.

INVERSOR CMOS

MODELO PRIMER

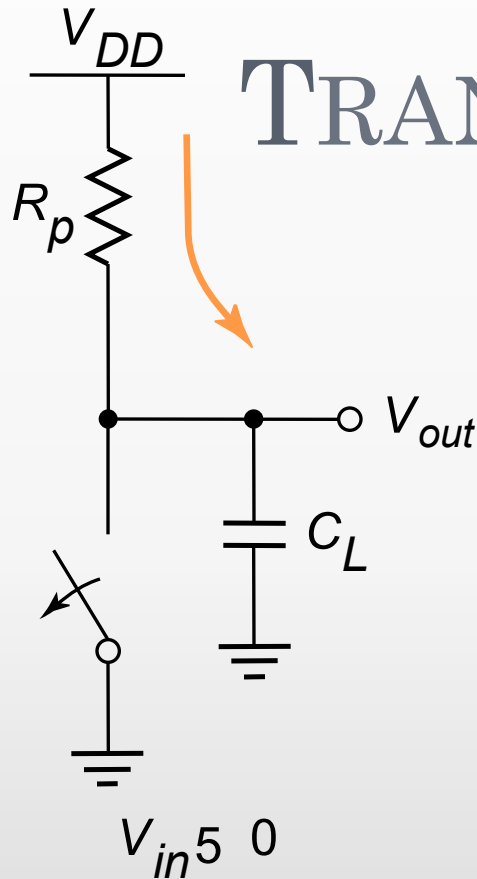
ORDEN ANÁLISIS DC



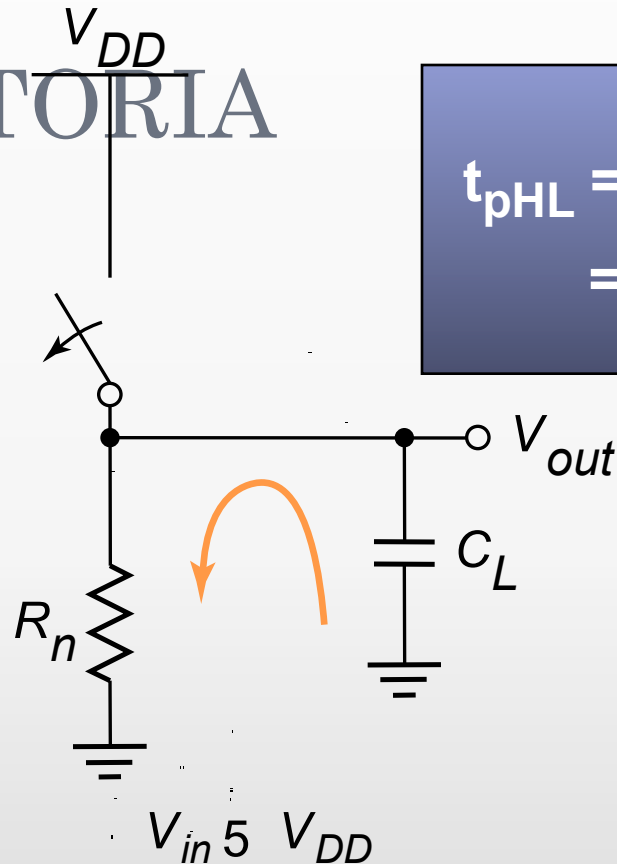
$$\begin{aligned} V_{OL} &= 0 \\ V_{OH} &= V_{DD} \\ V_M &= f(R_n, R_p) \end{aligned}$$



INVERSOR CMOS: RESPUESTA TRANSITORIA



(a) Low-to-high



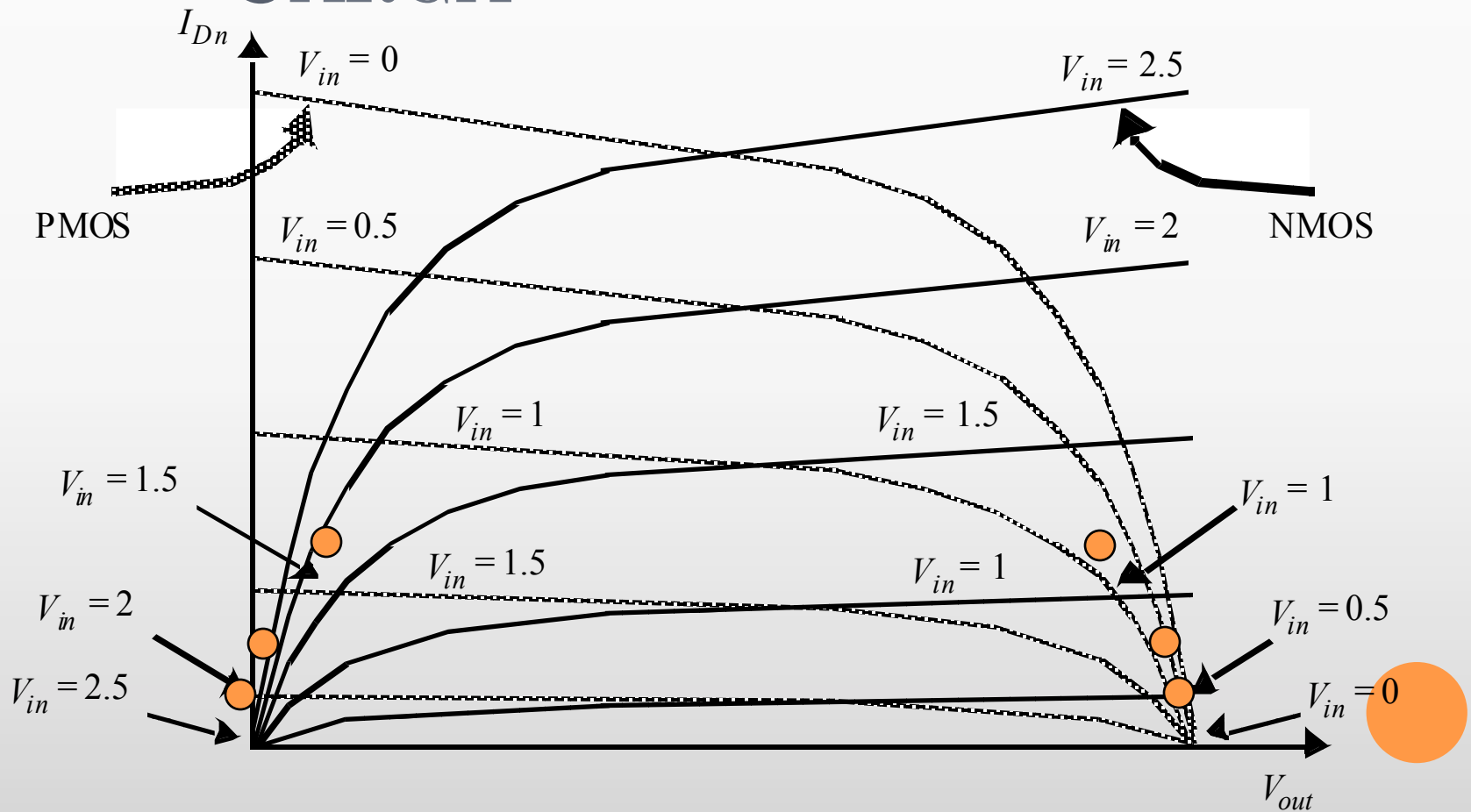
(b) High-to-low

$$t_{pHL} = f(R_{on} \cdot C_L) \\ = 0.69 R_{on} C_L$$

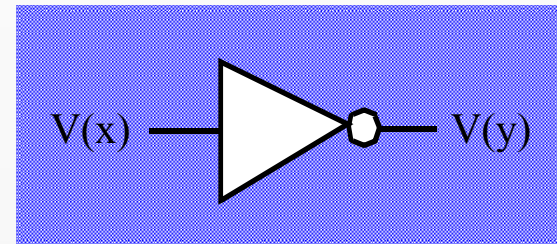
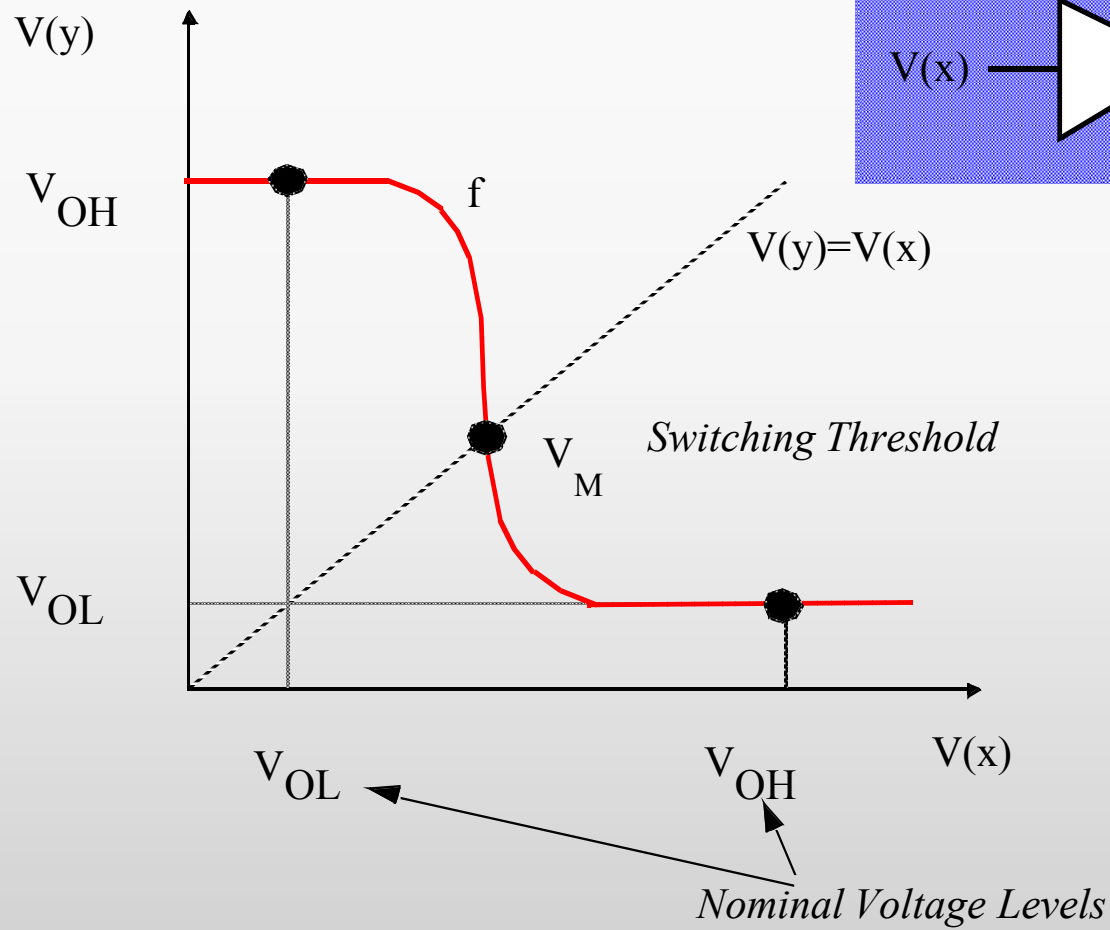


INVERSOR CMOS

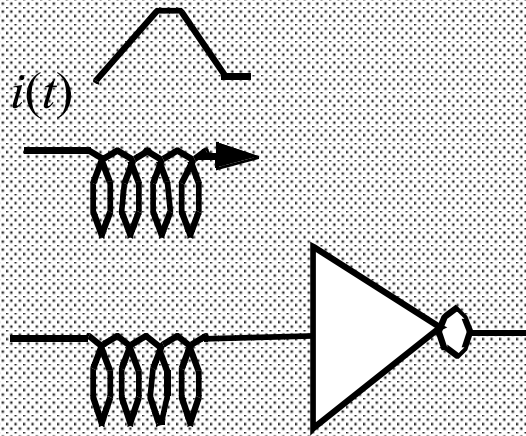
CARACTERÍSTICA DE CARGA



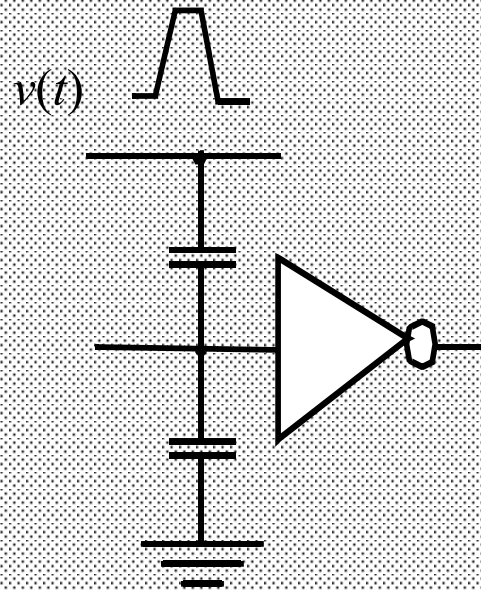
OPERACION DC: TRANSFERENCIA DE VOLTAJE



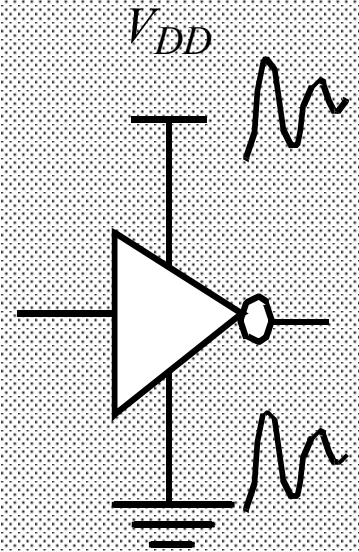
RUIDO EN CIRCUITOS DIGITALES



(a) Inductive coupling

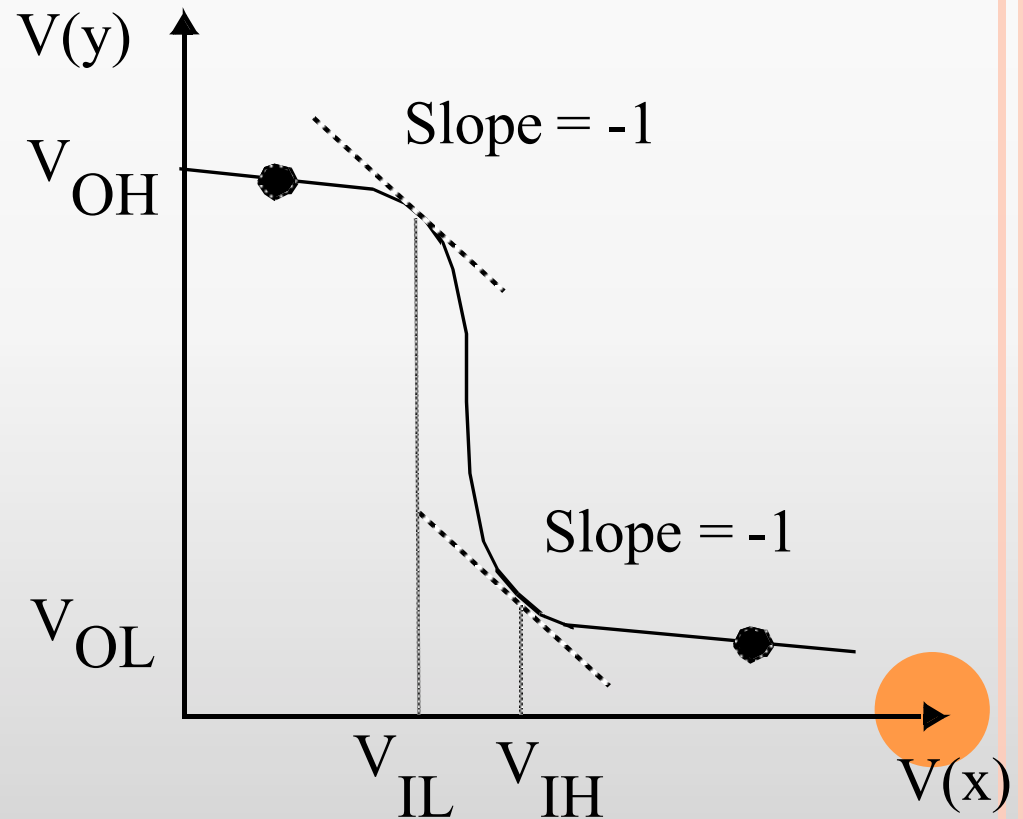
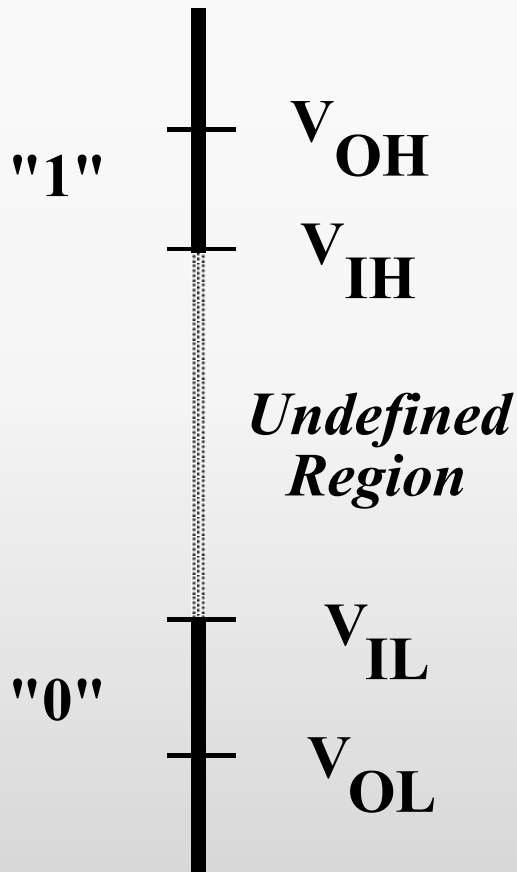


(b) Capacitive coupling

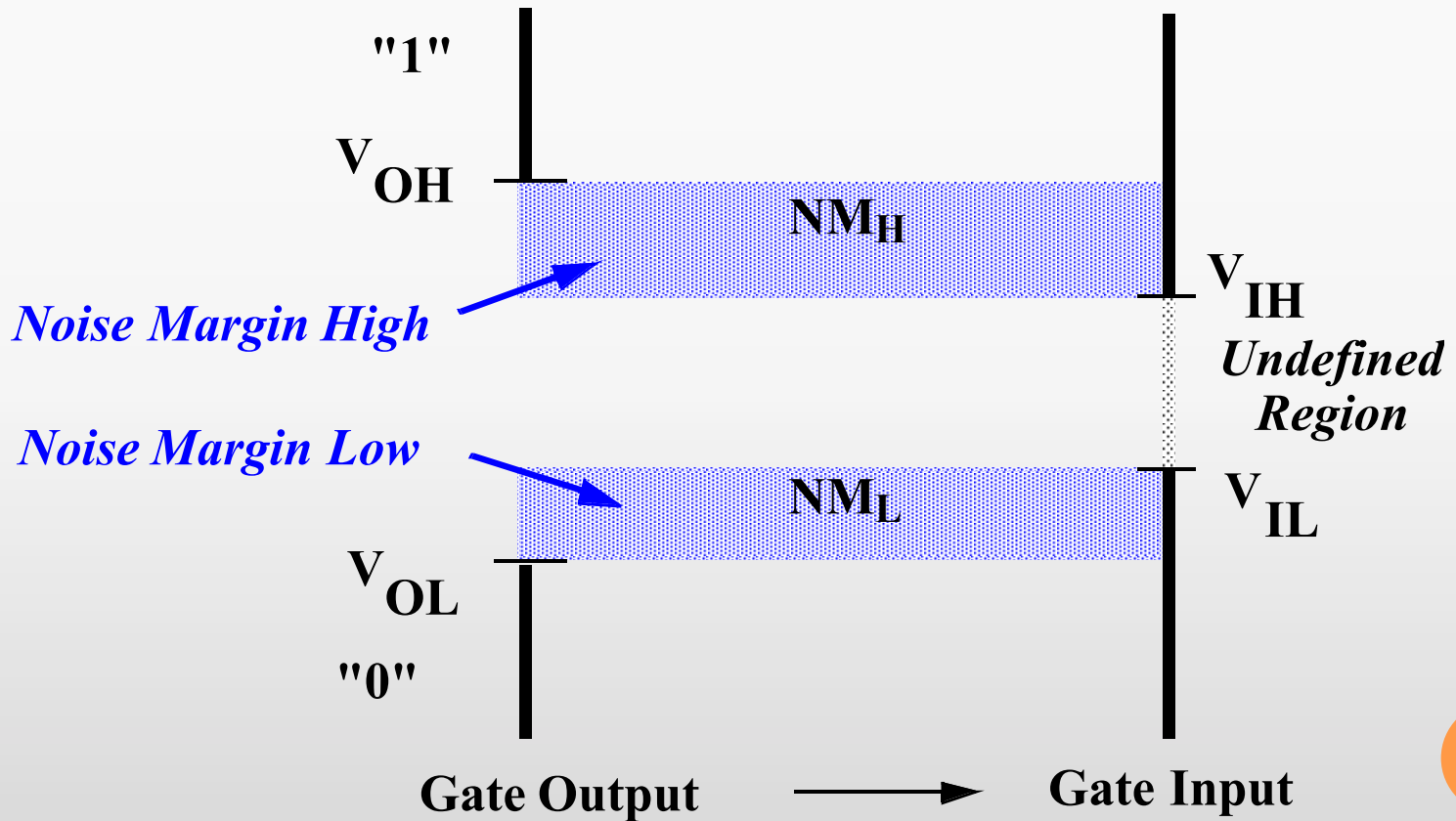


(c) Power and ground noise

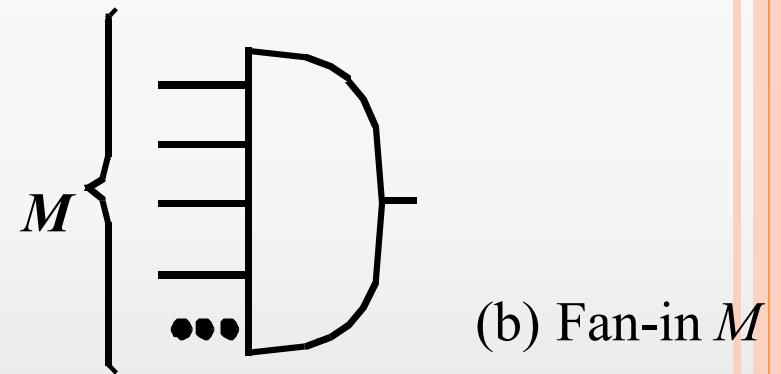
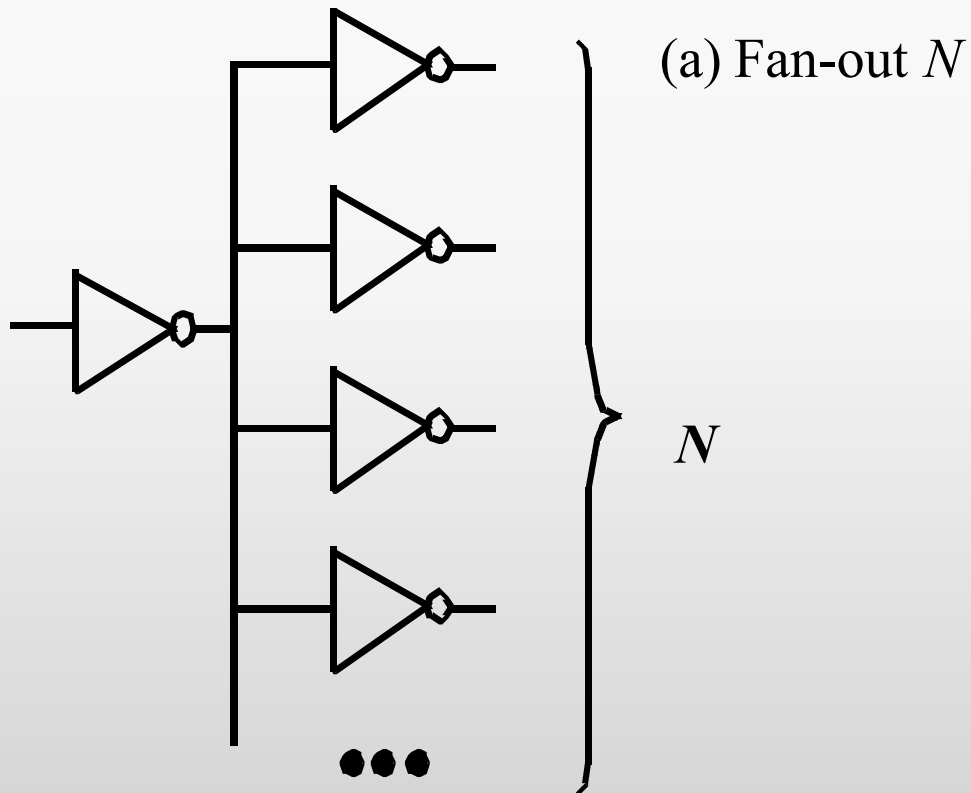
NIVELES DE LAS SEÑALES DIGITALES



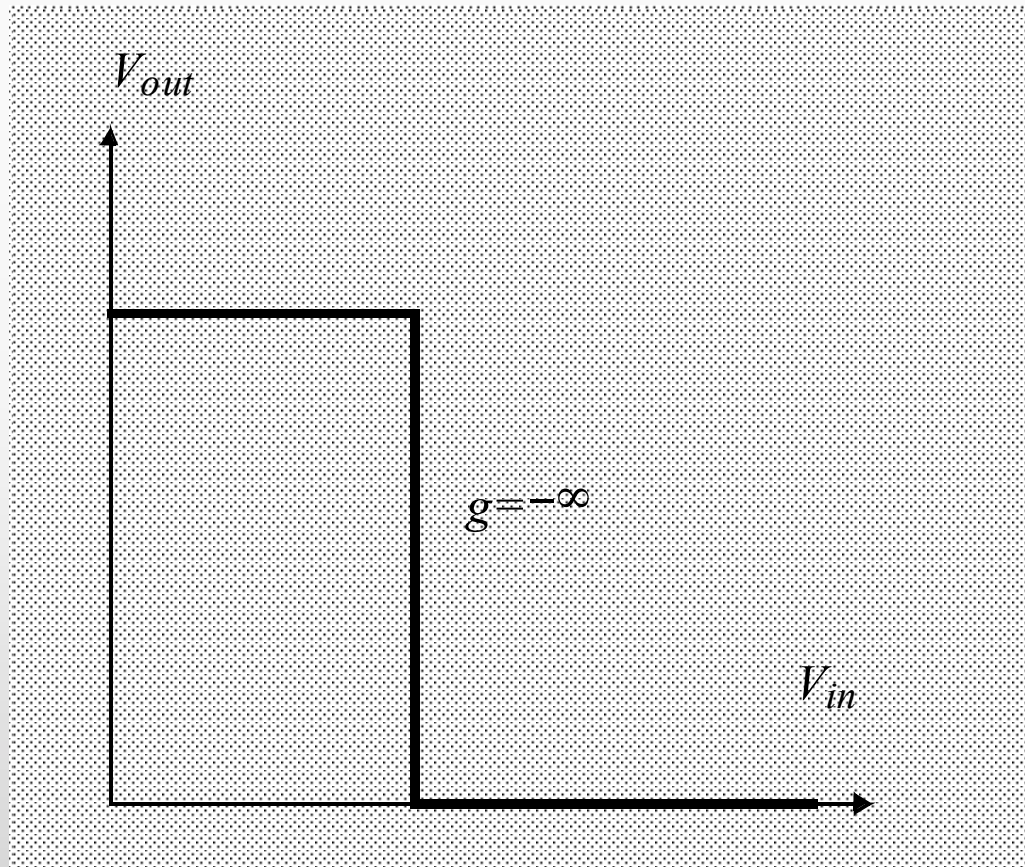
MARGEN DE RUIDO



FAN-IN Y FAN-OUT



COMPUERTA IDEAL

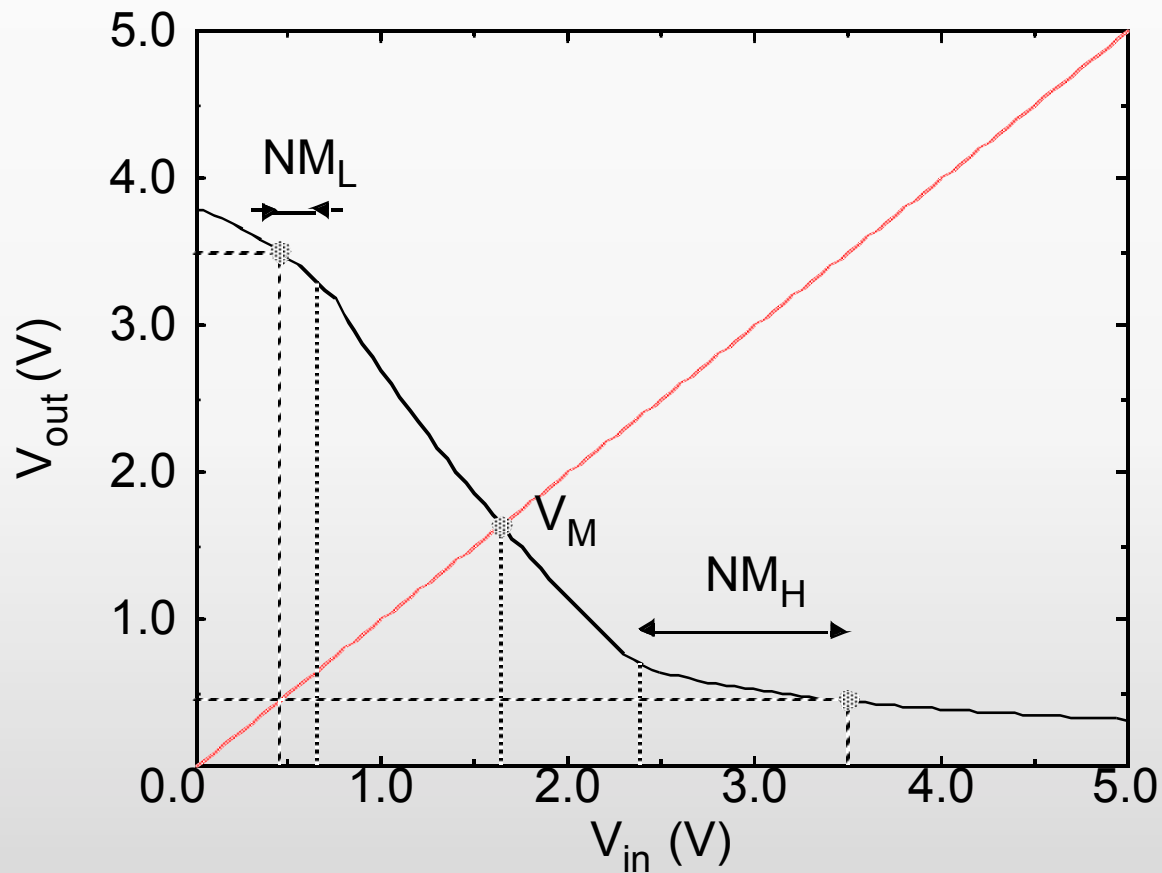


$$R_i = \infty$$

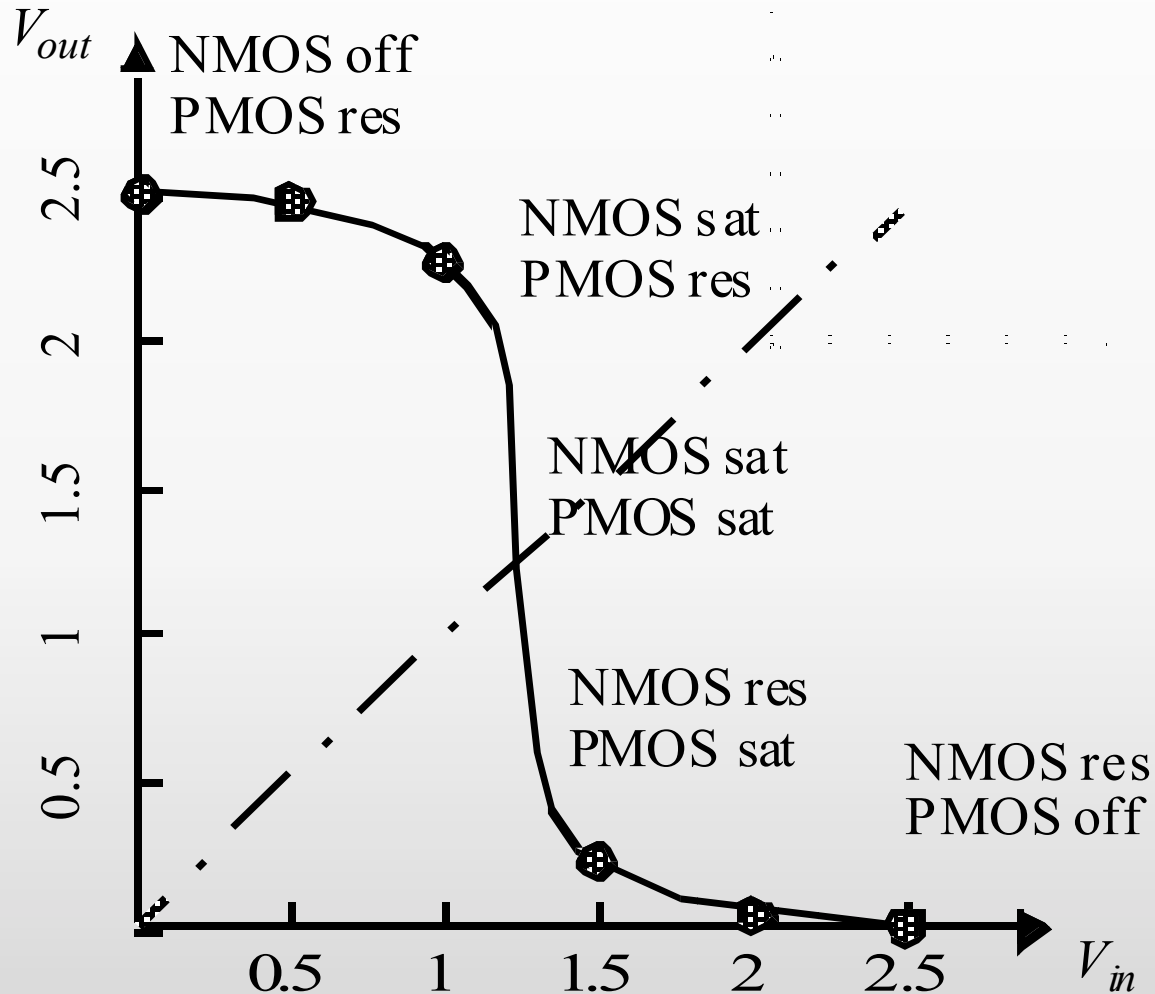
$$R_o = 0$$



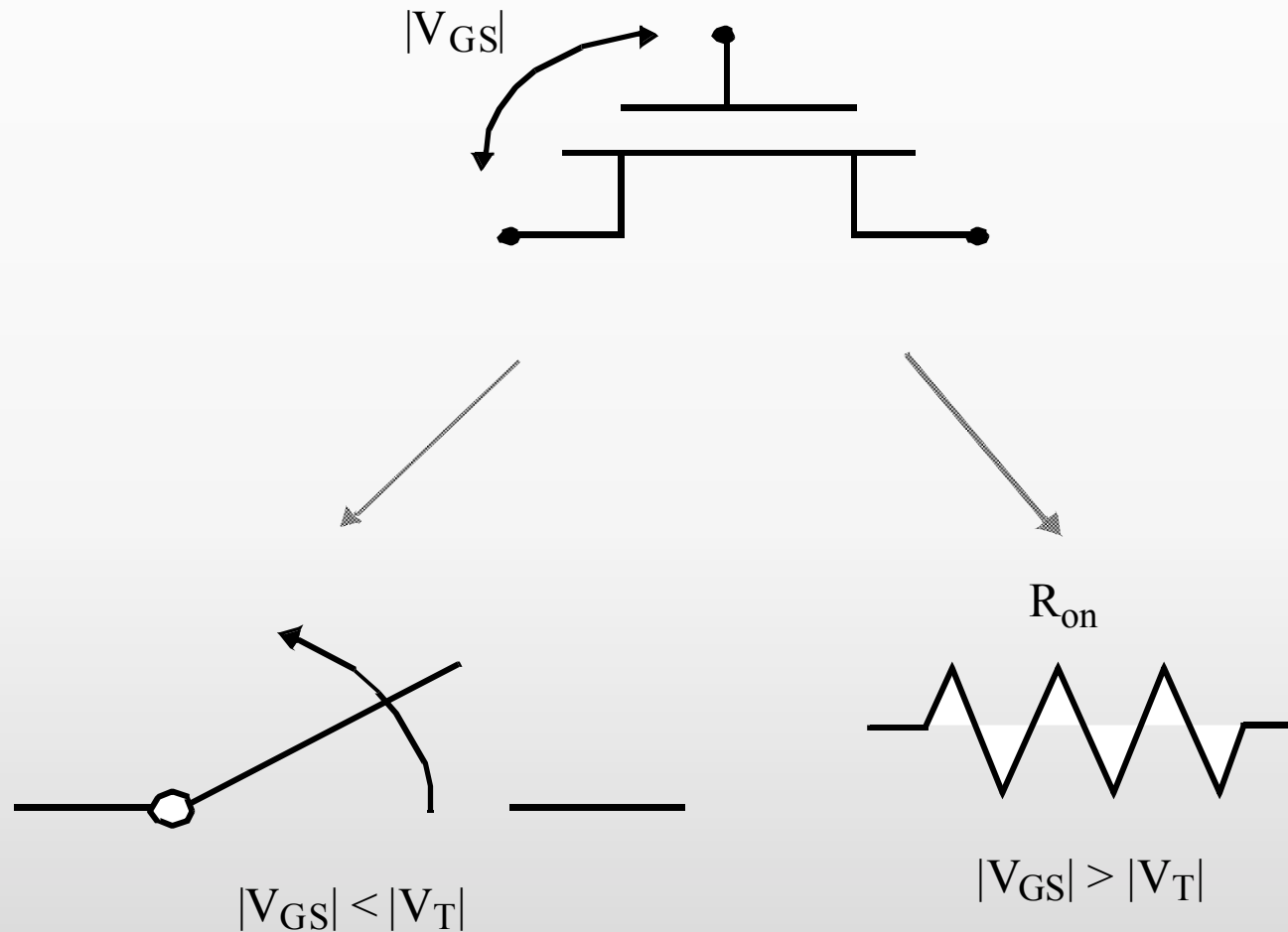
CARACTERÍSTICA REAL DEL INVERSOR



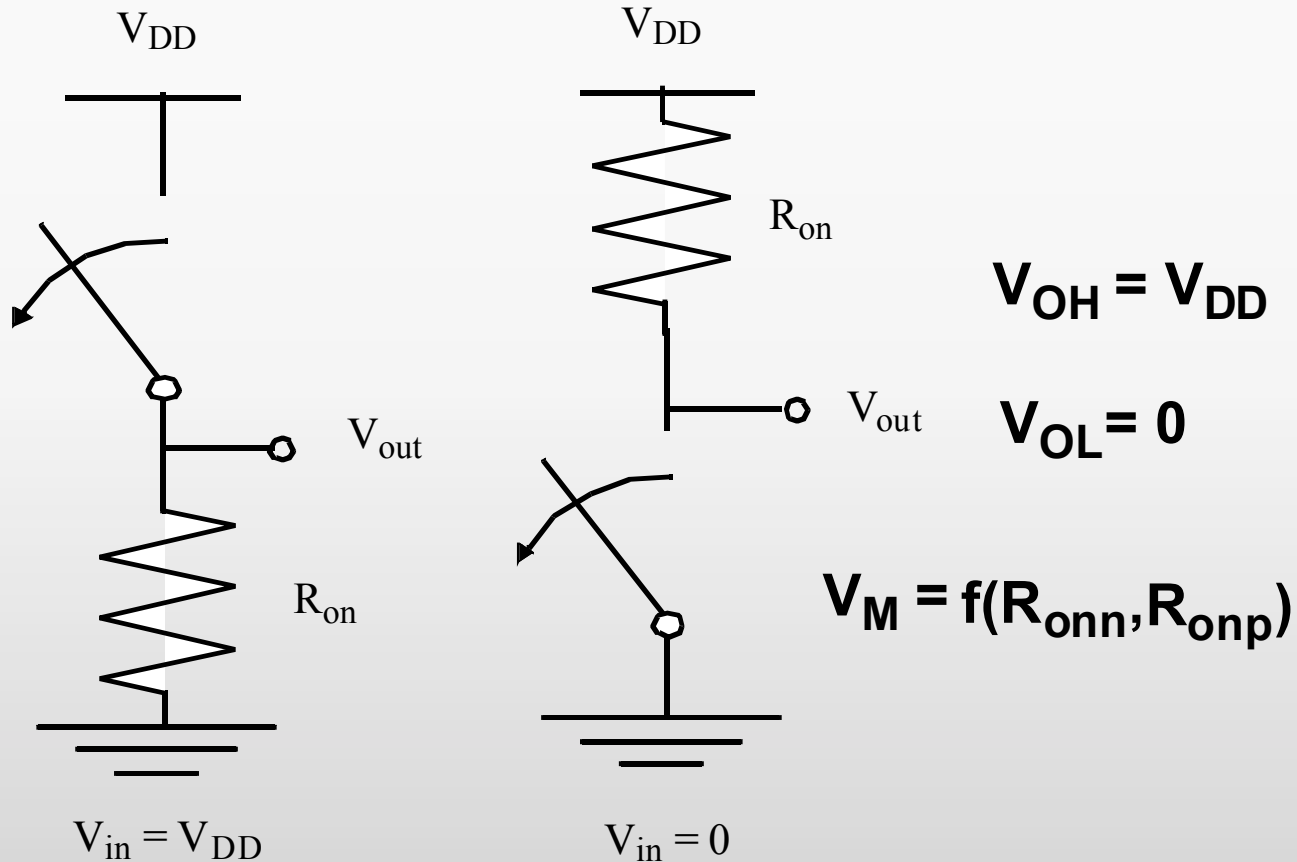
INVERTOR CMOS VTC



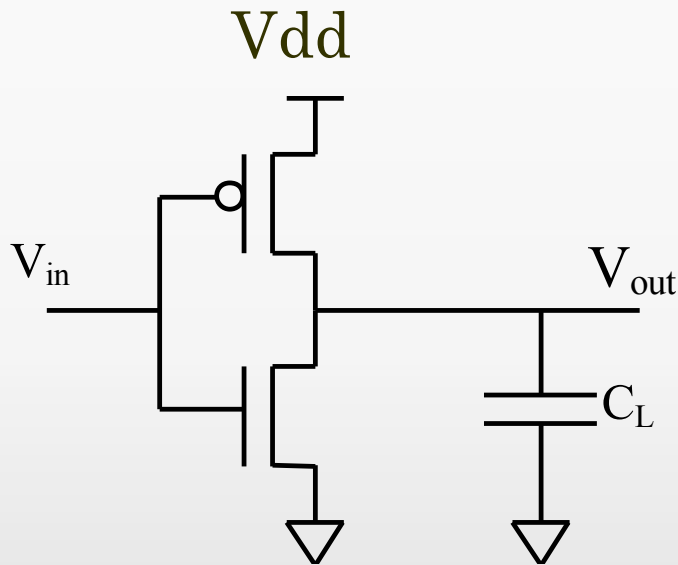
MODELO DE CONMUTACIÓN DEL TRANSISTOR MOS



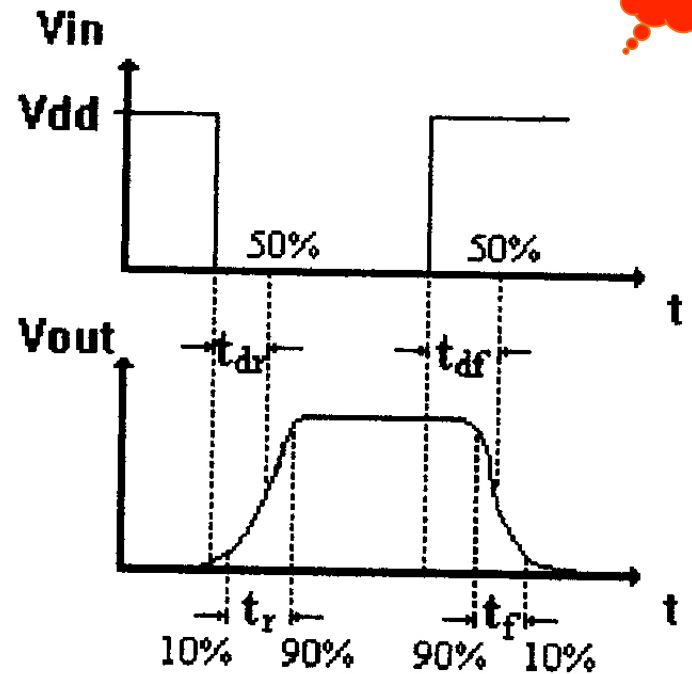
INVERSOR CMOS: ESTADO ESTACIONARIO



TIEMPOS DE RESPUESTA CMOS

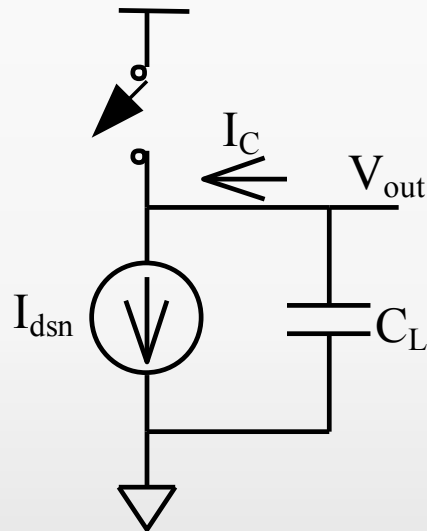


NEGADOR BASICO

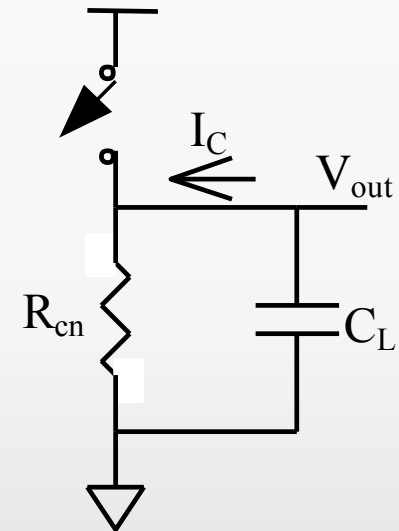


CIRCUITOS EQUIVALENTES

TIEMPO DE BAJADA



$$V_{out} \geq V_{DD} - V_{tn}$$



$$0 \leq V_{out} \leq V_{DD} - V_{tn}$$

$T_F \rightarrow$ TIEMPO DE BAJADA

En Zona de Saturación

$$C_L \frac{dV_{out}}{dt} + \frac{\beta_n}{2} (V_{DD} - V_{tn})^2 = 0 \quad I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2}, \quad 0 < V_{gs} - V_t < V_{ds}$$

$$t_f = t_{f1} + t_{f2}$$

$$t_{f1} = -2 \frac{C_L}{\beta_n (V_{DD} - V_{tn})^2} \int_{0.9 V_{DD}}^{V_{DD} - V_{tn}} (dV_{out})$$

$$t_{f1} = \frac{2 C_L (V_{tn} - 0.1 V_{DD})}{\beta_n (V_{DD} - V_{tn})^2}$$



$T_F \rightarrow$ TIEMPO DE BAJADA(1)

En Zona Lineal

$$C_L \frac{dV_{out}}{dt} + \beta_n \left[(V_{DD} - V_{tn}) \cdot V_{out} - \frac{V_{out}^2}{2} \right] = 0$$

$$I_{ds} = \beta \cdot \left[(V_{gs} - V_t) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right], \quad 0 < V_{ds} < V_{gs} - V_t$$

$$t_{f2} = - \frac{C_L}{\beta_n (V_{DD} - V_{tn})} \cdot \int_{V_{DD} - V_{tn}}^{0.1 V_{DD}} \left(\frac{dV_{out}}{\frac{V_{out}^2}{2(V_{DD} - V_{tn})} - V_{out}} \right) \quad t_{f2} = \frac{C_L}{\beta_n (V_{DD} - V_{tn})} \cdot \ln \left(\frac{19 V_{DD} - 20 V_{tn}}{V_{DD}} \right)$$

$$t_f = t_{f1} + t_{f2}$$

$$t_f = 2 \frac{C_L}{\beta_n \cdot V_{DD} \cdot (1 - n)} \left[\frac{n - 0.1}{1 - n} + \frac{\ln(19 - 20 \cdot n)}{2} \right]$$

$T_F \rightarrow$ TIEMPO DE BAJADA(2)

$$t_f = 2 \frac{C_L}{\beta_n \cdot V_{DD} \cdot (1 - n)} \left[\frac{n - 0.1}{1 - n} + \frac{\ln(19 - 20 \cdot n)}{2} \right]$$

donde $n = \frac{V_{tn}}{V_{DD}}$ $\beta_n = \frac{\epsilon_{SiO_2} \cdot \mu_n}{T_{ox}} \cdot \frac{W_n}{L_n}$

$$t_f \cong k_n \cdot \frac{T_{ox} \cdot L_n \cdot C_L}{\epsilon_{SiO_2} \cdot \mu_n \cdot W_n \cdot V_{DD}}$$

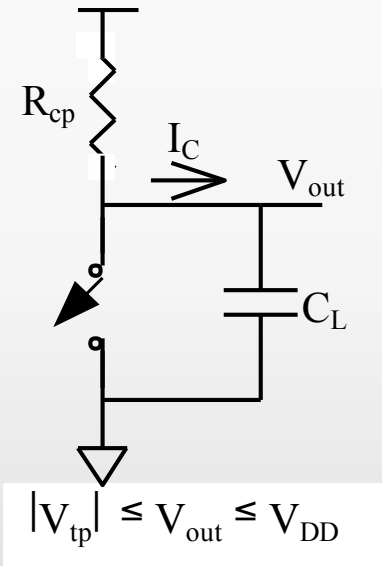
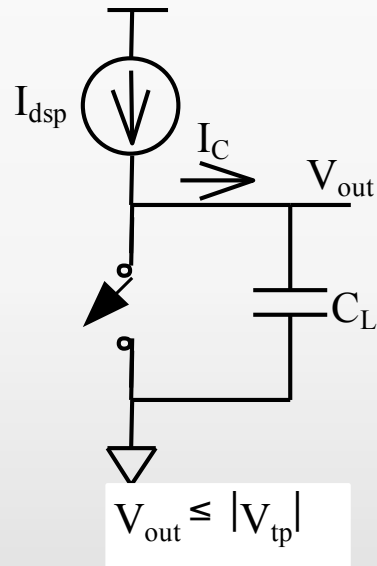
$$t_f \cong k_n' \cdot \frac{L_n \cdot C_L}{W_n}$$

Tecnología específica



CIRCUITOS EQUIVALENTES

TIEMPO DE SUBIDA



$T_R \rightarrow$ TIEMPO DE SUBIDA

$$t_r = 2 \frac{C_L}{\beta_p \cdot V_{DD} \cdot (1-p)} \left[\frac{p-0.1}{1-p} + \frac{\ln(19 - 20 \cdot p)}{2} \right]$$

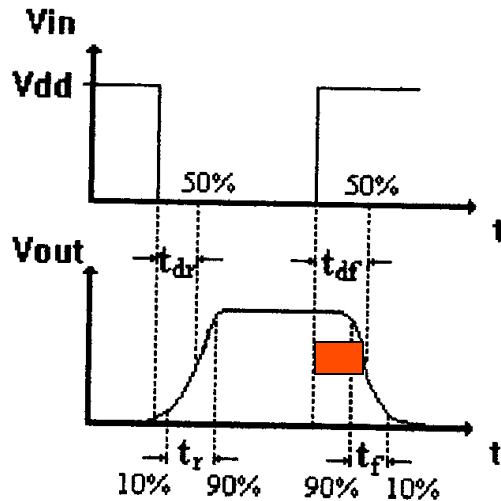
donde $p = \frac{|V_{tp}|}{V_{DD}}$ $\beta_p = \frac{\epsilon_{SiO_2} \cdot \mu_p}{T_{ox}} \cdot \frac{W_p}{L_p}$

$$t_r \cong k_p \cdot \frac{T_{ox} \cdot L_p \cdot C_L}{\epsilon_{SiO_2} \cdot \mu_p \cdot W_p \cdot V_{DD}}$$

$$t_r \cong k_p' \cdot \frac{L_p \cdot C_L}{W_p}$$

Tecnología específica

$T_{DF} \rightarrow$ TIEMPO DE RETARDO DE BAJADA



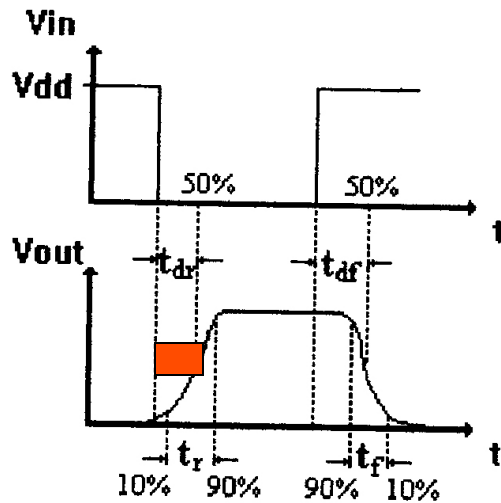
$$t_{df} = \frac{C_L}{\beta_n \cdot V_{DD} \cdot (1 - n)} \left[\frac{2 \cdot n}{1 - n} + \ln(3 - 4 \cdot n) \right]$$

$$t_{df} \cong c_n \cdot \frac{T_{ox} \cdot L_n \cdot C_L}{\epsilon_{SiO_2} \cdot \mu_n \cdot W_n \cdot V_{DD}}$$

Tecnología específica

$$t_{df} \cong c_n' \cdot \frac{L_n \cdot C_L}{W_n \cdot V_{DD}}$$

$T_{DR} \rightarrow$ TIEMPO DE RETARDO DE SUBIDA



$$t_{dr} = \frac{C_L}{\beta_p \cdot V_{DD} \cdot (1 + p)} \left[\frac{-2 \cdot p}{1 + p} + \ln(3 + 4 \cdot p) \right]$$

$$t_{dr} \cong C_p \cdot \frac{T_{ox} \cdot L_p \cdot C_L}{\epsilon_{SiO_2} \cdot \mu_p \cdot W_p \cdot V_{DD}}$$

Tecnología específica

$$t_{dr} \cong C_p' \cdot \frac{L_p \cdot C_L}{W_p \cdot V_{DD}}$$



DISIPACION DE POTENCIA

i_s : Corriente de saturación inversa

V : Voltaje del diodo

q : Carga del electrón

k : Constante de Boltzman

T^o : Temperatura [oK]

$$i_0 = i_s \left(e^{\frac{q \cdot V}{k \cdot T^o}} - 1 \right)$$

POTENCIA ESTATICA



$$P_s = \sum_1^n \text{corriente de fuga} \times \text{voltaje de alimentación}$$

n : Número de dispositivos



POTENCIA DINAMICA

$$P_d = \frac{1}{t_p} \left(\int_0^{t_p/2} i_n(t) \cdot V_{out}(t) \cdot dt + \int_{t_p/2}^{t_p} i_p(t) \cdot (V_{DD} - V_{out}(t)) \cdot dt \right)$$

i_n : Corriente transitoria del dispositivo n

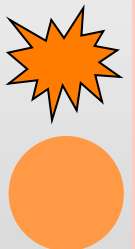
i_p : Corriente transitoria del dispositivo p

$$i_n(t) = C_L \frac{dV_{out}}{dt} \quad i_p(t) = C_L \frac{d(V_{DD} - V_{out})}{dt}$$

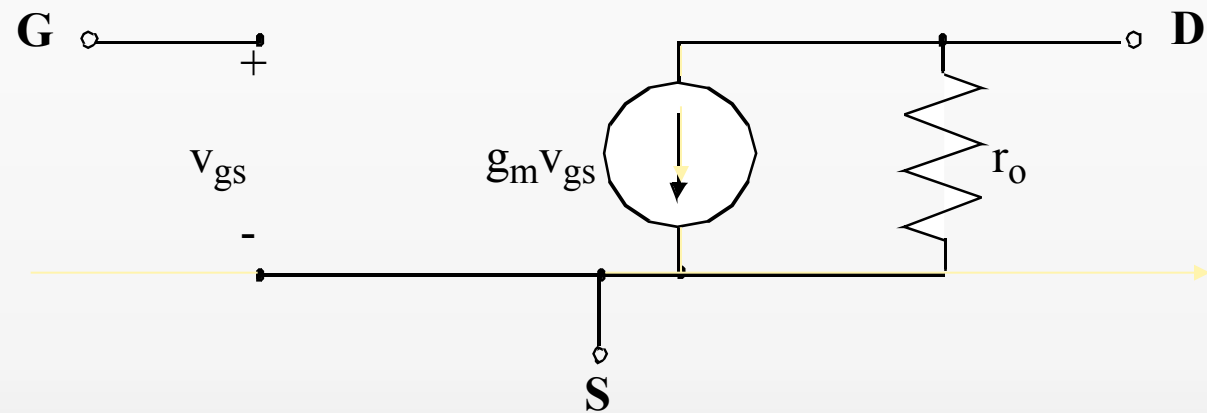
$$P_d = \frac{C_L \cdot V_{DD}^2}{t_p}$$

$$P_d = C_L \cdot V_{DD}^2 \cdot f_p$$

$$P_d = \frac{C_L}{t_p} \left(\int_0^{V_{DD}} V_{out} \cdot dV_{out} + \int_{tV_{DD}}^0 (V_{DD} - V_{out}) \cdot d(V_{DD} - V_{out}) \right)$$



MODELO PEQUEÑA SEÑAL MOSFET

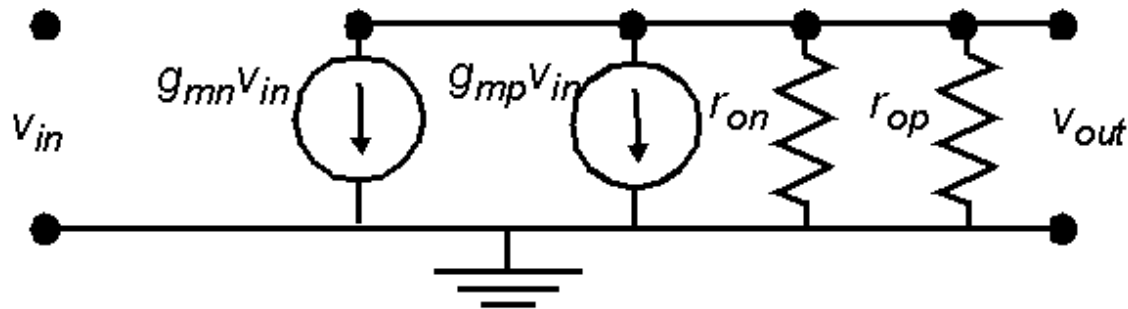


	g_m	r_o
linear	kV_{DS}	$[k(V_{GS}-V_T)V_{DS}]^{-1}$
saturation	$k(V_{GS}-V_T)$	$1/I_D$

DETERMINANDO V_{IH} Y V_{IL}

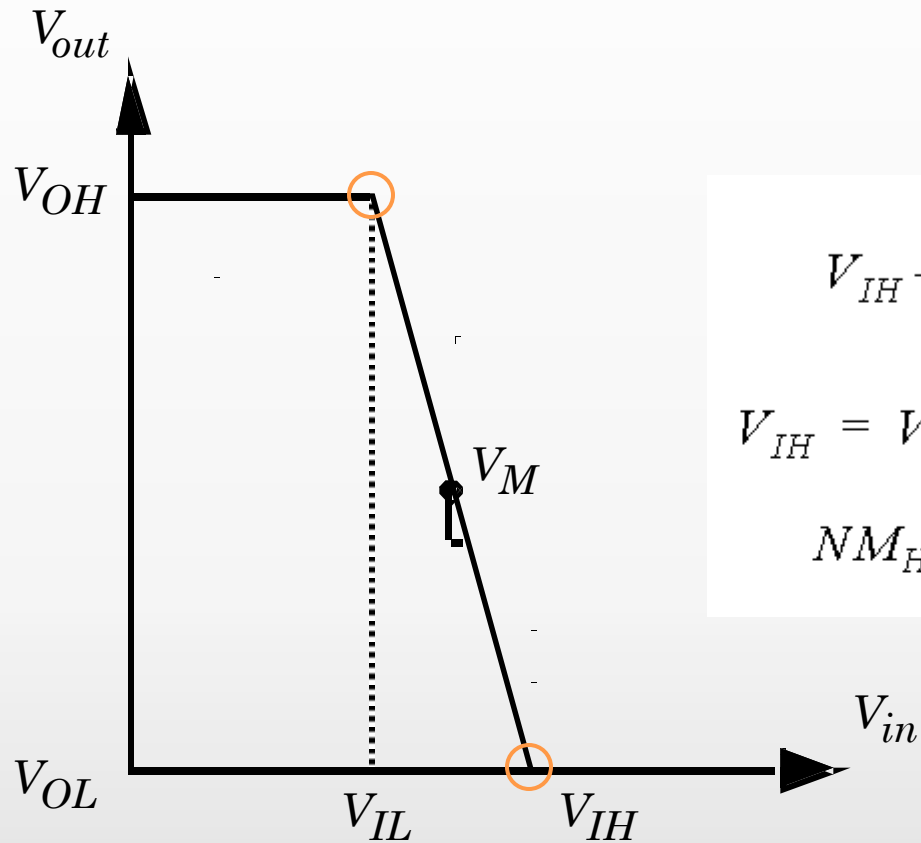
At V_{IH} (V_{IL}): $\frac{\partial V_{out}}{\partial V_{in}} = -1$

small-signal model of inverter



$$g = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp}) \times (r_{on} \parallel r_{op}) = -1$$

MATHTYPE 6.7.ZIP

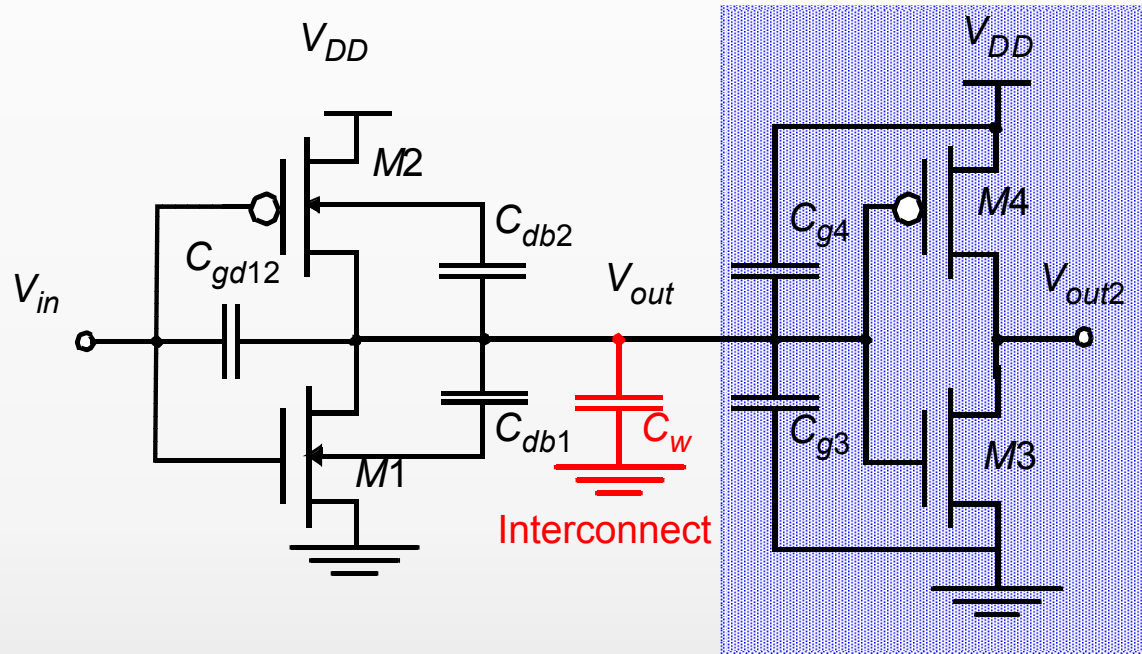


$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$
$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$
$$NM_H = V_{DD} - V_{IH} \quad NM_L = V_{IL}$$

Aproximación simplificada

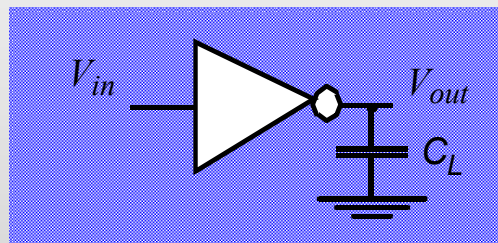


CAPACITANCIAS EQUIVALENTES



Fanout

Simplified
Model



TEMA DE TRABAJO

PROBLEMAS DE CIRCUITOS MICROELECTRONICOS SEDRA/
SMITH :

5.92, 5.93, 5.94, 5.95

