TA 6.4: A Sea-of-Gates FPGA

E. Goetting, D. Schultz, D. Parlour, S. Frake, R. Carpenter, C. Abellera, B. Leone, D. Marquez, M. Palczewski, E. Wolsheimer, M. Hart, K. Look, M. Voogel, G. West, V. Tong, A. Chang, D. Chung, W. Hsieh, L. Farrell, W. Carter

XILINX, Inc., San Jose, CA

The development of field-programmable gate arrays (FPGA) has been characterized by continuing increase in capacity and decrease in cost per gate. In an FPGA, both capacity and cost per gate are direct functions of the silicon area required to implement the logic cells and programmably interconnect them. Traditionally, the logic units and the programmable interconnect have competed for the same silicon area. The pass gates of SRAM FPGA and the dielectric antifuses of conventional antifuse FPGA, both require the use of diffusion[1-4].

This FPGA has programmable interconnect vertically stacked above the logic cells, allowing 2-fold reduction in silicon area while maintaining routability. This FPGA logic architecture is designed to efficiently implement HDL code, an increasingly important attribute as synthesis tools become prevalent in design entry.

The architecture and micrograph are shown in Figure 1. The core is an array of 1,728 configurable logic cells (CLC), logically organized into rows, and surrounded by IEEE 1149.1 compliant I/O cells (IOC). Covering the CLCs (implemented using metal 1 only) are the vertical routing (metal 2), and the horizontal routing (metal 3). Programmable connectivity between routing segments is provided by amorphous-silicon antifuses (MicroVias) constructed between metal 2 and metal 3. MicroVias provide a normally-off state (1GΩ), unless programmed to the on-state (40Ω typical). As shown in Figure 2, the MicroVias reside on top of the transistors that make up the CLC, resulting in programmable connection points without the use of silicon area.

The device employs 728,000 MicroVias, of which <2% are programmed for typical designs. Routing architecture consists of a total of 864 horizontal tracks and 804 vertical tracks, with a total wiring length in excess of 8m. Complete device routability is achieved for commercial designs with 100% CLC utilization. A portion of a synthesized 16b combinational multiplier placed and routed with the automatic tools is illustrated in Figure 3. To maximize viewability, routing is shown alongside the CLC, rather than over them as occurs in the device.

To derive an equivalent sea-of-gates gate array (SOG-GA) capacity for the device, parallel-synthesis is employed, with HDL designs synthesized in both the FPGA and gate array. The ratio of used gate array gates to utilized CLCs gives the capacity per CLC, averaging 3.25 gates. Assuming SOG-GA logic utilization of 50%, 1728 CLCs provide a core logic capacity equivalent to 11k SOG-GA gates. For designs using IEEE 1149.1 boundary scan, an additional 9k SOG-GA gates are required, bringing the equivalent capacity to 20k gates.

The architecture of the CLC, illustrated in Figure 4, achieves variable logic allocation by providing a combinational, synchronous, or buffer function, depending on configuration. Since the FPGA consists of thousands of independently-configurable CLC, this allows any combination of logic functions, up to the capacity of the device. This provides a logic flexibility commensurate with gate arrays, and also simplifies use of the FPGA since placement and floorplanning can be independent of logic types. The CLC configurations are set by configuration-control units (CCU) loaded at power-up from the on-chip MicroVia-programmable PROM.

The key structures in the CLC are a set of four optional input inverters, a selectable combinational logic function, a nearest-neighbor connectivity path, an internal feedback path, and a three-statable output driver. Optional input inverters provide universal and efficient inversion. With all inputs on the device invertable, output inversion can be eliminated in hardware, since all destinations is automatically inverted in the design software. The CLC logic function is selectable between a 4-input AND and a 4-input sum-of-products (SOP). The AND, along with its DeMorgan equivalents, provides single-level logic functions (AND, NAND, OR, NOR), while the SOP provides two-level logic functions (sum-of-products, product-of-sums, XOR, XNOR, MUX).

The nearest-neighbor connectivity path of the CLC mitigates the area-delay architectural tradeoff. Conventionally, the fan-in of an FPGA core logic cell is made narrow to minimize silicon area, or wide to minimize delay. Given differing area and delay requirements between designs and in a single design, it is advantageous to adjust fan-in as needed. The nearest-neighbor connection of the CLC does this, allowing nearest-neighbor CLC within the row to be optionally ganged to create high fan-in logic cells. Performance of these cells is understood by the synthesis tools, and they are selected automatically when delay minimization is required.

An optional internal feedback path in conjunction with the SOP combinational function facilitates a CLC latching function. The feedback path uses no programmable interconnect, providing fanout-independent setup and hold delays. Flip-flops combine a master and slave latch, connected via the nearest-neighbor path. When combined with the programmable input inversion, flip-flops and latches of all clock and reset polarities can be built. A power-on reset function initializes all CLCs configured as latches or flip-flops. The CLC output driver can be optionally three-stated by an input signal, allowing the CLC to be configured as a three-state buffer.

Waveforms of a 16b synchronous counter programmed into the device, operating at a clock period of 6.66ns are shown in Figure 5.

All programming and test functions are through a dedicated IEEE 1149.1 boundary scan port and a Vpp pin. Selection of the MicroVia to be programmed is via the port, with programming initiated by an 11V pulse on the Vpp pin. Voltage sensing circuits on the Vpp pin initiate an internal programming sequence. Resistance of the programmed connection is determined by circuits external to the FPGA in programming hardware. A IEEE 1149.1 instruction set is implemented, including IDCODE and USERCODE. The latter instruction provides access to a user-programmable 32b device identification register.

The device is fabricated using a 0.75μm, triple-layer metal CMOS process, with 2 additional masking layers. A MicroVia layer defines the programmable connections between second and third metal, while an additional implant provides the high-voltage nMOS transistors used in programming. The MicroVia characteristics are identified in Table 2.

References

[1] Carter, W., et al., "A User Programmable Reconfigurable Gate Array," IEEE CICC, 1986.

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[3] Hsieh, H.C., et al., "Third Generation Architecture Boosts Speed and Density of FPGA," EEE CICC, 1990.

[4] Ahrens, M., et al., "An FPGA Architecture Optimized for High Densities and Reduced Routing Delay," IEEE CICC, 1990.

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Figure 1: See page 346.

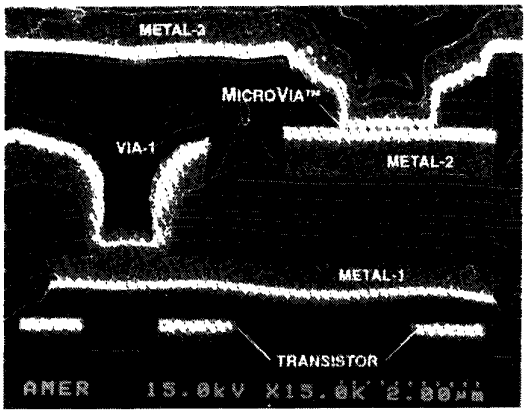

Figure 2: Process cross-section of sea-of-gates FPGA

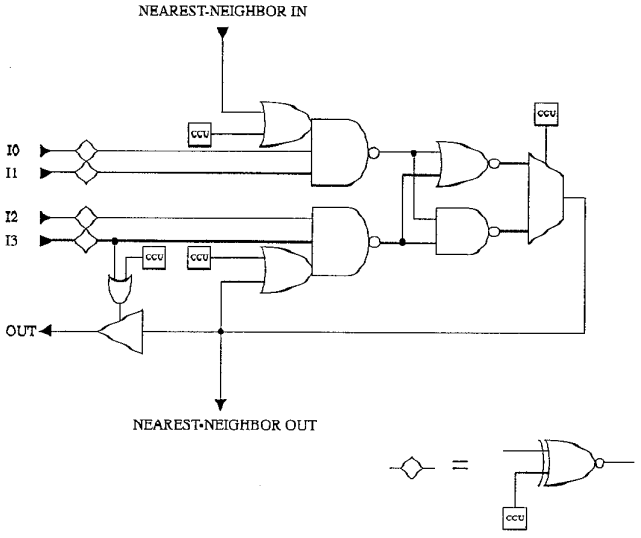

Figure 4: Configurable logic cell (CLC) architecture.

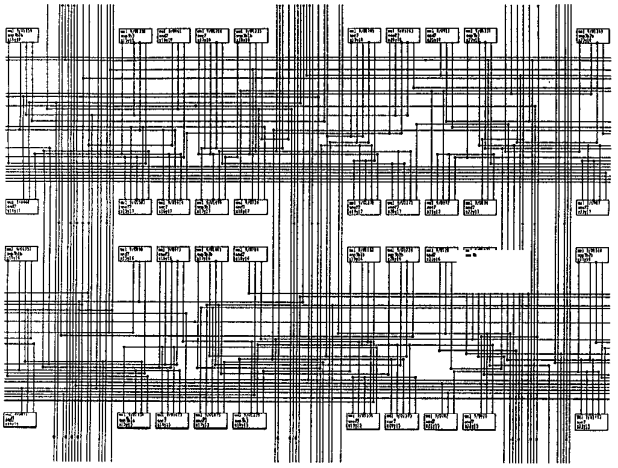

Figure 3: Place & route view of part of 16b combinational multiplier.

Construction	Metal 2-to-metal 3
Area	1.0x1.0µ m²
Off resistance	>1GΩ
On resistance:	40Ω
Filament area (typ.)	0.25x0.25µm²
Capacitance	2.0fF
Programming voltage	11.0V
Programming time	10ms

Table 2. Microvia characteristics.

Acknowledgements

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Gate array capacity	11k gates, 20k using boundary scan
Usable core gates	5.6k usable (1728 CLCx3.25 gates/CLC)
Routing capacity	8m interconnect, 728,000 MicroVias
Technology	0.75µm CMOS, 3-layer metallization,
MicroVia	amorphous-silicon metal-metal antifuse
Elements	1.2M (transistors and MicroVias)
Die size	7.2x6.6mm²
Supply voltage	3.3V, 5V
Power	DC: 15mW
	AC: design-dependent

Table 1. Sea-of-Gates (SOG) FPGA device characteristics.

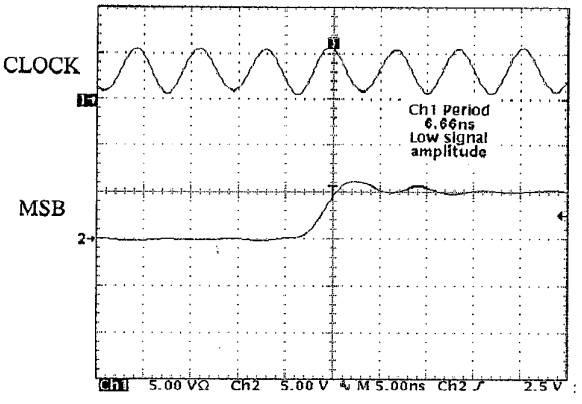

Figure 5: Operating waveforms of 16b counter (clock period = 6.66ns).

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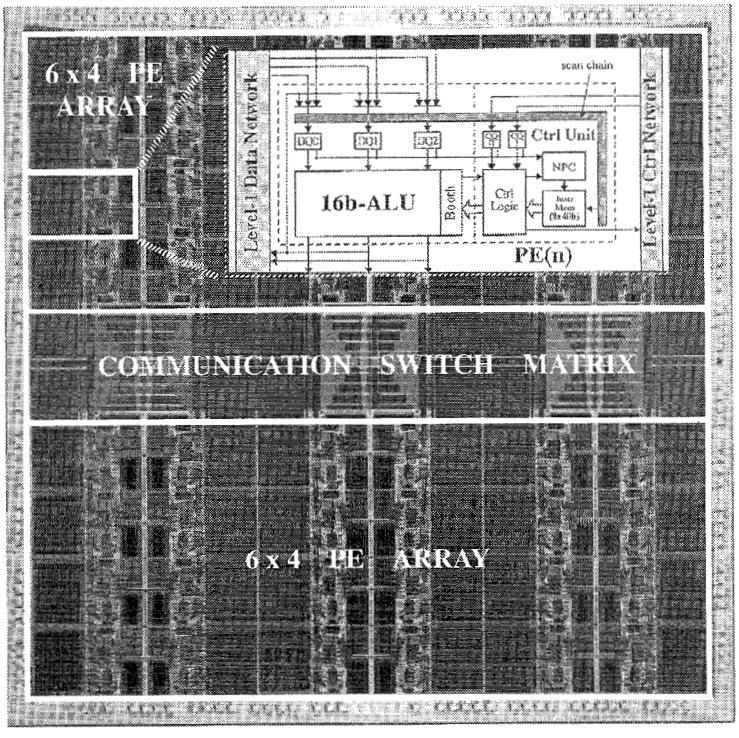

Figure 3: PADDI-2 chip micrograph.

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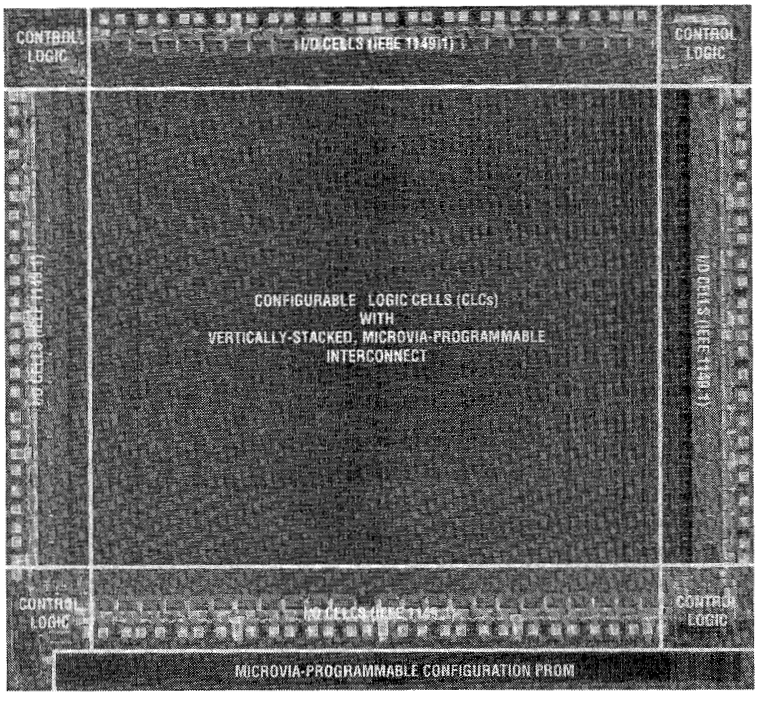

Figure 1: Sea of gates FPGA micrograph.