A Sea-of-Gates Architecture Based on VLSI System Design Requirements

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Abstract *- This paper presents a 1.0 μm double-metal layer CMOS sea-of-gates architecture based on requirements common to the entire VLSI application area instead of a specified field. These requirements include reduction of power consumption, transparent to design flow, be able to design circuits with densities limited only by the used technology, reduce the delay of critical paths and solve complex routing problems. The results of benchmark circuits will be presented to illustrate the functionality of the architecture.*

1. Introduction

The sea-of-gates design style has been widely accepted as a powerful method to produce integrated circuits with reduced design and fabrication times and costs. This design style is based on the use of a prefabricated array of transistors. Within this array, the dimensions, the locations and the arrangement of the transistors are fixed. Wiring is put on top of these transistors to personalize the integrated circuit. The used technology is also fixed. In order to be able to design high-performance VLSI circuits, some strict demands have to be made upon the used sea-of-gates architecture.

Over the past years, many sea-of-gates master array architectures have been presented [1-4]. These sea-of-gates architectures are all more or less based on some characteristics derived from intended application fields or logic implementation structures. The architectures have been tuned to the intended application field or logic implementation structure. For example, a common-gate architecture and the inclusion of extra transistors have been used to increase the density of memory structures [1-3]. Enlarged transistors have been used to increase the wiring possibilities [1] and extra n-channel MOS transistors have been added to support dynamic logic [2,3]. Even non-orthogonal transistor structures have been provided to support a two-dimensional design approach [3,4].

With growing system complexity, the need for more variations in the logic system functions within a single design will increase. The distinction between various applications will become more fuzzy in the future. New system architectures will also be developed to meet system specifications. Sea-of-gates architectures based on characteristics of specific application fields will not be able to cope with this growing complexity. More general design requirements have to be used to design sea-of-gates architectures. These requirements must cover the entire VLSI area.

In this paper a sea-of-gates architecture will be described based on these general design requirements.

2. Architectural Requirements

To be able to use the sea-of-gates architecture for complex VLSI circuits, the architecture must be based on basic, application field independent design requirements. These general high-performance VLSI design requirements for a sea-of-gates architecture are:

- reduction of the power consumption,
- independent of circuit implementation, logic structure and system architecture,
- possess the potential to design circuits with densities limited only by the used technology.

These are non-conflicting requirements and are all essential for efficient VLSI design.

Speed and routability are no primary requirements that should be taken into account during the design of the sea-of-gates architecture. Speed is very design dependent. The maximum system

frequency or throughput is determined by critical paths within a design. Only the speed of these paths has to be improved to meet the specifications. Several methods exist to reduce the delay:
- reducing the delay within logic cells by placing transistors in parallel,
- enlarging the fanout drive capability of logic cells by placing transistors in parallel,
- inserting buffers between logic cells to drive large load capacitances.

To show the strength of placing transistors in parallel some propagation delay simulations have been carried out using a two-input nand-gate loaded with four inverters and additional 200fF to account for wiring capacitance. The results are shown in table 1. To obtain the same delay with the use of single transistors, very large transistor widths must be used. This is a result of the fact that in a sea-of-gates array all the transistors have the same width, so the increased transistor widths applies also to the load gates. Furthermore the power consumption will increase and the transistor density will decrease.

Routability is also very design dependent. Even within a single design the routing demands may differ very widely and no general routing characteristics can be derived applying to complex VLSI designs. As a result, built-in routing possibilities will be unused or will be too small. For efficient routing the sea-of-gates architecture must only provide efficient means to increase the wiring space where needed.

3. Sea-of-Gates Architecture

In this section the resulting sea-of-gates architecture will be described. The architecture is based on a dense, uniform array of transistors. This has been achieved by a compact layout of the array transistors. The connectability areas of the source, drain and gate have been based on minimum connectability demands. This results in small-sized transistors which is important with regard to the reduced power consumption requirement. A continuous diffusion row with transistors helps to increase the transistor density. This increases also the flexibility of selecting the isolation locations between logic cells. Beside the pMOS and nMOS transistor no specific or extra transistor structures have been incorporated. These structures would destroy the uniformity and generality of the architecture. Figure 1 shows the layout and arrangement of four transistor pairs.

The overall array architecture is based on a row-oriented floorplan. Adjacent rows have been mirrored to share common power and ground rails. The sharing of common power and ground rails increase the overall transistor density. Table 2 shows some characteristics of the architecture based on the use of a 1.0 μm double-metal layer CMOS process.

Through the use of small-sized transistor pairs and the use of transistor isolation, the architecture is very efficient in allocating space needed for wiring channels without reserving too much overhead. This is a very important characteristic of the architecture when dealing with very complex and varying routing problems.

4. Circuit Design Examples

To illustrate the functionality of this sea-of-gates architecture, the design of some benchmark circuits is described. These circuits are selected to test the architecture for several aspects of VLSI design. The circuits are:
- static random access memory [5]: distributed on-chip memory becomes more and more important for complex systems and hence a flexible and efficient memory design is very important,
- systolic array circuit for matrices multiplication: this circuit incorporates aspects such as local storage of data, clock line and data line feed through and the use of regularity and hierarchy to reduce the design complexity; the systolic array has a complexity of 150 logic gates (logic gate: a two-input nand-gate consisting of 4 MOS transistors),
- arithmetic and logical circuit [5,6]: the 74F382 Arithmetic Logic Unit has been used to test a MSI-level circuit implementation of basic arithmetic and logic functions; the ALU has a complexity of 149 logic gates,
- multiplier design [1]: a ten-by-ten bit fully pipelined multiplier; the placing of the logic gates has been taken from an existing standard cell design; the multiplier has a complexity of 5.4 K logic gates and this circuit has been used to test automatic routing.

In all examples a 1.0 μm double-metal layer CMOS process has been used for the design of these circuits. No stacked contacts and vias are allowed within this process.

4.1 Static Random Access Memory

The 6-transistor SRAM CMOS memory-cell is a very powerful example to test the wirability of the architecture. This is because of the huge amount of wire segments (feedback connection, access transistor connection, word line and the bit lines) needed to implement a memory-cell. Furthermore, the word and bit lines within one cell must be designed such, that these lines are connected by abutment within the memory array.

The sea-of-gates architecture allows several memory architectures to be implemented, all with the same density. This is very important because the memory architecture will not be determined by the sea-of-gates architecture, but by the demands of surrounding on-chip functions.

Figure 2 shows the possible memory-cell designs. The basic 6-transistor memory cell occupies two transistor rows. The word and bit lines are indicated in the figure.

4.2 Systolic Array Circuit for Matrices Multiplication

This circuit performs the multiplication of two 2x2-matrices. The systolic array has been build using a basic processor element (BPE) several times with local connections between these BPEs. A BPE consists of four master/slave flip-flops and an arithmetic circuit to perform the multiplication and the addition. A two-phase nonoverlapping clock has been used. The two master clocks are distributed with local buffers to generate the complementary clock signals. The BPE has been designed to provide the necessary feed through tracks of data and clock lines. Figure 3 shows the layout of a BPE.

The area of the systolic array (7 BPEs) is 0.1 mm^2. The transistor utilization of this circuit is 82% (inclusion of necessary isolation transistors) and 58% without any isolation transistor.

4.3 Arithmetic and Logic Unit

The layout of the ALU is shown in Figure 4. This circuit layout shows a characteristic feature of circuit design. The required routing space varies within a single design. At places with a lot of interconnecting lines, wiring boxes have been allocated to incorporate these lines efficiently within the total design.

The area of ALU is 0.13 mm^2. The transistor utilization is 59% (inclusion of necessary isolation transistors) and 45% without any isolation transistor.

4.4 Multiplier

A wiring box allocation program has been used to create wiring boxes at congestion sites within the multiplier design. The area of the multiplier is 7.4 mm^2 (58% of the area has been allocated for routing). Additional routing experiments are being carried out to decrease the occupied area by a refinement of the placement, the allocated wiring boxes and the router cost function.

5. Conclusions and Future Work

A sea-of-gates architecture has been presented. This architecture is very suitable for complex VLSI design. Where as other architectures restrict application fields and routing flexibility at forehand, the presented architecture goes a level beyond by being routing and application field independent. This has been achieved by a compact and uniform layout of the sea-of-gates transistors.

The architecture will also be tested for a triple-metal layer CMOS process. Higher circuit densities will be achieved because the allocated wiring space can be moved to the third metal layer.

Acknowledgments

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Table 1

configuration	propagation delay [ns]
single transistors	1
two transistors parallel	0.5
three transistors parallel	0.4

two-input nand-gate; load: 4 inverters + 200fF wiring capacitance
W_n = 6.5 µm, W_p = 11.5 µm, technology: 1.0 µm double-metal layer CMOS process

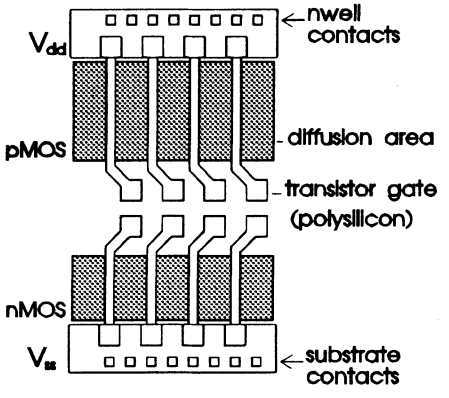

Figure 1. Layout of four transistor pairs.

Table 2

transistor pair dimensions	39.75µm x 5µm
transistor pair area	198.75µm^2
width pMOS	W = 11.5µm
length pMOS	L = 1.0µm
width nMOS	W = 6.5µm
length nMOS	L = 1.0µm
W_p / W_n	1.77
logic density	1.89k gates/mm^2
ROM density	6.7k cells/mm^2
SRAM density	628 cells/mm^2

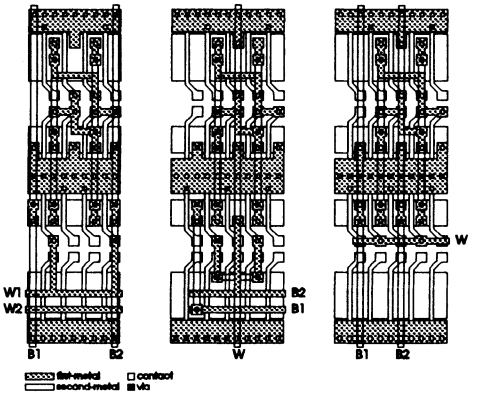

Figure 2. Memory-cell layouts.

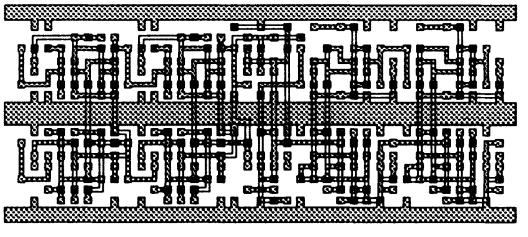

Figure 3. BPE layout.

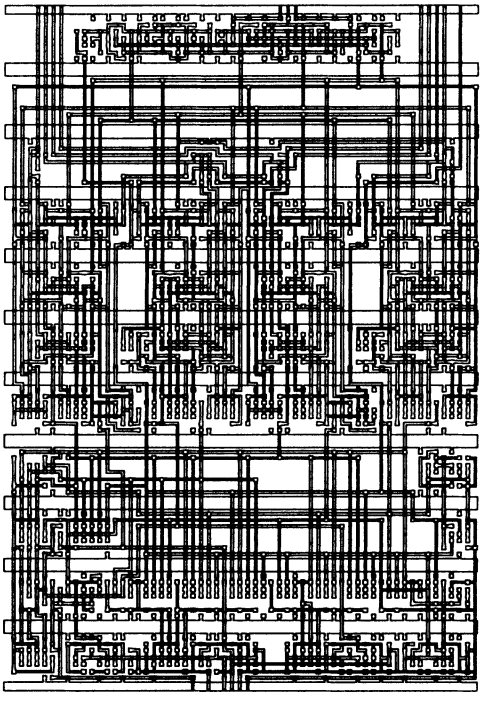

Figure 4. ALU layout (metal1 and 2 only).