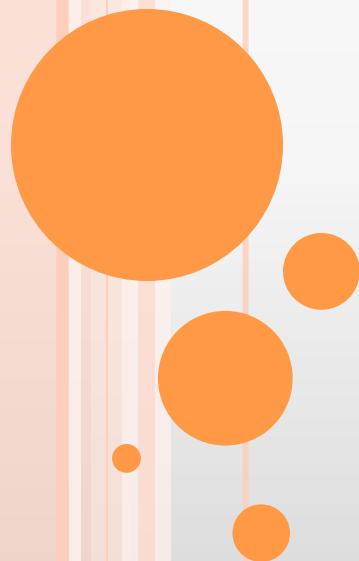
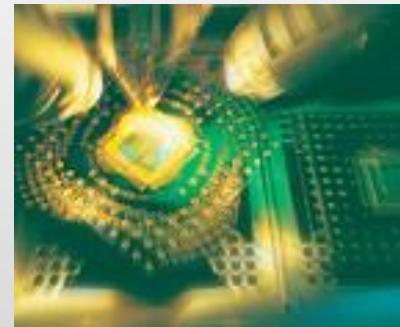


TECNICAS DE INTEGRACION



Ing. Iván Jaramillo J.
ijaramilloj@unal.edu.co
www.gmun.unal.edu.co/~ijaramilloj

II-2013



CLASIFICACIÓN DE LOS MATERIALES

Gap de Energía (eV)

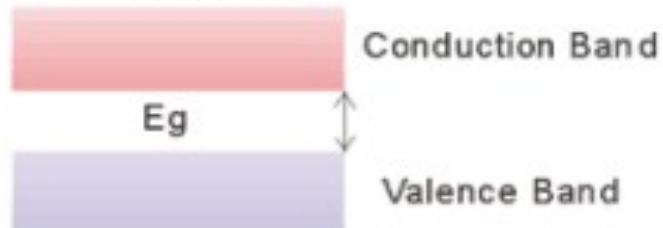
Aisladores	eV	Semiconductores	eV
Diamante	5,33	Silicio	1,14
Oxido de Zinc	3,2	Germanio	0,67
Cloruro de Plata	3,2	Telurio	0,33
Sulfuro de Cadmio	2,42	Antimonio de Indio	0,23

Tabla 1 Gap de energía de algunos aisladores y semiconductores.

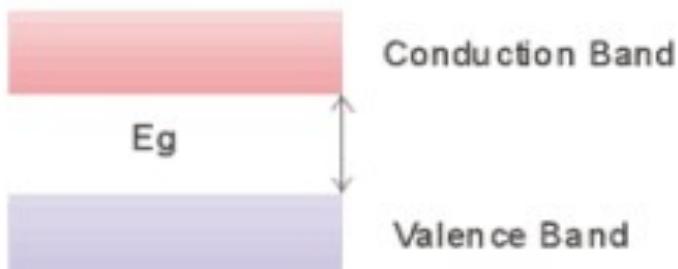
Metals



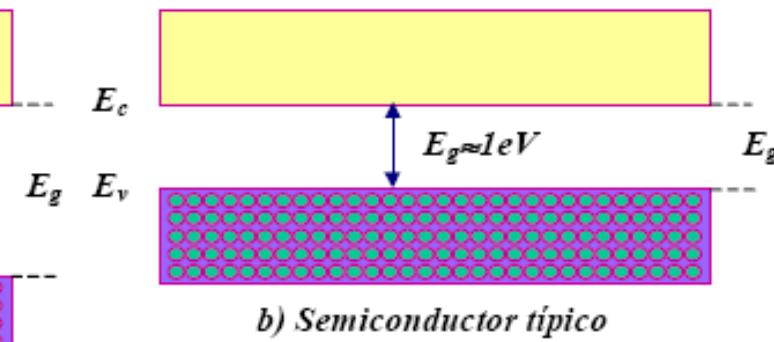
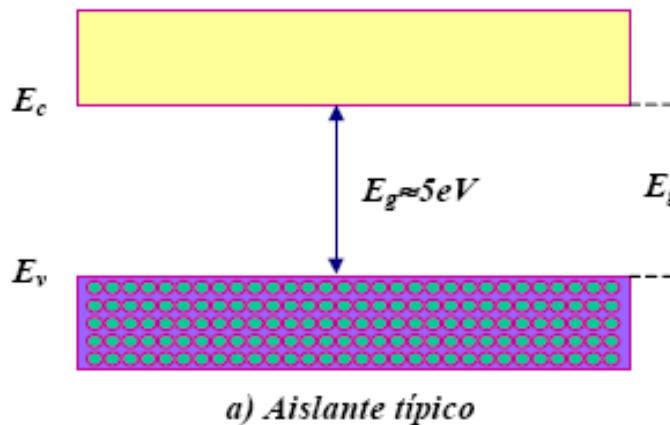
Semiconductors



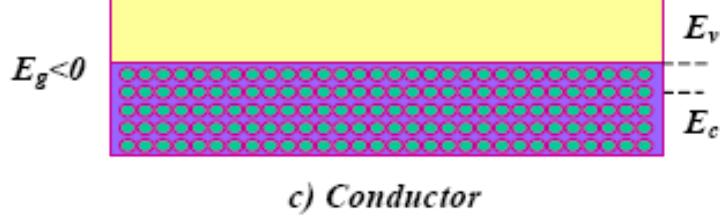
Insulators



BANDAS DE ENERGÍA



b) Semiconductor típico



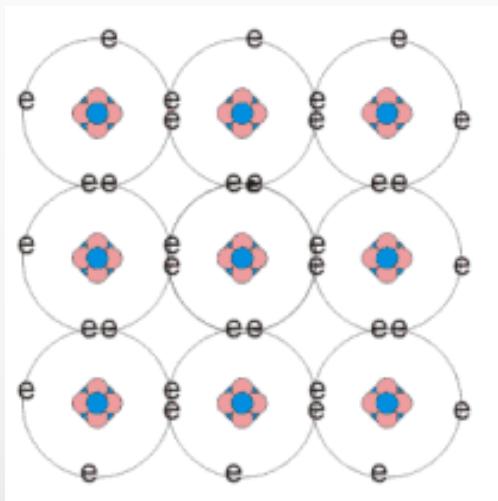
c) Conductor

BANDAS DE ENERGÍA – VALORES TÍPICOS

<i>Símbolo</i>	<i>Nombre</i>	<i>Ancho BP (eV)</i>	<i>Mov. elec. (cm²/V.s)</i>	<i>Mov. huecos (cm²/V.s)</i>	<i>Dist. crist. (Å)</i>
<i>SPb</i>	<i>Galena</i>	0,37	575	200	5,93
<i>SZn</i>	<i>Blenda</i>	3,60	110	-	5,41
<i>Ge</i>	<i>Germanio</i>	0,67	3900	1900	5,65
<i>Si</i>	<i>Silicio</i>	1,11	1350	480	5,43
<i>AsGa</i>	<i>Arseniuro de Galio</i>	1,43	8500	400	5,65

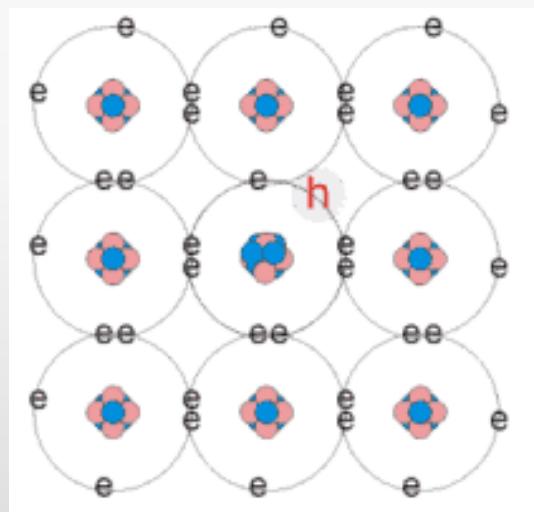


ADICIÓN DE IMPUREZAS

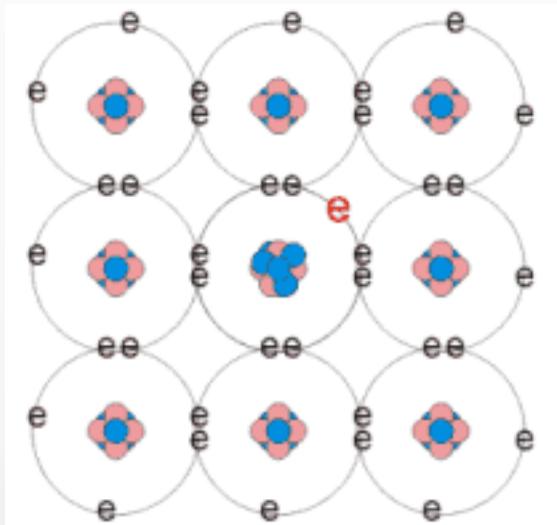


Aceptores:
Grupo III

Boro
Galio
Indio



TIPO-N

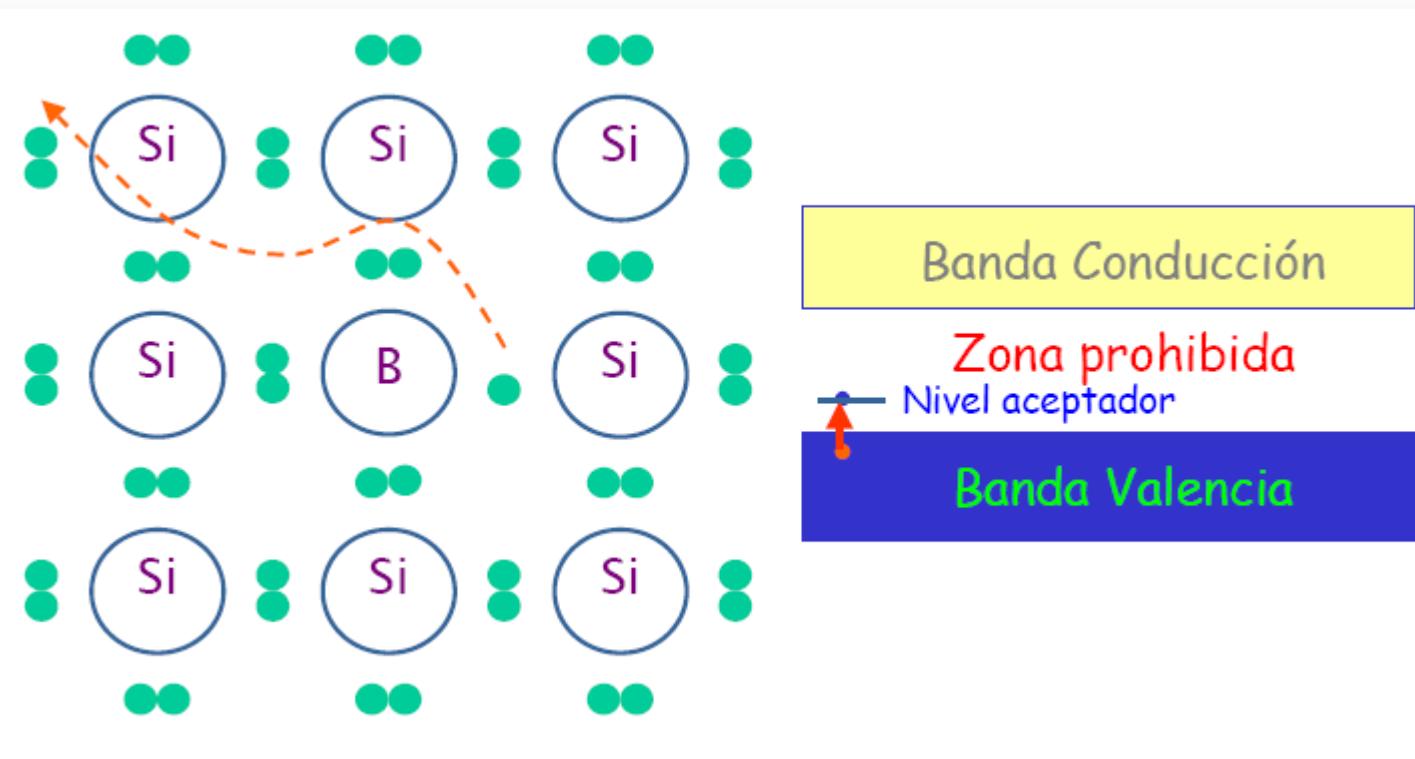


Donadores:
Grupo V

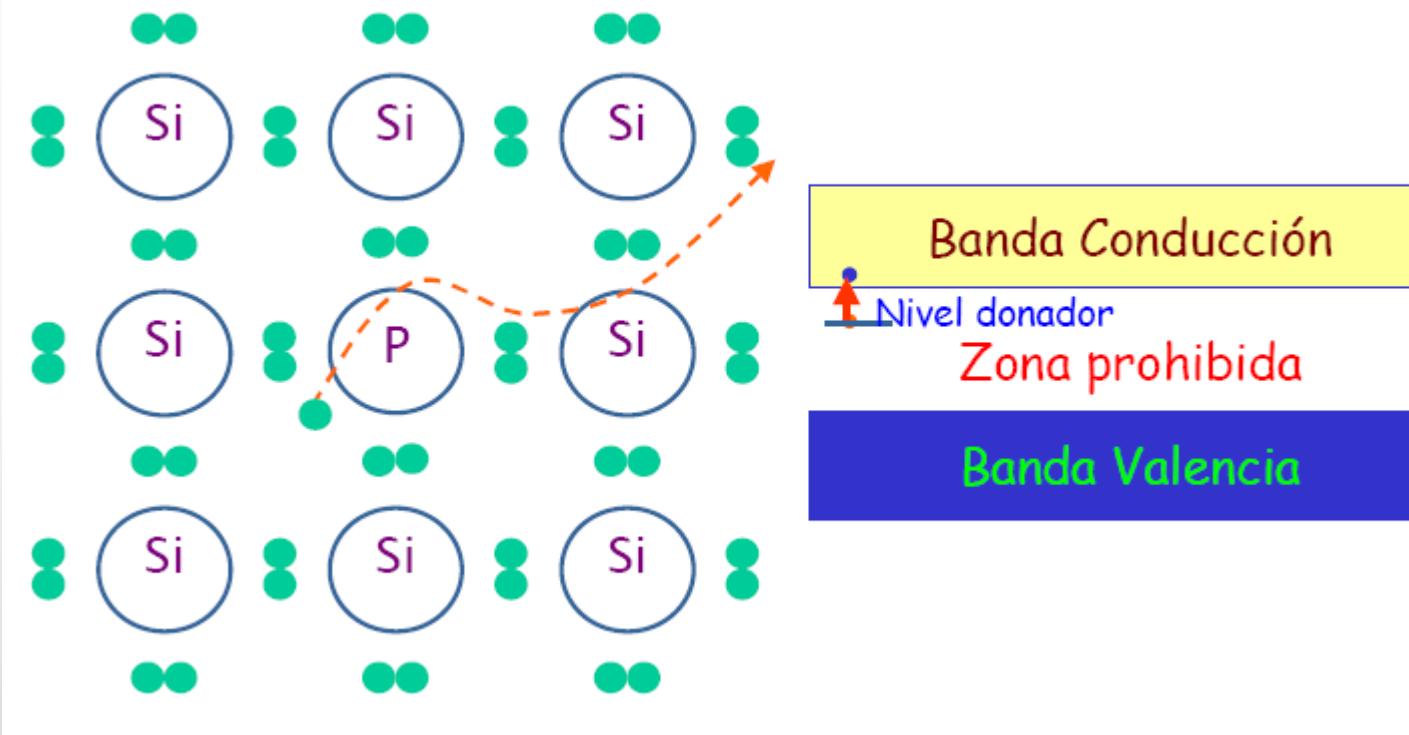
Antimonio
Arsénico
Fósforo



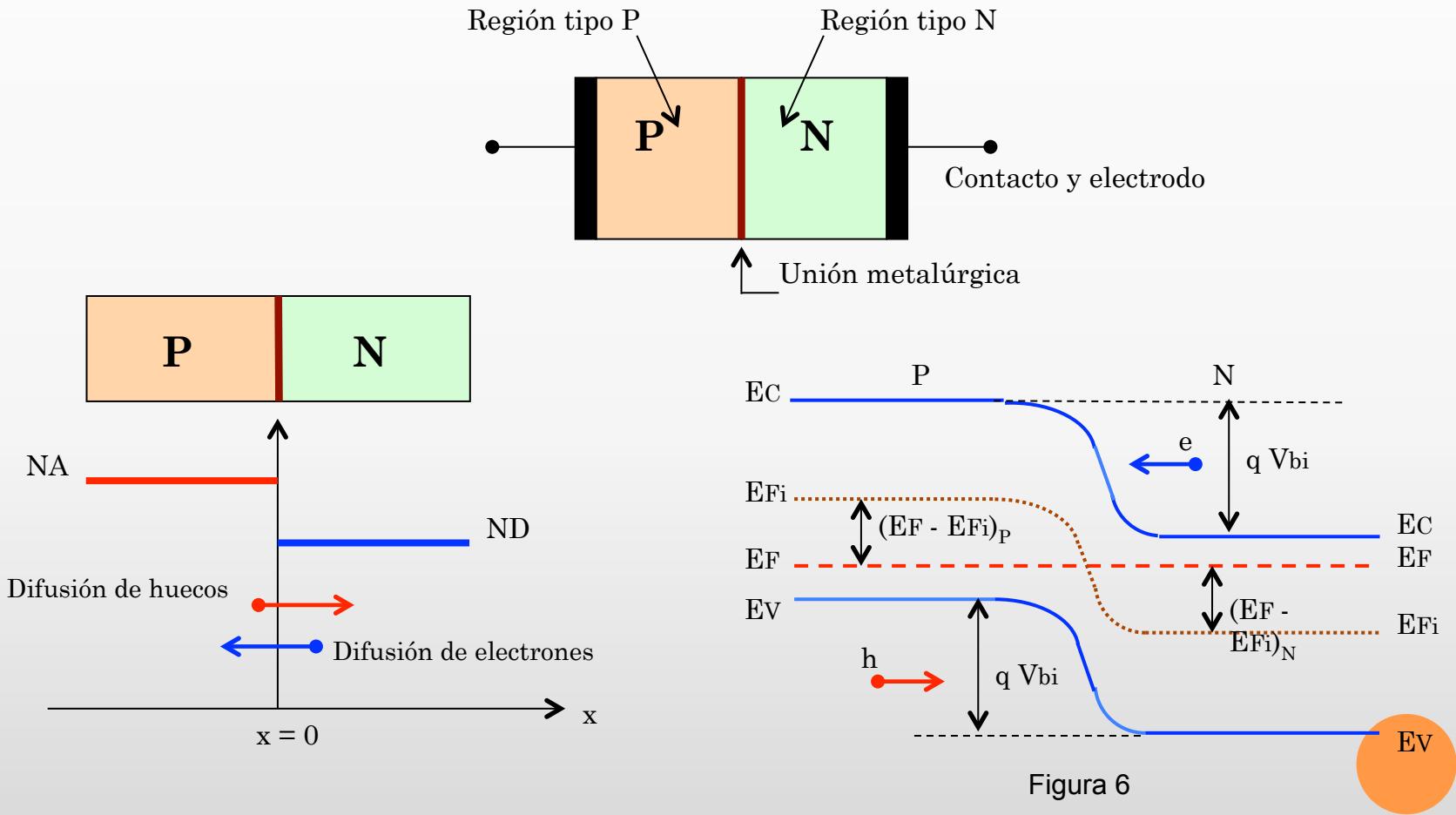
MATERIALES TIPO P



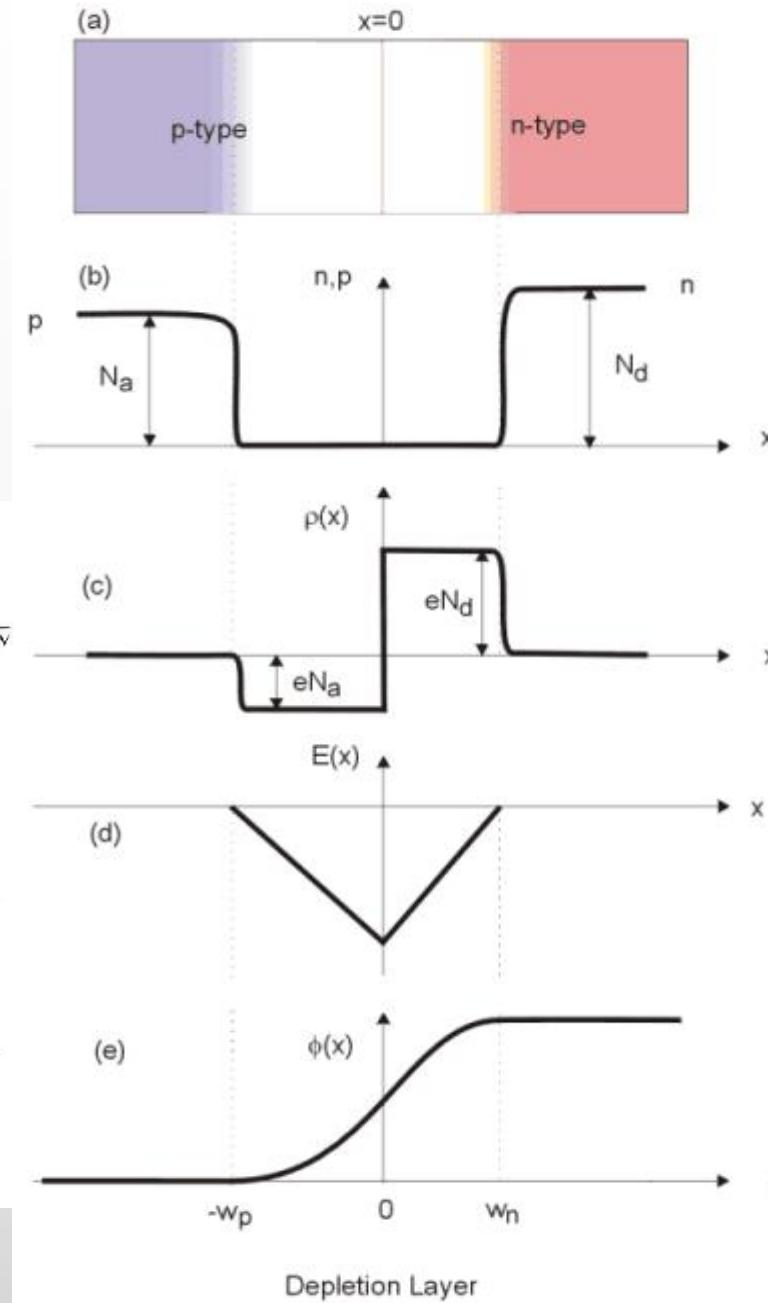
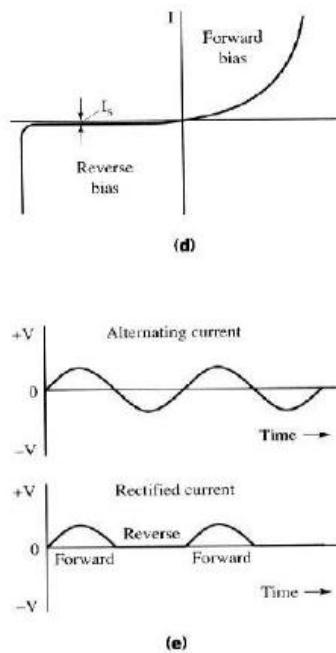
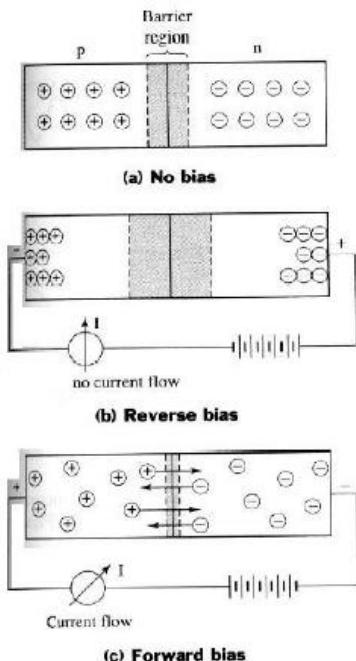
MATERIALES TIPO N



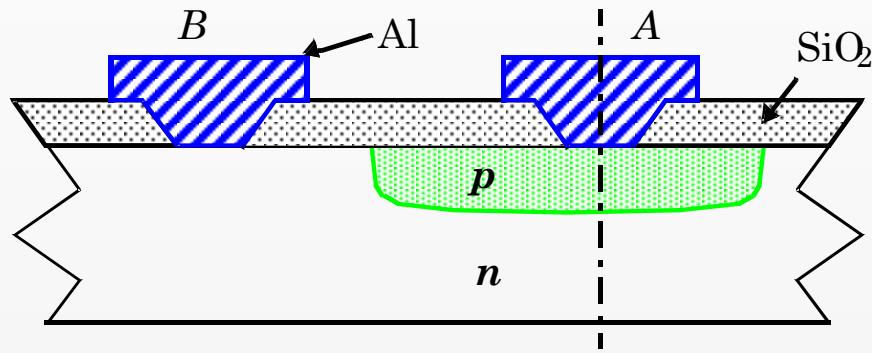
JUNTURA PN



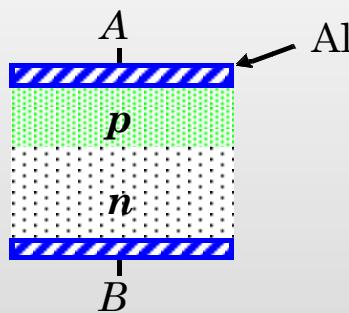
COMPORTAMIENTO JUNTURA PN



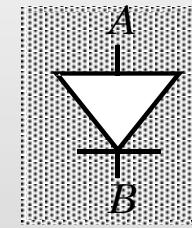
EL DIODO



Cross-section of -junction in an IC process

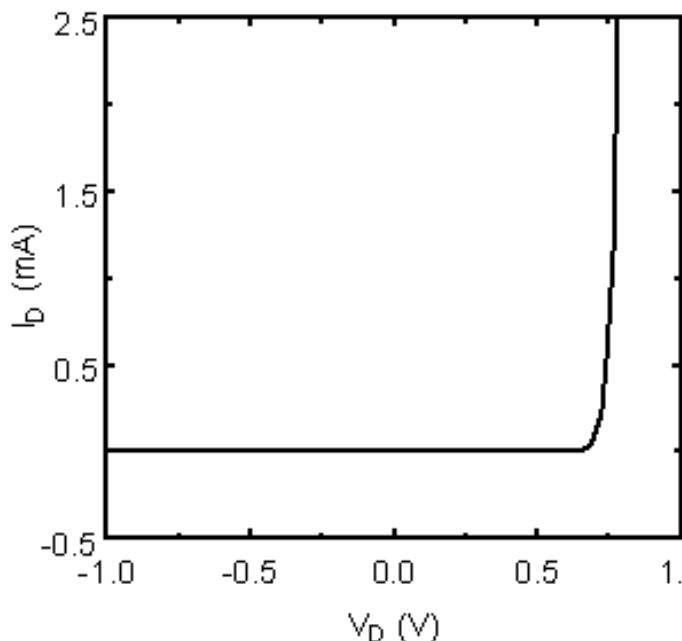


One-dimensional
representation

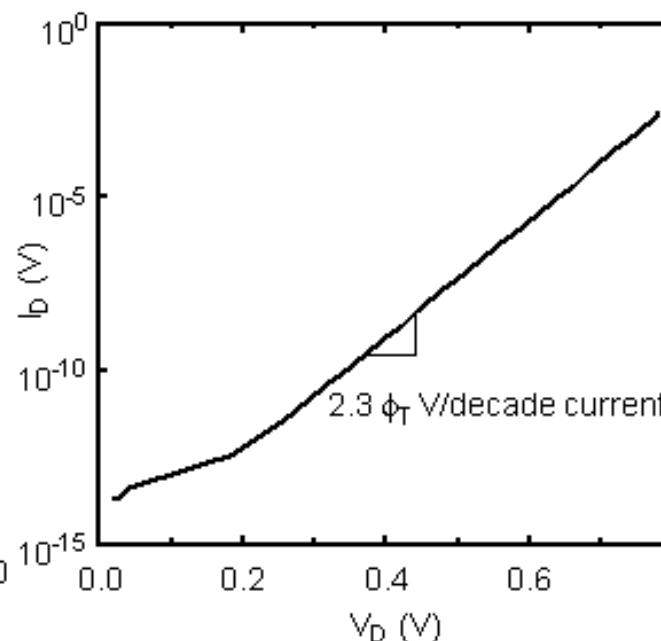


diode symbol

RESPUESTA DEL DIODO



(a) On a linear scale.

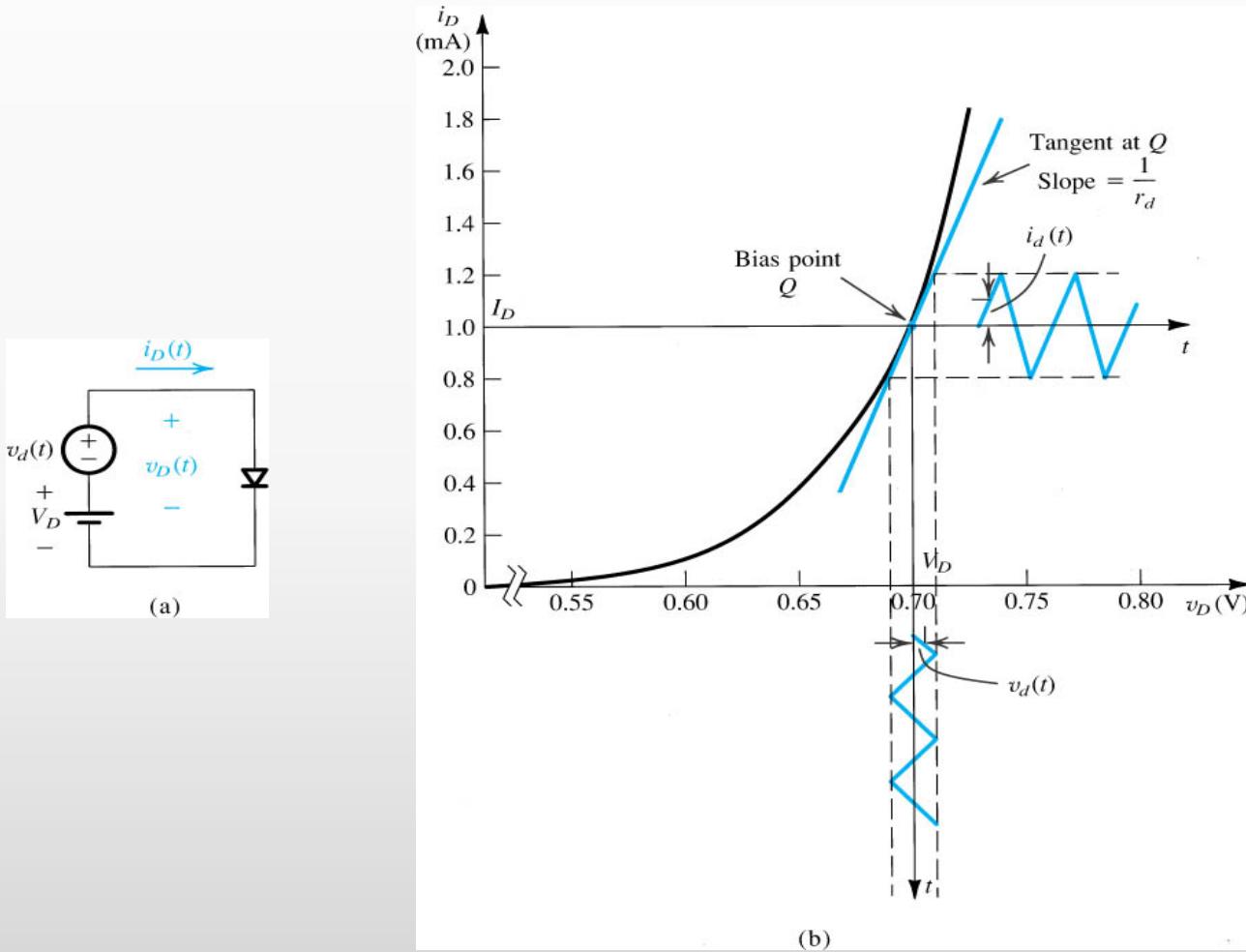


(b) On a logarithmic scale (forward bias).

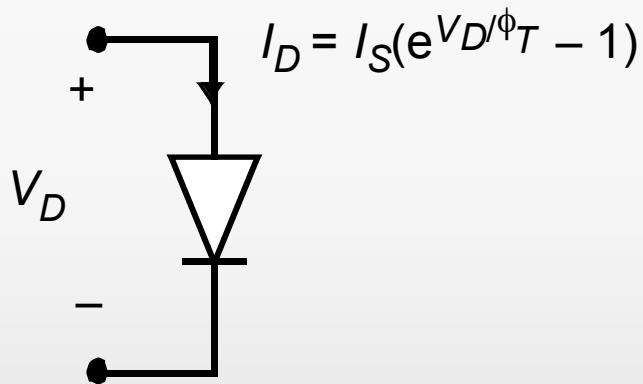
$$I_D = I_S \left(e^{V_D / \phi_T} - 1 \right)$$



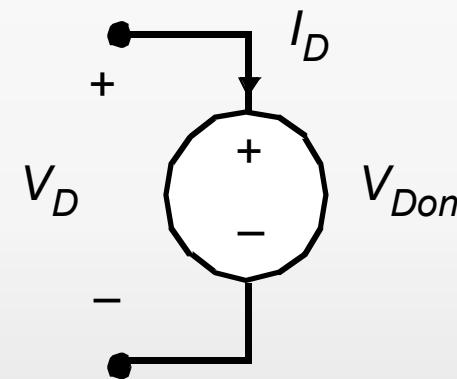
COMPORTAMIENTO DINÁMICO DEL DIODO



MODELOS DEL DIODO



(a) Ideal diode model



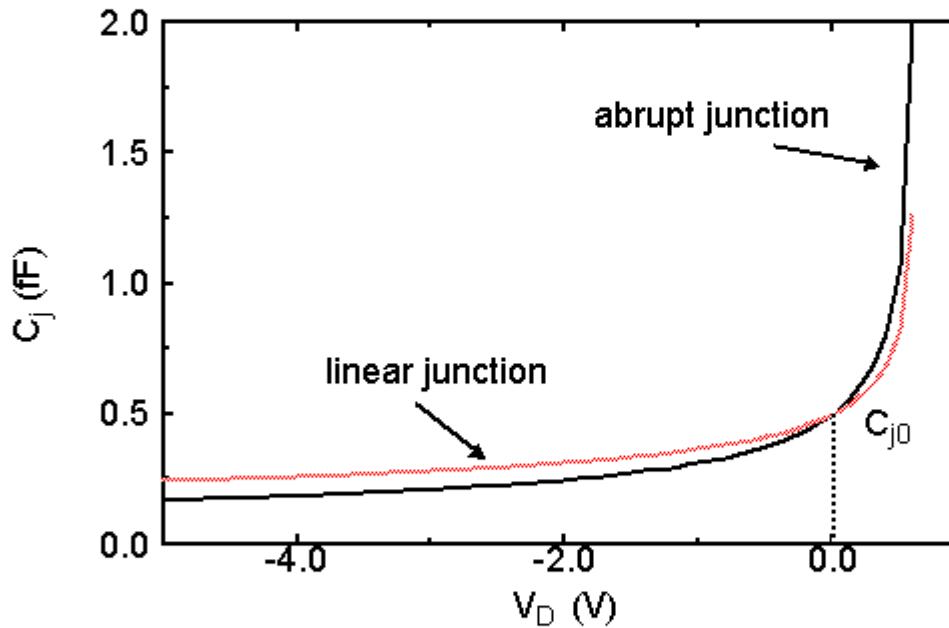
(b) First-order diode model

PARÁMETROS SPICE

Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E-14
Emission coefficient	n	N	-	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	sec	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	-	0.5
Junction potential	ϕ_0	VJ	V	1

First Order SPICE diode model parameters.

CAPACITANCIA DE JUNTURA

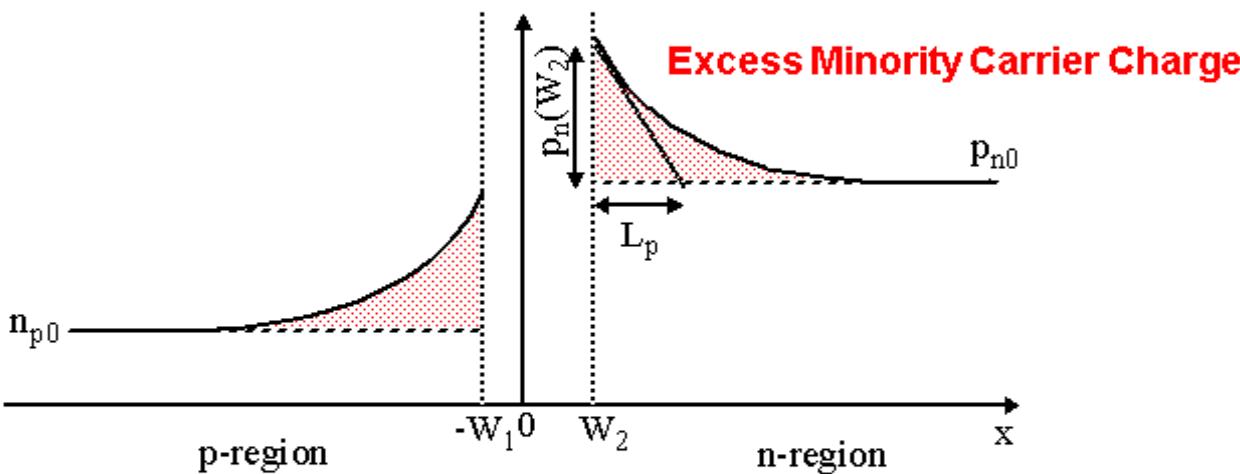


$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$m = 0.5$: abrupt junction
 $m = 0.33$: linear junction



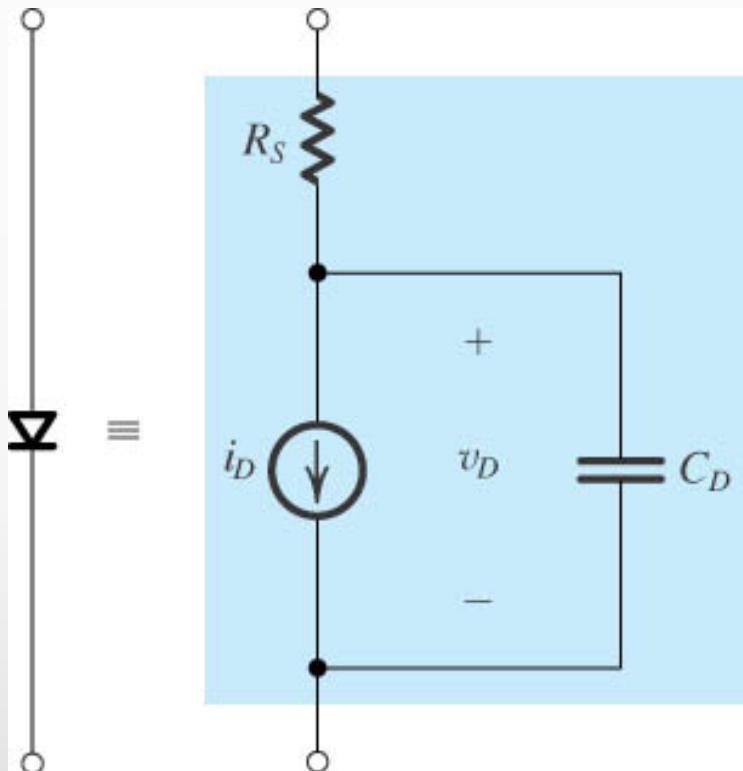
CAPACITANCIA DE DIFUSIÓN



$$C_d = \frac{dQ_D}{dV_D} = \tau_T \frac{dI_D}{dV_D} \approx \frac{\tau_T I_D}{\phi_T}$$



MODELO SPICE



$$i_D = I_S (e^{v_D/nV_T} - 1)$$

$$C_D = C_d + C_j = \frac{\tau_T}{V_T} I_S e^{v_D/nV_T} + C_{j0} \left(1 - \frac{v_D}{V_0}\right)^m$$

APROXIMACION EN SISTEMAS DIGITALES

Cambios abruptos en la tensión



PROYECTO FINAL - ASIGNACIÓN

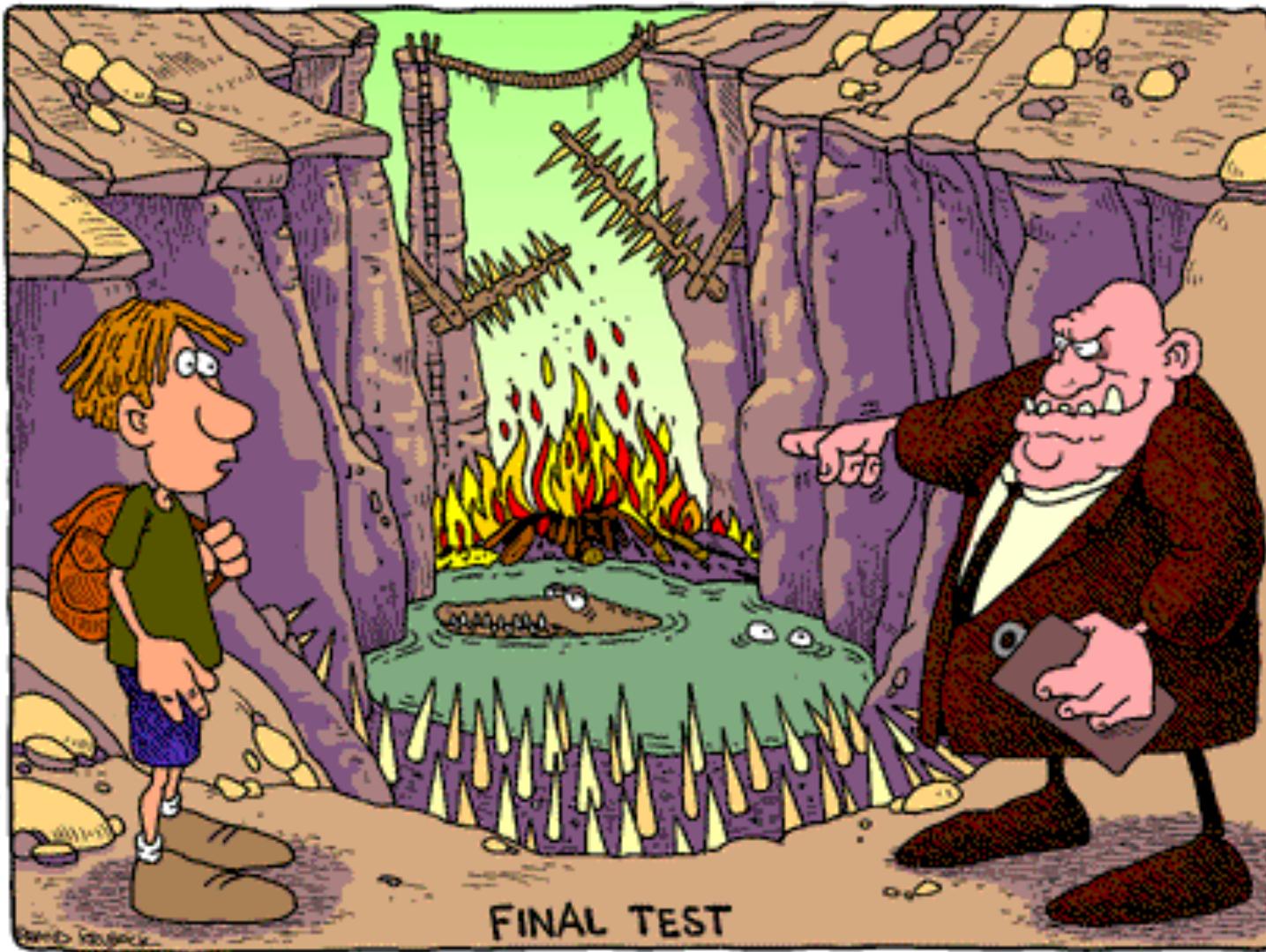
- Temas por definir
- Dos proyectos por grupo



CRONOGRAMA

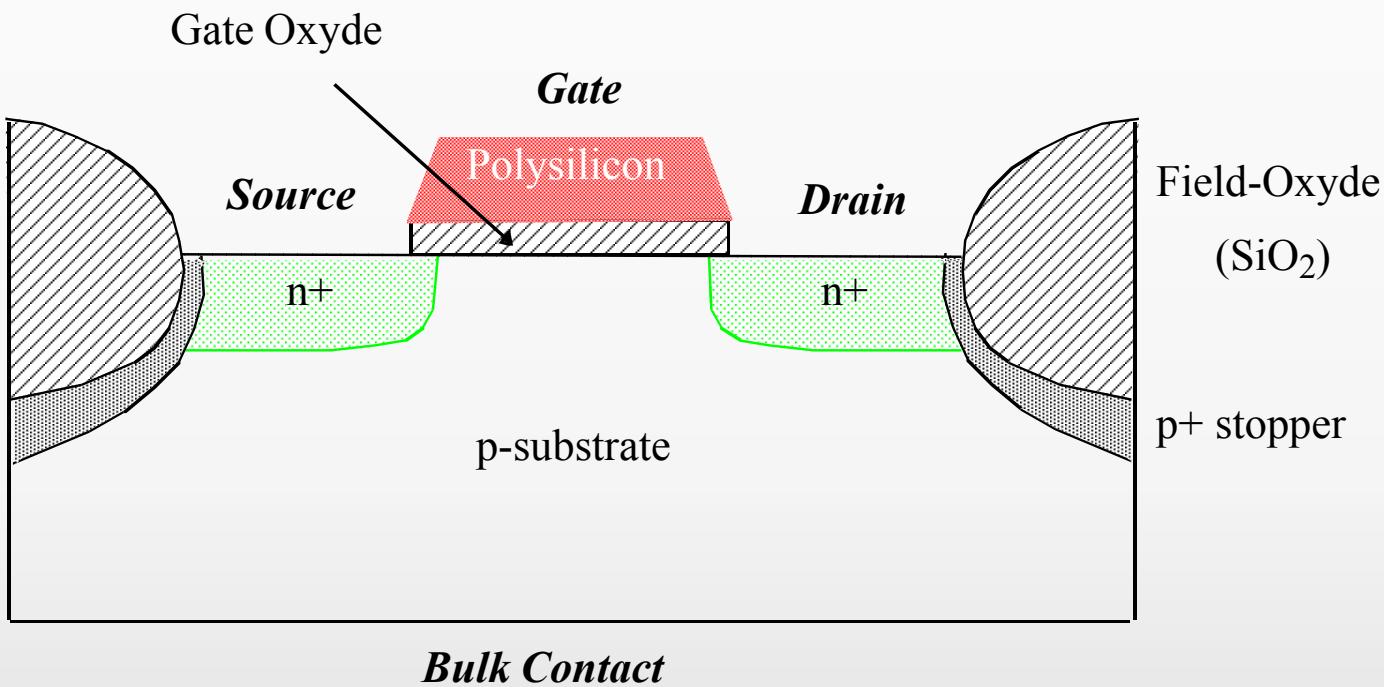
- Septiembre 26 – Asignación Proyecto
- Octubre 3 – Definición de alcance y jefes de proyecto
- Octubre 10 – Entrega Informe No. 1
 - Segmentación en módulos
 - Especificaciones generales
 - Especificaciones de cada modulo
 - Responsables
- Octubre 17 – Correcciones Inf. No.1
- Noviembre 14 – Prueba módulos en FPGA –
Entrega Informe No. 2 (Implementación sobre FPGA – VHDL)
- Diciembre 5 – Entrega Celdas Estándar – Informe 3
- Diciembre 19 – Entrega Informe No. 4 – Entrega Final y sustentación.





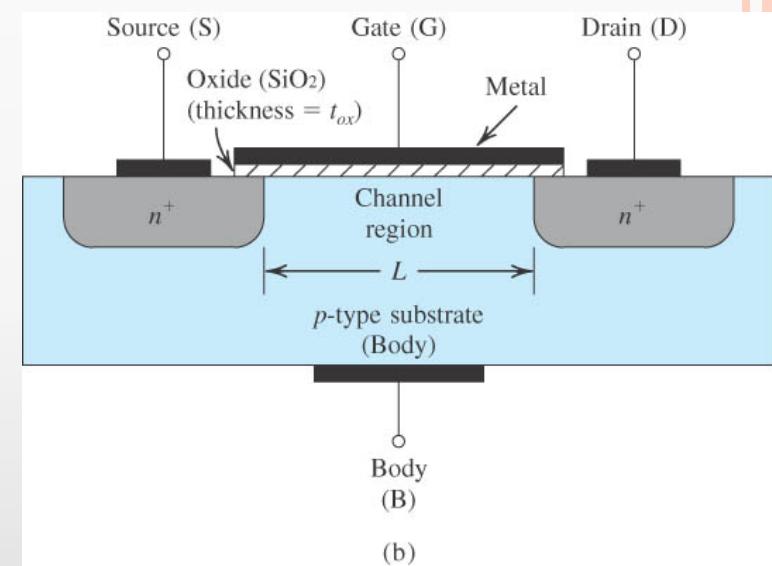
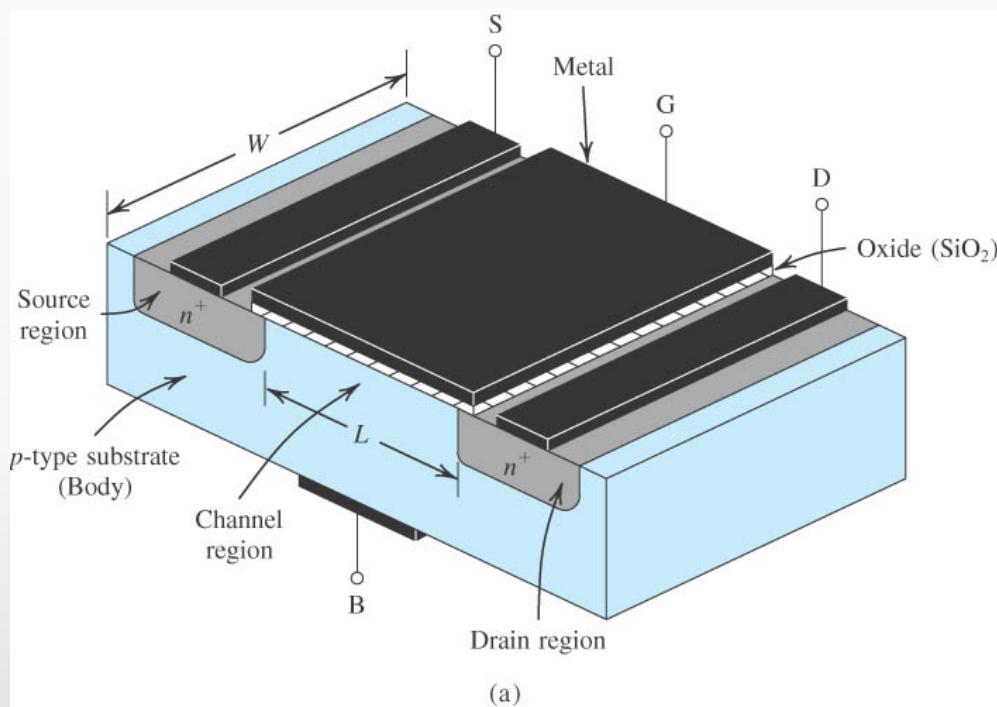
FINAL TEST

ESTRUCTURA DEL MOSFET

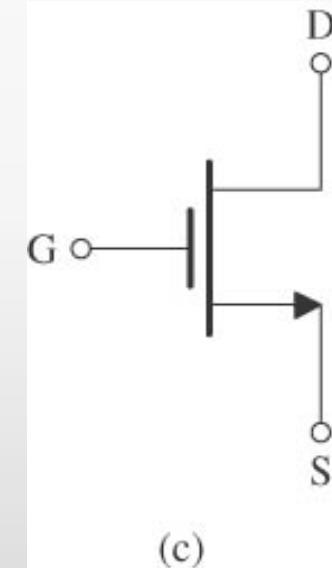
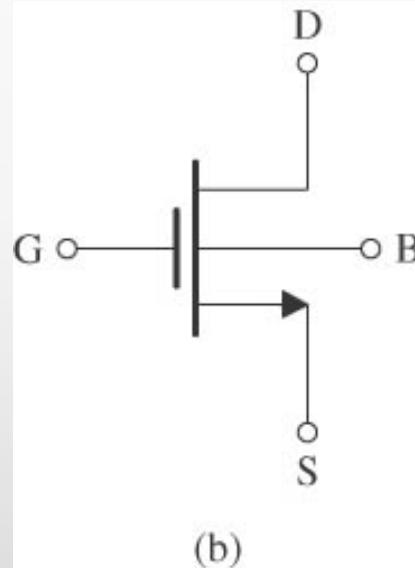
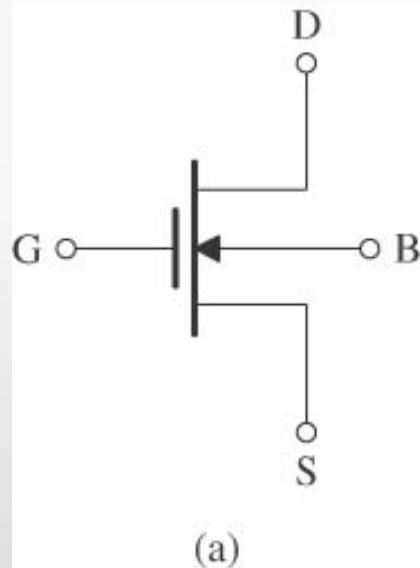


CROSS-SECTION of NMOS Transistor

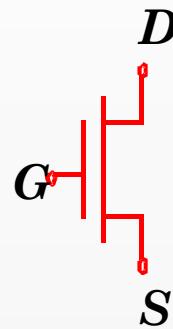
ESTRUCTURA DETALLADA



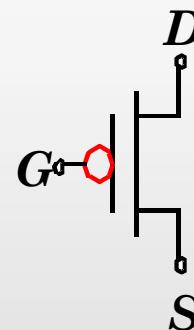
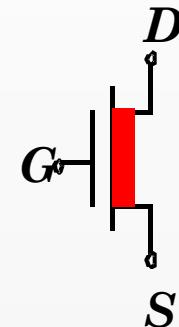
SIMBOLOGÍA



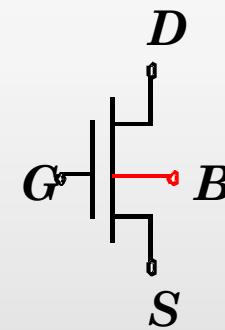
SÍMBOLOS DEL MOSFET



NMOS Enhancement NMOS Depletion



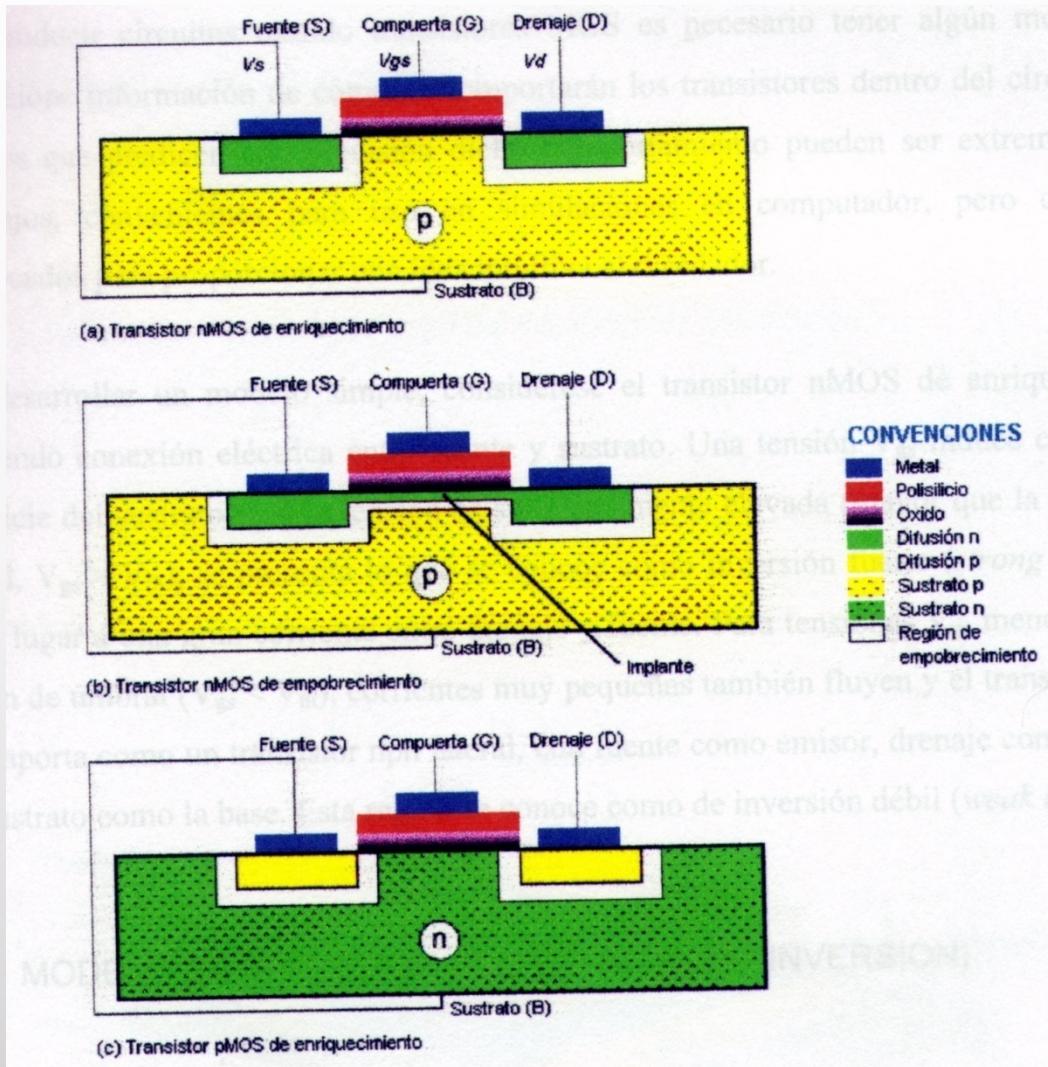
PMOS Enhancement



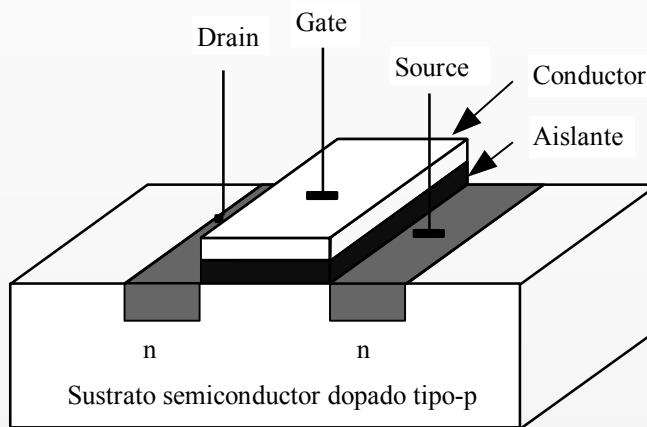
NMOS with
Bulk Contact



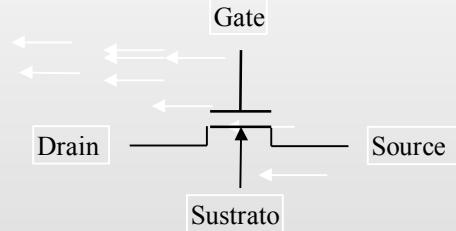
COMPONENTES BASICOS DE LOS MOSFET'S



TRANSISTOR NMOS



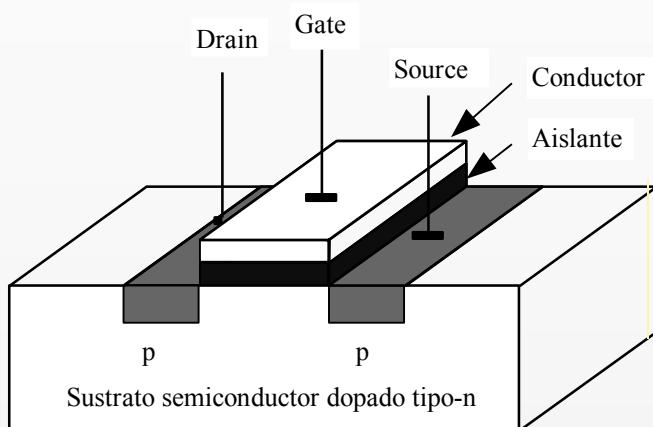
ESTRUCTURA FISICA



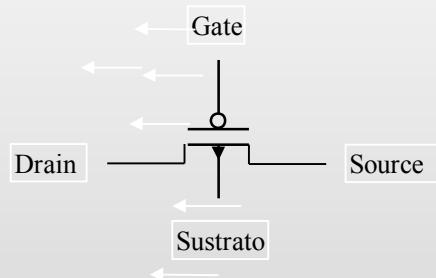
SIMBOLO ESQUEMATICO



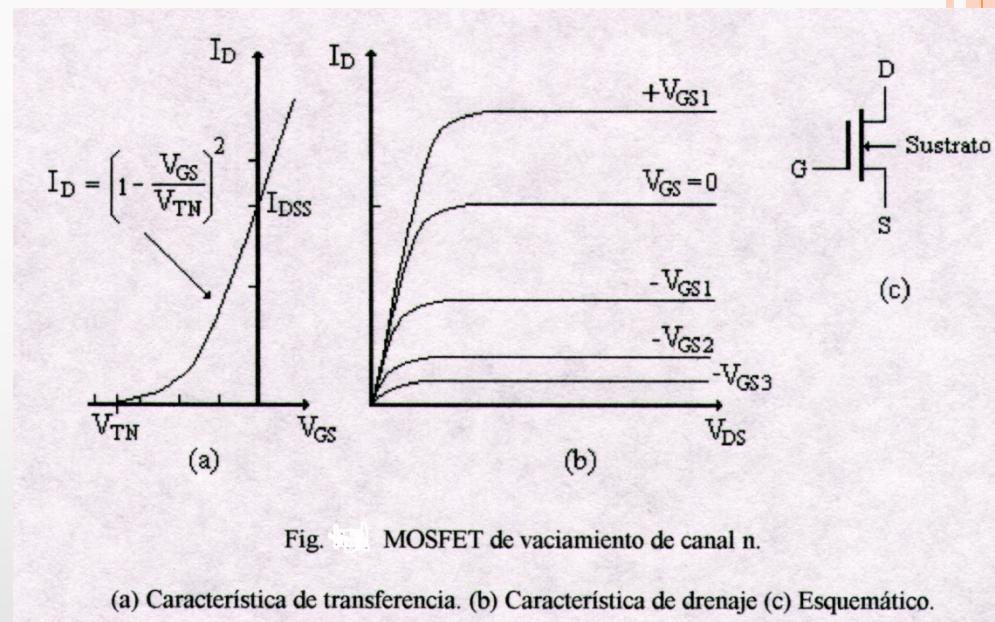
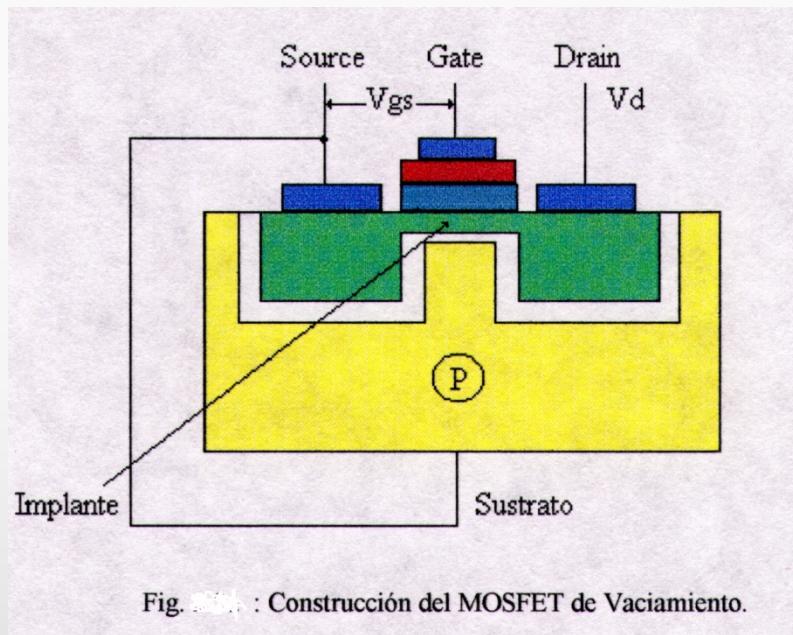
TRANSISTOR PMOS



ESTRUCTURA FISICA



MOSFET DECREMENTAL O VACIAMIENTO



MOSFET INCREMENTAL O ENRIQUECIMIENTO

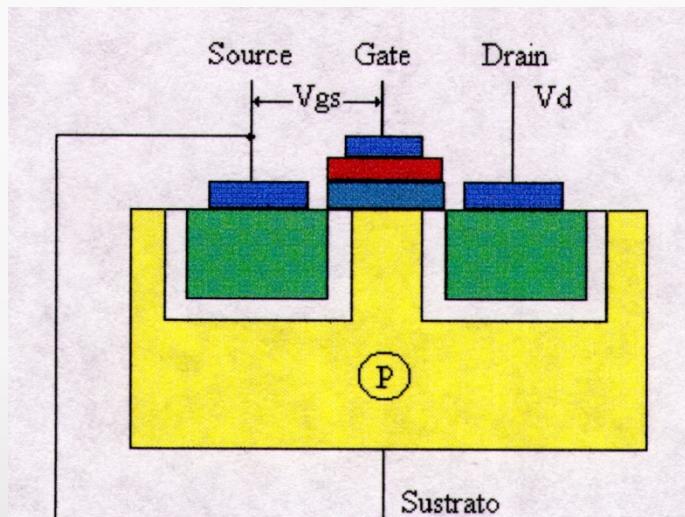


Fig. Construcción del MOSFET de Enriquecimiento.

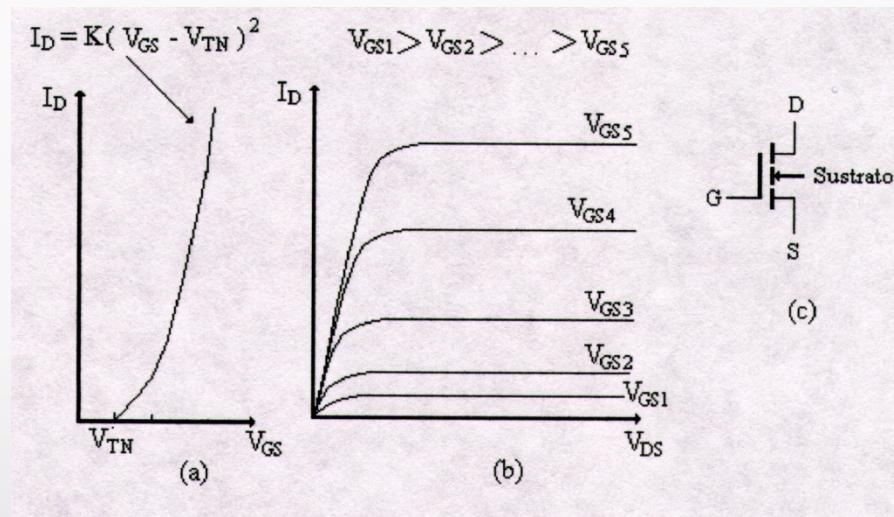
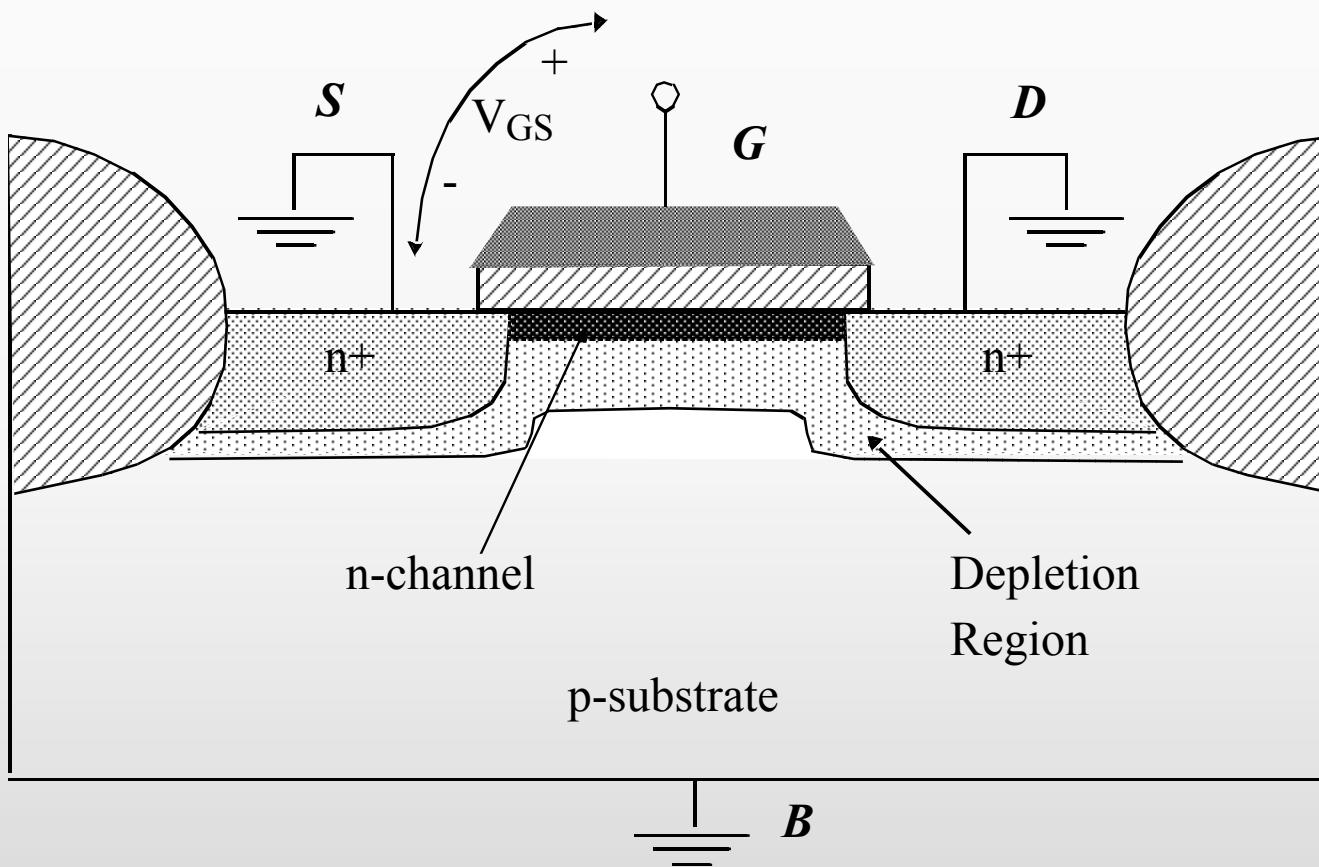


Fig. MOSFET de enriquecimiento canal n.

(a) Característica de transferencia. (b) Característica de drenaje (c) Esquemático.

CONCEPTO NIVEL DE UMBRAL



TENSION DE UMBRAL


$$V_t = V_{t\text{-mos}} + V_{fb}$$

$V_{t\text{-mos}}$: Voltaje de umbral de un condensador MOS ideal

V_{fb} : Voltaje de *flat-band*



TENSIÓN DE UMBRAL (1)


$$V_{t - mos} = 2 \cdot \Phi_b + \frac{Q_b}{C_{ox}}$$

Φ_b : Potencial de sustrato

Q_b : Término de carga del sustrato

C_{ox} : Capacitancia unitaria



TENSIÓN DE UMBRAL (2)

$$\Phi_b = \frac{kT}{q} \cdot \ln\left(\frac{N_A}{N_i}\right)$$

$$Q_b = \sqrt{2\epsilon_{Si} q N_A 2 \Phi_b}$$

N_A : Densidad de portadores en el sustrato semiconductor dopado [cm⁻³]

N_i : Concentración de portadores en el silicio intrínseco ($= 1.45 \times 10^{10}$ cm⁻³ a 300

°K) k : Constante de Boltzman (1.38×10^{-23} J/°K)

T : Temperatura [°K]

q : Carga del electrón (1.602×10^{-19} c)

ϵ_{Si} : Permitividad del silicio (1.06×10^{-12} F/cm)



TENSIÓN DE UMBRAL (3)

$$\Rightarrow V_{fb} = \Phi_{ms} - \frac{Q_{fc}}{C_{ox}}$$

Q_{fc} representa la carga fija debida a los estados de las superficies que se originan por las imperfecciones en la interface óxido-silicio

$$\Phi_{ms} = -\left(\frac{E_g}{2} \pm \Phi_b\right)$$

E_g : Banda de energía del silicio, dada por

$$E_g = \left(1.16 - 0.704 \times 10^{-3} \frac{T^2}{T + 1108} \right)^5$$



TENSION DE UMBRAL - RESUMEN

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

↑ ↑ ↑
Workfunction Surface Charge Implants
Difference Depletion Layer Charge

Body Effect Coefficient

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

with

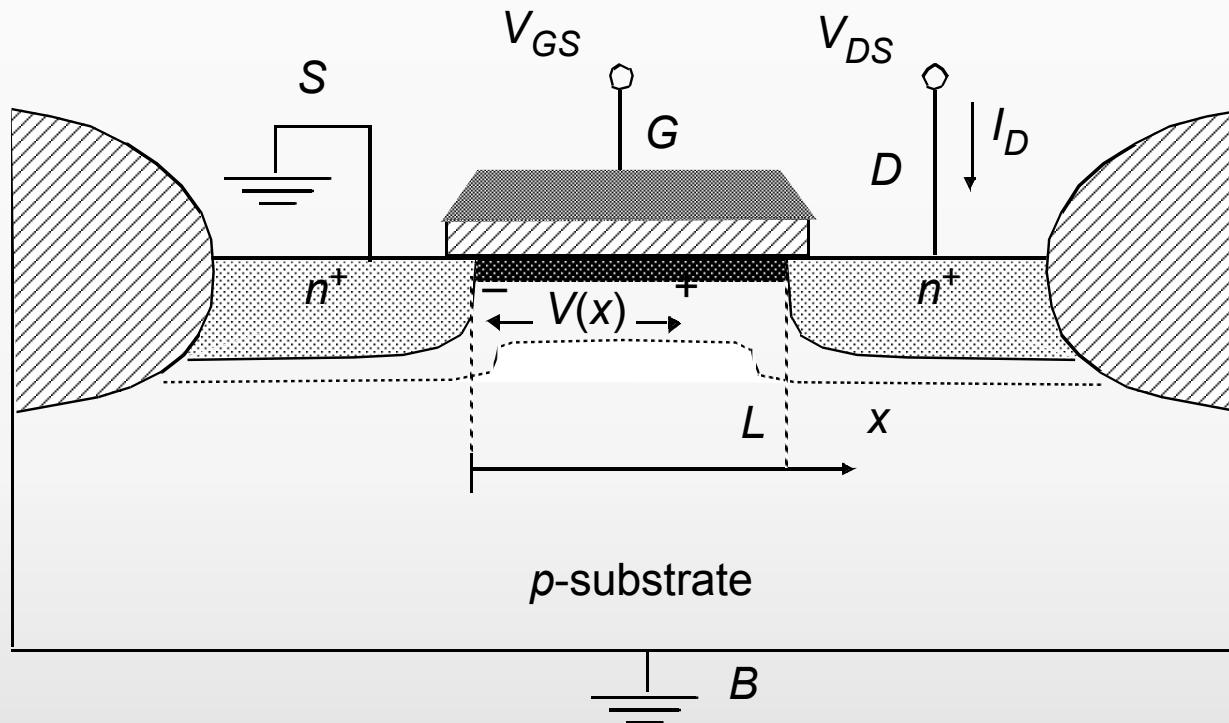
$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$$



RELACIÓN TENSIÓN - CORRIENTE



MOS transistor and its bias conditions



ZONAS DE OPERACION

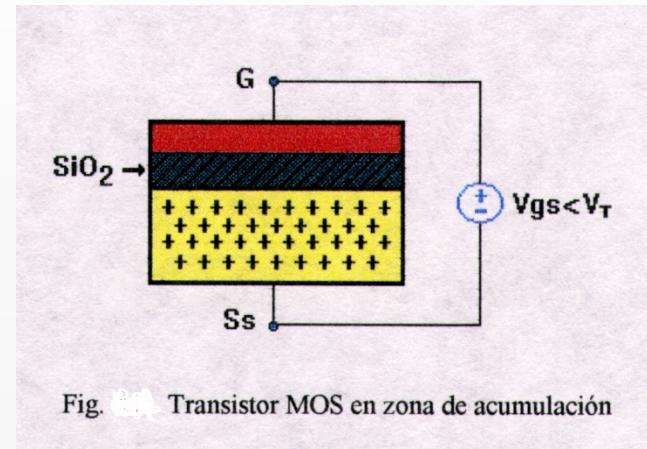


Fig. 1.11 Transistor MOS en zona de acumulación

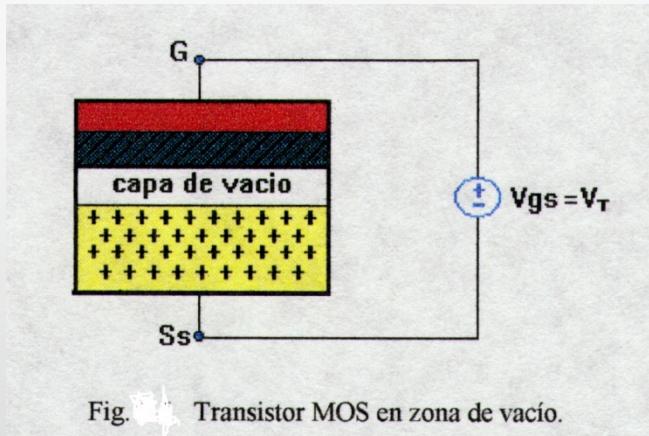


Fig. 1.12 Transistor MOS en zona de vacío.

VACIO

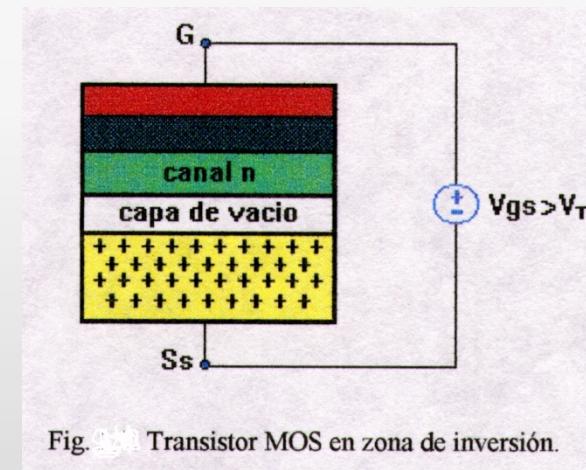


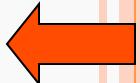
Fig. 1.13 Transistor MOS en zona de inversión.

INVERSION

ZONAS DE OPERACIÓN(1)

Región Corte

$$I_{ds} = 0, \quad V_{gs} \leq V_t$$



Región Lineal

$$C_g = C_{ox} \cdot W \cdot L = \frac{\epsilon_{SiO_2}}{T_{ox}} \cdot W \cdot L$$

C_{ox} : Capacitancia por unidad de área

W : Ancho del canal

L : Largo del canal

ϵ_{SiO_2} : Permitividad del aislante de Gate (Dióxido de Silicio)

T_{ox} : Espesor del aislante de Gate



ZONAS DE OPERACIÓN(2)

La carga Q está dada por la siguiente relación

$$Q = C_g (V_{gs} - V_t)$$

Las cargas en exceso son aceleradas por un campo eléctrico E

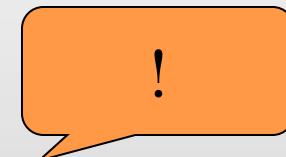
$$E = \frac{V_{ds}}{L} \quad I_{ds} = \frac{Q}{\tau}$$

τ : Tiempo de tránsito

$$\tau = \frac{L}{v} = \frac{L}{E \cdot \mu} = \frac{L}{\frac{V_{ds}}{L} \cdot \mu} = \frac{L^2}{V_{ds} \cdot \mu}$$

v : Velocidad de desplazamiento
de los portadores

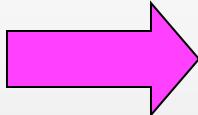
μ : Movilidad de los
portadores en el canal



ZONAS DE OPERACIÓN(3)

$$I_{ds} = \frac{C_g \cdot \mu \cdot V_{ds}}{L^2} \cdot (V_{gs} - V_t)$$

Al aumentar V_{ds} se pierde linealidad


$$I_{ds} = \beta \cdot \left[(V_{gs} - V_t) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right], \quad 0 < V_{ds} < V_{gs} - V_t$$

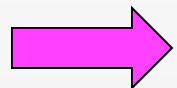
$$\beta = \frac{C_{ox} \cdot \mu \cdot W}{L} = \frac{\epsilon_{SiO_2} \cdot \mu}{T_{ox}} \cdot \frac{W}{L}$$

β es el factor de ganancia del transistor MOS

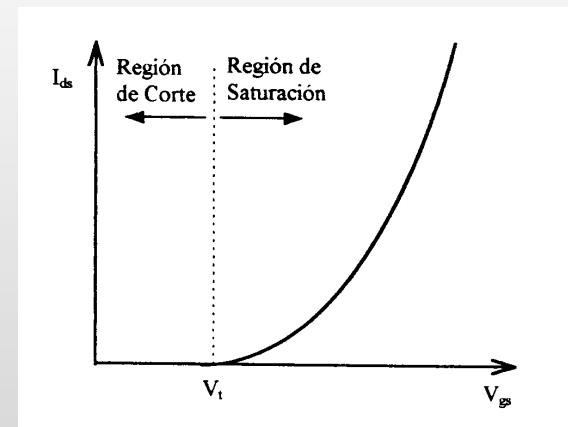
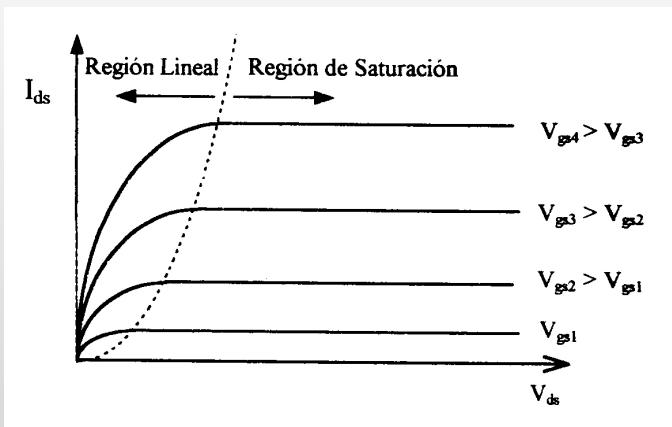


ZONAS DE OPERACIÓN(4)

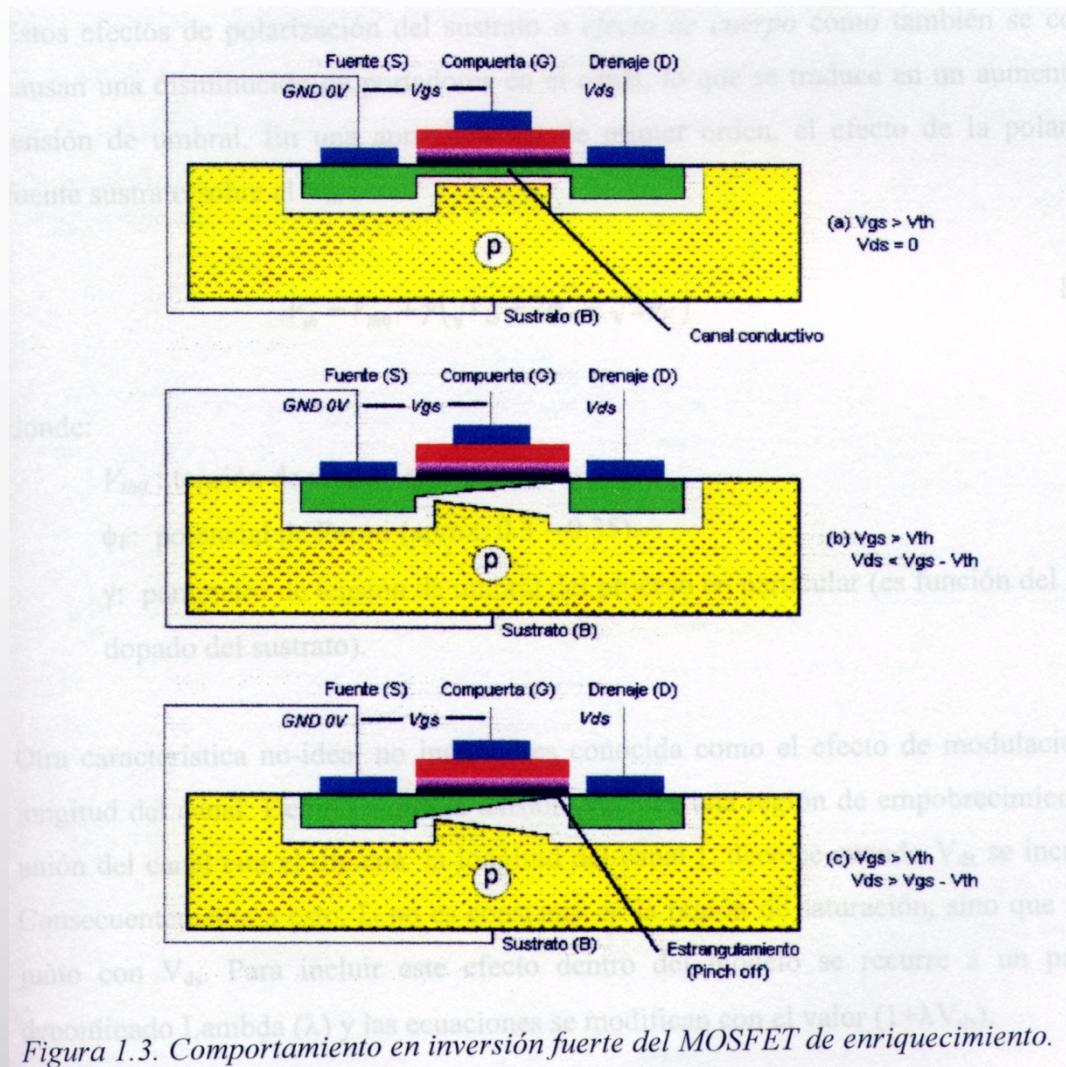
Región Saturación



$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2}, \quad 0 < V_{gs} - V_t < V_{ds}$$



COMPORTAMIENTO DEL MOSFET



ZONA DE INVERSION

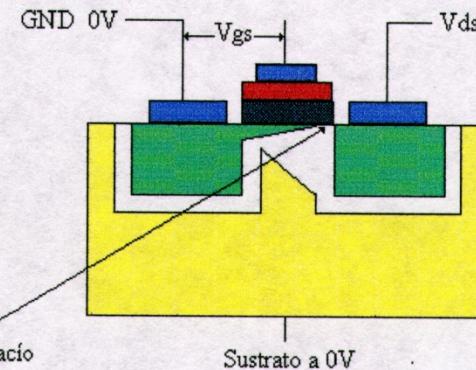


Fig. 1. Transistor MOS en la región de Saturación de la zona de inversión.

SATURACION

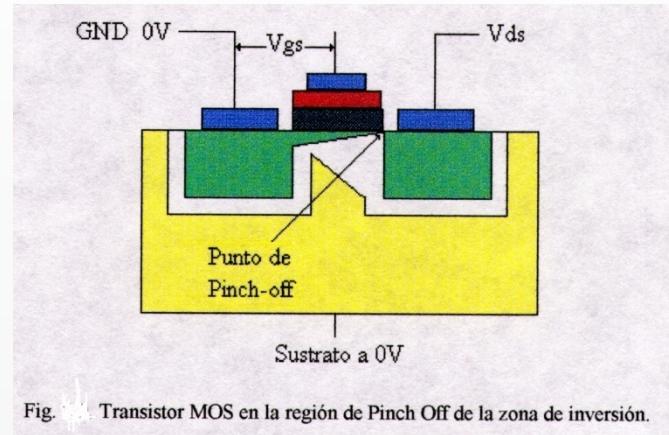


Fig. 2. Transistor MOS en la región de Pinch Off de la zona de inversión.

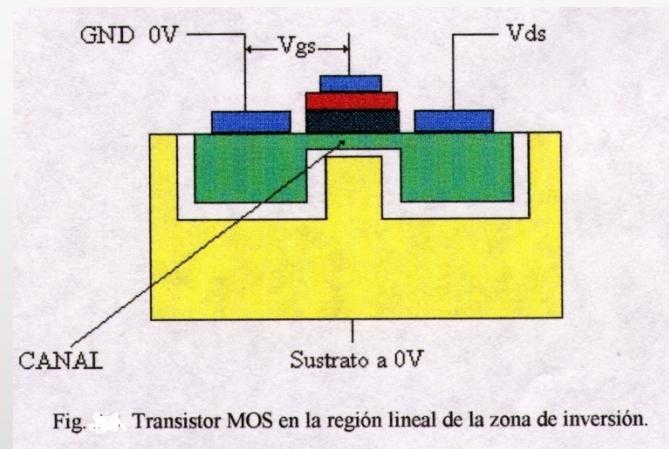


Fig. 3. Transistor MOS en la región lineal de la zona de inversión.

PINCH OFF

LINEAL

ECUACIONES DE OPERACIÓN

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

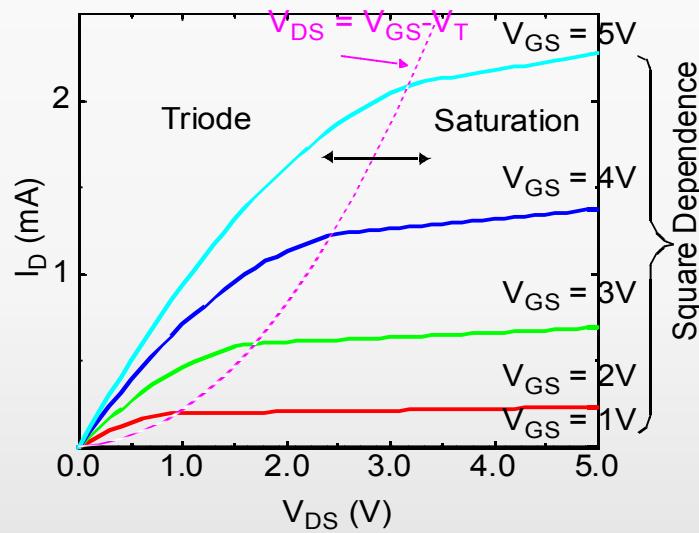
Process Transconductance
Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

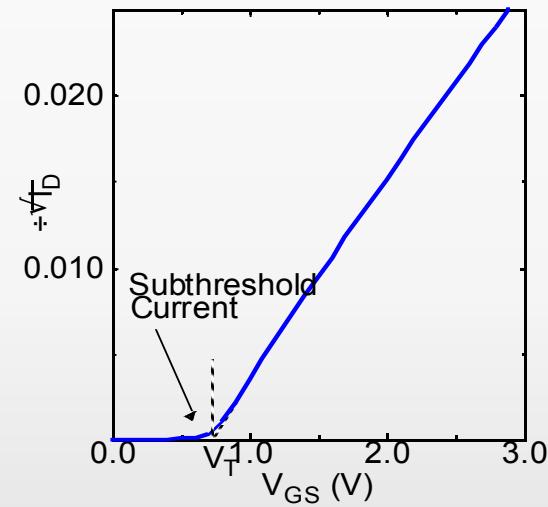
Channel Length Modulation

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Relación I-V



(a) I_D as a function of V_{DS}

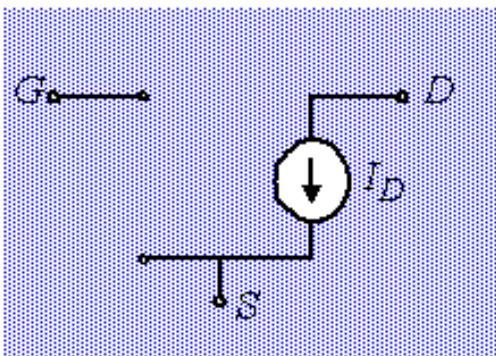


(b) $\sqrt{I_D}$ as a function of V_{GS} (for $V_{DS} = 5V$)

NMOS Enhancement Transistor: $W = 100 \mu\text{m}$, $L = 20 \mu\text{m}$



MODELO DE ANÁLISIS



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'nW}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$



PARAMETROS DE CONSTRUCCION

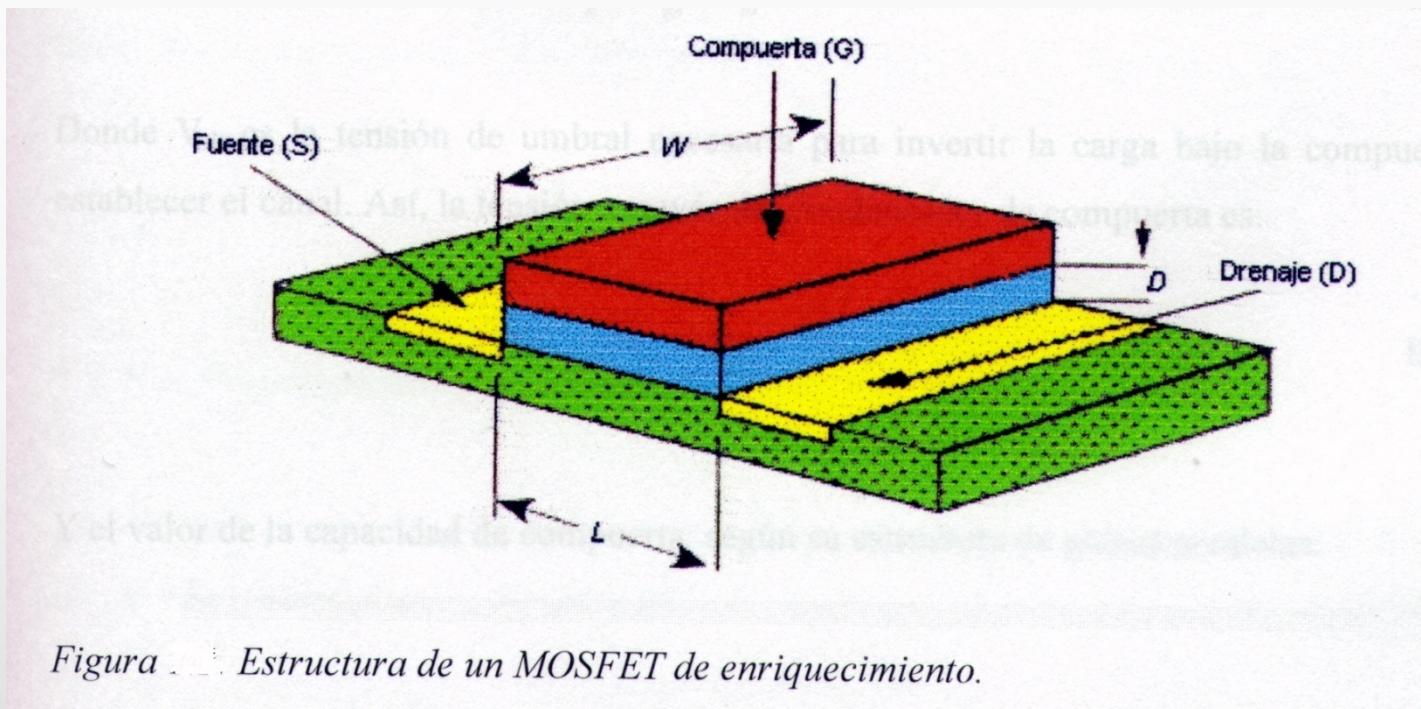
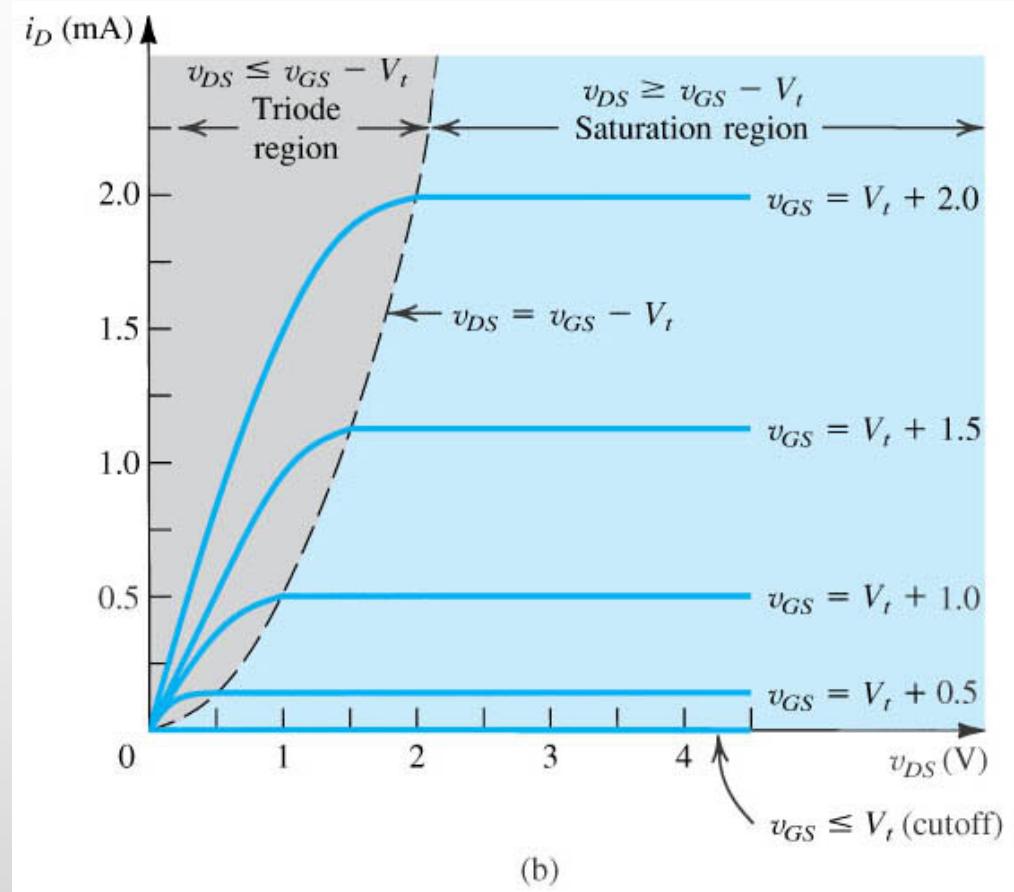
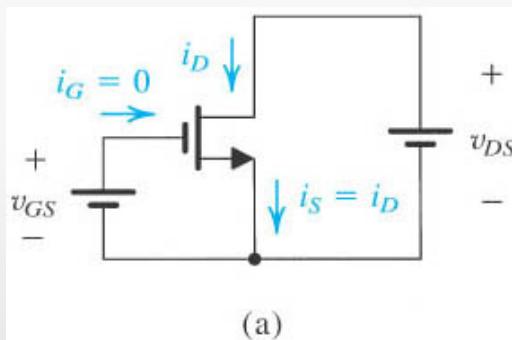


Figura 1. Estructura de un MOSFET de enriquecimiento.

MOSFET CANAL N - ENRIQUECIMIENTO



TEMA DE TRABAJO

- PROBLEMAS DE CIRCUITOS
MICROELECTRONICOS – SEDRA/
SMITH
 - Cuarta Edición
- CAP 5: 4, 5 Y 6

