***LAB 4 DEMO* – Single Cycle CPU and C Stuff Cont….**

Team _____ ***Reviewer***_____

Designing a Single Cycle CPU (430)

Hardware - 280

(100) All modules integrated

Data Memory in SRAM
Instruction Memory on Cyclone II
Register File
ALU
Program Counter
Instruction Register
Instruction Decoder
Control Block
Instruction Address Calculation
Multiplexers

(60) Functional

Fully
Partially
None

(40) Single Cycle Instruction Cycle Implemented

How demonstrated

(60) All Instructions Supported

NOP, ADD, SUB, AND, OR, XOR, SLT, SLL, LW, SW, J, JR, BGT

How Does Program Start and End

(10) How are Instructions Entered into Instruction Memory

(10) How is Data Entered into Data Memory

Software 100

(50) Test Program Assembled

(50) Test Program Executes

Fully
Partially
None

Presentation 50