

LAB 5 DEMO – Pipelined CPU and C Stuff Final Phase....

Team _____

Reviewer _____

Designing a Pipelined CPU (410)

Hardware - 260

(80) All modules integrated

Data Memory in SRAM – sign extended on use

Instruction Memory on Cyclone II

Register File

ALU

Program Counter

Instruction Register

Instruction Decoder

Control Block

Instruction Address Calculation

Multiplexers

Pipeline Registers

(60) Functional

Fully

Partially

None

(40) Pipeline Implemented

How

How Demonstrated

(40) All Instructions Supported

NOP, ADD, SUB, AND, OR, XOR, SLT, SLL, LW, SW, J, JR, BGT

How Does Program Start and End

(40) Hazards Handled - How

Data Hazards – RAW

$C = C + 4$; and $D = C - 3$;

$G = E \mid F$; and $G = (E \wedge F) \& H$;

$G = E \& F$; and $G = (E \wedge F) \& H$;

Instruction Hazard – Branch

if $((A - B) > 3 \dots \text{else}$

Software 100

(50) C Test Program Assembled

(50) C Test Program Executes

Fully

Partially

None

Presentation 50