BIRZEIT UNIVERSITY
Electrical and Computer Engineering Department
ENCS3330
Design of Low Power NXN Magnitude Comparator Using Transmission Gate (TG) Logic Technique

---

Layan Wael – 1191882
Masa Emwas- 1203359
Amer Jaber – 1183311

I. ABSTRACT

Designing low-power, high-speed, and reliable integrated circuits is crucial for advancing technology. This paper introduces the use of Transmission Gates as a novel method for implementing digital logic circuits, focusing on reducing power consumption and propagation delays. We designed an N*N bit magnitude comparator using both traditional CMOS logic and Transmission Gate techniques. The Transmission Gate comparator requires fewer transistors than the CMOS version. Power consumption analysis shows that the CMOS comparator uses more power, while the Transmission Gate implementation is much more efficient. Additionally, the Transmission Gate design significantly reduces delay compared to the CMOS approach. Overall, the Transmission Gate method improves power efficiency and performance. Our circuit simulations were conducted using ELECTRIC TOOL EDA with 22 nm process technology.

II. INTRODUCTION

In our project, we focus on designing an N X N bit magnitude comparator using Transmission Gate techniques, leveraging advanced 22nm CMOS technology. The primary objectives include minimizing propagation delay, optimizing power efficiency, and effectively utilizing chip area. Power consumption is a critical concern, and our design approach aims to achieve significant reductions compared to traditional CMOS logic. We start by implementing a 1-bit comparator and gradually scale up to an N X N bit comparator, ensuring scalability and adaptability. Transmission Gate technology is chosen for its potential to improve speed performance and reduce power consumption by efficiently controlling signal paths using both NMOS and PMOS transistors. Through comprehensive analysis and simulation using ELECTRIC TOOL EDA, this paper evaluates the effectiveness of Transmission Gate in meeting the stringent demands of modern digital circuit design.

Figure 1: 4-bit Comparator.

.

III. THEORY

THEORY OF 1-BIT AND 2-BIT COMPARATORS

1-BIT COMPARATOR

A 1-bit comparator is a digital circuit that compares two single-bit binary numbers, A and B. The output of a 1-bit comparator indicates whether A is greater than, equal to, or less than B. The truth table for a 1-bit comparator is as follows:

A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Table 2: Truth table 1-BIT COMPARATOR

From the above truth table logical expressions for each output can be expressed as follows.

CASES : A>B: AB',A<B: A'B,A=B: A'B' + AB

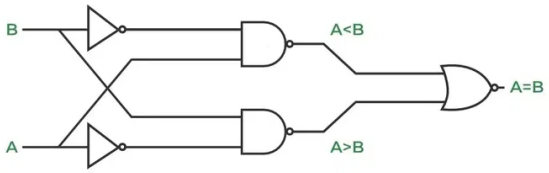


Figure 2: Logic Circuit for 1-bit Comparator

```
A>B:A1B1’ + A0B1’B0’ + A1A0B0’
A=B: A1’A0’B1’B0’ + A1’A0B1’B0 + A1A0B1B0 + A1A0’B1B0’
   : A1’B1’ (A0’B0’ + A0B0) + A1B1 (A0B0 + A0’B0’)
   : (A0B0 + A0’B0’) (A1B1 + A1’B1’)
   : (A0 Ex-Nor B0) (A1 Ex-Nor B1)
A<B:A1’B1 + A0’B1B0 + A1’A0’B0
```

2-bit Comparator

A 2-bit comparator compares two 2-bit binary numbers, A and B, where A = A1A0 and B = B1B0. The comparator determines if A is greater than, equal to, or less than B. The truth table for a 2-bit comparator is as follows:

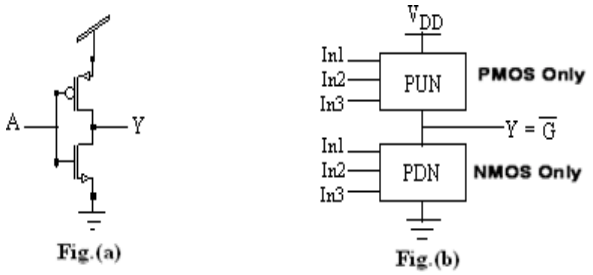
A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Table 3: Truth table 2-BIT COMPARATOR

Implement Technique

- **Using CMOS Logic Style**

CMOS logic style employs inverters built with both NMOS and PMOS transistors, shown in Figure 3(a). Depending on whether the input A is low or high, either the PMOS or NMOS transistor conducts, directing the output Y towards either VDD (logic high) or ground (logic low), respectively. This method ensures efficiency by activating either the pull-up network (PUN) of PMOS transistors, which connects Y to VDD, or the pull-down network (PDN) of NMOS transistors, which connects Y to ground, as illustrated in Figure 3(b). This configuration allows CMOS logic to handle multiple inputs with 2N transistors for an N-input gate, offering robust noise immunity and consistent voltage margins close to VDD and ground levels. Despite these advantages, CMOS logic consumes more power compared to other logic styles due to its use of both NMOS and PMOS transistors simultaneously for each input, necessitating a larger transistor count in designs. (Static CMOS logic uses complementary pairs of p-type and n-type MOSFETs to implement logic functions. Each gate consists of a pull-up network (PUN) of PMOS transistors and a pull-down network (PDN) of NMOS transistors. For a 2-bit comparator: The PUN connects the output to VDD when the output should be high. The PDN connects the output to GND when the output should be low.CMOS logic provides full output voltage swing, high noise immunity, and no static power dissipation, but it requires more transistors.)



Figurer3: Inverter Schematic

Simulation results for 2-Bit Magnitude Comparator using CMOS style

IVand SV (volts)	PC (watts)	Delay Time (seconds)	Power-Delay Product (ws)
0.6	5.3343e-009	3.0386e-008	16.2088e-017
0.8	8.6669e-009	3.0321e-008	26.2789e-017
1.0	1.4058e-008	3.0234e-008	4.2502e-016
1.2	2.1032e-008	2.9963e-008	6.3018e-016
1.4	2.8080e-008	2.9958e-008	8.4122e-016

Table 4: Results for 2-Bit Comparator using CMOS

Values in the table: Increasing the supply voltage directly increases power consumption, as power consumption is directly proportional to the supply voltage . Conversely, increasing the supply voltage reduces delay, since delay is inversely proportional to the supply voltage. These relationships underscore the trade-offs involved in choosing supply voltage in CMOS circuits: higher voltage boosts performance by reducing delay but also escalates power usage.

Transmission Gate Implementation Approach

Transmission Gate (TG): also known as a Pass Gate is constructed with parallel-connected NMOS and PMOS transistors uses a combination of NMOS and PMOS transistors to create a bidirectional switch controlled by a control signal C. When C is high or low, both transistors conduct, establishing a low-resistance path between A and Y. Conversely, when C is low or high, both transistors are off, resulting in a high impedance state between A and Y. Depending on whether A is 0 or 1, the signal passes through the NMOS (for '0') or the PMOS (for '1'). This design feature facilitates a full output swing and robust noise margin, but it requires a larger transistor count, leading to higher power dissipation. But, managing the control signal in both true and complementary forms don’t adds complexity to the design process.

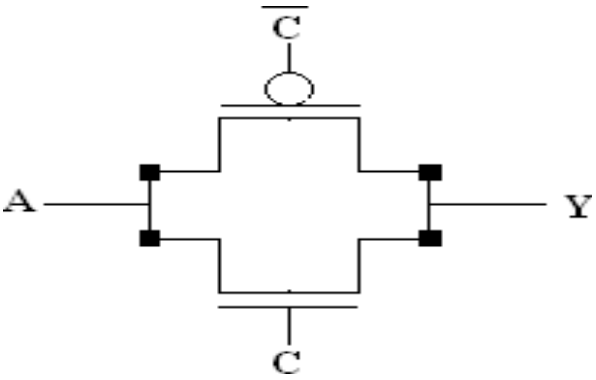


Figure 4: symbol for transmission gate

In the TG implementation of a 2-bit comparator:
- When the control signal is high (C=1), both NMOS and PMOS transistors are on, allowing the signal to pass through.
- When the control signal is low (C=0), both transistors are off, and the path is open, representing a high-impedance state.

. Simulation results for 2-Bit Magnitude Comparator using TG style

IV& SV(volts)	PC	Delay Time (seconds)	Power-Delay Product (ws)
0.6	4.0802e-009	2.9994e-008	12.2381e-017
0.8	8.2429e-009	2.9988e-008	24.7188e-017
1.0	1.3249e-008	2.9981e-008	3.9721e-016
1.2	1.9855e-008	2.8940e-008	5.7460e-016

Table 5: Performances metric for 2-bit comparator

Increasing the supply voltage increases power consumption, as power usage directly correlates with the supply voltage. Simultaneously, increasing the supply voltage decreases delay because delay decreases as supply voltage increases. These relationships highlight the trade-offs involved in choosing the supply voltage for CMOS circuits: higher voltage boosts performance by reducing delay but also escalates power consumption.

Comparison of Approaches

When comparing the use of CMOS design versus Transmission Gate in a specific project, several factors suggest that opting for Transmission Gate may be advantageous:

Power Consumption Impact:

CMOS designs typically require a larger number of transistors, leading to higher overall power consumption compared to Transmission Gate, which can often achieve similar functionality with fewer transistors, thereby reducing power consumption.

Speed of Operation:

Transmission Gate can offer faster switching times in certain scenarios compared to CMOS, particularly when toggling between high and low probability states.

Noise Resilience:

Transmission Gate provides higher noise margins due to its high-impedance state, making it suitable for applications where noise immunity is critical.

Design Complexity:

While Transmission Gate may involve more complex handling of control signals and complementary forms, it can sometimes offer a more efficient and straightforward design compared to CMOS, which might require additional circuitry to achieve the same function.

Based on these points, opting for Transmission Gate could be preferable for our project if minimizing power consumption, achieving high speed or performance, or enhancing noise immunity are crucial considerations in circuit design. However, the choice should ultimately balance all factors related to performance, cost, and complexity based on the specific project requirements.

Best Approach

In terms of delay, area, power consumption, and speed:

Delay:

Transmission Gate logic typically offers lower delay.

Area:

Both approaches require a significant number of transistors, but in our project gate transmission might use fewer transistors due to simpler control signals.

Speed: Transmission Gate logic might offer faster operation due to lower delay.

Power Delay Product (PDP)

PDP is the product of power consumption and delay, indicating the energy efficiency of the circuit. Lower PDP values are preferable.

PDP Comparison

Transmission Gate Logic: Generally lower PDP due to lower delay.
Static CMOS Logic: Higher PDP due to higher power consumption.

Based on PDP, Transmission Gate logic** tends to be more efficient for high-speed applications as our project, while ****Static CMOS logic**** is better for low

Power Consumption vs. Process Node

Power consumption vs. process node for Intel processors

Process Node	Power Consumption (W)
180 nm	100
90 nm	65
65 nm	45
45 nm	30
32 nm	20
22 nm	15
14 nm	10
10 nm	7
7 nm	5
5 nm	4

Table 6: Power consumption vs. process node.

You can see a clear pattern: with each new process node, power consumption goes down. This happens because smaller feature sizes let more transistors fit into the same area, and smaller transistors can use lower voltages.

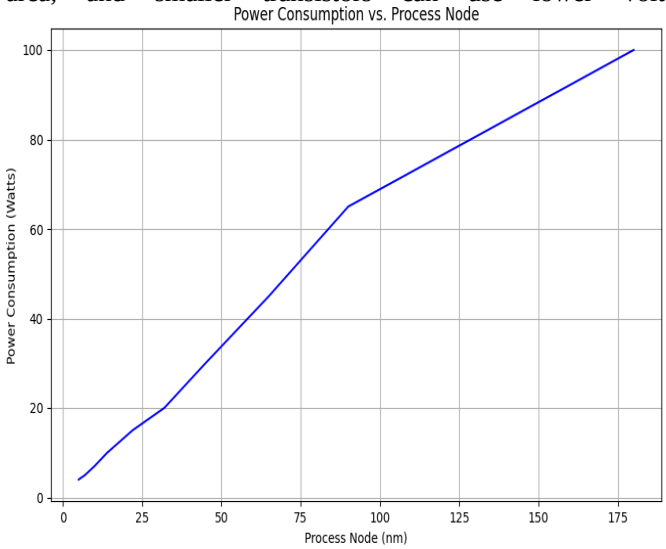


Figure 5: Power consumption vs. process node.

Cost

Cost vs. process node for Intel processors

Process Node (nm)	Manufacturing Cost (USD/chip)
180	100
90	80
65	60
45	40
32	30
22	25
14	20
10	15
7	10
5	5

Table 7: Cost vs. process node

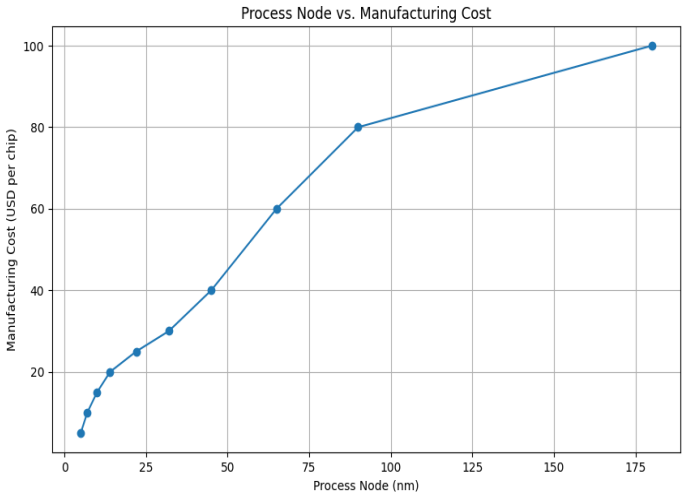


Figure 6: Cost vs. process node.

Manufacturing costs often go up at first when semiconductor process nodes shrink because of the higher development and production expenses. However, as the technology improves, costs can come down, making, for example, 7 nm nodes cheaper than 10 nm ones. Still, there can be exceptions, like the 5 nm node, which might be more expensive due to the advanced materials and processes involved. This creates challenges for the semiconductor industry, which has to find ways to reduce costs despite the complexities of precise manufacturing and packaging for smaller chips. Despite these hurdles, the industry remains dedicated to making smaller chips more affordable.

Performance vs. process node for Intel processors

Process Node (nm)	CPU Speed (GHz)
180	1.6
90	2.8
65	3.2
45	3.5
32	3.7
22	4.2
14	4.5
10	4.8
7	5

Table 8: Performance vs. process node.

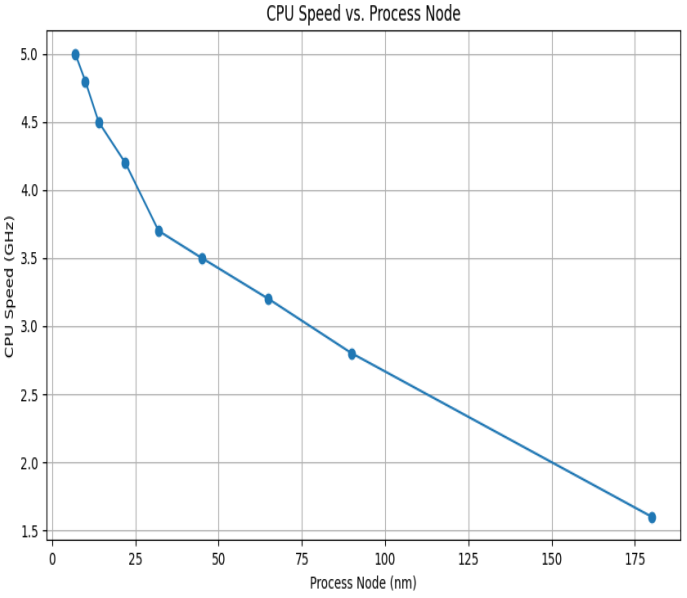


Figure 7: Performance vs. process node.

There is a clear connection between CPU speed and the size of semiconductor process nodes—smaller nodes boost performance. For example, as we've moved from 180 nm to 7 nm, CPU speeds have jumped from 1.6 GHz to 5 GHz. This shows how advances in semiconductor technology improve CPU performance with smaller manufacturing processes. However, as we near the limits of miniaturization, around 10 nm, the performance gains slow down due to increased noise
and physical constraints. To overcome this, the industry is looking
into new materials and architectures to keep enhancing performance. Smaller transistors help by allowing faster switching, higher transistor density, and better efficiency, leading to lower power consumption and heat generation. Despite these challenges, ongoing innovation in the semiconductor field continues to focus on improving chip performance and efficiency.

I. DESIGN IMPLEMENTATION AND RESULT

i. AND schematic implementation

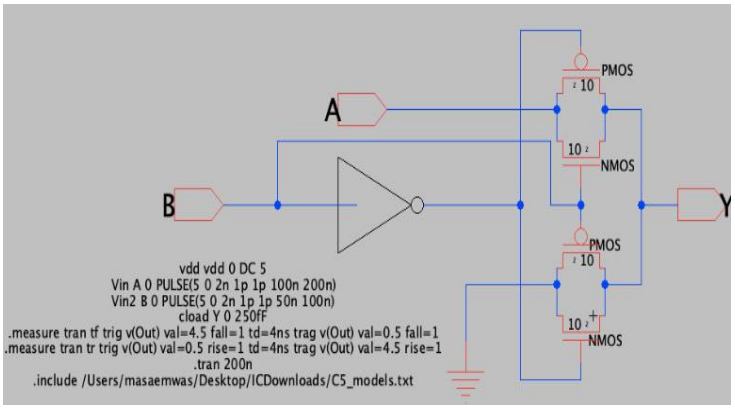


Figure 8: AND schematic

- The code we put in schematic Inverter to appear the wave above.

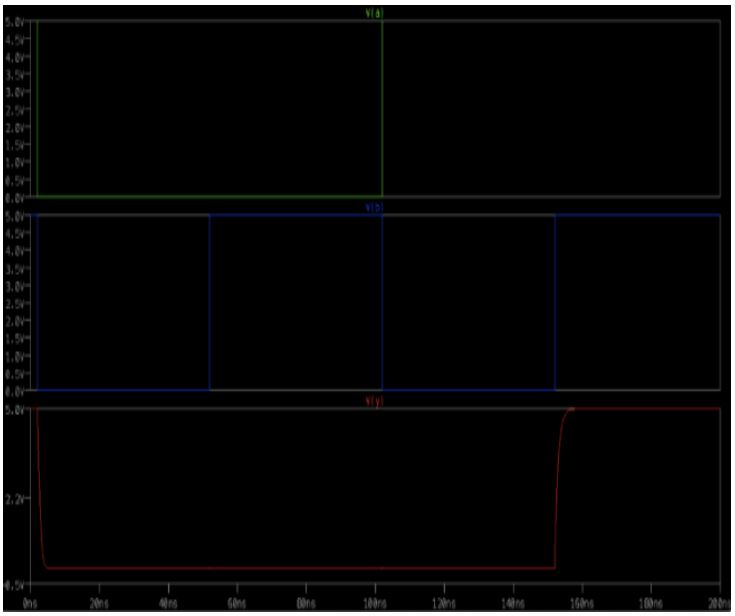


Figure 9: AND schematic output waveform

2. AND

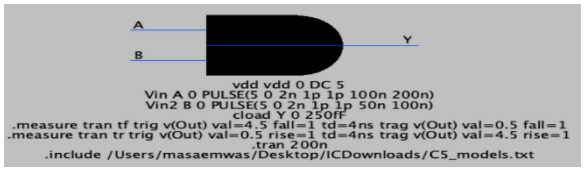


Figure 11: code and icon for AND

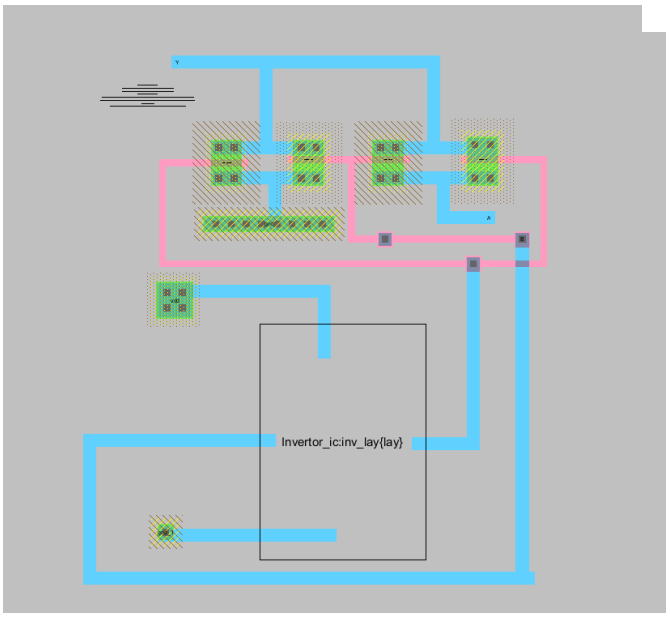


Figure 12: Layout 1 for AND.

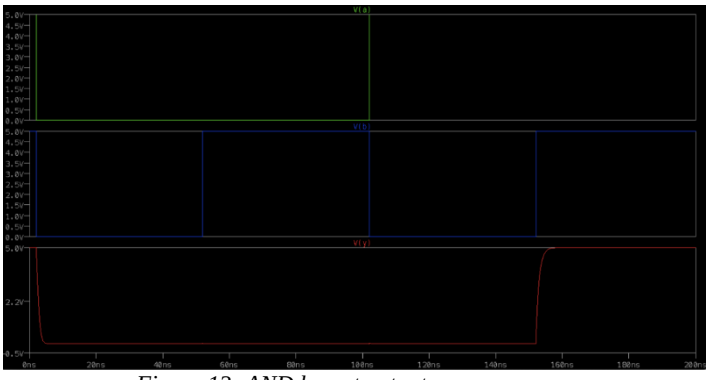


Figure 13: AND layout output wave.

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Table 9: Truth table of AND.

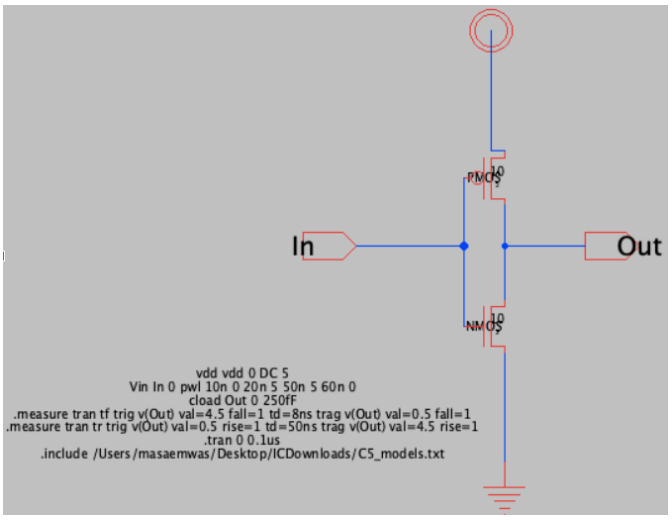


Figure 14: Inverter schematic.

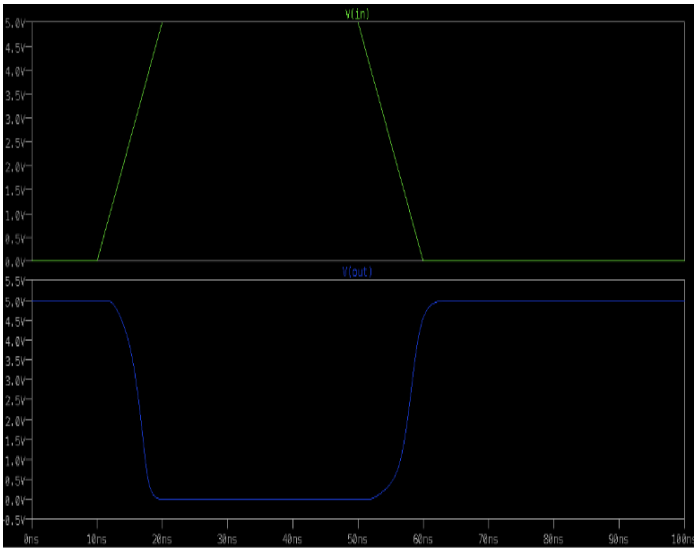


Figure 15: Inverter waveform.

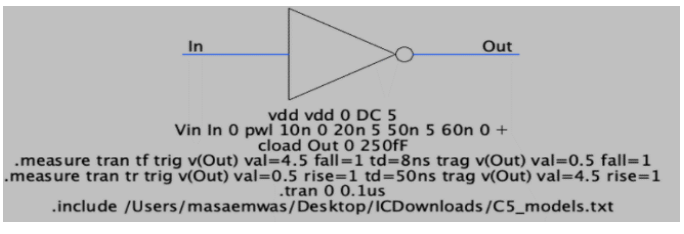


Figure 16: Code of Inverter schematic.

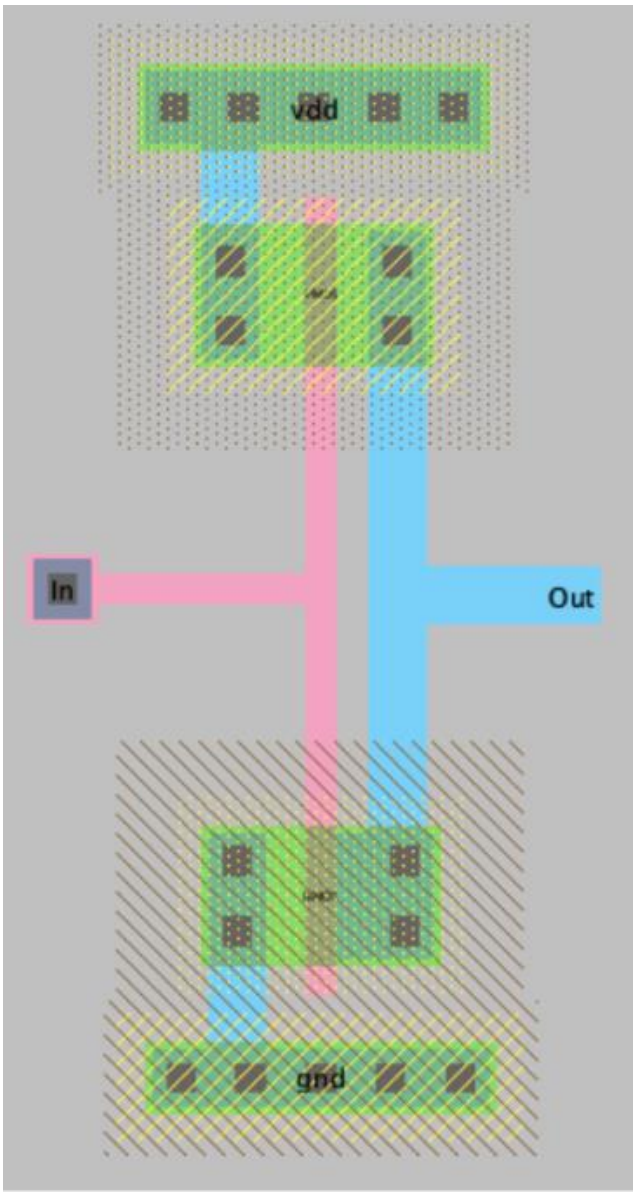


Figure 17: Inverter Layout.

NOR Schematic

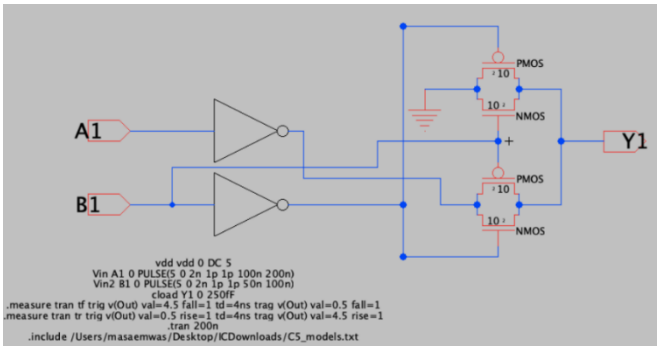


Figure 18: NOR Schematic

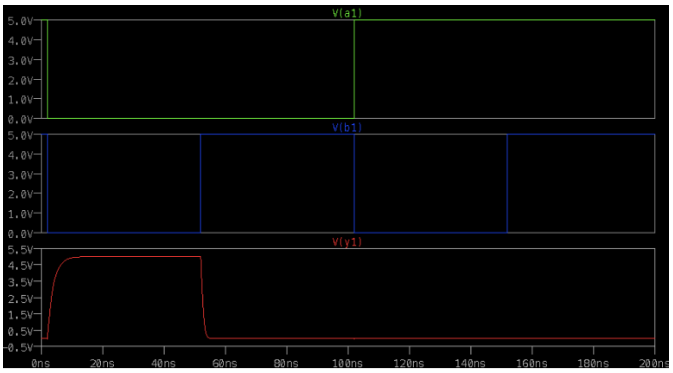
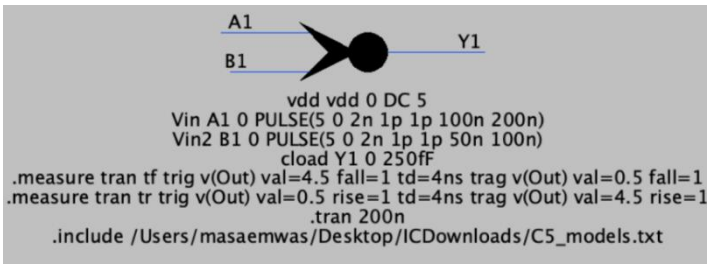
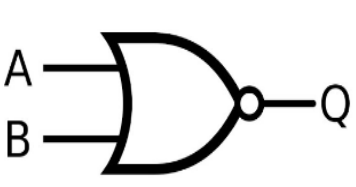


Figure 19: NOR schematic output wave.



. Figure 20: The NOR layout code



Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Table 10: NOR truth table with icon.

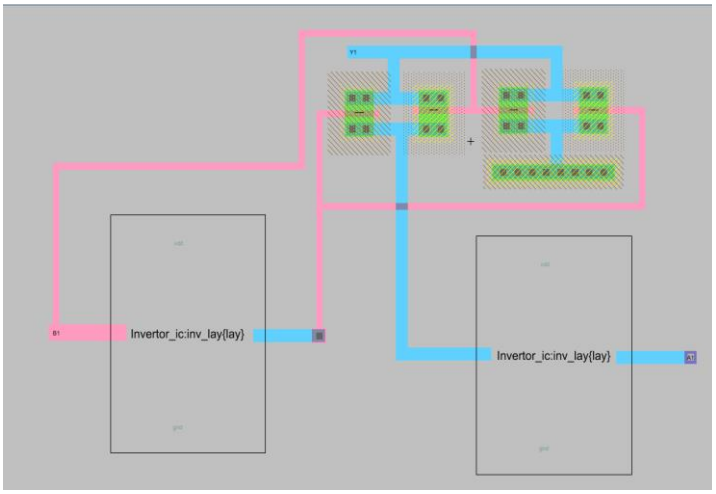


Figure 21: NOR Layout

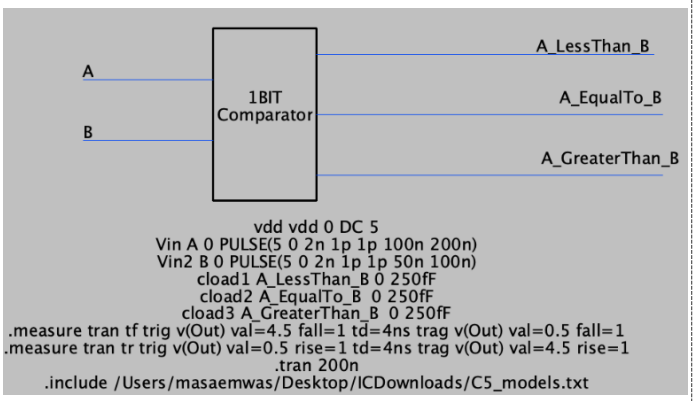


Figure 24: The 1-BIT Comparator Layout code.

ONE-BIT COMPARATOR

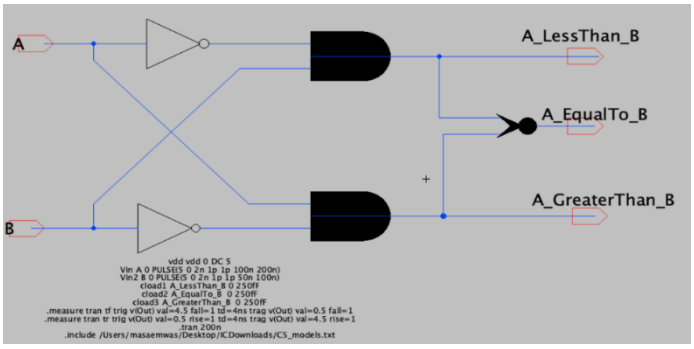


Figure 22: ONE BIT COMPARATOR Schematic

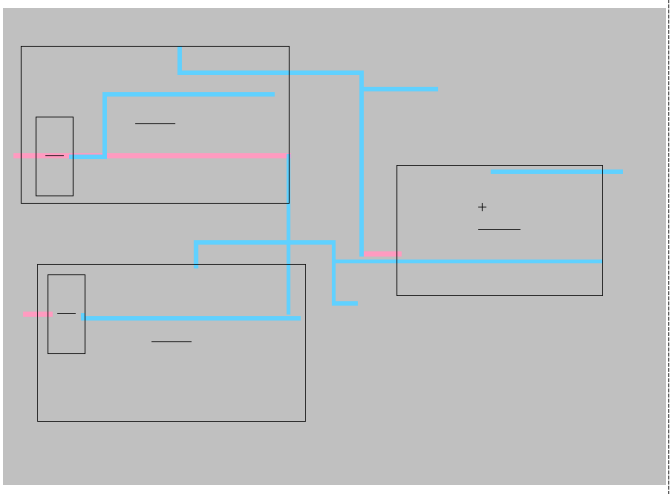


Figure 25: 1-BIT Comparator Layout.

OR-GATE

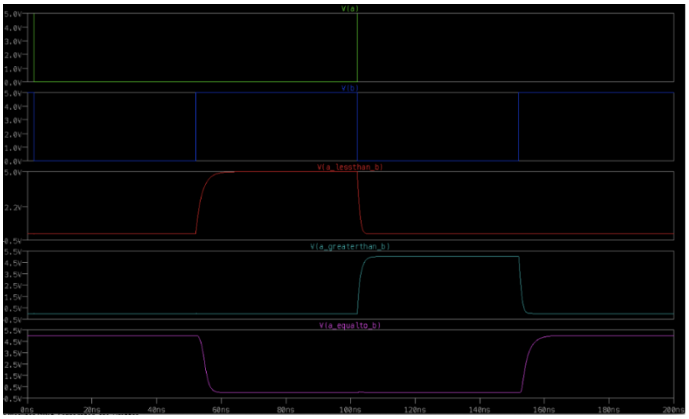


Figure 23: One-BIT Comparator Layout output waveform.

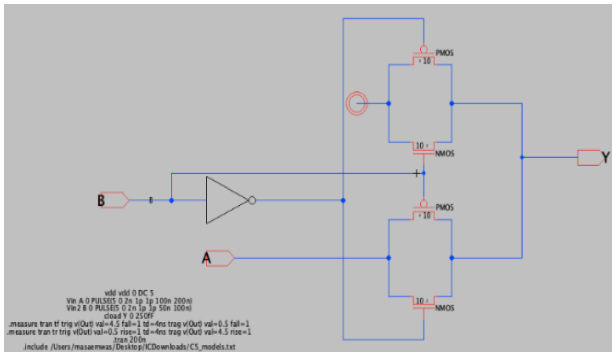


Figure 26: OR Schematic

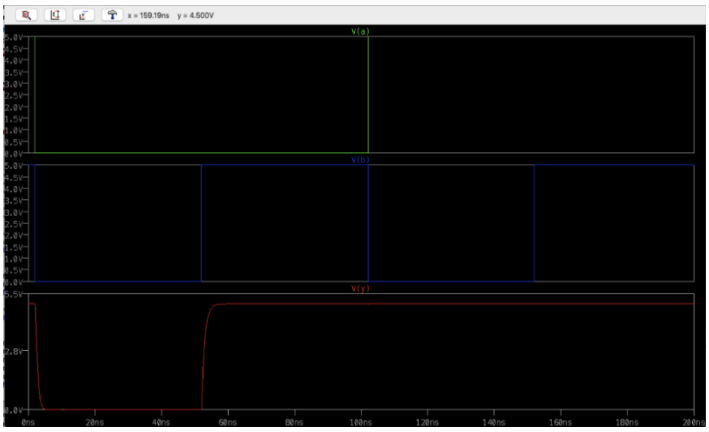


Figure 27: OR Gate Layout output waveform

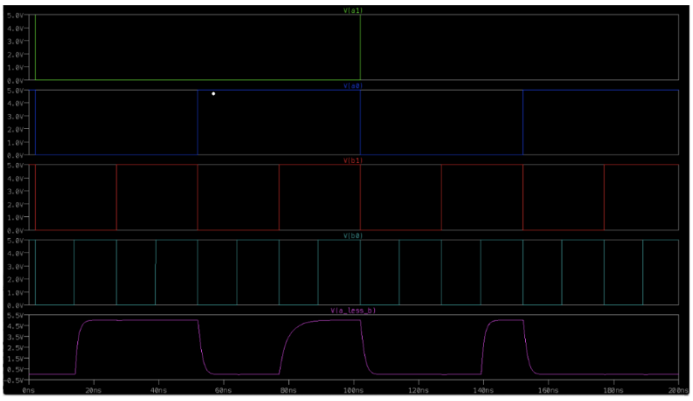


Figure.31: 2-BIT Comparator waveform A<B

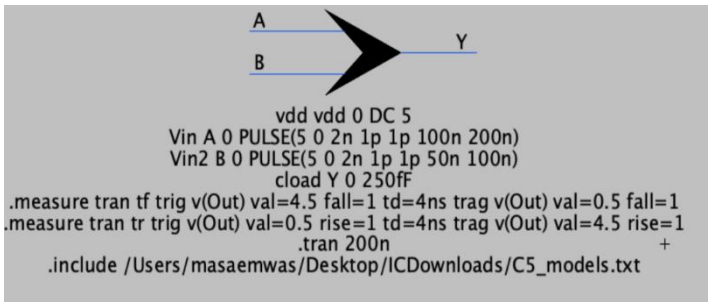


Figure 28: OR Gate Layout code

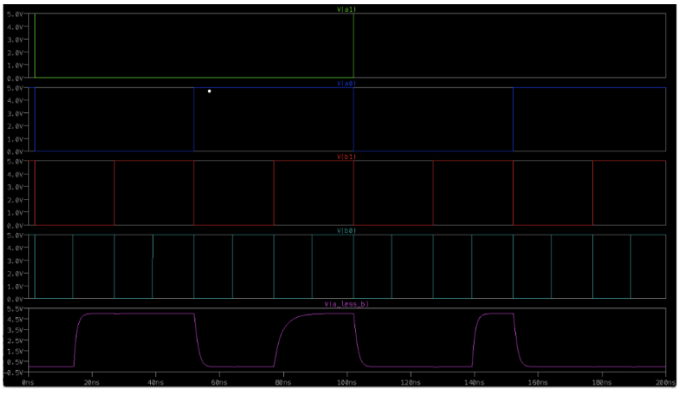


Figure. 32: 2-BIT Comparator Waveform A=B

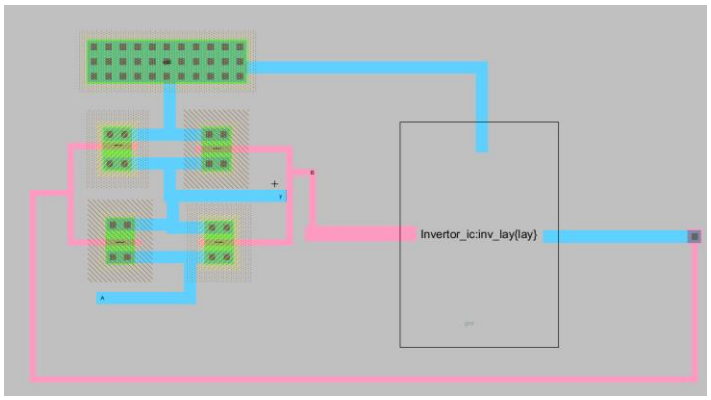


Figure 29: OR Layout.

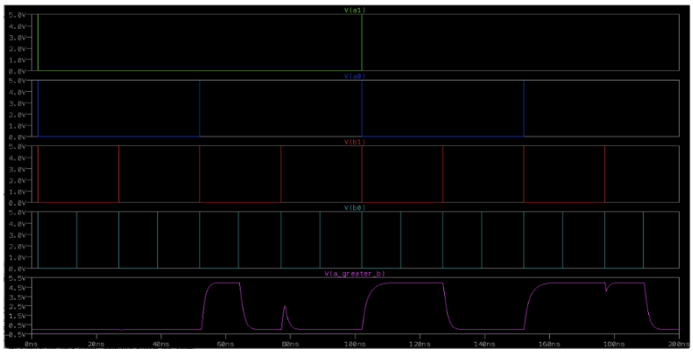


Figure.33: 2-BIT Comparator waveform A>B

2ND BIT COMPARATOR COMPLETE

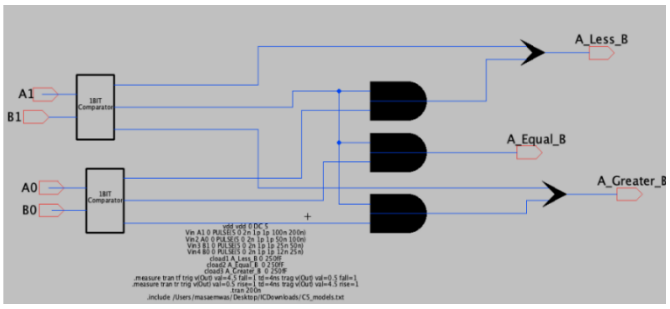


Figure 30:. 2-BIT Comparator Schemati

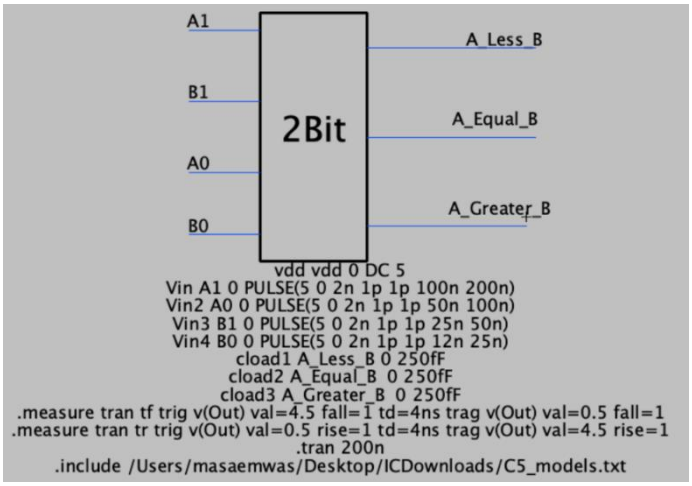


Figure 34: The 2-BIT Comparator Layout code.

4-bit comp Comparator

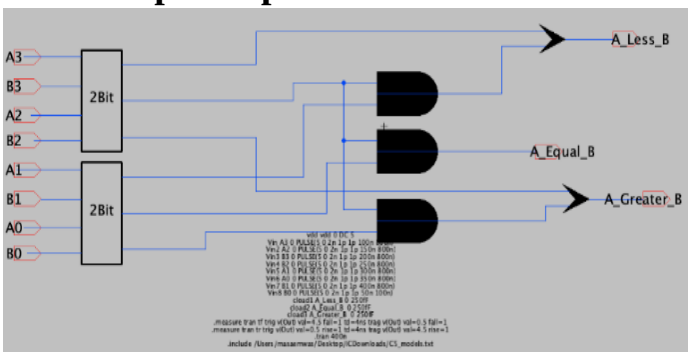


Figure 37. 4-BIT Comparator Schematic

4-BIT Comparator output bellow by change code to fet more output value.

.

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Table 11: Truth Table of 2-BIT Comparator.

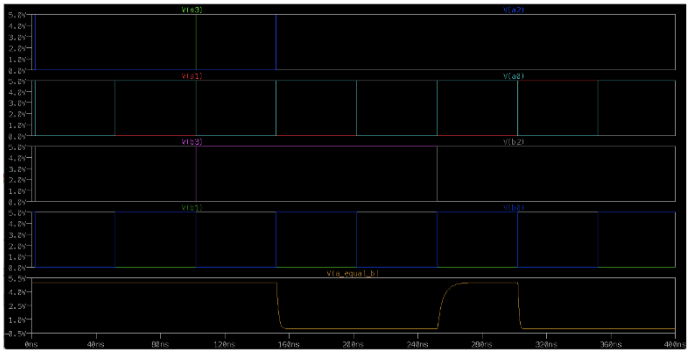


Figure 38 4-BIT Comparator waveform

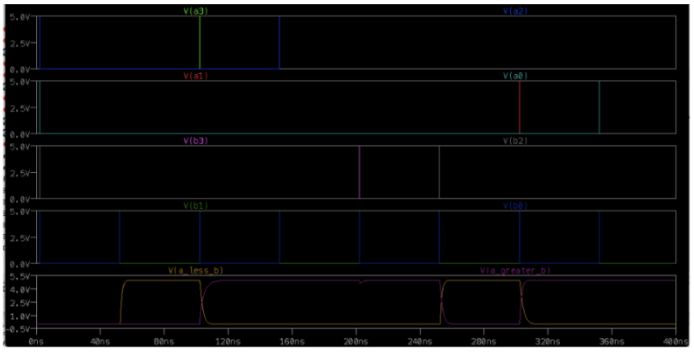


Figure 39 4-BIT Comparator waveform Of Less-Than (A<B) and Greater Than (A>B)

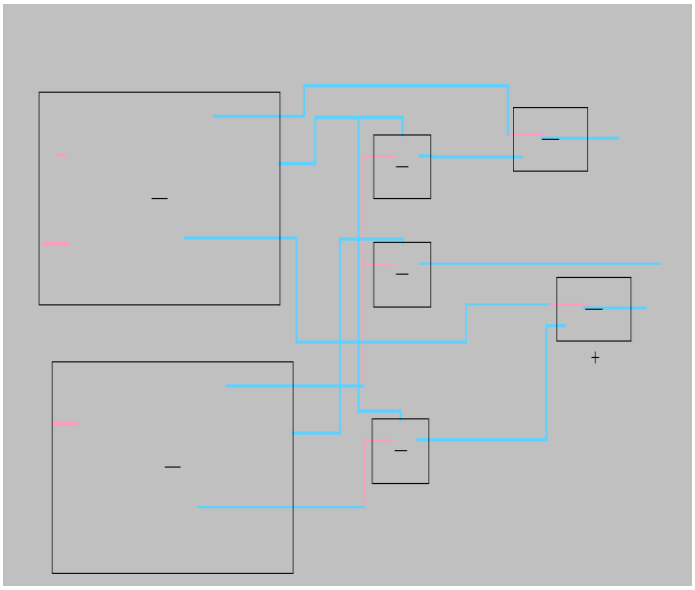


Figure 36: 2-BIT Comparator Layout.

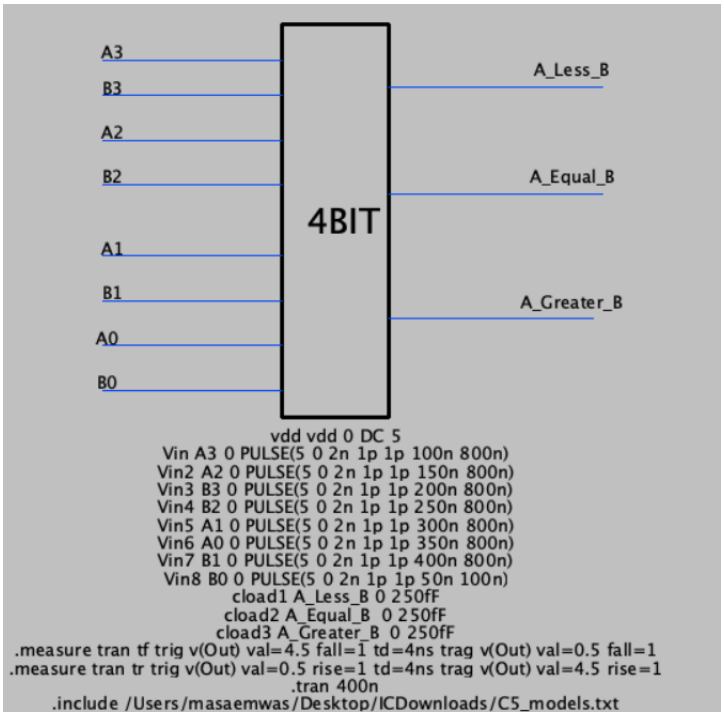


Figure 40: 4-BIT Comparator Layout code

- The code we use in layout Full adder to appear the wave above.

A3	A2	A1	A0	B3	B2	B1	B0	A<B	A>B
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	1	0	1
1	1	0	0	1	0	0	0	0	1
1	1	0	0	1	1	0	1	1	0
1	1	1	0	1	1	0	0	0	1
1	1	1	1	1	1	0	1	0	1

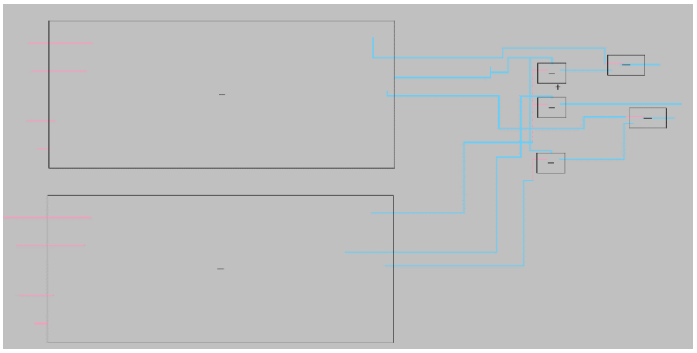


Figure 41: 4-BIT Comparator Layout.

A3	A2	A1	A0	B3	B2	B1	B0	A=B
0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1	1
1	0	0	0	1	0	0	0	1
1	1	0	1	1	0	0	1	0
1	1	0	0	1	0	0	0	0
1	1	0	1	1	1	0	1	1
1	1	1	0	1	1	0	0	0
1	1	1	1	1	1	0	1	0

Table 12: Truth Table 4-BIT Comparator

8-BIT Comparator

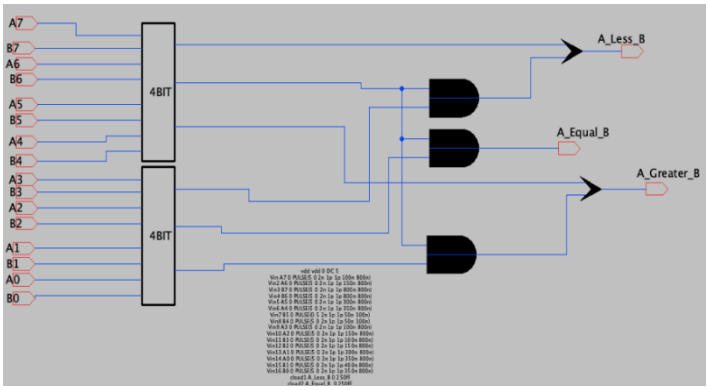


Figure42. 8-BIT Comparator Schematic

A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	A>B	A<B	A=B
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0
1	1	0	0	1	1	0	0	0	0	0	1	1	1	0	0	1	0	0
1	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0
1	1	0	0	1	1	0	0	0	0	0	1	1	1	0	0	1	0	0
1	1	1	0	1	1	1	0	0	0	0	0	1	1	0	0	1	0	0
1	1	1	1	1	1	1	1	0	0	0	1	1	1	0	1	1	0	0

Table13: Truth Table 8-BIT Comparator

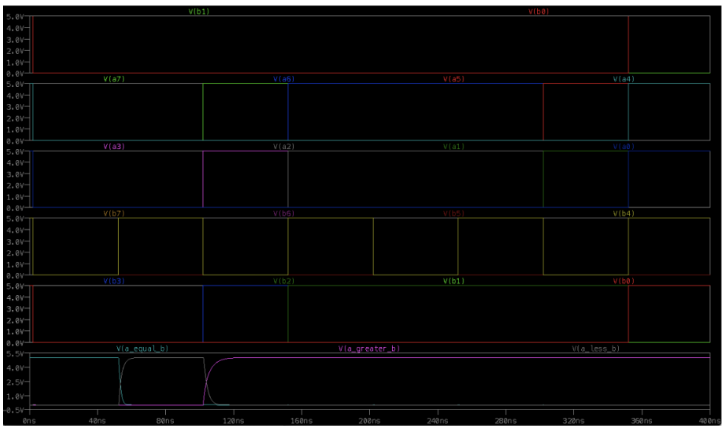


Figure43. 8-BIT Comparator waveform

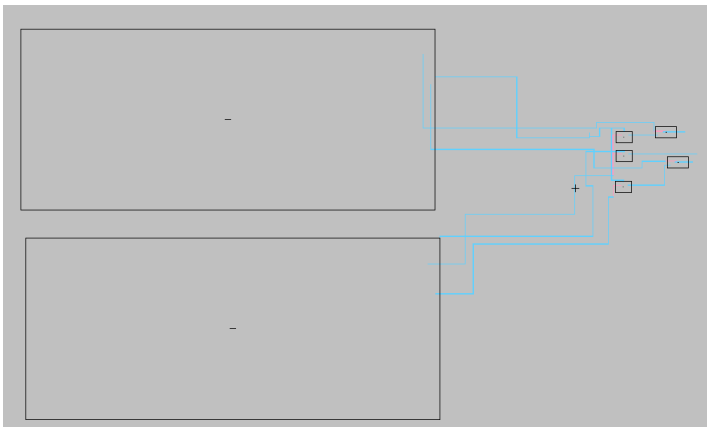


Figure 46: 8-BIT Comparator Layout

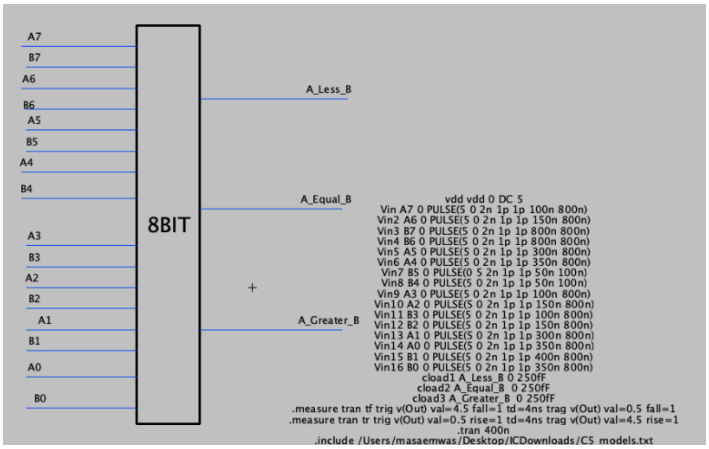


Figure 44: 8-BIT Comparator Layout code

CONCLUSION

In summary, this study has explored how Transmission Gate (TG) technology can be a beneficial alternative to traditional CMOS logic for designing advanced digital circuits, particularly focusing on n*n bit magnitude comparators. Using simulations with ELECTRIC TOOL EDA at 22nm process technology, we've highlighted the advantages of Transmission Gate.

The TG magnitude comparator demonstrated clear benefits over CMOS. It used only 14 transistors for a 1-bit comparator, 58 for 2 bits, 146 for 4 bits, and 322 for 8 bits, showing significant space savings as the bit size increased. Transmission Gate (TG) technology is chosen for implementing comparators due to its significant advantages in digital circuit design. TG circuits require fewer transistors compared to traditional CMOS logic, leading to lower power consumption and reduced heat generation, which enhances overall system reliability. These circuits also offer fast switching times and minimal propagation delays, making them ideal for applications needing high-speed performance and real-time responsiveness. Another key benefit is their robust noise immunity; TG circuits maintain signal integrity even in noisy environments by employing a high-impedance state when the control signal is inactive. Moreover, TG designs support full output swing, ensuring accurate and reliable digital outputs that reach close to supply voltages (VDD and ground). Their scalability allows TG technology to efficiently handle multi-bit comparators without increasing complexity, making it versatile and adaptable for various circuit requirements. Overall, these attributes make Transmission Gate technology a compelling choice for comparator implementation, particularly where reducing power consumption, minimizing delays, and enhancing noise immunity are crucial considerations

Gates/Performance Metric	Area (um^2)	Power	Delay(sec))
Inverter	40	1800 MicroWatt	6.54276e-08
AND	120	78.35 mWatt	50ns
NOR	160	97.5mW	100ns
OR	120	92.2mW	30ns

Table 14: Performance Metric For Basic Gates.

Gates/Performance Metric	Area (um^2)	Power	Delay	Power/Delay Product
1-Bit Comp	480	2.716375e-09	1.5193e-08	4.12698e-017
2-Bit Comp	1560	5.43275e-09	3.0386e-08	16.2088e-017
4-Bit Comp	3720	1.08655e-08	6.0772e-08	6.60318e-016
8-Bit Comp	8040	2.1731e-08	1.21544e-07	2.64127e-015

Table 15: Performance Metric For NxN Comparators.

REFERENCES

[1] https://research.ijcaonline.org/iceice/number6/iceice043.pdf [Accessed 10 June 2024, 14:45]

[2] https://www.quora.com/What-is-the-effect-of-temperature-on-CMOS-circuits [Accessed 9 June 2024, 20:00]

[3] https://www.researchgate.net/publication/275726067_Performance_Analysis_of_Magnitude_Comparator_using_Different_Design_Techniques [Accessed 12 June 2024, 16:00]

[4] https://www.ijesi.org/papers/Vol(2)1%20(version%202)/C211324.pdf [Accessed 13 June 2024, 19:30]

[5] https://www.geeksforgeeks.org/magnitude-comparator-in-digital-logic/ [Accessed 14 June 2024, 11:00]

[6] https://www.academia.edu/35425460/AREA_POWER_AND_DELAY_EFFICIENT_2_BIT_MAGNITUDE_COMPARATOR_Major_project_report?fbclid=IwZXh0bgNhZW0CMTAAAR22qApaI-Ru6rWQk5x7y3zCaJNfA8rt4LzLjHpPYVkEkFMAh6c6SGLM8Dc_aem_ZmFrZWR1bW15MTZieXRlcw [Accessed 14 June 2024, 12:00]

[7] LTSpice – Help

[8] https://drive.google.com/drive/folders/1bd9Z02yrsCj5Nvbs6psNKHpVX5ytUDtJ?fbclid=IwAR00uEI699q0JjAZSXP3-mCUIMxZslvkJt3ksZ8RrJROiobhkyQD0fll4s4