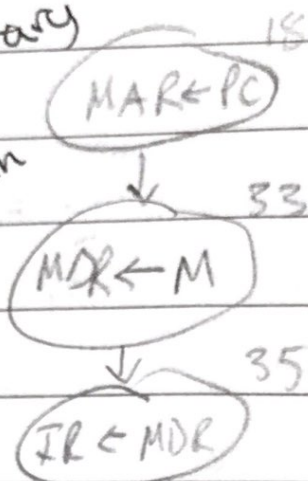


PC & MAR both are registers

Arbitrary
State
Diagram

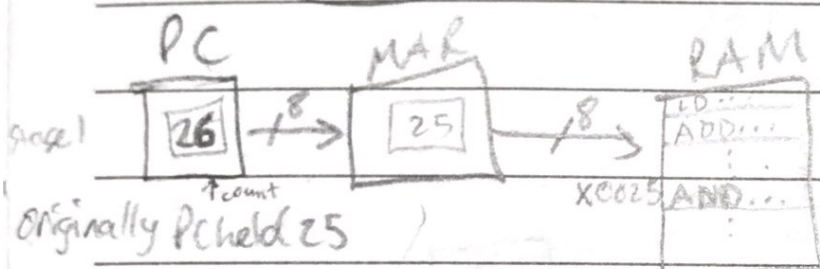


states correspond to ROM location

Arbitrary

10 11 10 01

AND R3, R2, R1



rudimentary control unit



MDR ← RAM

Bit 7 → 87 10111001 80

87 10111001 80

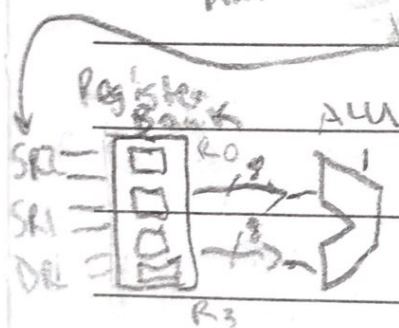
Decoder (Rom)



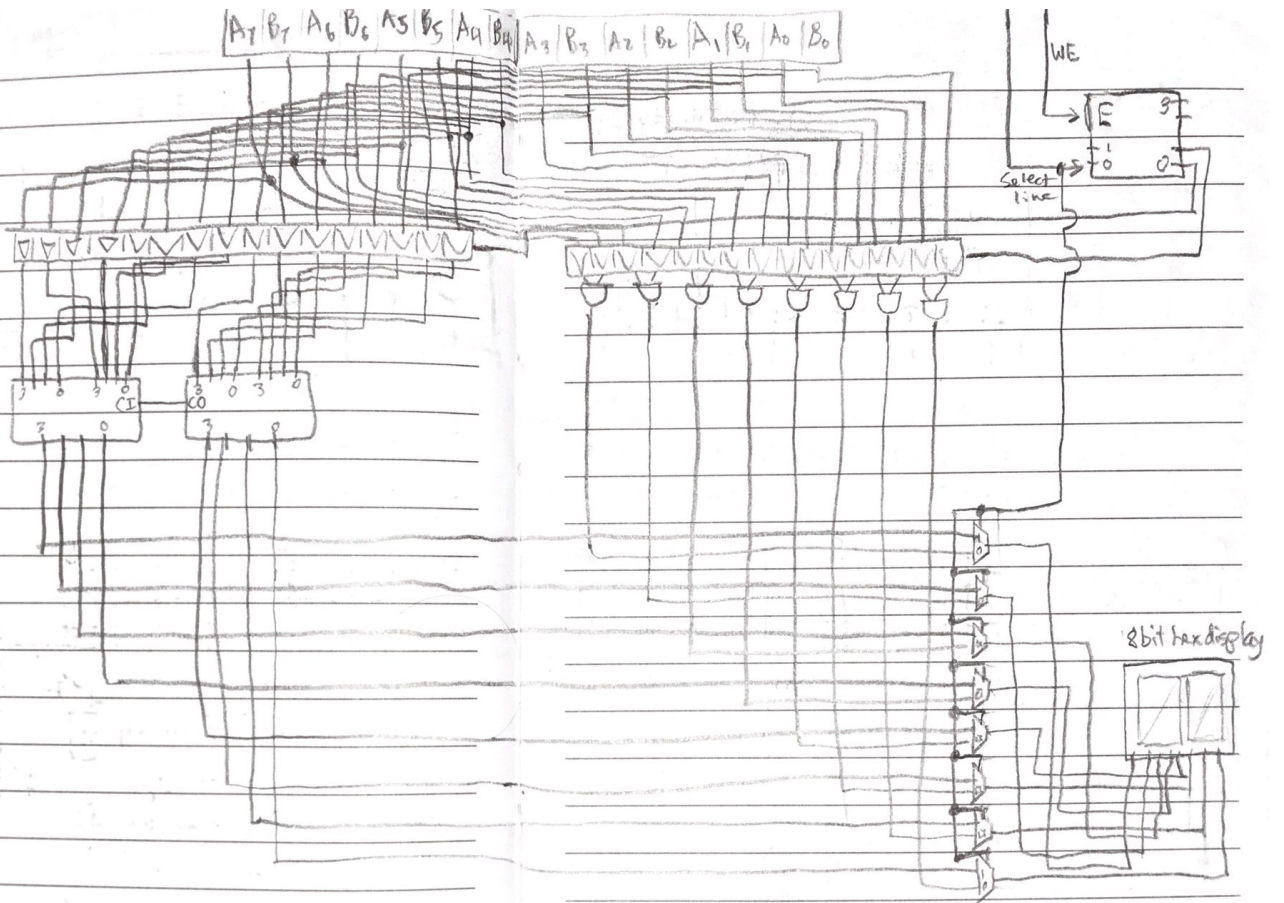
can be more lines into ROM

num of memory spaces you need

num of states in process
size of each mem space = # control lines



ALU



What needs to happen?

$IR[5],$
 $DR \leftarrow SR_1 + SR_2, \text{ set } CC,$
 $DR \leftarrow SR_1 \& SR_2, \text{ set } CC,$
 $[BEN],$
 $MAR \leftarrow PC, PC \leftarrow PC + 1,$
 $MDR \leftarrow M,$
 $IR \leftarrow MDR,$
 $IR[5] \& N + IR[4] \& 2 + IR[3] \& P, [IR[7:6]],$
 $MAR \leftarrow PC + \text{off } 4,$
 $MDR \leftarrow M[MAR],$
 $DR \leftarrow MDR, \text{ set } CC,$
 $MAR \leftarrow PC + \text{off } 4,$
 $MDR \leftarrow SR,$
 $M[MAR] \leftarrow MDR,$
 $PC \leftarrow PC + \text{off } 3,$

| Hex | # | Address | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|---------|-------|---|---|---|---|---|---|---|
| 0 | 0 | 0000 | | | | | | | | |
| 1 | 1 | 0001 | | | | | | | | |
| 2 | 2 | 0010 | | | | | | | | |
| 3 | 3 | 0011 | | | | | | | | |
| 4 | 4 | 0100 | | | | | | | | |
| 5 | 5 | 0101 | | | | | | | | |
| 6 | 6 | 0110 | | | | | | | | |
| 7 | 7 | 0111 | | | | | | | | |
| 8 | 8 | 1000 | | | | | | | | |
| 9 | 9 | 1001 | | | | | | | | |
| A | 10 | 1010 | | | | | | | | |
| B | 11 | 1011 | | | | | | | | |
| C | 12 | 1100 | | | | | | | | |
| D | 13 | 1101 | | | | | | | | |
| E | 14 | 1110 | | | | | | | | |
| F | 15 | 1111 | | | | | | | | |

The bits 0-7
 will be designated
 to select lines
 by us to control
 flow, for
 example, 1 line
 to determine
 Add/AND