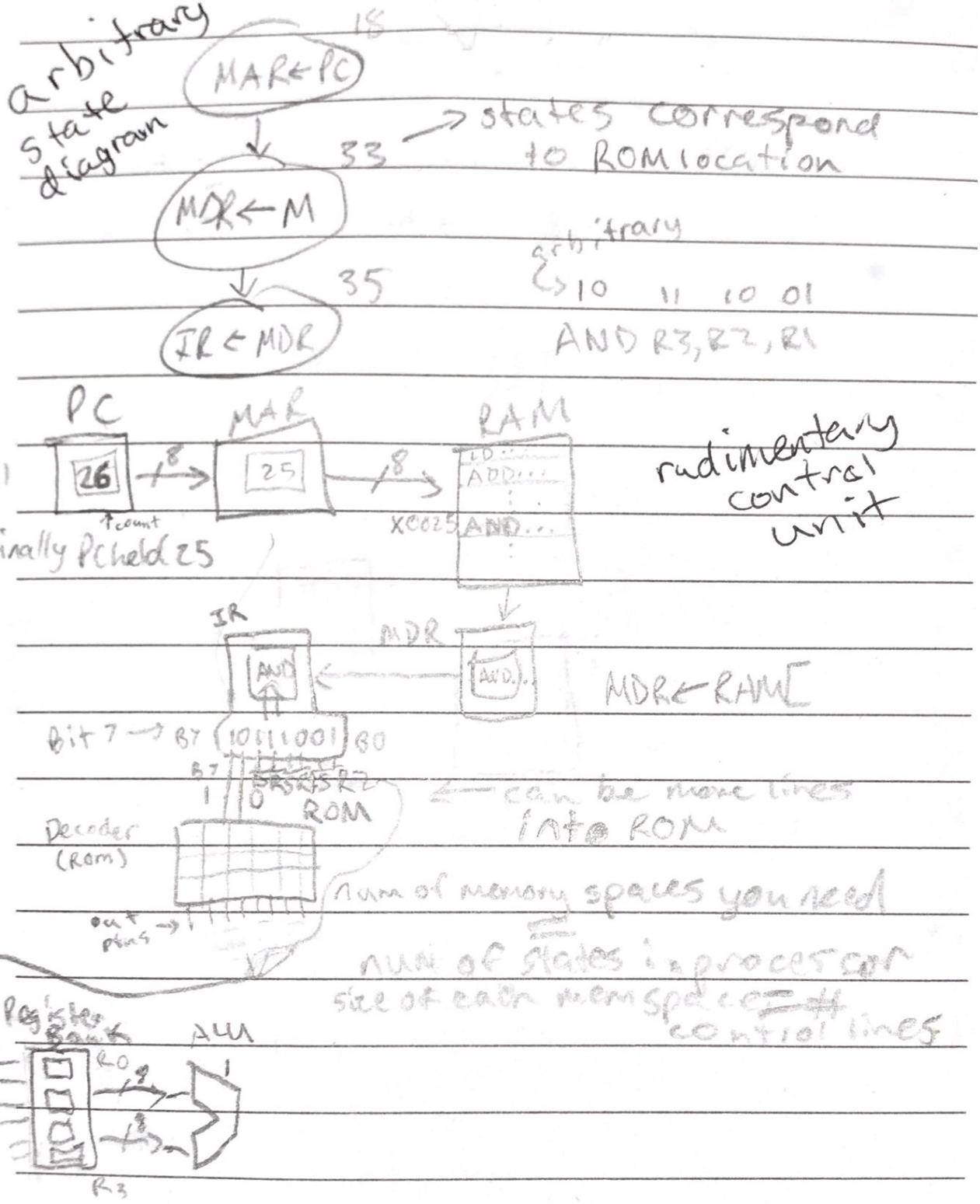
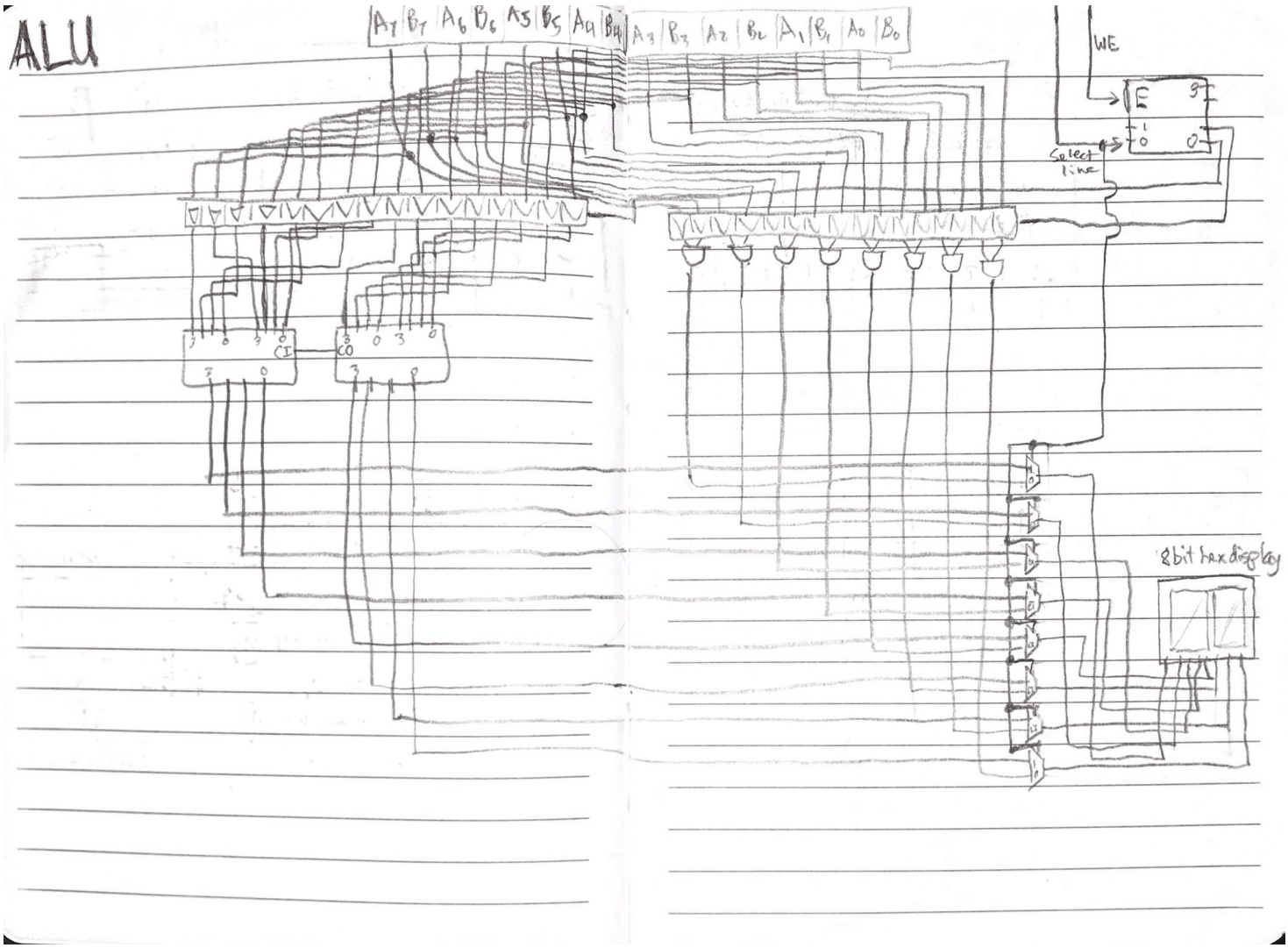
PC & MAR both are registers




ALU
A7 B7 A6 B6 A5 B5 A4 B4 A3 B3 A2 B2 A1 B1 A0 B0
WE
Select line
8bit hex display

What needs to happen?

IR[5],

DR ← SR1 + SR2, set CC,

DR ← SR1 & SR2, set CC,

[BEN],

MAR ← PC, PC ← PC+1,

MDR ← M,

IR ← MDR,

IR[5] & N + IR[4] & Z + IR[3] & P, [IR[7:6]],

MAR ← PC + off4,

MDR ← M[MAR],

DR ← MDR, set CC,

MAR ← PC + off4,

MDR ← SR,

M[MAR] ← MDR,

PC ← PC + off3,

ROM

Hex #	Address	Bit 7	6	5	4	3	2	1	0
0	0000								
1	0001								
2	0010								
3	0011								
4	0100								
5	0101								
6	0110								
7	0111								
8	1000								
9	1001								
A	1010								
B	1011								
C	1100								
D	1101								
E	1110								
F	1111								

The bits 0-7 will be designated to select lines by us to control flow, for example, 1 line to determine Add/AND

GWLC ISA:

	Opcode							
LD	0	0	0	R0/R1	Offset 4			
ST	0	0	1	R0/R1	offset 4			
ADD	0	1	DR		SR		SR	
AND	1	0	DR		SR		SR	
BR	1	1	n	z	p	offset 3		
Bit#:	7	6	5	4	3	2	1	0

Finite state diagram