CSE460

Lab Assignment 5

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Section: 4

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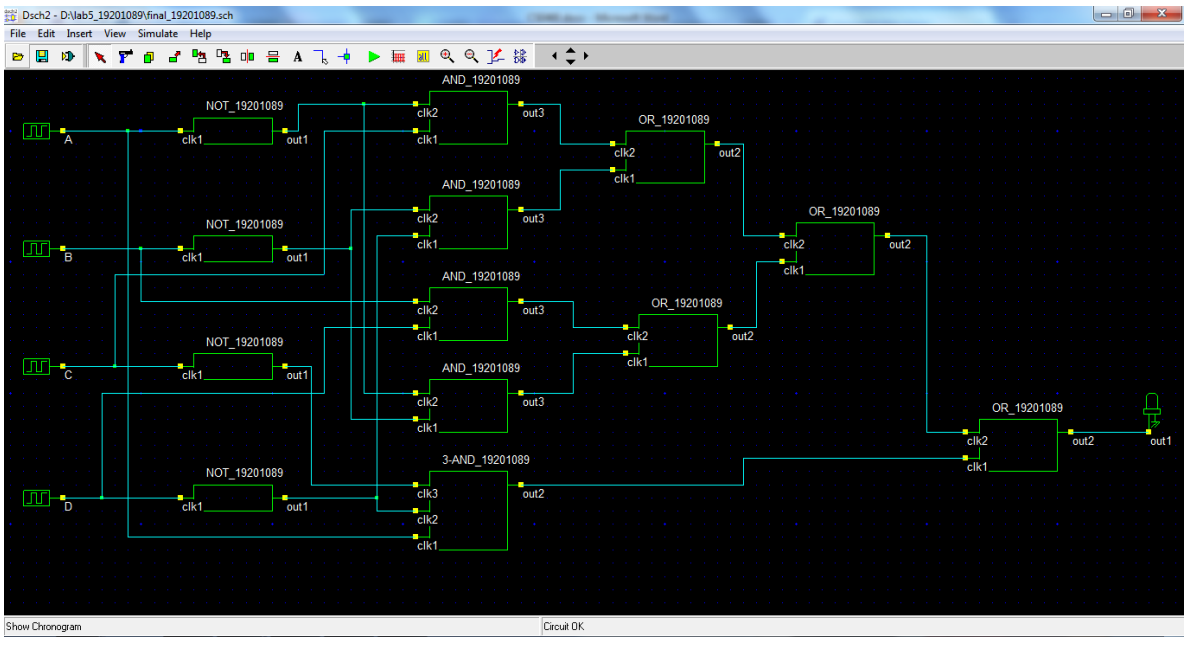
Problem: Derive the Boolean logic expression from the following K-Map and implement the logic function using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but cannot use readily available logic gates.

Solution:

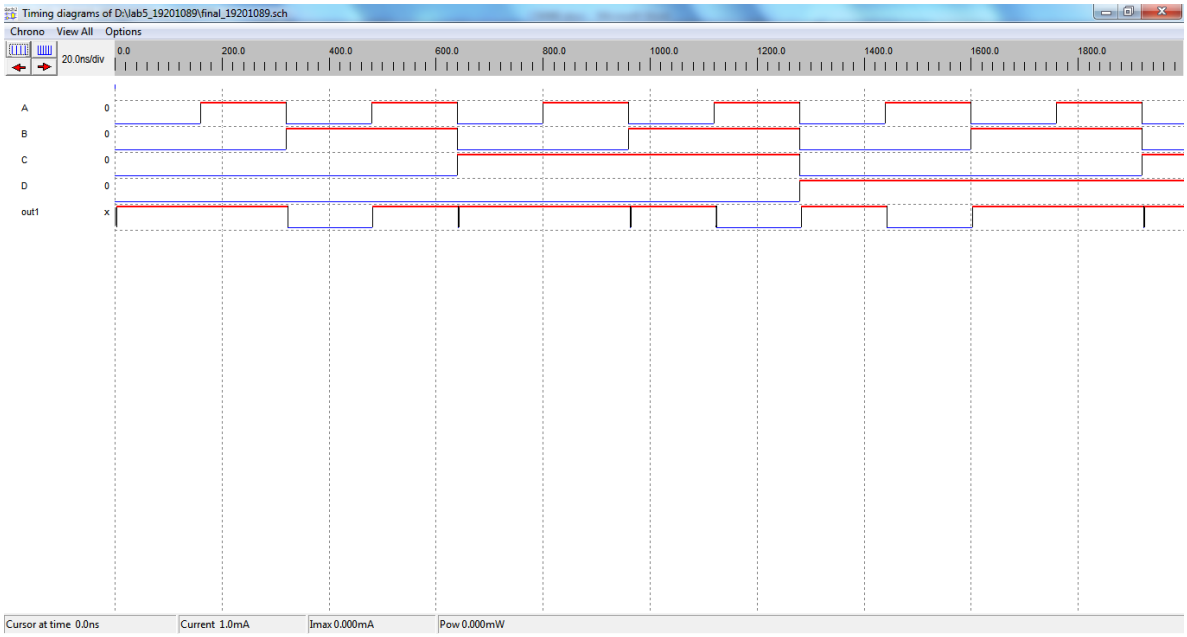
CD \ AB	00	01	11	10
00	1	0	1	1
01	1	d	d	0
11	d	d	1	0
10	1	1	0	1

Boolean expression: $\overline{B}\overline{D} + BD + \overline{A}C + \overline{A}\overline{B} + A\overline{C}\overline{D}$

Circuit Design:



Timing Diagram:



Explanation:

Truth Table:

A	B	C	D	output
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

In timing diagram, when the input all 0, then output is 1. When input is 1, 0, 0, 0 then output is 1. When input is 0, 1, 0, 0 then output is 0. This all match with the truth table. Similarly, the following input-output match in the following clock cycle as well. So we can determine that the simulation is correct.