CSE460

Lab Assignment 6

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Section: 4

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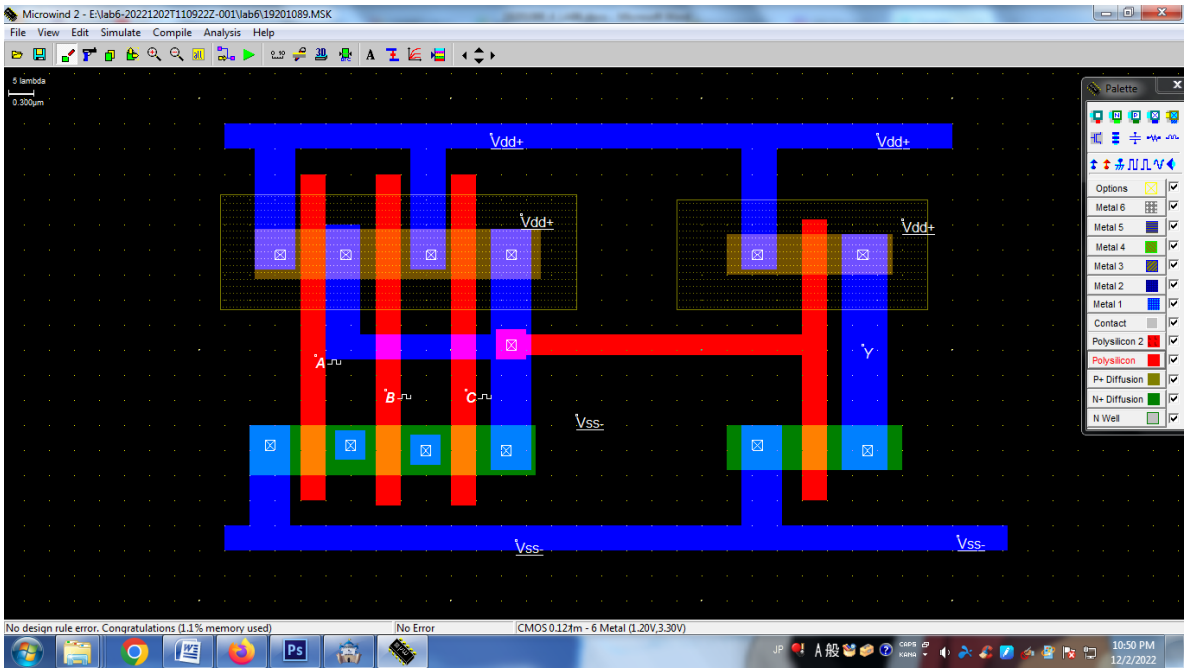
Task: Draw the layout of AND3 and verify it with timing diagram.

Layout:



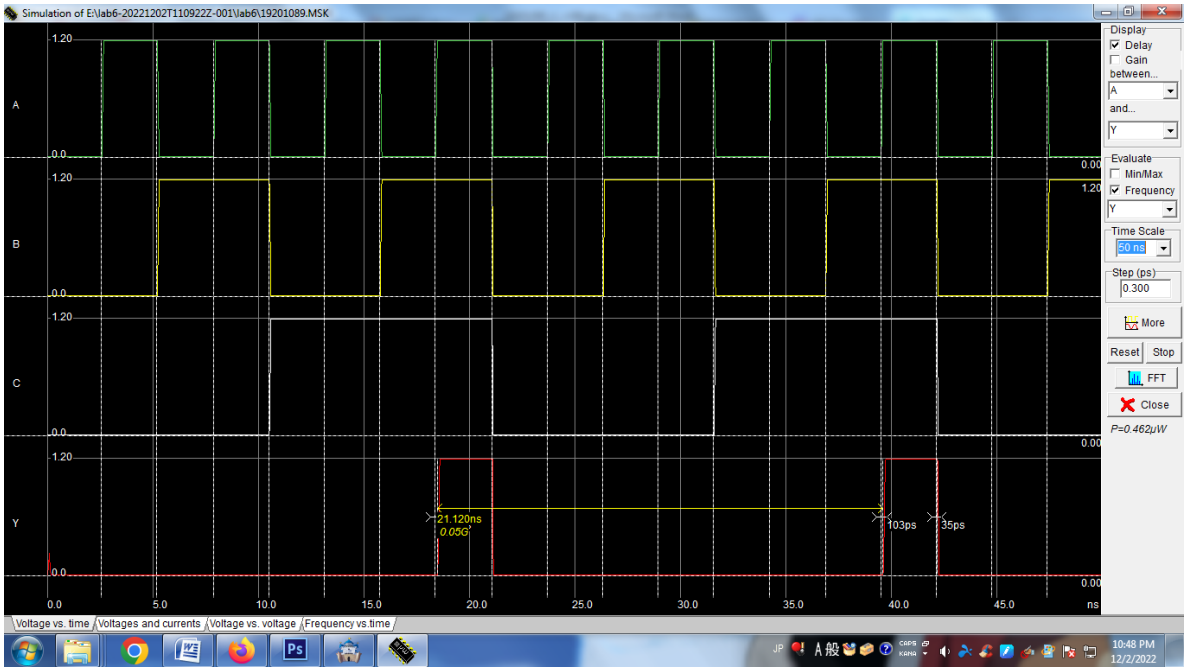
Here, I have drawn the layout of NAND3 and connected an inverter to the output to invert it. So this becomes the layout of AND3.

Truth Table:

Expression: A. B. C

A	B	C	Output (Y)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Timing Diagram:



Discussion:

We know that for AND gate, the output is 1 only if all the inputs are 1. In the timing diagram, we can see two instances where the output, Y is high. For both cases, A, B and C are all high. In every other case, at least one of the inputs is low. So the output is also low. We can confirm this from the truth table and hence, verify that the simulation is accurate.