CSE460

Lab Assignment 4

Submitted by: Masiat Hasin Rodoshi

ID: 19201089

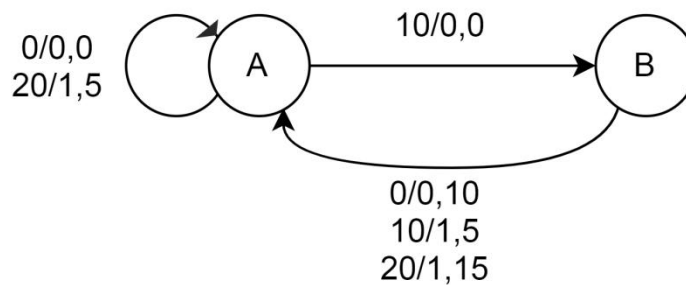Section: 4

Date: 16.11.2022

Problem Description:

We are to design a vending machine using Verilog such that:

- We can only insert no money, Tk 10 and Tk 20.
- If the inserted amount is equal to or more than Tk 20, then the product is bought and otherwise, the machine goes back to initial state and gives change if necessary.

A. State Diagram

B. the machine will return 4 types of changes- Tk 0, Tk 5, Tk 10 and Tk 15. Chg should be 2 bits to represent the returned money in code.

C. State Assigned Table

Present State	Next State			Output					
				buy			chg		
	00 (00)	01 (10)	10 (20)	00 (00)	01 (10)	10 (20)	00 (00)	01 (10)	10 (20)
0 (A)	0	1	0	0	0	1	00 (0)	00 (0)	01 (5)
1 (B)	0	0	0	0	1	1	10 (10)	01 (5)	11 (15)

D. Verilog Code

module lab4_19201089(clk, reset, cash_in, buy, chg, present_state, next_state);

    input clk, reset;

    input [1:0]cash_in;

```verilog
output reg buy;

output reg [1:0]chg;


output reg present_state, next_state;


parameter A = 1'b0, B = 1'b1;
parameter [1:0] in_tk0 = 2'b00,

                        in_tk10 = 2'b01,

                        in_tk20 = 2'b10,


                        chg_tk0 = 2'b00,

                        chg_tk5 = 2'b01,

                        chg_tk10 = 2'b10,

                        chg_tk15 = 2'b11;


always @(posedge clk, posedge reset)
begin

        if (reset == 1)

        begin

                present_state = A;

                next_state = A;

                buy = 0;

                chg = chg_tk0;

        end

        else
```

```verilog
begin
    present_state = next_state;
    case (present_state)
        A:
        begin
            if(cash_in == in_tk0)
            begin
                next_state = A;
                buy = 0;
                chg = chg_tk0;
            end
            else if(cash_in == in_tk10)
            begin
                next_state = B;
                buy = 0;
                chg = chg_tk0;
            end
            if(cash_in == in_tk20)
            begin
                next_state = A;
                buy = 1;
                chg = chg_tk5;
            end
        end
```
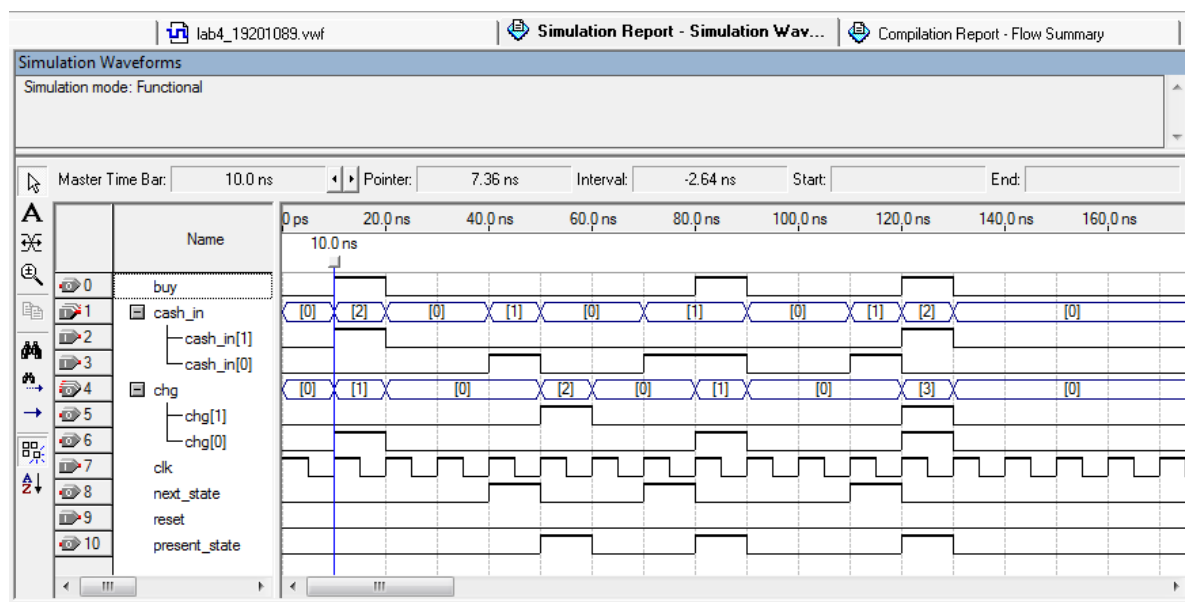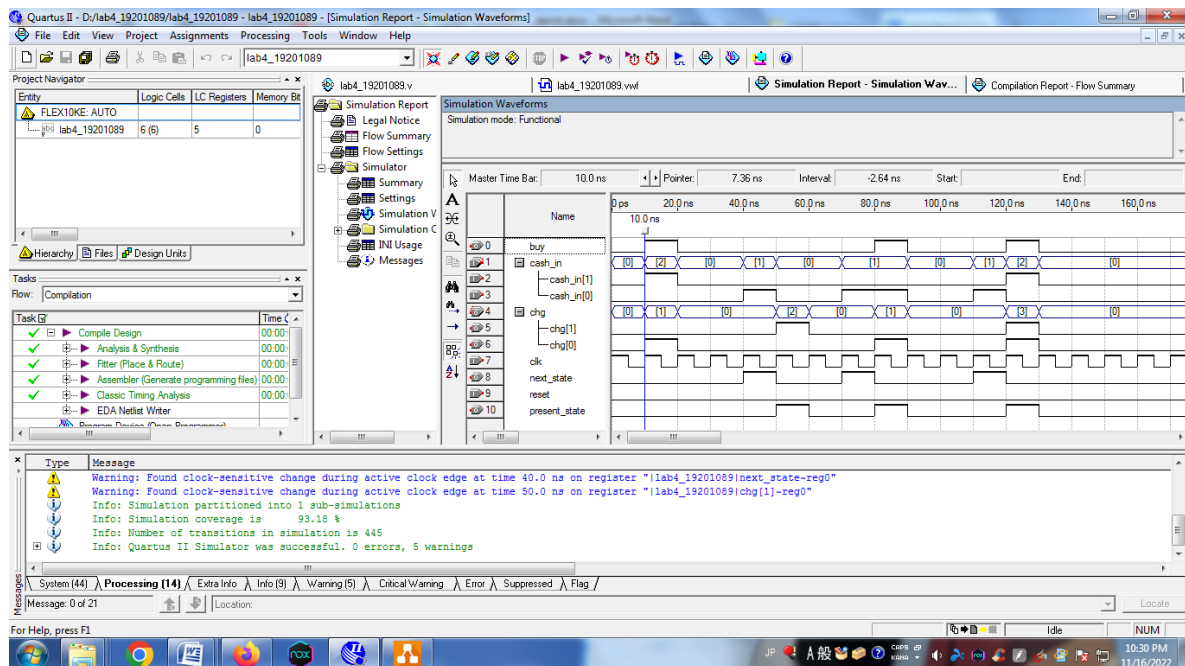
```verilog
			B:
			begin
				if(cash_in == in_tk0)
				begin
					next_state = A;
					buy = 0;
					chg = chg_tk10;
				end
				else if(cash_in == in_tk10)
				begin
					next_state = A;
					buy = 1;
					chg = chg_tk5;
				end
				if(cash_in == in_tk20)
				begin
					next_state = A;
					buy = 1;
					chg = chg_tk15;
				end
			end
		endcase
	end
end
endmodule
```

E.

At 10ns, we gave input Tk 20 (10). The machine returned change Tk 5 (01) immediately because 20 is greater than the price of the product which is Tk 15. The machine also let us buy the product (buy = 1). At 40ns, we gave input Tk 10 (01) but this amount is less than Tk 15. So, the machine waited for further input but we didn't input any money. So, the machine returned the Tk 10 (10) back to us and didn't let us buy the product (buy = 0). At 70ns, we input Tk 10 (01) followed by another Tk 10 (01) and this times our total was Tk 20 which is greater than Tk 15. So, the machine returned Tk 5

(01) and let us buy the product (buy = 1). Finally, at 120ns, We first insert Tk 10 (01) and then input Tk 20 (10) making our total Tk 30. So, the machine returned Tk 15 (11) and we were able to buy the product (buy = 1).