CSE460

Lab Assignment 3

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Section: 4

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Problem statement: A sequential circuit has two inputs, **w1** and **w2**, and an output, **z**. Its function is to compare the input sequences on the two inputs. If **w1 = w2** during any **four** consecutive clock cycles, the circuit produces **z = 1**; otherwise, **z = 0**.

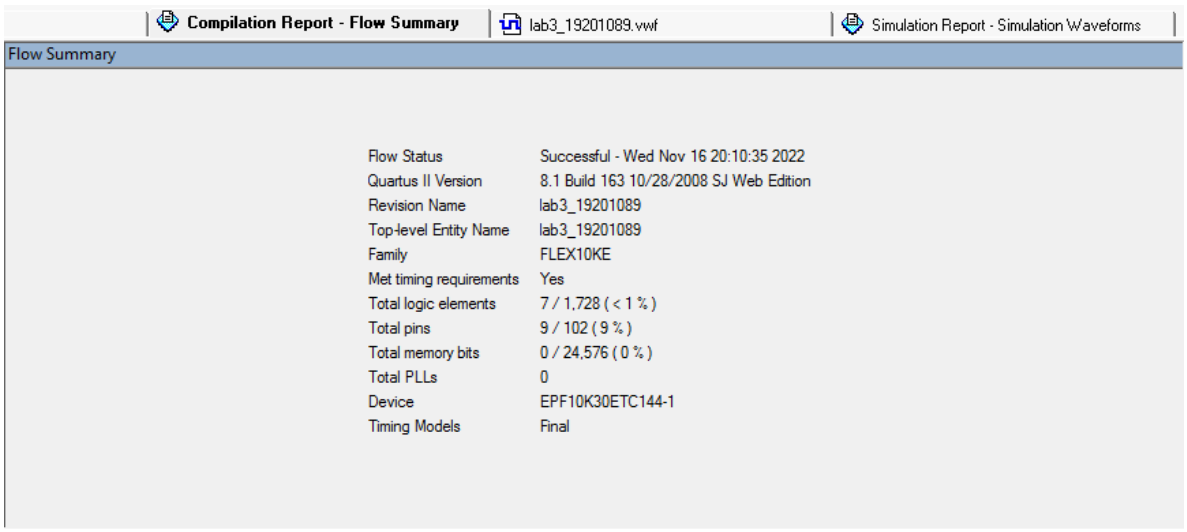
Code implementation:

```
module lab3_19201089(z,w1,w2,clk,reset,next_state,current_state);

input clk, reset, w1, w2;

output reg z;

output reg [1:0] current_state, next_state;

parameter [1:0] A=2'b00, B =2'b01, C =2'b10, D =2'b11;

        always @(posedge clk, posedge reset)

                if (reset == 1)

                begin

                        current_state = A;

                        next_state = A;

                end

                else

                begin

                        current_state = next_state;

                        case(current_state)

                                A: if ((w1 == 0 && w2 == 1) || (w1 == 1 && w2 == 0))

                                                begin

                                                z <= 0;

                                                next_state <= A;

                                                end

                else

                                                begin
```

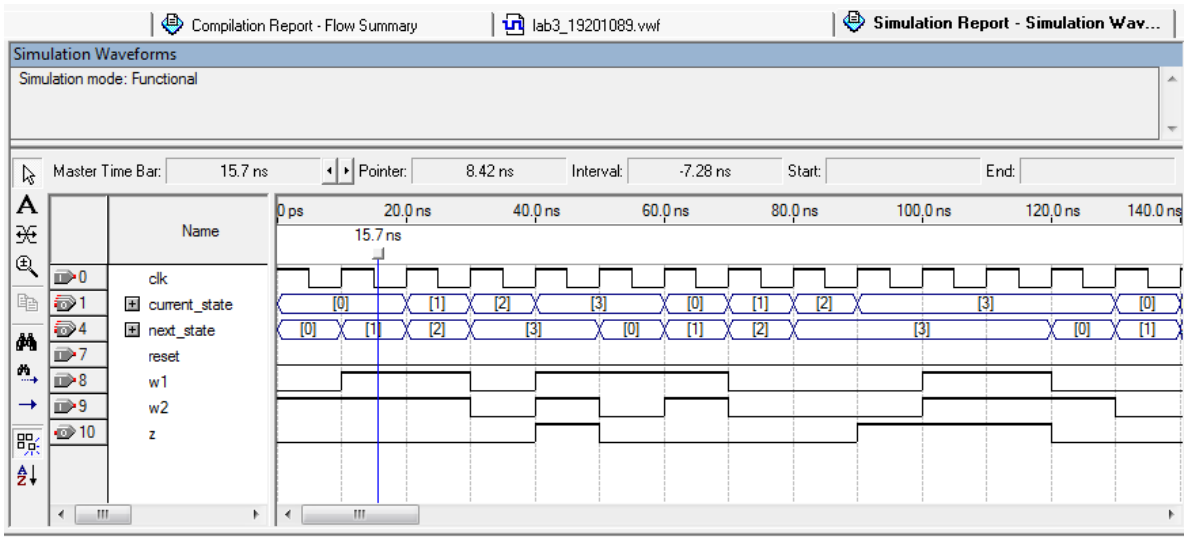
```
                z <= 0;
                next_state <= B;
                end

B: if ((w1 == 0 && w2 == 0) || (w1 == 1 && w2 == 1))
                begin
                z <= 0;
                next_state <= C;
                end
        else
                begin
                z <= 0;
                next_state <= A;
                end
C: if ((w1 == 0 && w2 == 0) || (w1 == 1 && w2 == 1))
                begin
                z <= 0;
                next_state <= D;
                end
        else
                begin
                z <= 0;
                next_state <= A;
                end
D: if ((w1 == 0 && w2 == 0) || (w1 == 1 && w2 == 1))
```

```
                    begin
                    z <= 1;
                    next_state <= D;
                    end
                else
                    begin
                    z <= 0;
                    next_state <= A;
                    end
            endcase
        end
endmodule
```

Compilation report:



Simulation report:



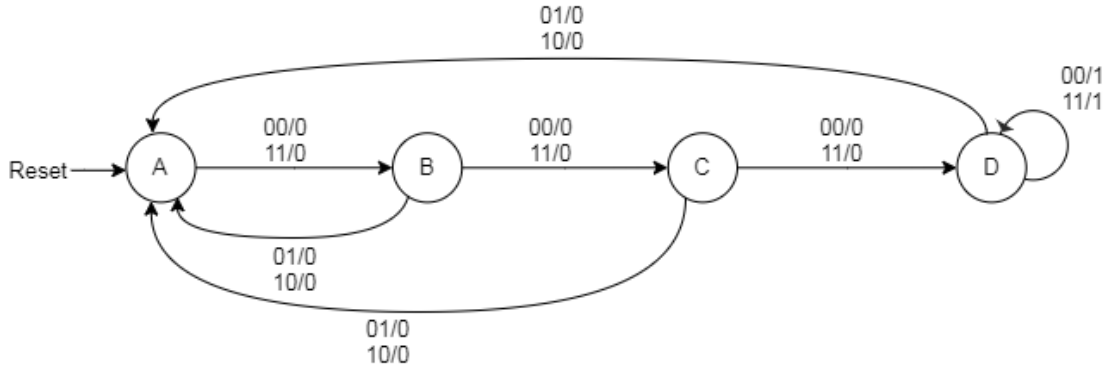
Discussion:

According to the question, we are to design a finite state machine that takes two inputs, w1 and w2 and gives the output z. If w1 = w2 for any four consecutive clock cycles, then z = 1, otherwise z = 0.

For example:

w1 : 0 1 1 0 1 1 1 0 0 0 1 1 0
w2 : 1 1 1 0 1 0 1 0 0 0 1 1 1
z : 0 0 0 0 1 0 0 0 0 1 1 1 0

This is a mealy type machine because the output is generated in the same clock cycle where the conditions have been met. We can see the FSM for this problem below.



Since the length of the accepted string is four, we have four states and we go to the next state when w1 = w2 and w1, w2 can be either 0 or 1. State D is the final accepting state where z= 1 and we will remain here as long as w1 = w2. However, in any state, if we find w1 ≠ w2, we will return to state A which is the starting state and try again to find a sequence that meets the requirements.

In the timing diagram, at time = 40ns, we find z = 1 because in this clock cycle and the previous three clock cycles, the values of w1 were equal to w2. Similarly, from time 90-110ns, z=1 because the consecutive four values including their respective clock cycles saw w1 = w2. Therefore, we can say that the simulation is accurate.