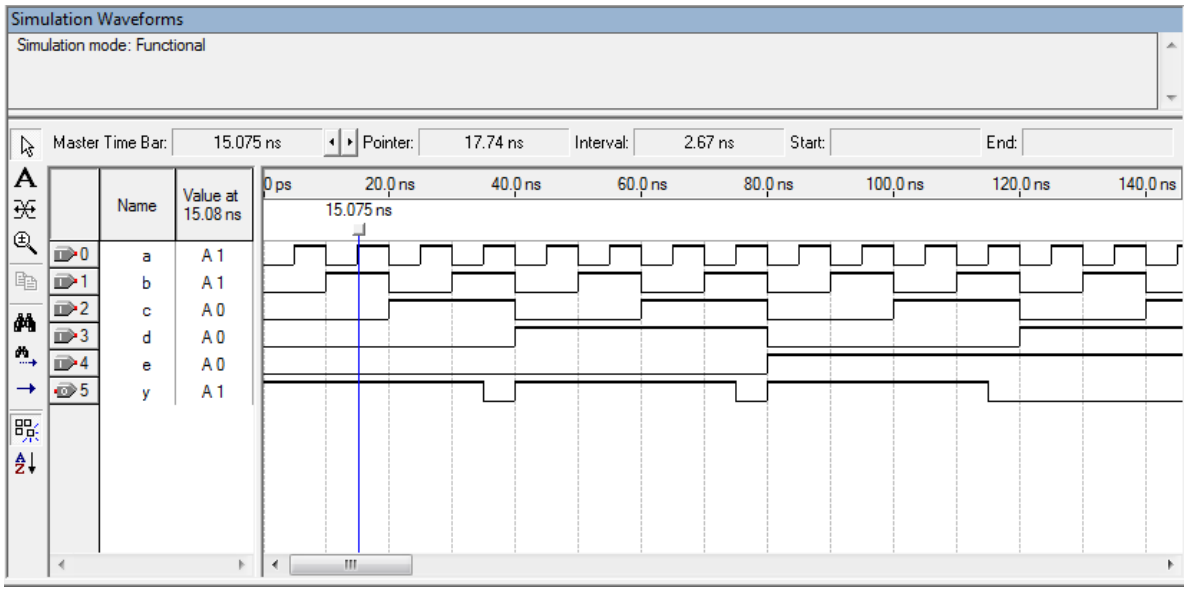
Problem Statement: Write a Verilog code to implement the AOI-32 gate and verify it with the timing diagram in Quartus.

Code:

```
module lab1 (a,b,c,d,e,y);


input a,b,c,d,e;

output y;


assign p = a&b&c;

assign q = d&e;

assign r = p|q;

assign y = ~r;


endmodule
```

Simulation report

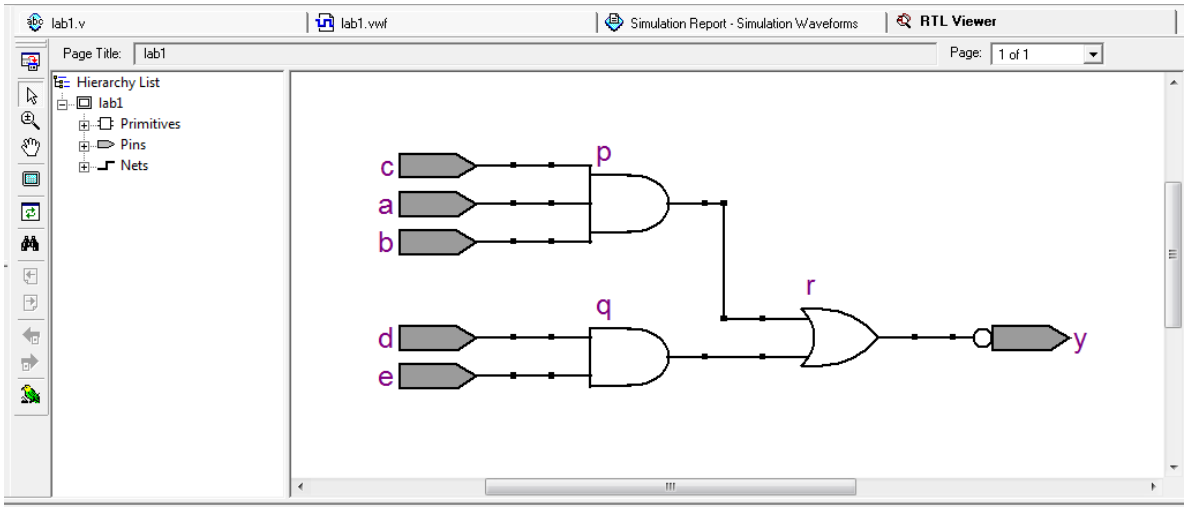


Truth Table

The boolean expression of the AOI-32 gate is $\overline{(ABC + DE)}$

sl.	A	B	C	P = A&B&C	D	E	Q = D&E	R = P|Q	Y = ~R
1	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0	0	1
3	0	0	0	0	1	0	0	0	1
4	0	0	0	0	1	1	1	1	0
5	0	0	1	0	0	0	0	0	1
6	0	0	1	0	0	1	0	0	1
7	0	0	1	0	1	0	0	0	1
8	0	0	1	0	1	1	1	1	0
9	0	1	0	0	0	0	0	0	1
10	0	1	0	0	0	1	0	0	1
11	0	1	0	0	1	0	0	0	1
12	0	1	0	0	1	1	1	1	0
13	0	1	1	0	0	0	0	0	1
14	0	1	1	0	0	1	0	0	1
15	0	1	1	0	1	0	0	0	1
16	0	1	1	0	1	1	1	1	0
17	1	0	0	0	0	0	0	0	1
18	1	0	0	0	0	1	0	0	1
19	1	0	0	0	1	0	0	0	1
20	1	0	0	0	1	1	1	1	0
21	1	0	1	0	0	0	0	0	1
22	1	0	1	0	0	1	0	0	1
23	1	0	1	0	1	0	0	0	1
24	1	0	1	0	1	1	1	1	0
25	1	1	0	0	0	0	0	0	1
26	1	1	0	0	0	1	0	0	1
27	1	1	0	0	1	0	0	0	1
28	1	1	0	0	1	1	1	1	0
29	1	1	1	1	0	0	0	1	0
30	1	1	1	1	0	1	0	1	0
31	1	1	1	1	1	0	0	1	0
32	1	1	1	1	1	1	1	1	0

RTL View



Let us compare the results from the truth table and the timing diagram. Here, Y' is the result found in timing diagram.

sl. in truth table	A	B	C	D	E	Y	Y'	Time (ns)
7	0	0	1	1	0	1	1	60
2	0	0	0	0	1	1	1	80
4	0	0	0	1	1	0	0	120

The timing diagram shows the result in time. We consider higher level as 1 and lower level as 0. From the truth table, the second row shows that a, b, c, d inputs are 0 and e is 1. The output is 1. We can see from the simulation report at 80 ns that the output indeed is 1 for this combination of inputs. In the fourth row, the inputs a, b, c are 0 and the inputs d, e are 1 and the output is 0. At 120 ns in the timing diagram, the output is 0 for the input combination. Similarly, the seventh row of the truth table shows that the output is 1 if inputs a, b, e are 0 and c, d are 1. We can see that at 60 ns, the output is indeed 1 for said inputs. Based on these comparisons, we can say that the timing diagram complies with the truth table and is accurate.