ST7735R

262K Color Single-Chip TFT Controller/Driver

1 Introduction

The ST7735R is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 396 source line and 162 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bit/9-bit/16-bit/18-bit parallel interface. Display data can be stored in the on-chip display data RAM of 132 x 162 x 18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

2 Features

Single chip TFT-LCD Controller/Driver with RAM
On-chip Display Data RAM (i.e. Frame Memory)
132 (H) x RGB x 162 (V) bits

LCD Driver Output Circuits:
Source Outputs: 132 RGB channels
Gate Outputs: 162 channels
Common electrode output

Display Colors (Color Mode)
Full Color: 262K, RGB=(666) max., Idle Mode OFF
Color Reduce: 8-color, RGB=(111), Idle Mode ON

Programmable Pixel Color Format (Color Depth) for Various Display Data input Format
12-bit/pixel: RGB=(444) using the 384k-bit frame memory and LUT
16-bit/pixel: RGB=(565) using the 384k-bit frame memory and LUT
18-bit/pixel: RGB=(666) using the 384k-bit frame memory and LUT

Various Interfaces
Parallel 8080-series MCU Interface
(8-bit, 9-bit, 16-bit & 18-bit)
Parallel 6800-series MCU Interface
(8-bit, 9-bit, 16-bit & 18-bit)
3-line serial interface
4-line serial interface

Display Features
Support both normal-black & normal-white LC
Software programmable color depth mode

Built-in Circuits
DC/DC converter
Adjustable VCOM generation
Non-volatile (NV) memory to store initial register setting
Oscillator for display clock generation
Factory default value (module ID, module version, etc) are stored in NV memory
Timing controller

Built-in NV Memory for LCD Initial Register Setting
7-bits for ID2
8-bits for ID3
7-bits for VCOM adjustment

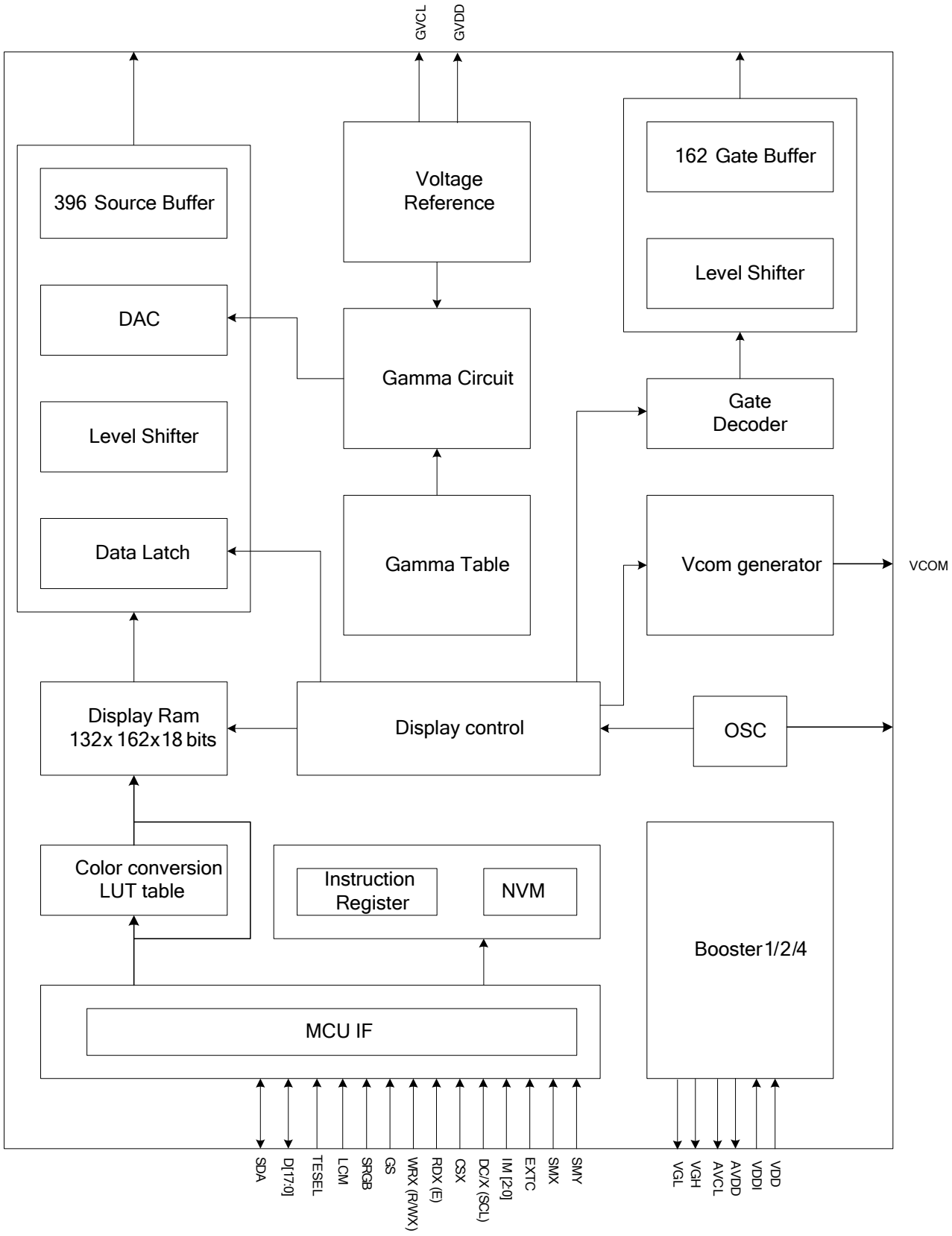
Wide Supply Voltage Range
I/O Voltage (VDDI to DGND): 1.65V~3.7V (VDDI ≤ VDD)
Analog Voltage (VDD to AGND): 2.3V~4.8V

On-Chip Power System
Source Voltage (GVDD to AGND): 3.0V~4.5V
VCOM level (VCOM to AGND): -0.4V to -2.0V
Gate driver HIGH level (VGH to AGND): +10.0V to +15V
Gate driver LOW level (VGL to AGND): -13V to -7.5V

Operating Temperature: -30℃ to +85℃

ST7735R	**Parallel Interface: 8080,6800(8-bit/9-bit/16-bit/18-bit)** **Serial Interface: 3-line, 4-line**

5 Block diagram



6 Driver IC Pin Description

6.1 Power Supply Pin

Name	I/O	Description	Connect pin
VDD	I	Power supply for analog, digital system and booster circuit.	VDD
VDDI	I	Power supply for I/O system.	VDDI
AGND	I	System ground for analog system and booster circuit.	GND
DGND	I	System ground for I/O system and digital system.	GND

6.2 Interface logic pin

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect pin</th></tr>
<tr><td>P68</td><td>I</td><td>-8080/6800 MCU interface mode select.
-P68='1', select 6800 MCU parallel interface.
-P68='0', select 8080 MCU parallel interface.
-If not used, please fix this pin at DGND level.</td><td>DGND/VDDI</td></tr>
<tr><td>IM2</td><td>I</td><td>MCU Parallel interface bus and Serial interface select
IM2='1', Parallel interface
IM2='0', Serial interface</td><td>DGND/VDDI</td></tr>
<tr><td>IM1,IM0</td><td>I</td><td>- MCU parallel interface type selection
-If not used, please fix this pin at VDDI or DGND level.
<table>
<tr><th>IM1</th><th>IM0</th><th>Parallel interface</th></tr>
<tr><td>0</td><td>0</td><td>MCU 8-bit parallel</td></tr>
<tr><td>0</td><td>1</td><td>MCU 16-bit parallel</td></tr>
<tr><td>1</td><td>0</td><td>MCU 9-bit parallel</td></tr>
<tr><td>1</td><td>1</td><td>MCU 18-bit parallel</td></tr>
</table></td><td>DGND/VDDI</td></tr>
<tr><td>SPI4W</td><td>I</td><td>- SPI4W='0', 3-line SPI enable.
- SPI4W='1', 4-line SPI enable.
-If not used, please fix this pin at DGND level.</td><td>DGND/VDDI</td></tr>
<tr><td>RESX</td><td>I</td><td>-This signal will reset the device and it must be applied to properly initialize the chip.
-Signal is active low.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>-Chip selection pin
-Low enable.</td><td>MCU</td></tr>
<tr><td>D/CX
(SCL)</td><td>I</td><td>-Display data/command selection pin in MCU interface.
-D/CX='1': display data or parameter.
-D/CX='0': command data.
-In serial interface, this is used as SCL.
-If not used, please fix this pin at VDDI or DGND level.</td><td>MCU</td></tr>
<tr><td>RDX</td><td>I</td><td>-Read enable in 8080 MCU parallel interface.
-If not used, please fix this pin at VDDI or DGND level.</td><td>MCU</td></tr>
</table>

WRX (D/CX)	I	-Write enable in MCU parallel interface. -In 4-line SPI, this pin is used as D/CX (data/ command selection). -If not used, please fix this pin at VDDI or DGND level.	MCU
D[17:0]	I/O	-D[17:0] are used as MCU parallel interface data bus. -D0 is the serial input/output signal in serial interface mode. -In serial interface, D[17:1] are not used and should be fixed at VDDI or DGND level.	MCU
TE	O	-Tearing effect output pin to synchronies MCU to frame rate, activated by S/W command. -If not used, please open this pin.	MCU
OSC	O	-Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command. -When this pin is inactive (function OFF), this pin is DGND level. -If not used, please open this pin.	-

Note1. When in parallel mode, no use data pin must be connected to "1" or "0".

Note2. When CSX="1", there is no influence to the parallel and serial interface.

6.3 Mode selection pin

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect pin</th></tr>
<tr><td>EXTC</td><td>I</td><td>-During normal operation, please open this pin.
<table>
<tr><th>EXTC</th><th>Enable/disable modification of extend command</th></tr>
<tr><td>0</td><td>Normal operation mode</td></tr>
<tr><td>1</td><td>Use NVM command set</td></tr>
</table></td><td>Open</td></tr>
<tr><td>GM1,
GM0</td><td>I</td><td>-Panel resolution selection pins.
<table>
<tr><th>GM1</th><th>GM0</th><th>Selection of panel resolution</th></tr>
<tr><td>0</td><td>0</td><td>132RGB x 162 (S1~S396 & G1~G162 output)</td></tr>
<tr><td>1</td><td>1</td><td>128RGB x 160 (S7~S390 & G2~G161 output)</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>SRGB</td><td>I</td><td>-RGB direction select H/W pin for color filter setting.
<table>
<tr><th>SRGB</th><th>RGB arrangement</th></tr>
<tr><td>0</td><td>S1, S2, S3 filter order = ’R’, ’G’, ’B’</td></tr>
<tr><td>1</td><td>S1, S2, S3 filter order = ‘B’, ‘G’, ‘R’</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>SMX</td><td>I</td><td>-Module source output direction H/W selection pin.
<table>
<tr><th>SMX</th><th colspan="2">Scanning direction of source output</th></tr>
<tr><td></td><td>GM= ‘00’</td><td>GM= ‘11’</td></tr>
<tr><td>0</td><td>S1 -> S396</td><td>S7 -> S390</td></tr>
<tr><td>1</td><td>S396 -> S1</td><td>S390 -> S7</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>SMY</td><td>I</td><td>-Module Gate output direction H/W selection pin.
<table>
<tr><th>SMY</th><th colspan="2">Scanning direction of gate output</th></tr>
<tr><td></td><td>GM= ‘00’</td><td>GM= ‘11’</td></tr>
<tr><td>0</td><td>G1 -> G162</td><td>G2 -> G161</td></tr>
<tr><td>1</td><td>G162 -> G1</td><td>G161 -> G2</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>LCM</td><td>I</td><td>-Liquid crystal (LC) type selection pins.
<table>
<tr><th>LCM</th><th>Selection of LC type</th></tr>
<tr><td>0</td><td>Normally white LC type</td></tr>
<tr><td>1</td><td>Normally black LC type</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>GS</td><td>I</td><td>-Gamma curve selection pin.
<table>
<tr><th>GS</th><th>Selection of gamma curve</th></tr>
<tr><td>0</td><td>GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8</td></tr>
<tr><td>1</td><td>GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0</td></tr>
</table></td><td>VDDI/DGND</td></tr>
</table>

<table>
<tr><td>VPP</td><td>I</td><td>When writing NVM, it needs external power supply voltage (7.5V).</td><td></td></tr>
<tr><td>TESEL</td><td>I</td><td>Input pin to select horizontal line number in TE signal.
This pin is only for GM[1:0]='00' mode
<table>
<tr><th>TESEL</th><th>Selection of gamma curve</th></tr>
<tr><td>0</td><td>TE output 162 lines</td></tr>
<tr><td>1</td><td>TE output 160 lines</td></tr>
</table></td><td>VDDI/DGND</td></tr>
</table>

6.4 Driver output pins

Name	I/O	Description	Connect pin
S1 to S396	O	- Source driver output pins.	-
G1 to G162	O	- Gate driver output pins.	-
AVDD	O	Power pin for analog circuits. Connect a capacitor for stabilization.	Capacitor
AVCL	O	- A power supply pin for generating GVCL. - Connect a capacitor for stabilization.	Capacitor
VGH	O	- Power output pin for gate driver	
VGL	O	- Power output (Negative) pin for gate driver	
GVDD	O	- A power output of grayscale voltage generator. - When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.	
GVCL	O	- A power output(Negative) of grayscale voltage generator. - When internal GVCL generator is not used, connect an external power supply (AVCL+0.5V) to this pin.	-
VCOM	O	- A power supply for the TFT-LCD common electrode.	Common electrode
VCC	O	- Monitoring pin of internal digital reference voltage. - Please open these pins.	
VDDIO	O	- VDDI voltage output level for monitoring.	-
DGNDO	O	- DGND voltage output level for monitoring.	-

6.5 Test pins

Name	I/O	Description	Connect pin
TEST2P TEST1P	I	-These test pins for Driver vender test used. -Please connect these pins to DGND.	DGND
TESTOP[8] TESTOP[7] TESTOP[6] TESTOP[5] TESTOP[4] TESTOP[3] TESTOP[2] TESTOP[1]	O	-These test pins for Driver vender test used. -Please open these pins.	Open
Dummy	-	-These pins are dummy (have no function inside). -Can allow signal traces pass through these pads on TFT glass. -Please open these pins.	Open

7 Driver electrical characteristics

7.1 Absolute operation range

Item	Symbol	Rating	Unit
Supply voltage	VDD	- 0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +1.95	V
Driver supply voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic input voltage range	VIN	0.3 ~ VDDI + 0.3	V
Logic output voltage range	VO	0.3 ~ VDDI + 0.3	V
Operating temperature range	TOPR	-30 ~ +85	℃
Storage temperature range	TSTG	-40 ~ +125	℃

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC characteristic

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	Typ	Max		
Power & operation voltage							
System voltage	VDD	Operating voltage	2.3	2.75	4.8	V	
Interface operation voltage	VDDI	I/O supply voltage	1.65	1.8	3.7	V	
Gate driver high voltage	VGH		10		15	V	
Gate driver low voltage	VGL		-12.4		-7.5	V	
Gate driver supply voltage		| VGH-VGL |	17.5		27.5	V	
Input / Output							
Logic-high input voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-low input voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-high output voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-low output voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-high input current	IIH	VIN = VDDI			1	uA	Note 1
Logic-low input current	IIL	VIN = VSS	-1			uA	Note 1
Input leakage current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM voltage							
VCOM amplitude	VCOM		-2		-0.425	V	
Source driver							
Source output range	Vsout		0.1		GVDD	V	
Gamma reference voltage	GVDD		3.0		5.0	V	
Source output settling time	Tr	Below with 99% precision			20	us	Note 2
Output offset voltage	Voffset				35	mV	Note 3

Notes:

1. TA= -30 to 85℃.

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The Max. value is between measured point of source output and gamma setting value.

7.3 Power consumption

Ta=25℃, Frame rate = 60Hz, the registers setting are IC default setting.

Operation mode	Image	Current consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal mode	Note 1	TBD	TBD	TBD	TBD
	Note 2	TBD	TBD	TBD	TBD
Partial + Idle mode (40 lines)	Note 1	TBD	TBD	TBD	TBD
	Note 2	TBD	TBD	TBD	TBD
Sleep-in mode	N/A	TBD	TBD	TBD	TBD

Notes:

1. All pixels black.

2. All pixels white.

3. The Current Consumption is DC characteristics of ST7735R.

4. Typical: VDDI=1.8V, VDD=2.75V; Maximum: VDDI=1.65 to 3.7V, VDD=2.3 to 4.8V

8 Timing chart

8.1 Parallel interface characteristics: 18, 16, 9 or 8-bit bus (8080 series MCU interface)

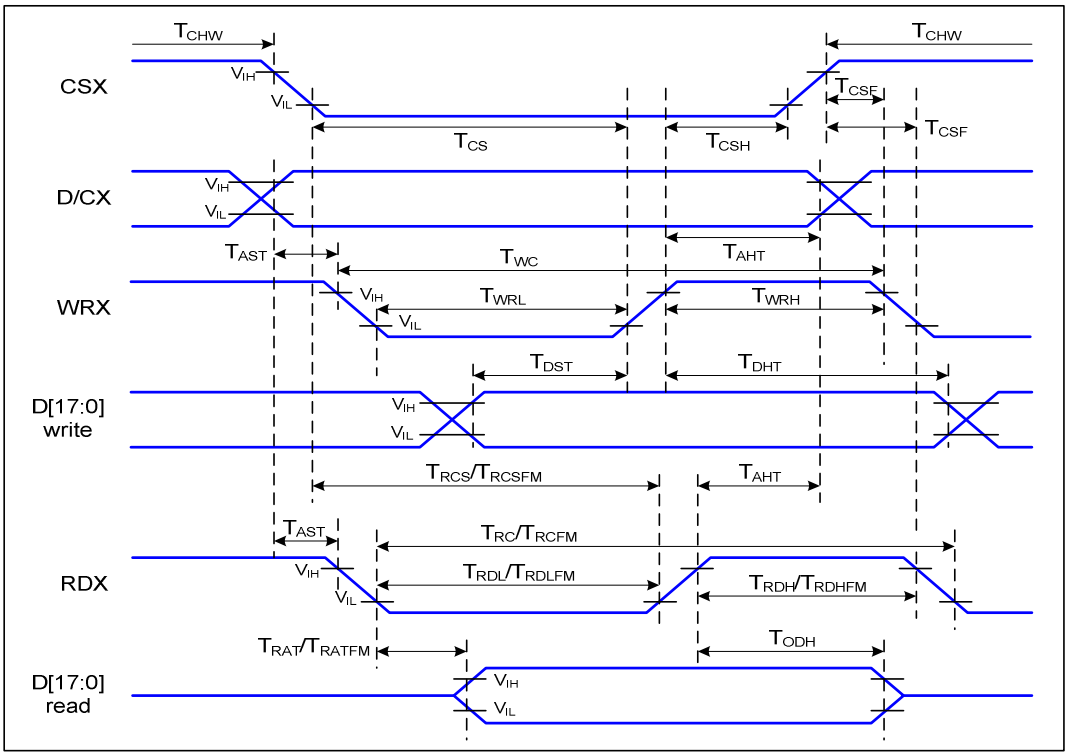


Figure 8.1.1 Parallel interface timing characteristics (8080 series MCU interface)

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.3~4.8V

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	TAST	Address setup time	10		ns	-
	TAHT	Address hold time (Write/Read)	10		ns	
CSX	TCHW	Chip select “H” pulse width	0		ns	-
	TCS	Chip select setup time (Write)	15		ns	
	TRCS	Chip select setup time (Read ID)	45		ns	
	TRCSFM	Chip select setup time (Read FM)	355		ns	
	TCSF	Chip select wait time (Write/Read)	10		ns	
	TCSH	Chip select hold time	10		ns	
WRX	TWC	Write cycle	66		ns	
	TWRH	Control pulse “H” duration	15		ns	
	TWRL	Control pulse “L” duration	15		ns	
RDX (ID)	TRC	Read cycle (ID)	160		ns	When read ID data
	TRDH	Control pulse “H” duration (ID)	90		ns	
	TRDL	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	TRCFM	Read cycle (FM)	450		ns	When read from frame memory
	TRDHFM	Control pulse “H” duration (FM)	90		ns	
	TRDLFM	Control pulse “L” duration (FM)	355		ns	
D[17:0]	TDST	Data setup time	10		ns	For CL=30pF
	TDHT	Data hold time	10		ns	
	TRAT	Read access time (ID)		40	ns	
	TRATFM	Read access time (FM)		340	ns	
	TODH	Output disable time	20	80	ns	

Table 8.1.1 8080 parallel Interface Characteristics

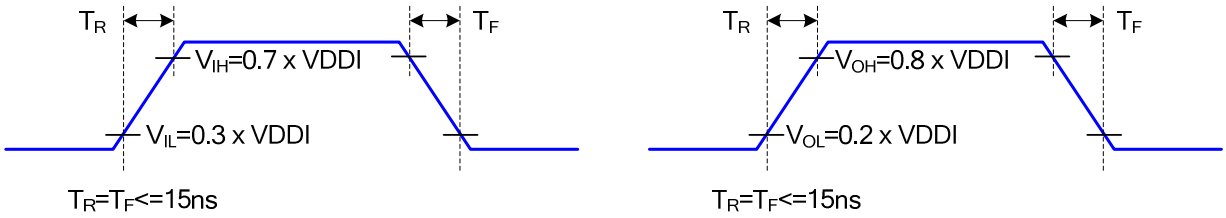


Figure 8.1.2 Rising and falling timing for input and output signal

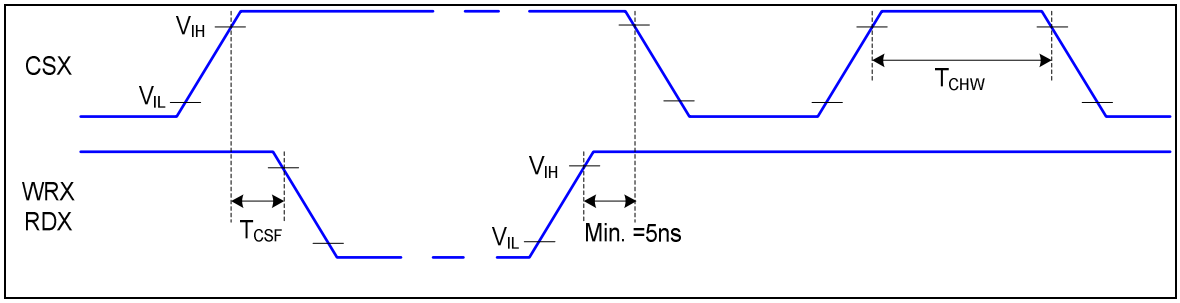


Figure 8.1.3 Chip selection (CSX) timing

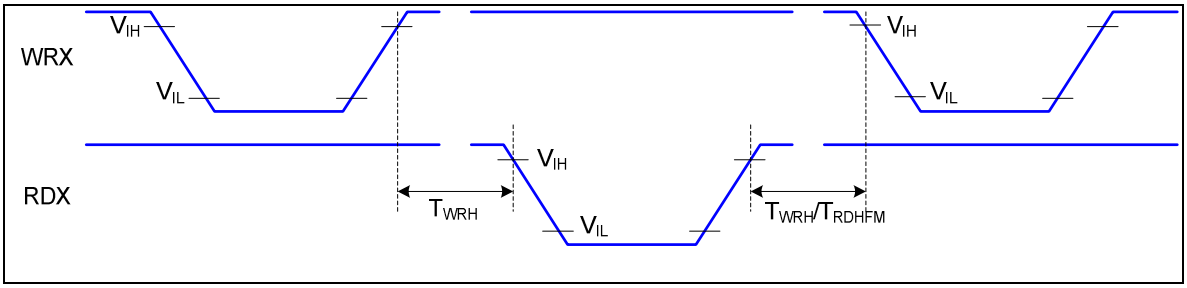


Figure 8.1.4 Write-to-read and read-to-write timing

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.2 Parallel interface characteristics: 18, 16, 9 or 8-bit bus (6800 series MCU interface)

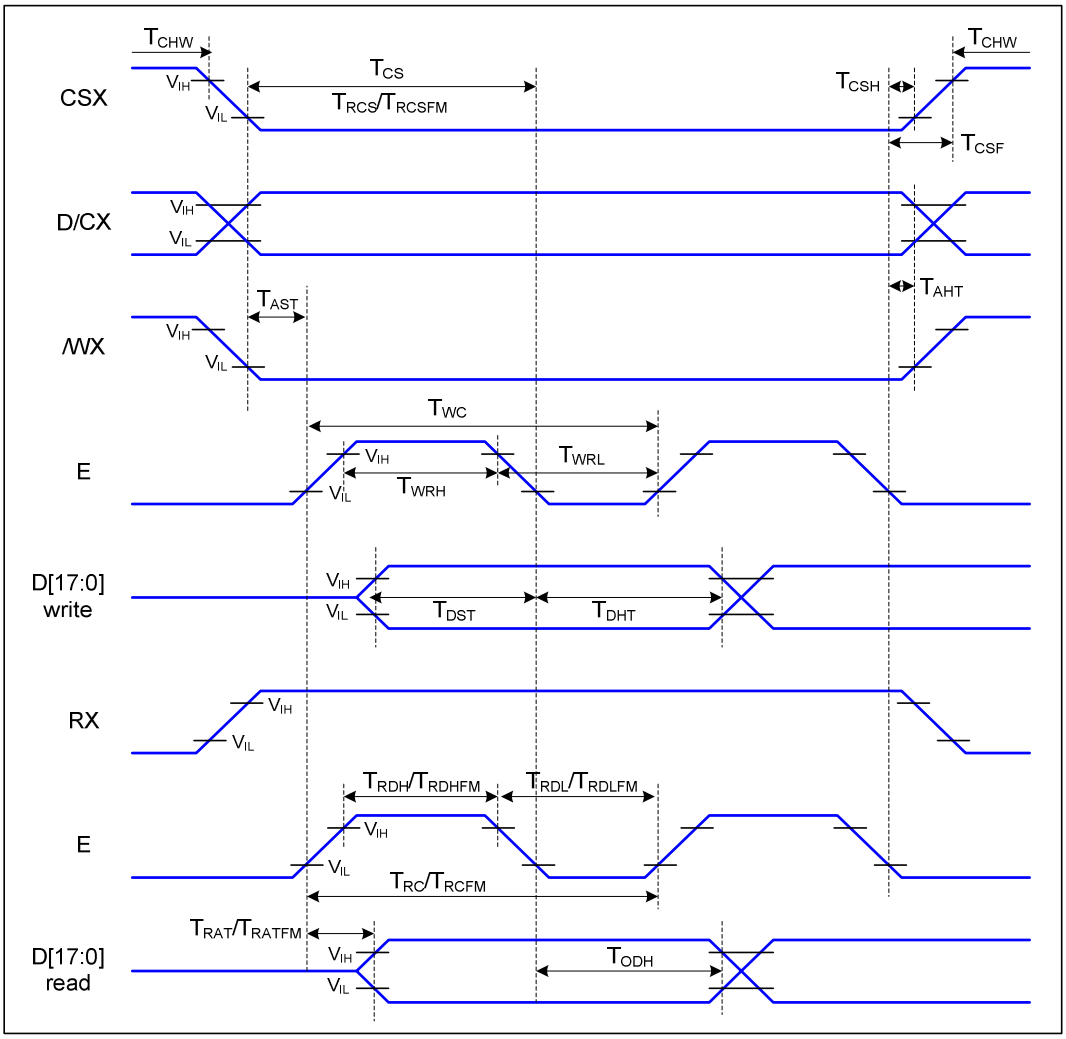


Figure 8.2.1Parallel interface timing characteristics (6800-series MCU interface)

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.3~4.8V

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	
	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 8.2.1 6800 parallel Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.3 Serial interface characteristics (3-line serial)

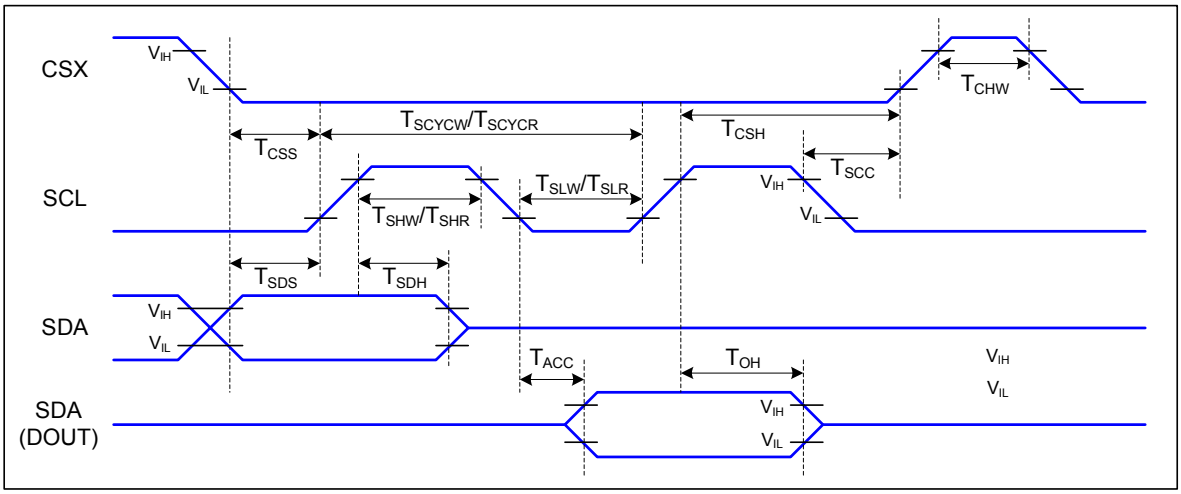


Figure 8.3.1 3-line serial interface timing

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.3~4.8V

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	TCSS	Chip select setup time (write)	15		ns	
	TCSH	Chip select hold time (write)	15		ns	
	TCSS	Chip select setup time (read)	60		ns	
	TSCC	Chip select hold time (read)	65		ns	
	TCHW	Chip select “H” pulse width	40		ns	
SCL	TSCYCW	Serial clock cycle (Write)	66		ns	
	TSHW	SCL “H” pulse width (Write)	15		ns	
	TSLW	SCL “L” pulse width (Write)	15		ns	
	TSCYCR	Serial clock cycle (Read)	150		ns	
	TSHR	SCL “H” pulse width (Read)	60		ns	
	TSLR	SCL “L” pulse width (Read)	60		ns	
SDA (DIN) (DOUT)	TSDS	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	TSDH	Data hold time	10		ns	
	TACC	Access time	10	50	ns	
	TOH	Output disable time	15	50	ns	

Table 8.3.1 3-line Serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.4 Serial interface characteristics (4-line serial)

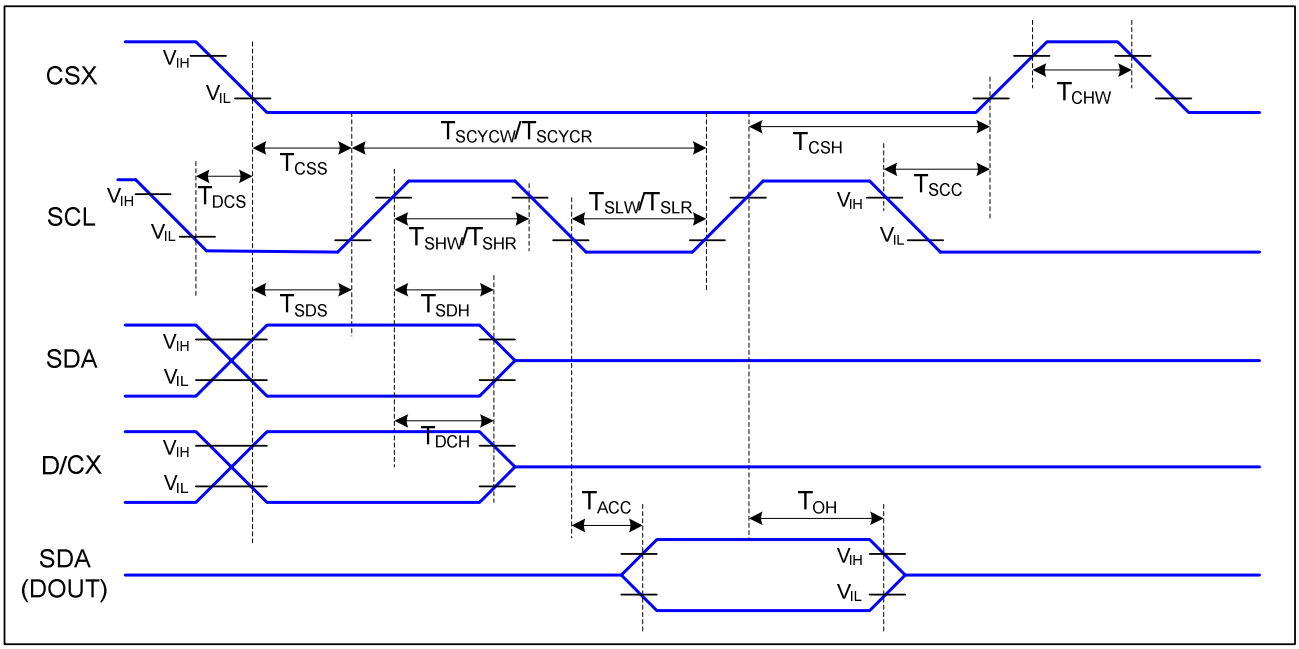


Figure 8.4.1 4-line serial interface timing

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.3~4.8V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time (write)	45		ns	
	TCSH	Chip select hold time (write)	45		ns	
	TCSS	Chip select setup time (read)	60		ns	
	TSCC	Chip select hold time (read)	65		ns	
	TCHW	Chip select “H” pulse width	40		ns	
SCL	TSCYCW	Serial clock cycle (Write)	66		ns	-write command & data ram
	TSHW	SCL “H” pulse width (Write)	15		ns	
	TSLW	SCL “L” pulse width (Write)	15		ns	
	TSCYCR	Serial clock cycle (Read)	150		ns	-read command & data ram
	TSHR	SCL “H” pulse width (Read)	60		ns	
	TSLR	SCL “L” pulse width (Read)	60		ns	
D/CX	TDCS	D/CX setup time	10		ns	
	TDCH	D/CX hold time	10		ns	
SDA (DIN) (DOUT)	TSDS	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	TSDH	Data hold time	10		ns	
	TACC	Access time	10	50	ns	
	TOH	Output disable time	15	50	ns	

Table 8.4.1 4-line Serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

9 Function description

9.1 Interface type selection

The selection of given interfaces are done by setting IM2, IM1, and IM0 pins as shown in following table.

P68	IM2	IM1	IM0	Interface	Read back selection
-	0	-	-	3-line serial interface	Via the read instruction
0	1	0	0	8080 MCU 8-bit parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	1	0	1	8080 MCU 16-bit parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	1	1	0	8080 MCU 9-bit parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	1	1	1	8080 MCU 18-bit parallel	RDX strobe (18-bit read data and 8-bit read parameter)
-	0	-	-	3-line serial interface	Via the read instruction
1	1	0	0	6800 MCU 8-bit parallel	E strobe (8-bit read data and 8-bit read parameter)
1	1	0	1	6800 MCU 16-bit parallel	E strobe (16-bit read data and 8-bit read parameter)
1	1	1	0	6800 MCU 9-bit parallel	E strobe (9-bit read data and 8-bit read parameter)
1	1	1	1	6800 MCU 18-bit parallel	E strobe (18-bit read data and 8-bit read parameter)

Table 9.1.1 Selection of MCU interface

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	-	-	3-line serial interface	Note1	Note1	SCL	D[17:1]: unused, D0: SDA
0	1	0	0	8080 8-bit parallel	RDX	WRX	D/CX	D[17:8]: unused, D7-D0: 8-bit data
0	1	0	1	8080 16-bit parallel	RDX	WRX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
0	1	1	0	8080 9-bit parallel	RDX	WRX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
0	1	1	1	8080 18-bit parallel	RDX	WRX	D/CX	D17-D0: 18-bit data
-	0	-	-	3-line serial interface	Note1	D/CX	SCL	D[17:1]: unused, D0: SDA
1	1	0	0	6800 8-bit parallel	E	WRX	RS	D[17:8]: unused, D7-D0: 8-bit data
1	1	0	1	6800 16-bit parallel	E	WRX	RS	D[17:16]: unused, D15-D0: 16-bit data
1	1	1	0	6800 9-bit parallel	E	WRX	RS	D[17:9]: unused, D8-D0: 9-bit data
1	1	1	1	6800 18-bit parallel	E	WRX	RS	D17-D0: 18-bit data

Table 9.1.2 Pin connection according to various MCU interface

Note: Unused pins can be open, or connected to DGND or VDDI.

9.2 8080-series MCU parallel interface (P68 = '0')

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command. The interface functions of 8080-series parallel interface are given in following table.

IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
1	0	0	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
				1	↑	1	Read 8-bit display data (D7 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)
1	0	1	16-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 16-bit display data or 8-bit parameter (D15 to D0)
				1	↑	1	Read 16-bit display data (D15 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)
1	1	0	9-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
				1	↑	1	Read 9-bit display data (D8 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)
1	1	1	18-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 18-bit display data or 8-bit parameter (D17 to D0)
				1	↑	1	Read 18-bit display data (D17 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)

Table 9.2.1 the function of 8080-series parallel interface

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

9.2.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

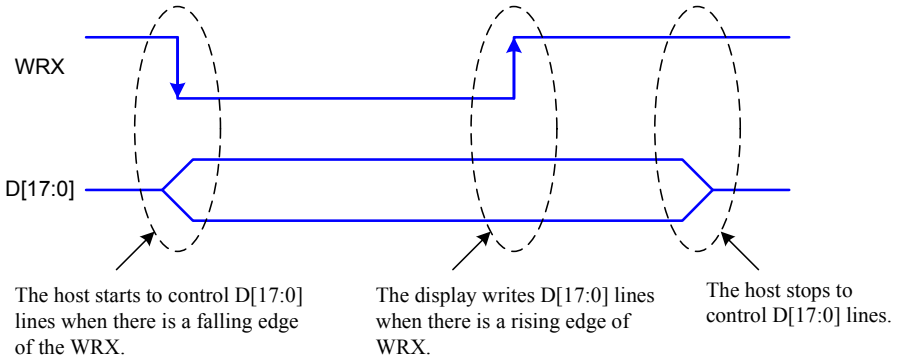


Figure 9.2.1 8080-series WRX protocol

Note: WRX is an unsynchronized signal (It can be stopped).

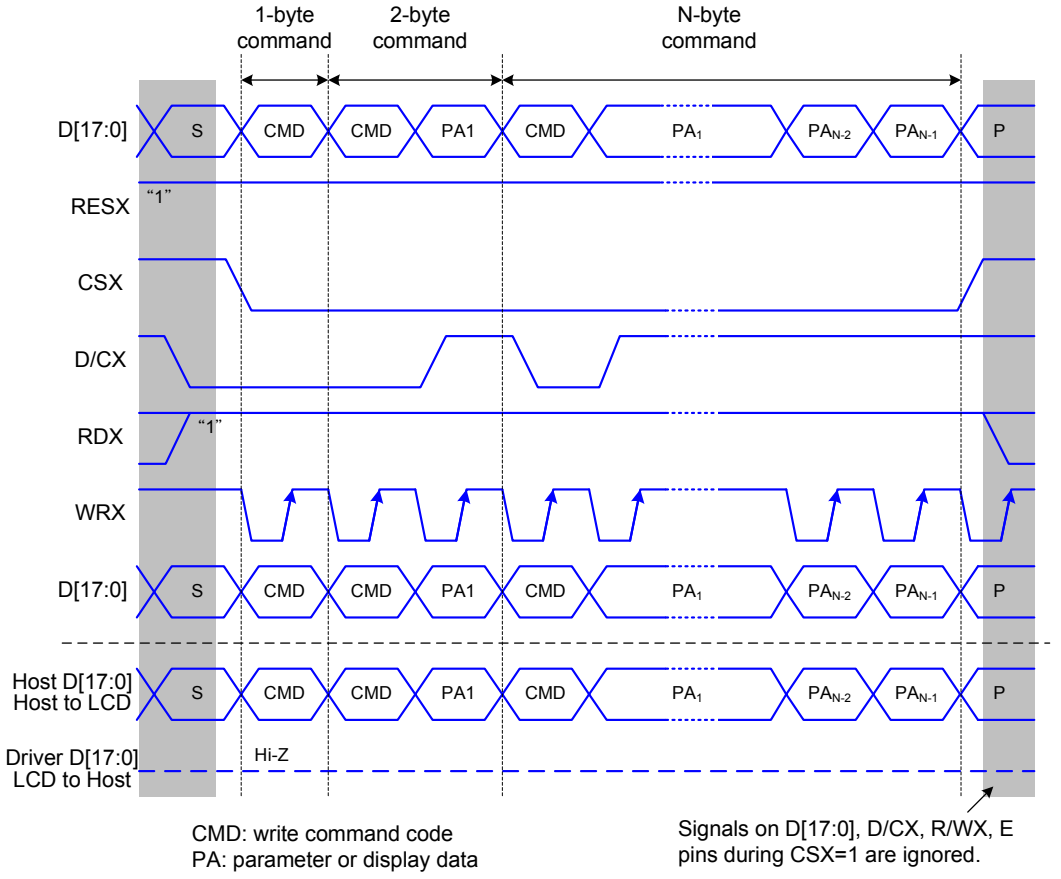


Figure 9.2.2 8080-series parallel bus protocol, write to register or display RAM

9.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

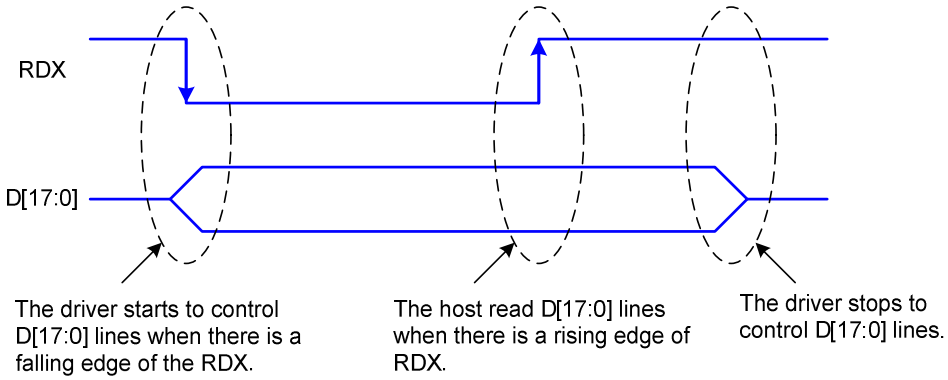


Figure 9.2.3 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

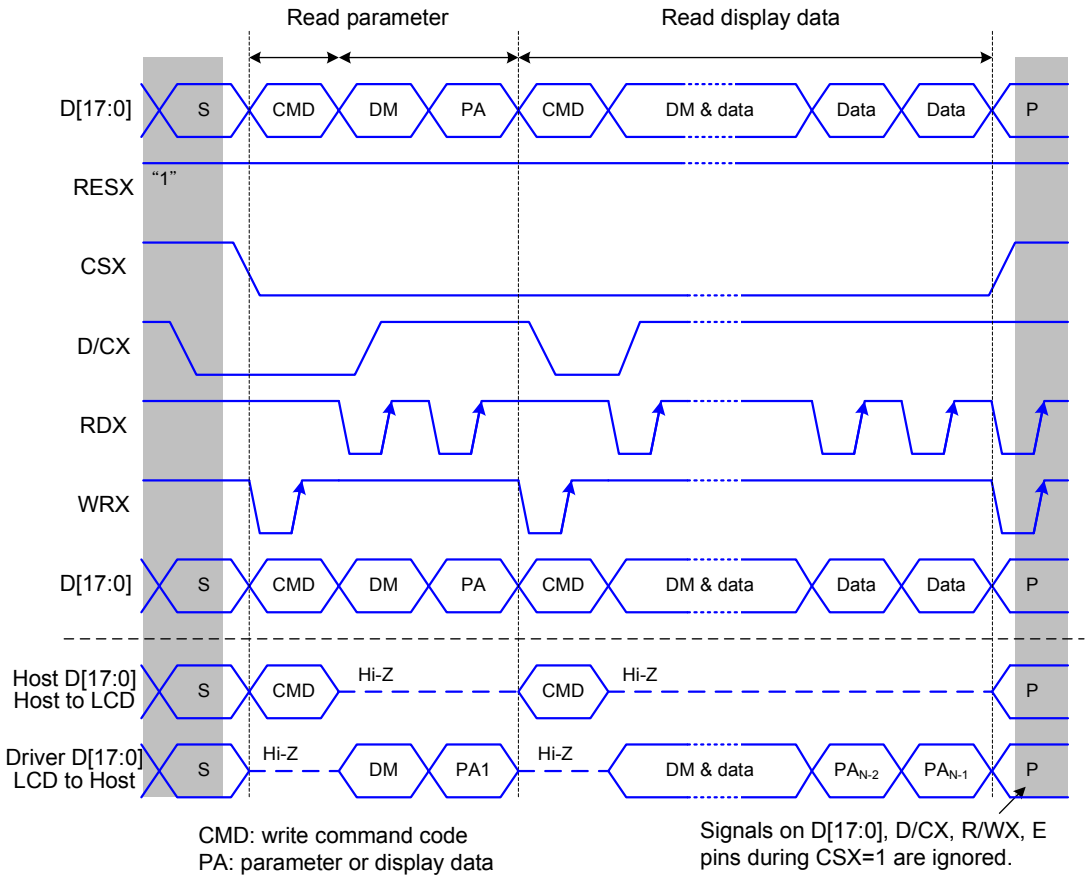


Figure 9.2.4 8080-series parallel bus protocol, read data from register or display RAM

9.3 6800-series MCU parallel interface (P68 = '1')

The MCU uses one of following interface: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-lines with 16-data parallel interface, or 21-lines with 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data bus.

The LCD driver reads the data at the falling edge of E signal when R/WX= '1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C= '0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0.The interface functions of 6800-series parallel interface are given in Table 8.1.1.

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	1	↓	Read 8-bit Display data (D7 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	0	1	16-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	1	↓	Read 16-bit Display data (D15 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	0	9-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	1	↓	Read 9-bit Display data (D8 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	1	18-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	1	↓	Read 18-bit Display data (D17 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)

Table 9.3.1 The function of 6800-series parallel interface

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

9.3.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control signals (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

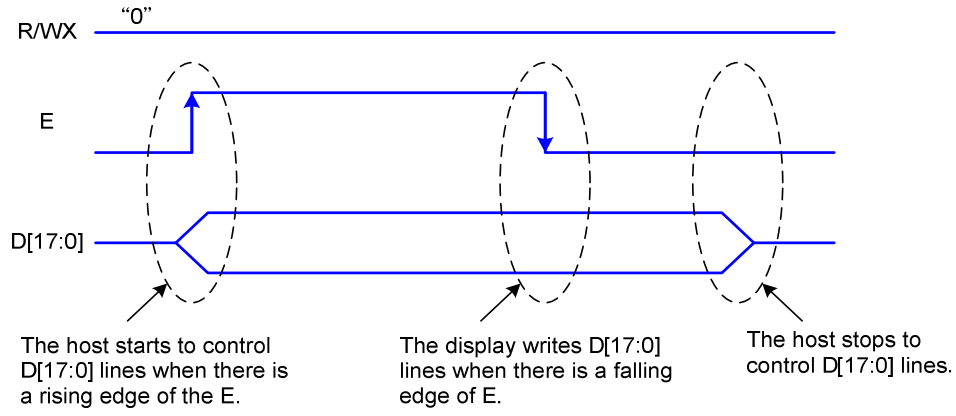


Figure 9.3.1 6800-Series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

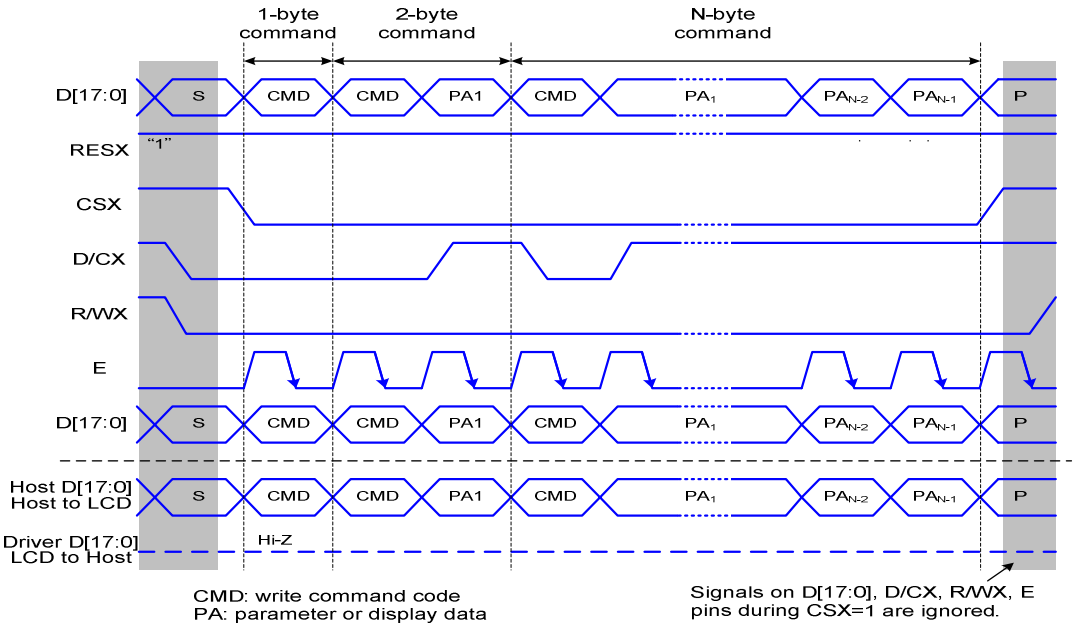


Figure 9.3.2 6800-series parallel bus protocol, write to register or display RAM

9.3.2 9.3.2 Read cycle sequence

The read cycle (E low-high-low sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a rising edge of E and the host reads data when there is a falling edge of E.

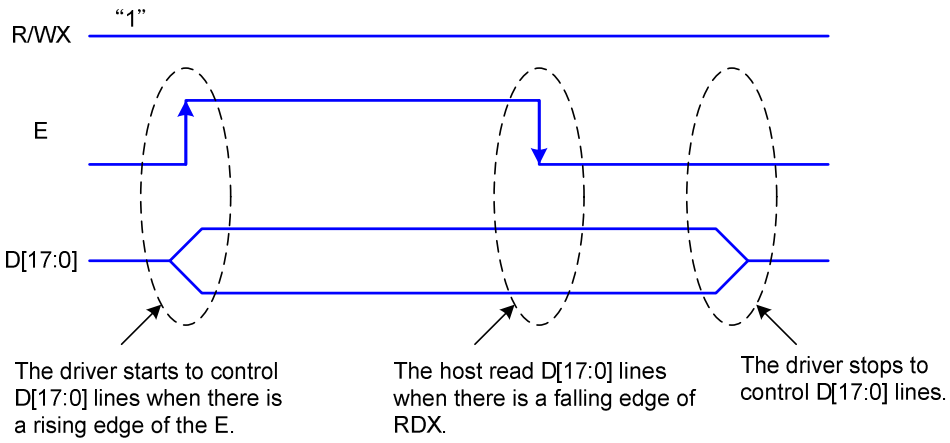


Figure 9.3.3 6800-series read protocol

Note: E is an unsynchronized signal (It can be stopped)

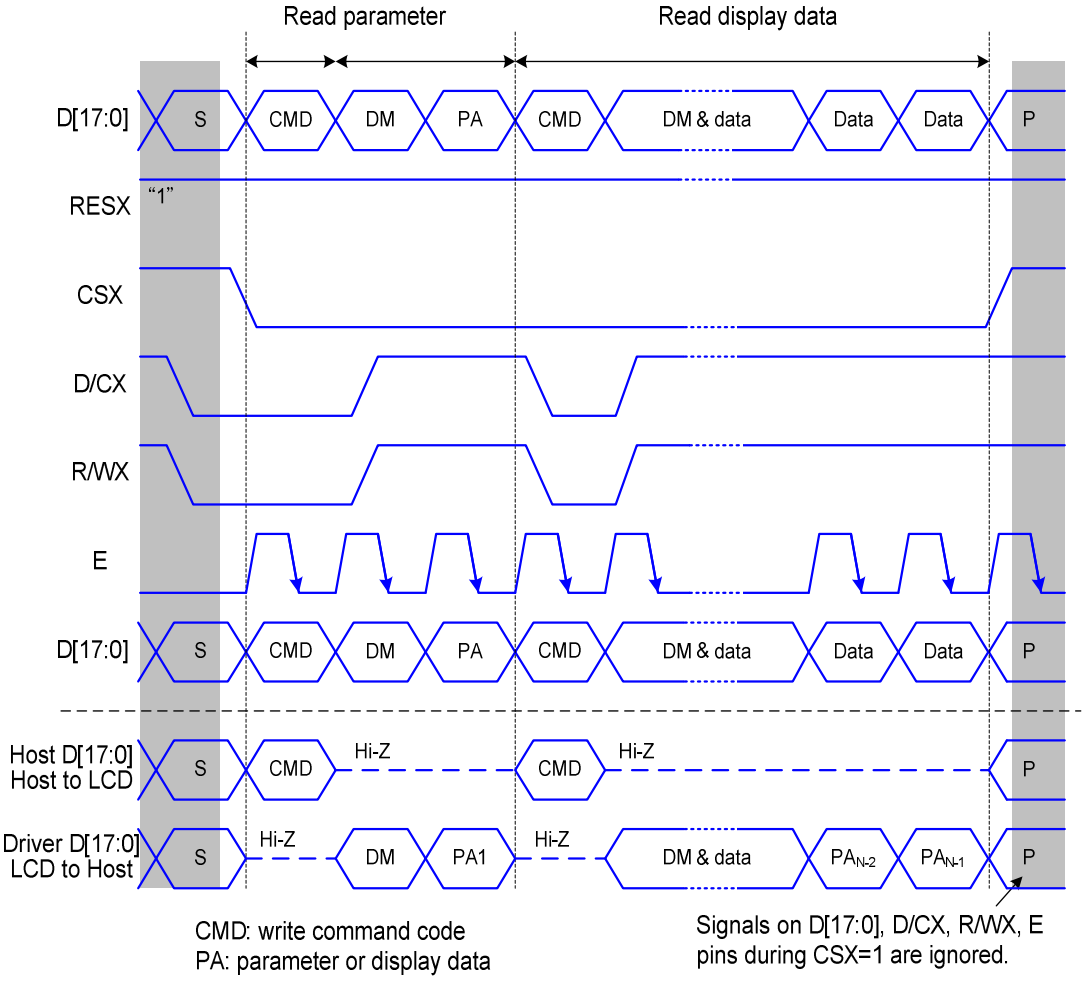


Figure 9.3.4 6800-series parallel bus protocol, read data form register or display RAM

9.4 Serial interface

The selection of this interface is done by IM2. See the Table 9.4.1.

IM2	4WSPI	Interface	Read back selection
0	0	3-line serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	1	4-line serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)

Table 9.4.2 Selection of serial interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bts bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

9.4.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

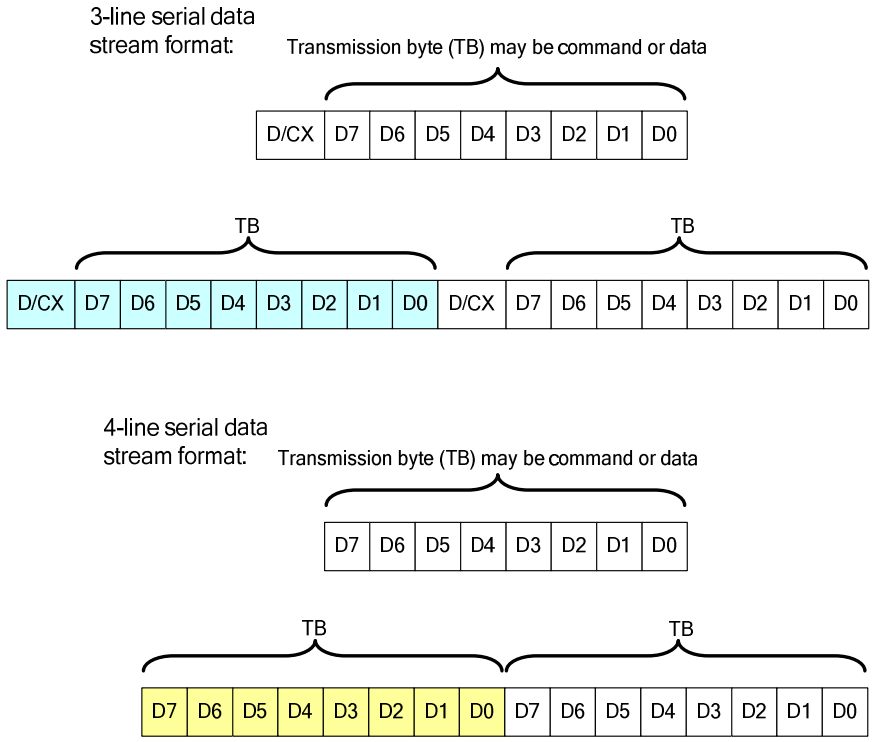


Figure 9.4.1 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Figure 9.4.2). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-lines serial interface) or 8th rising edge of SCL (4-lines serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-lines serial interface) or D7 (4-lines serial interface) of the next byte at the next rising edge of SCL..

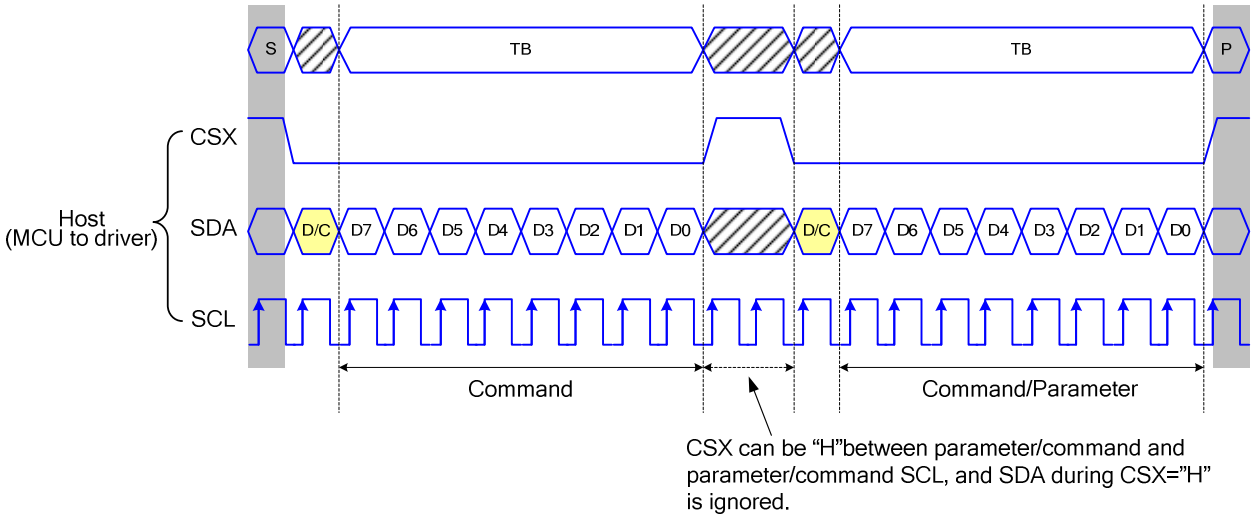


Figure 9.4.3 3-line serial interface write protocol (write to register with control bit in transmission)

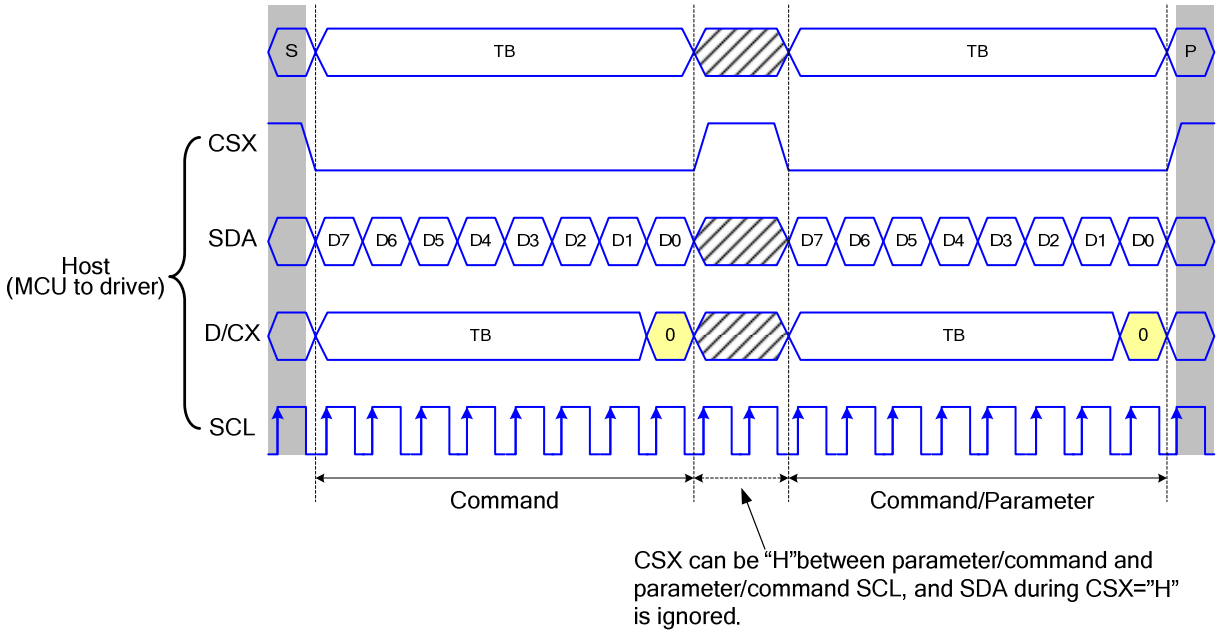


Figure 9.4.4 4-line serial interface write protocol (write to register with control bit in transmission)

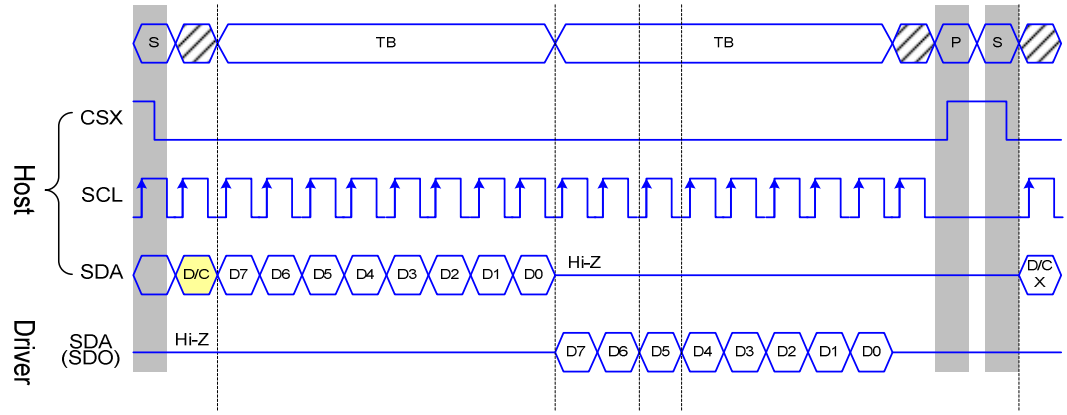
9.4.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

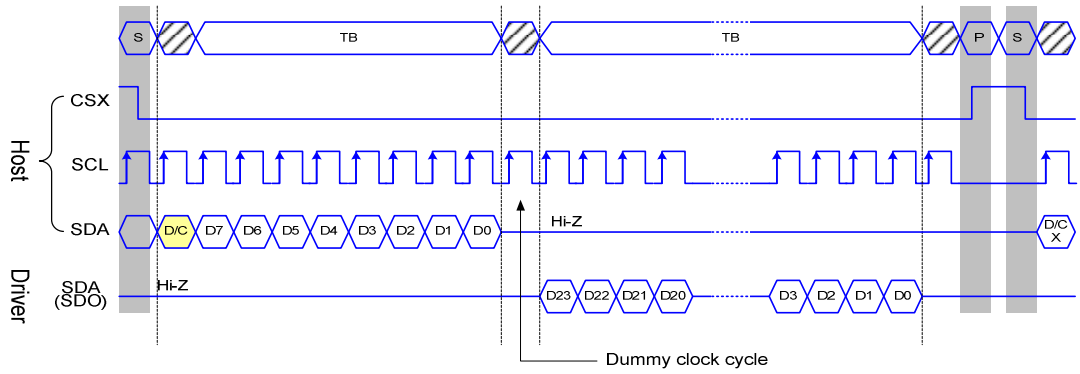
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

9.4.3 3-line serial protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

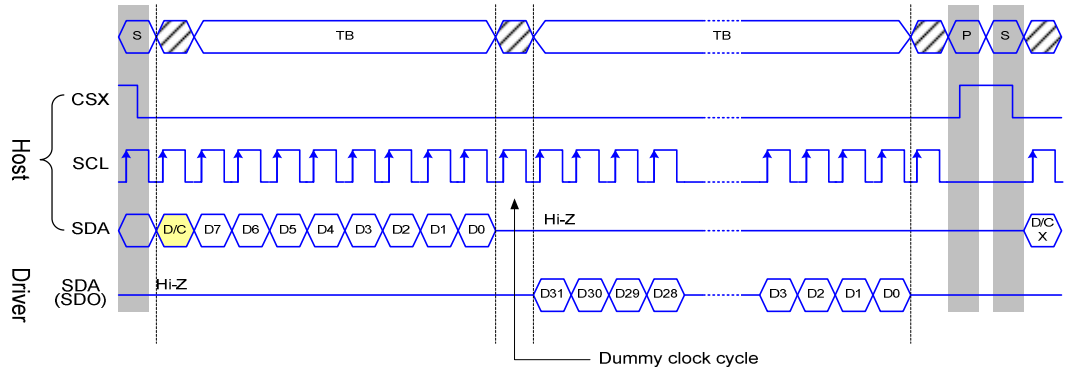
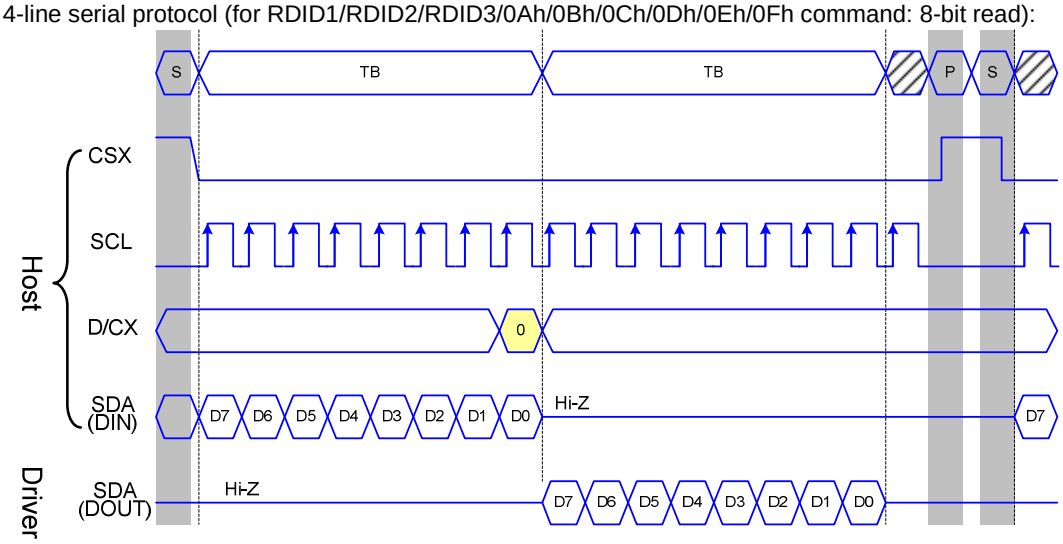


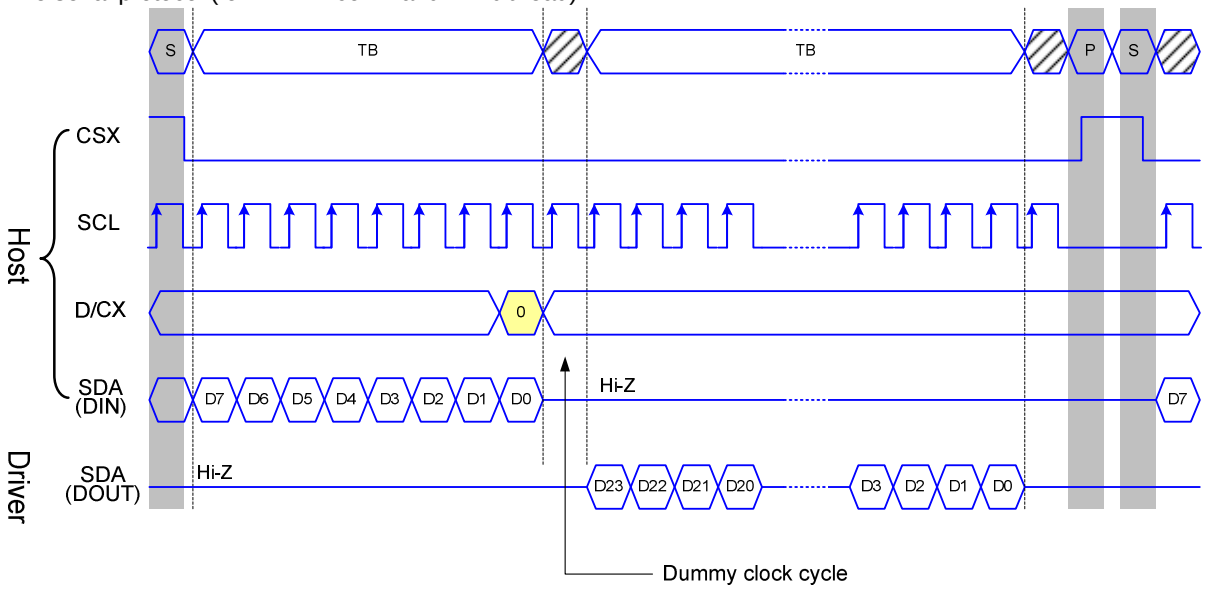
Figure 9.4.5 3-line serial interface read protocol

9.4.4 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

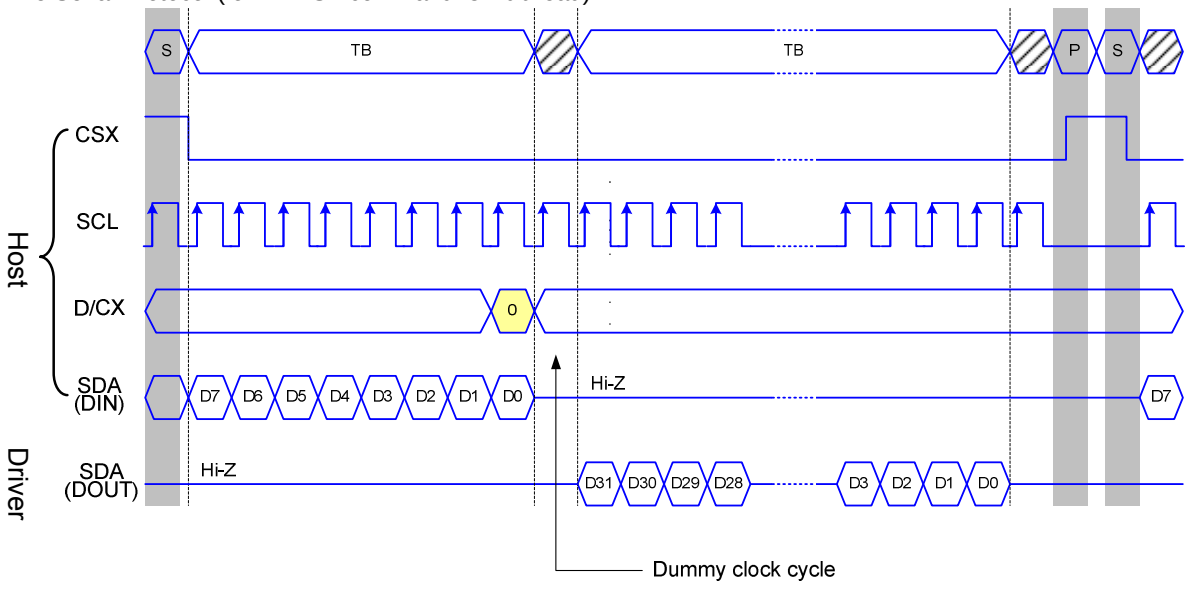


Figure 9.4.6 4-line serial interface read protocol

9.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example

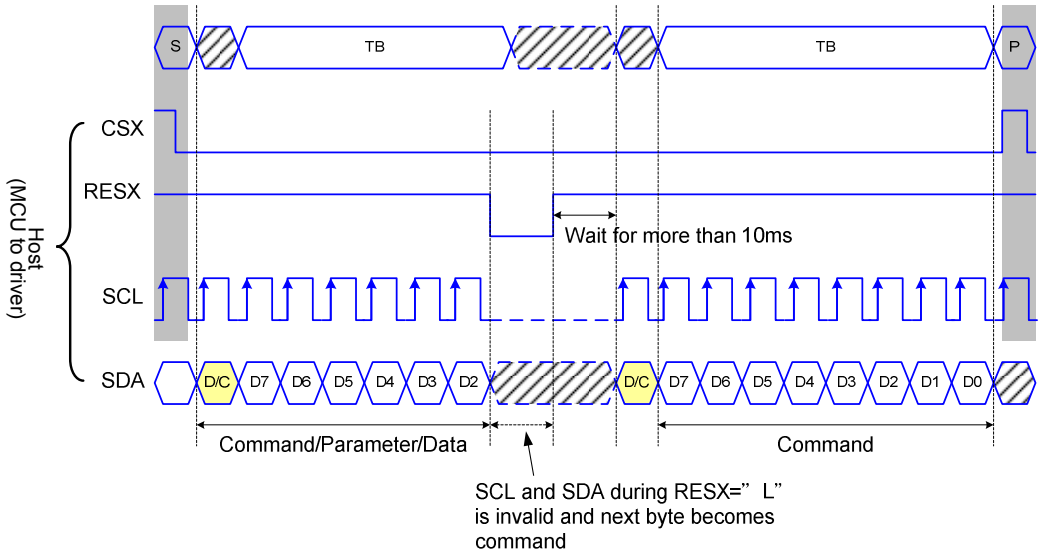


Figure 9.5.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

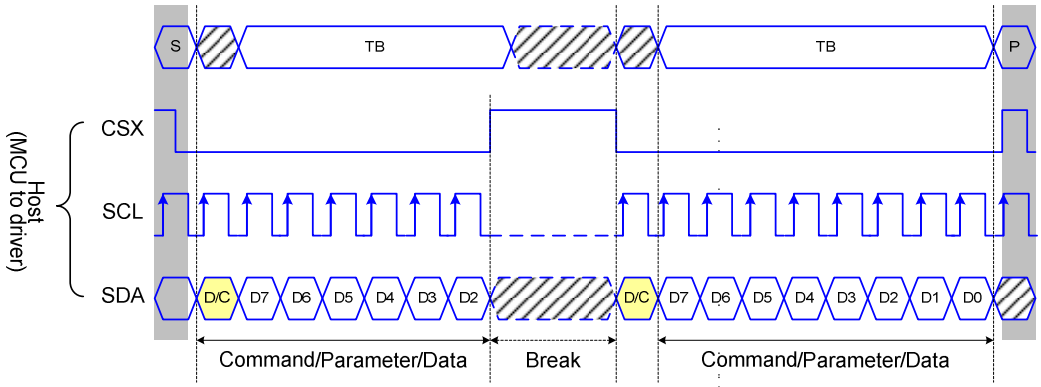


Figure 9.5.2 Serial bus protocol, write mode – interrupted by CSX

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

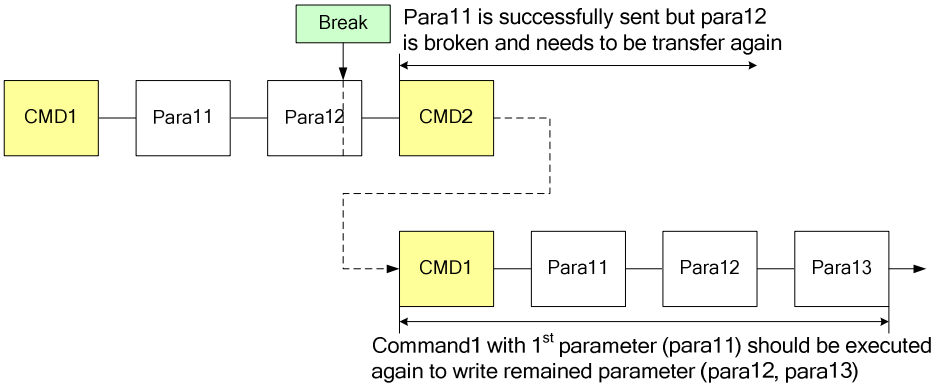


Figure 9.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

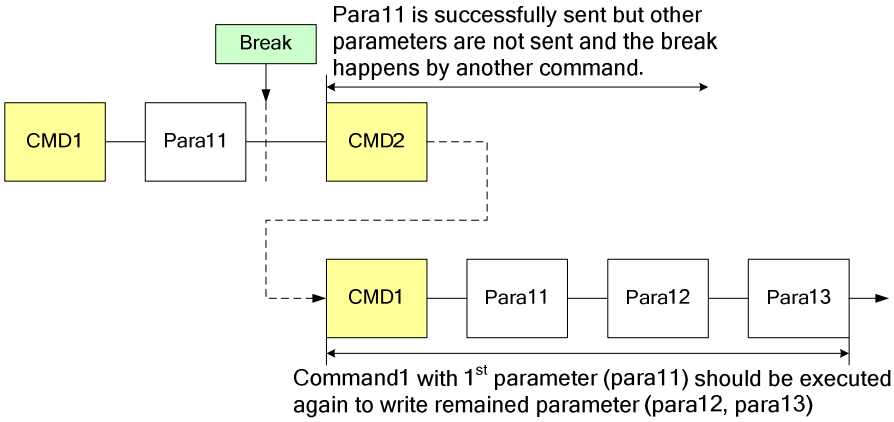


Figure 9.5.4 Write interrupts recovery (both serial and parallel Interface)

9.6 Data transfer pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command‘s parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

9.6.1 Serial interface pause

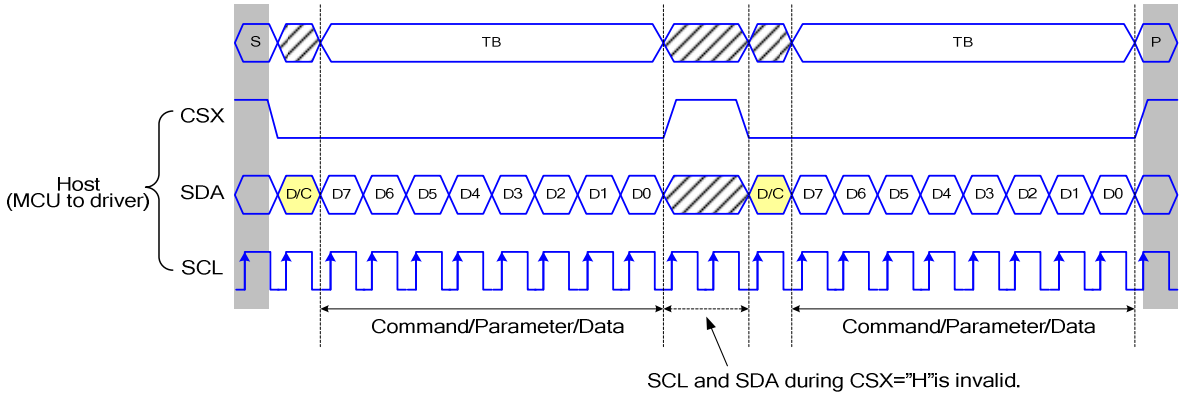


Figure 9.6.1 Serial interface pause protocol (pause by CSX)

9.6.2 Parallel interface pause

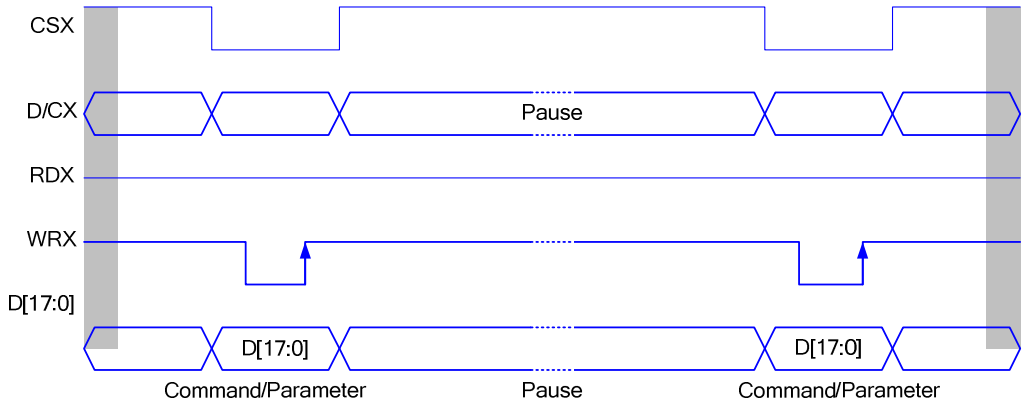


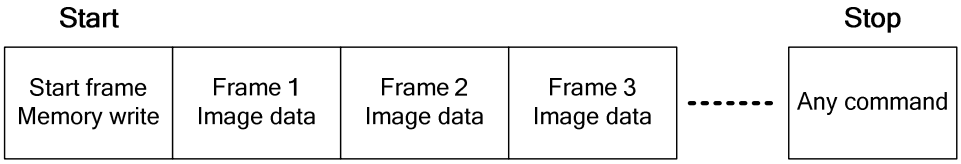
Figure 9.6.2 Parallel bus pause protocol (paused by CSX)

9.7 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

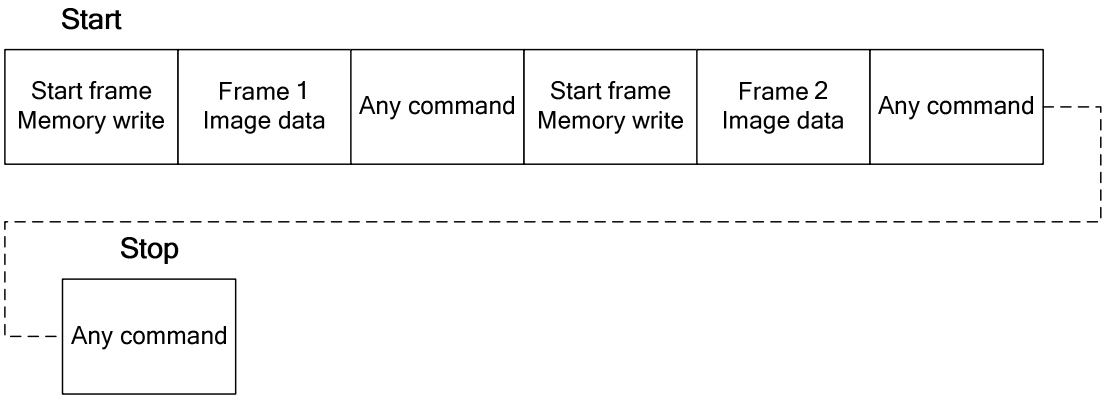
9.7.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



9.7.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

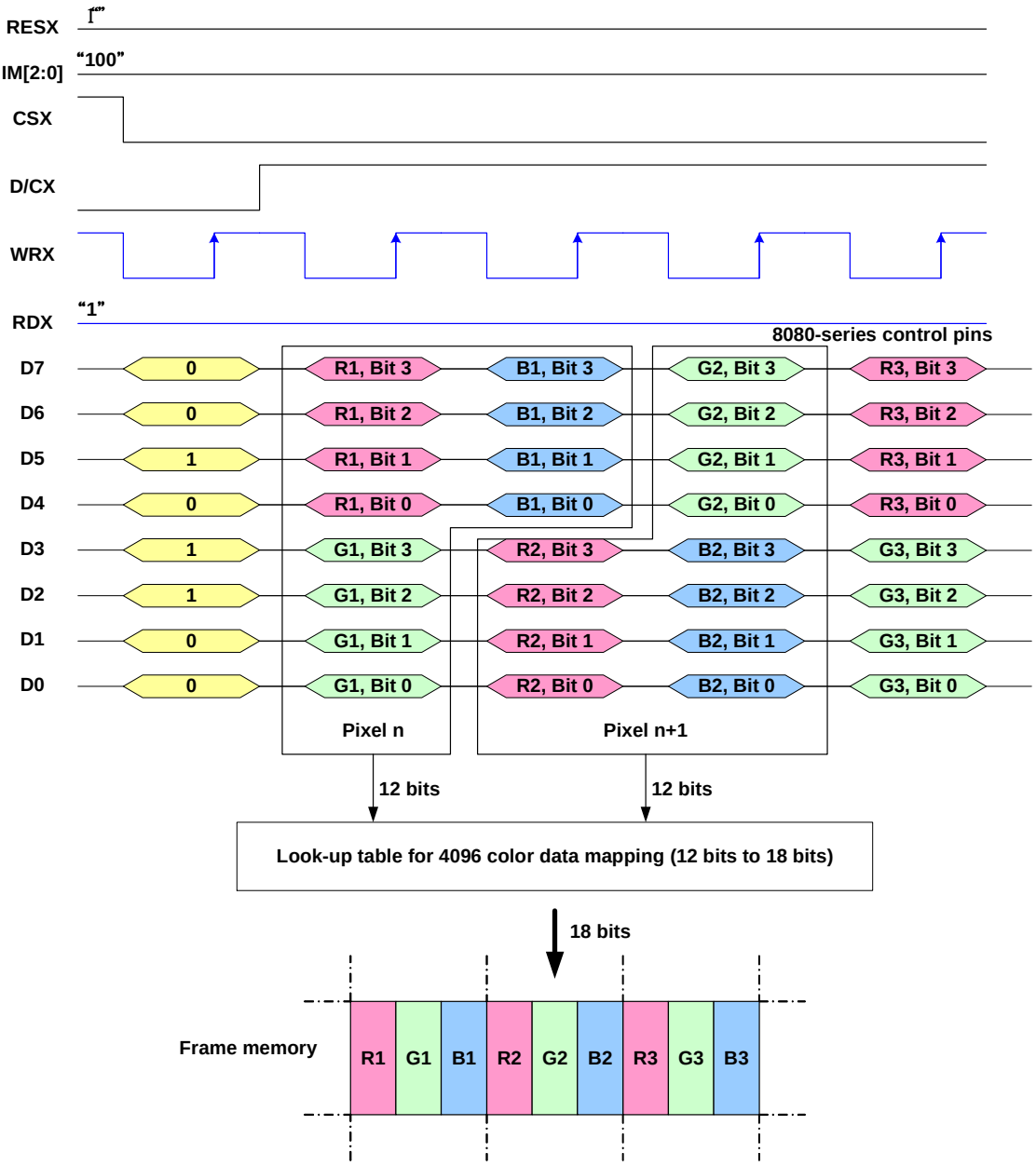
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

9.8 Data Color Coding

9.8.1 8-bit Parallel Interface (IM2, IM1, IM0= “100”)

Different display data formats are available for three Colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

9.8.2 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= “03h”



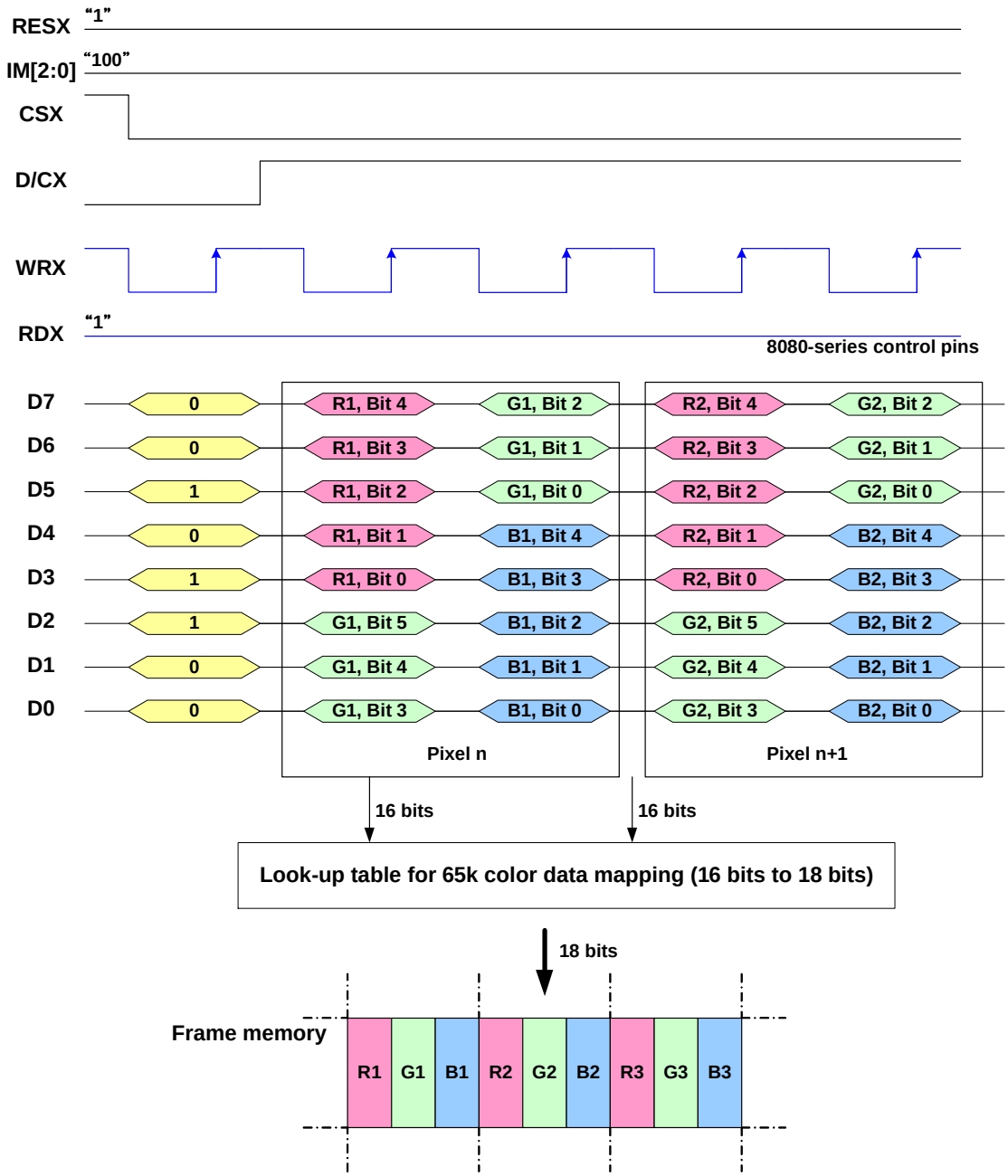
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

9.8.3 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= “05h”

There is 1 pixel (3 sub-pixels) per 2-byte



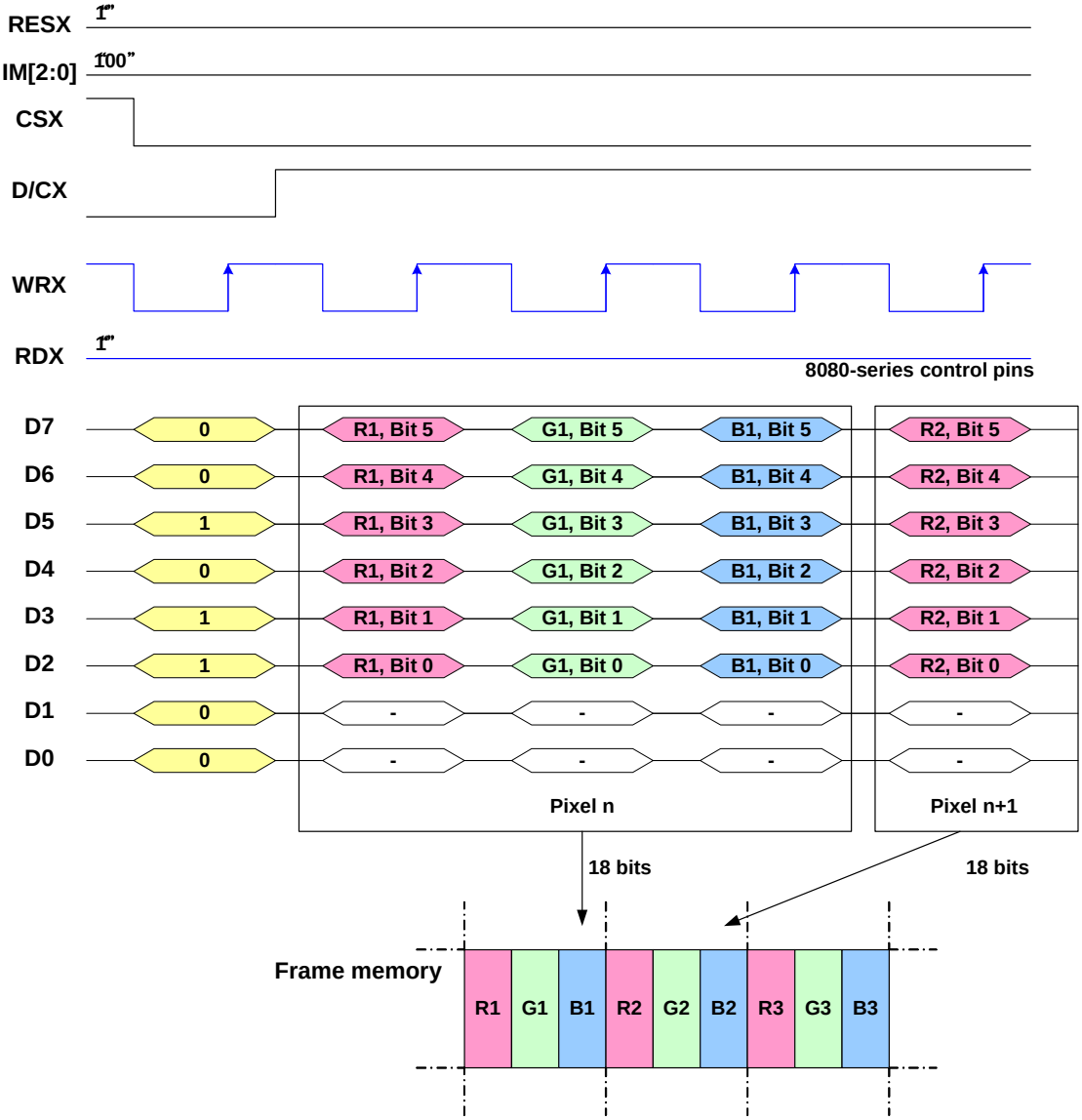
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.4 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= “06h”

There is 1 pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

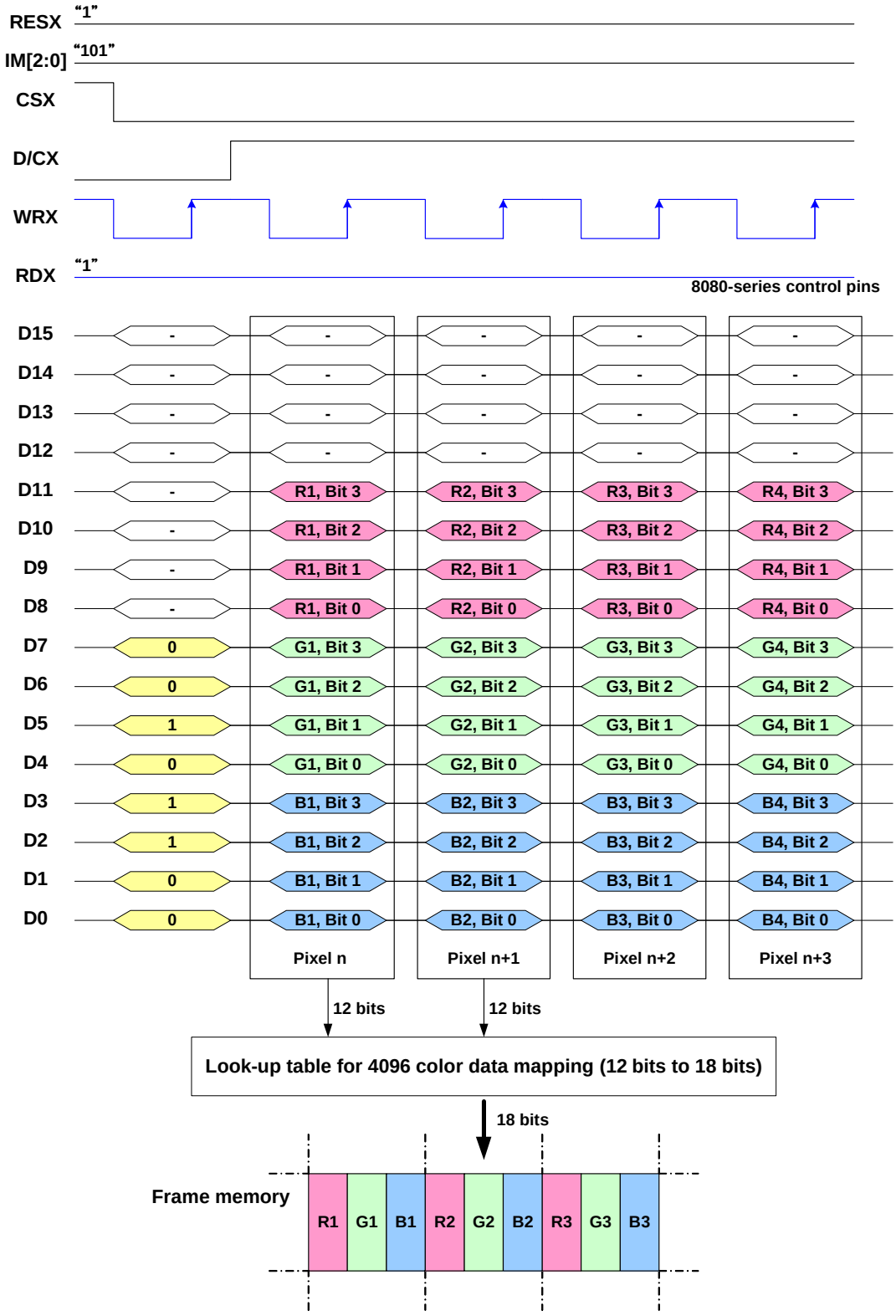
Note 3: ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.5 16-Bit Parallel Interface (IM2,IM1, IM0= “101”)

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

9.8.6 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= “03h”

There is 1 pixel (3 sub-pixels) per 1 byte

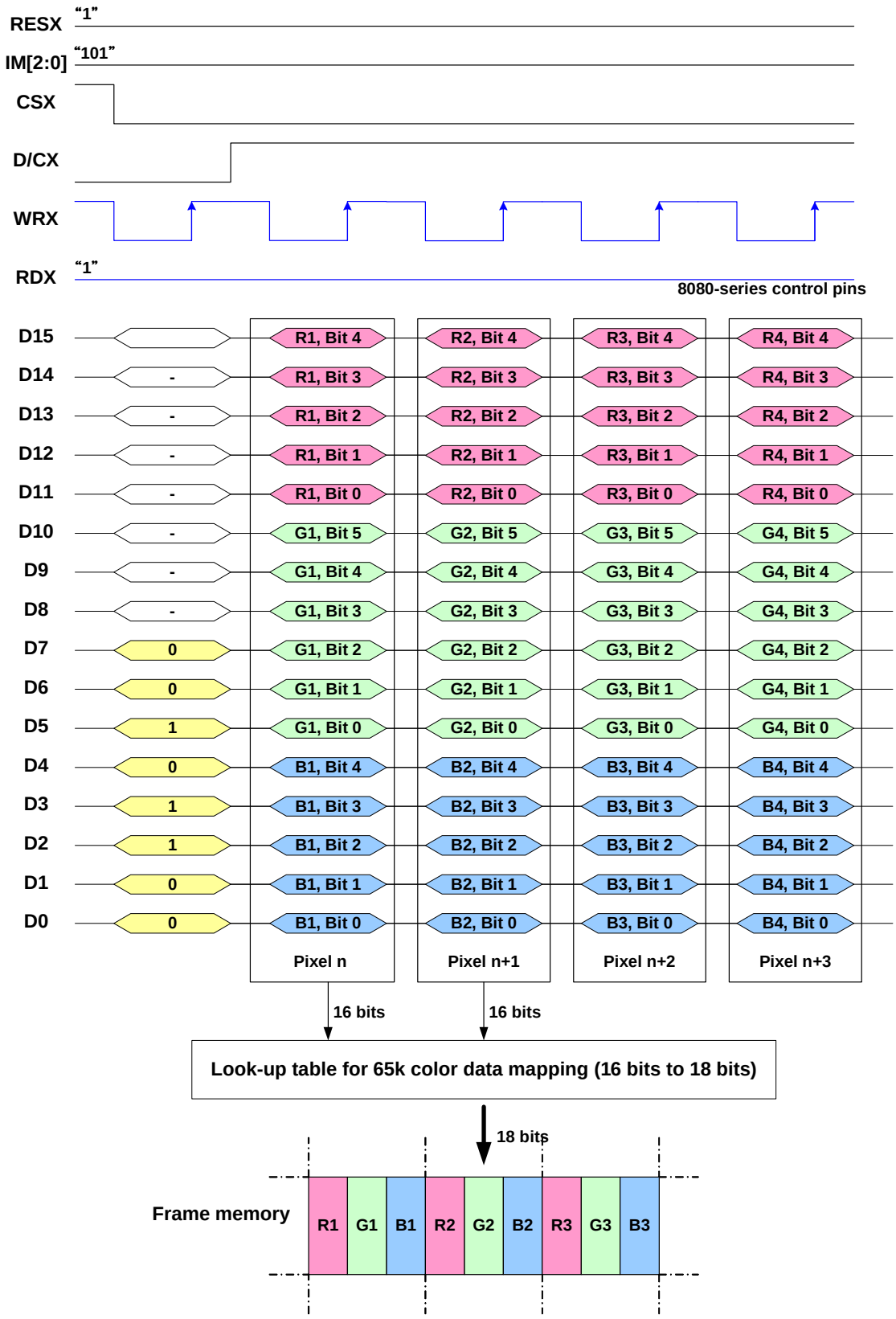


Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.7 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= “05h”

There is 1 pixel (3 sub-pixels) per 1 byte



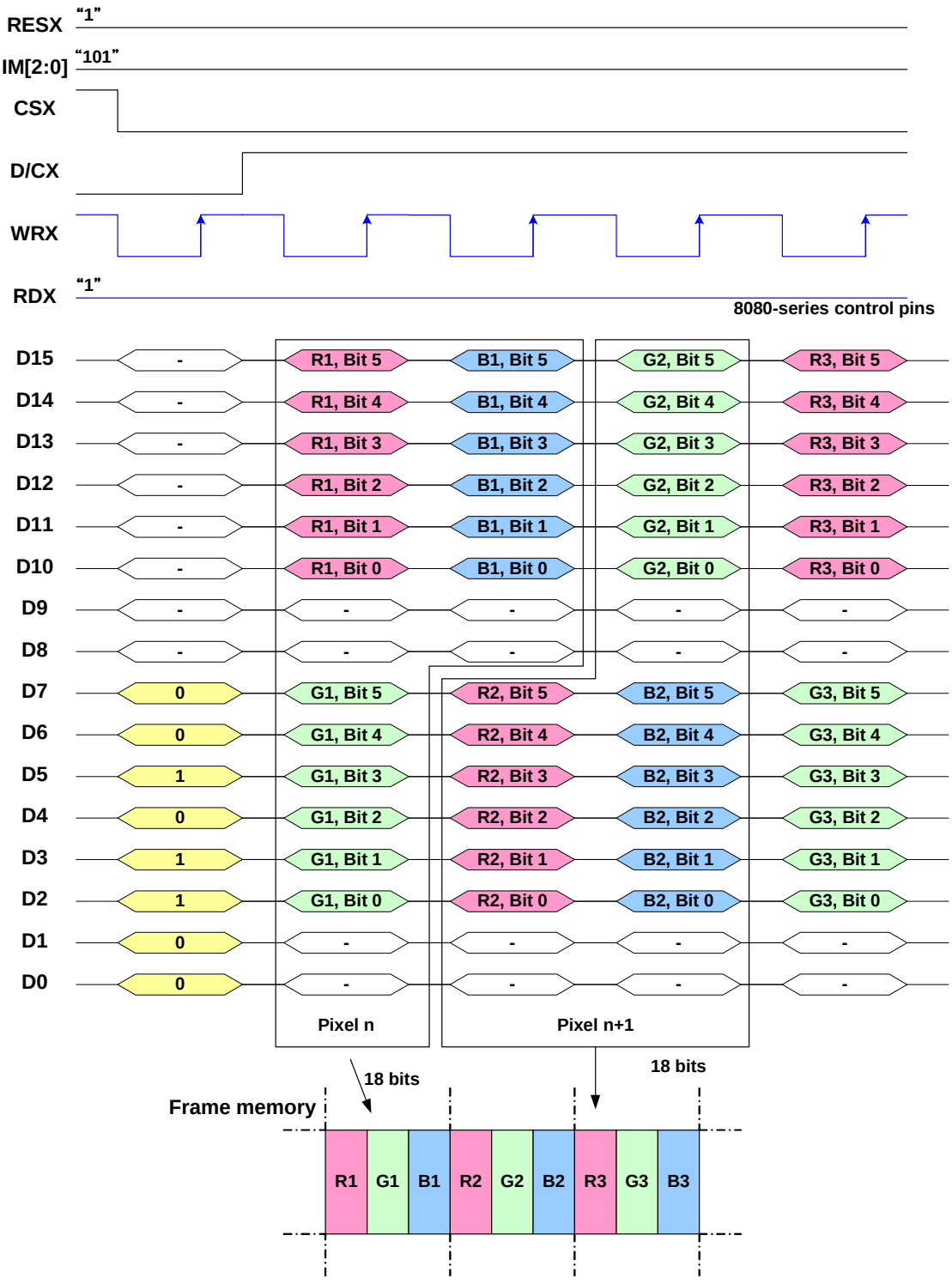
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

9.8.8 16-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= “06h”

There are 2 pixels (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

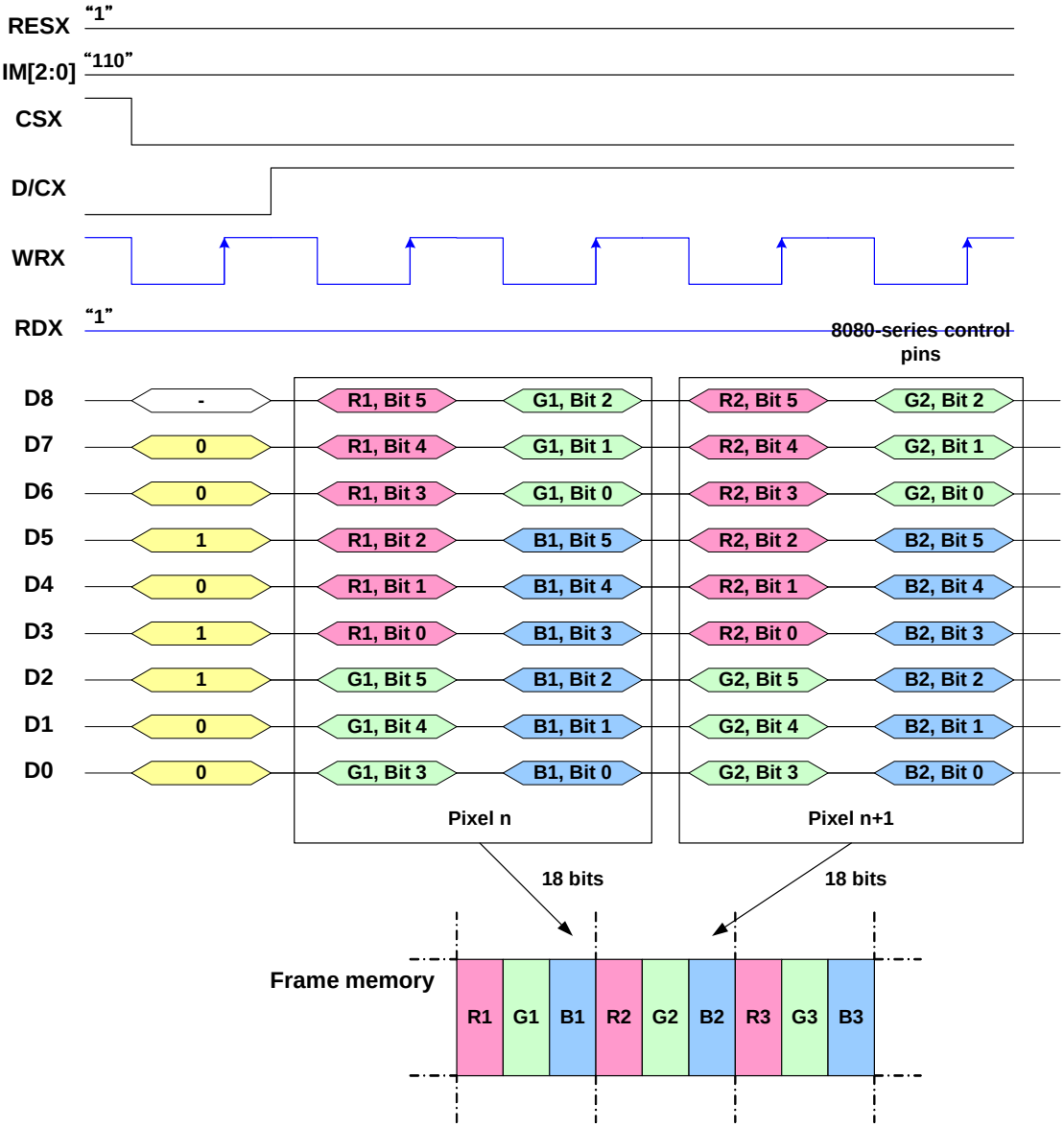
Note 3: ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.9 9-Bit Parallel Interface (IM2, IM1, IM0="110")

Different display data formats are available for three colors depth supported by listed below.
-262k colors, RGB 6,6,6-bit input

9.8.10 Write 9-bit data for RGB 6-6-6-bit input (262k-color)

There is 1 pixel (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

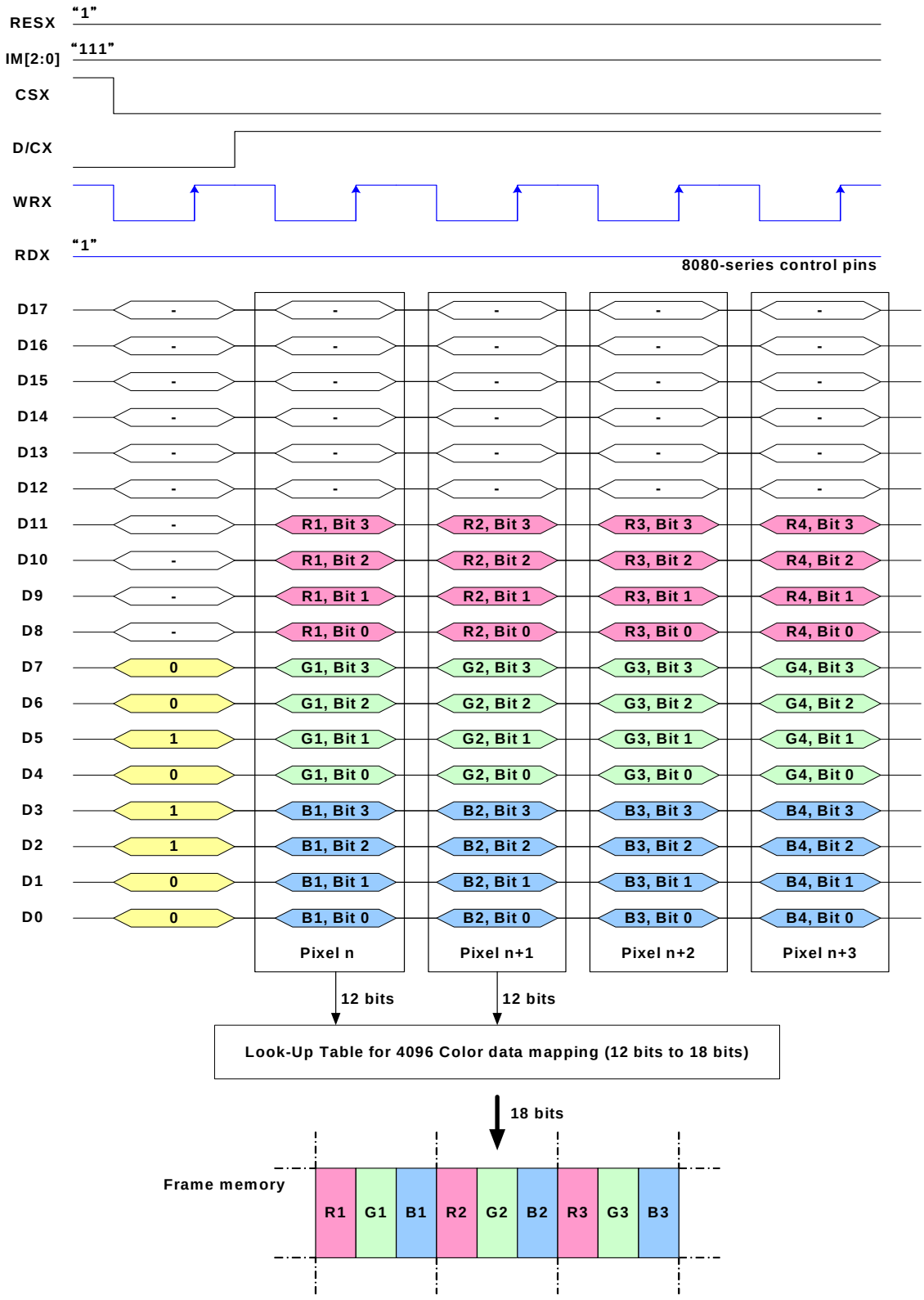
Note 3: '-' = Don't care - Can be set to '0' or '1'

9.8.11 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

9.8.12 18-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

There is 1 pixel (3 sub-pixels) per 1 byte

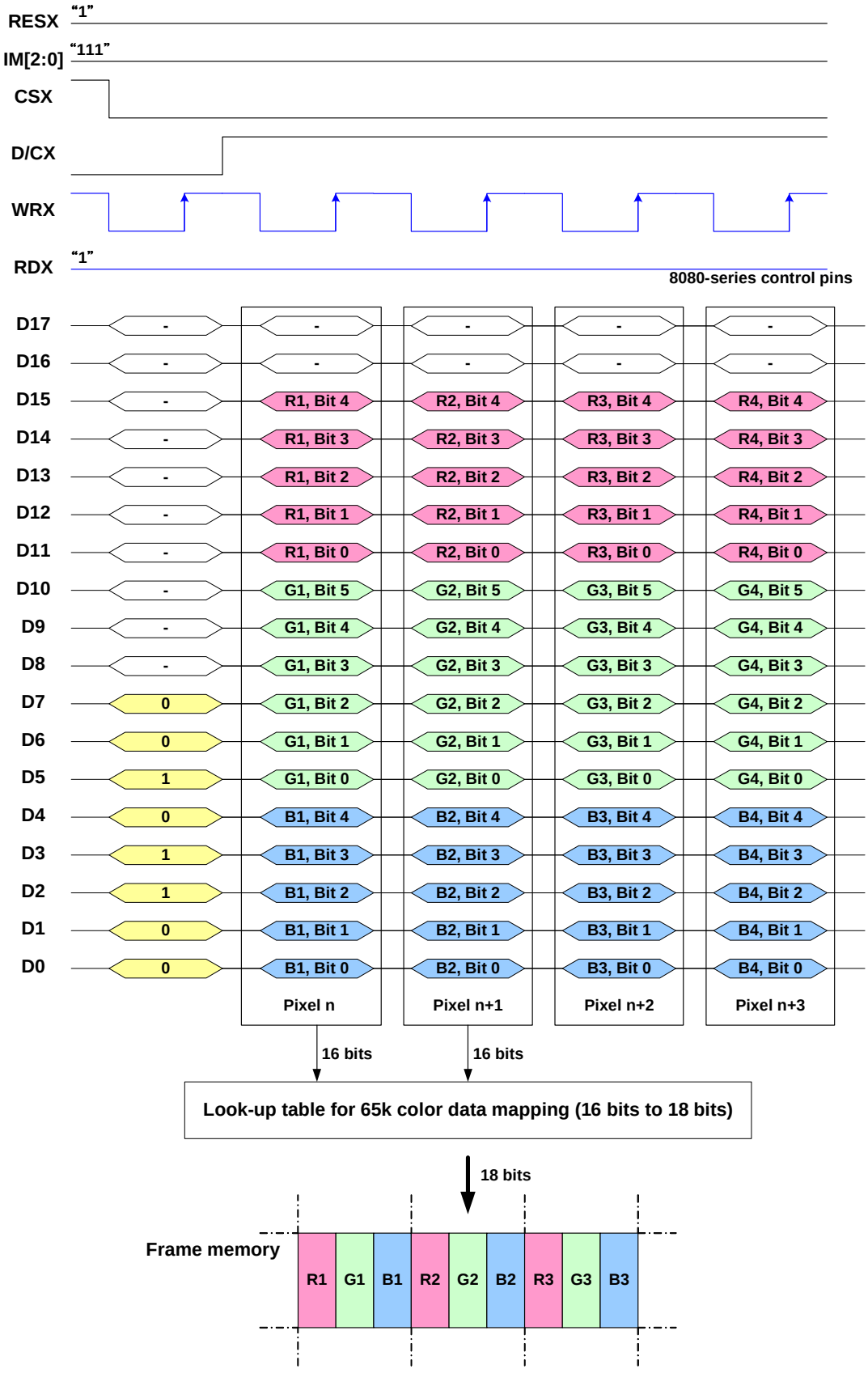


Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.13 18-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

There is 1 pixel (3 sub-pixels) per 1 byte

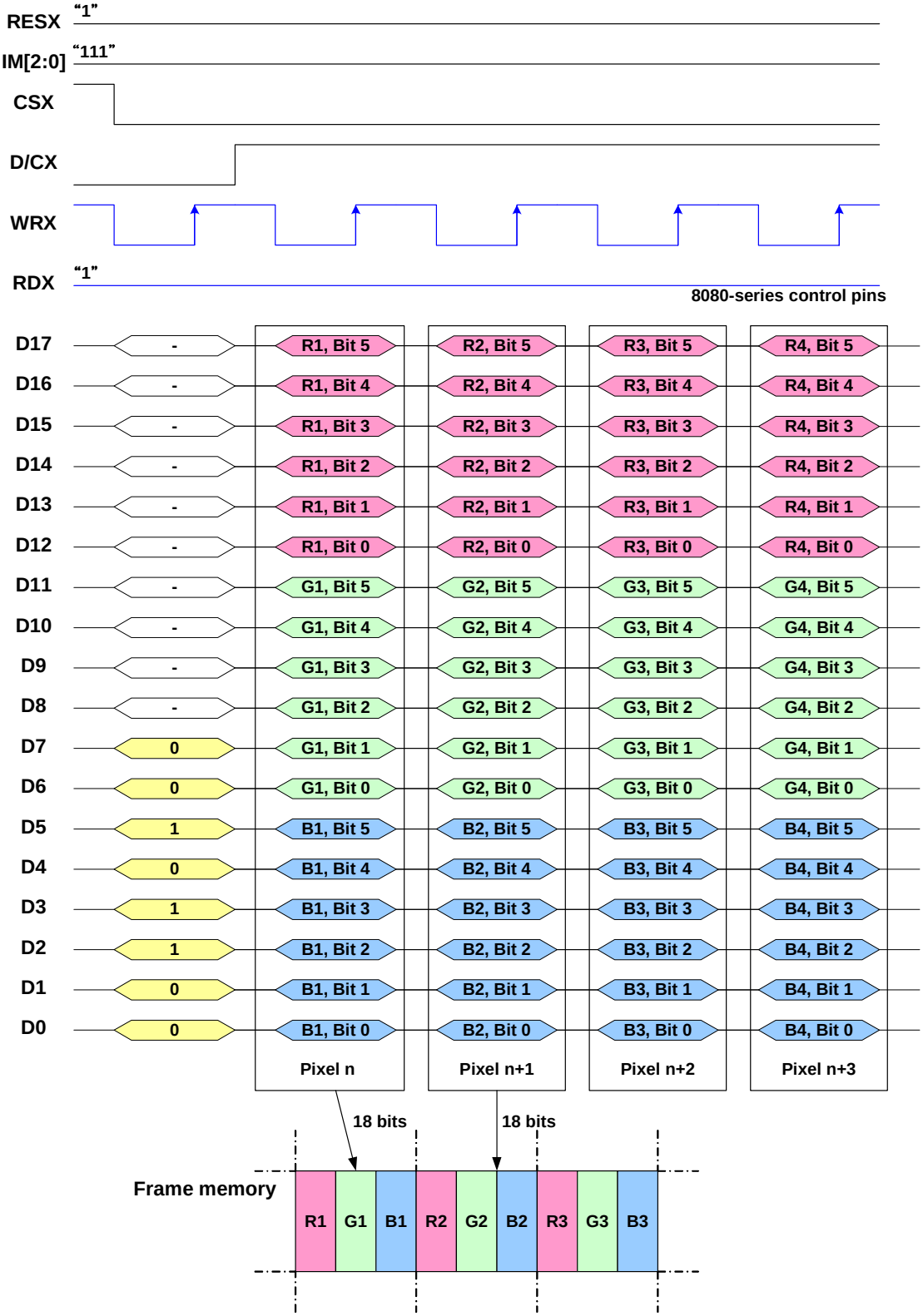


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

9.8.14 18-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 1 byte



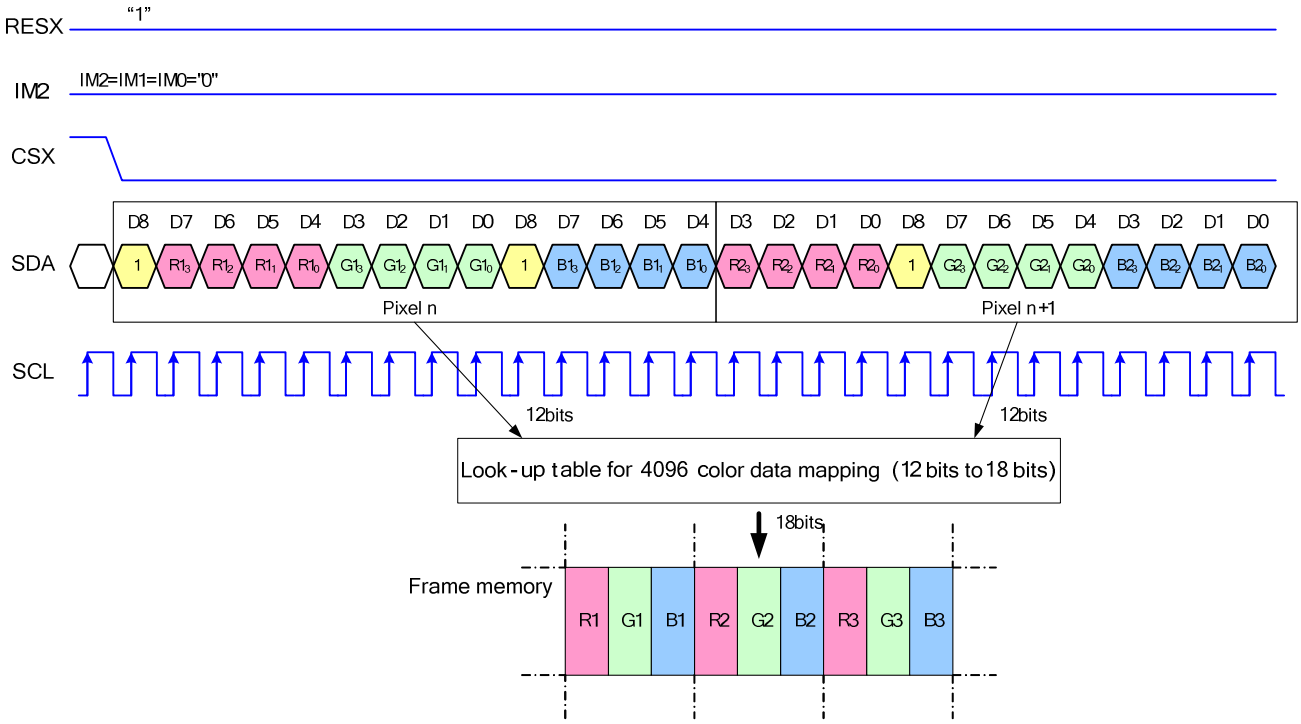
Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

9.8.15 3-line serial Interface

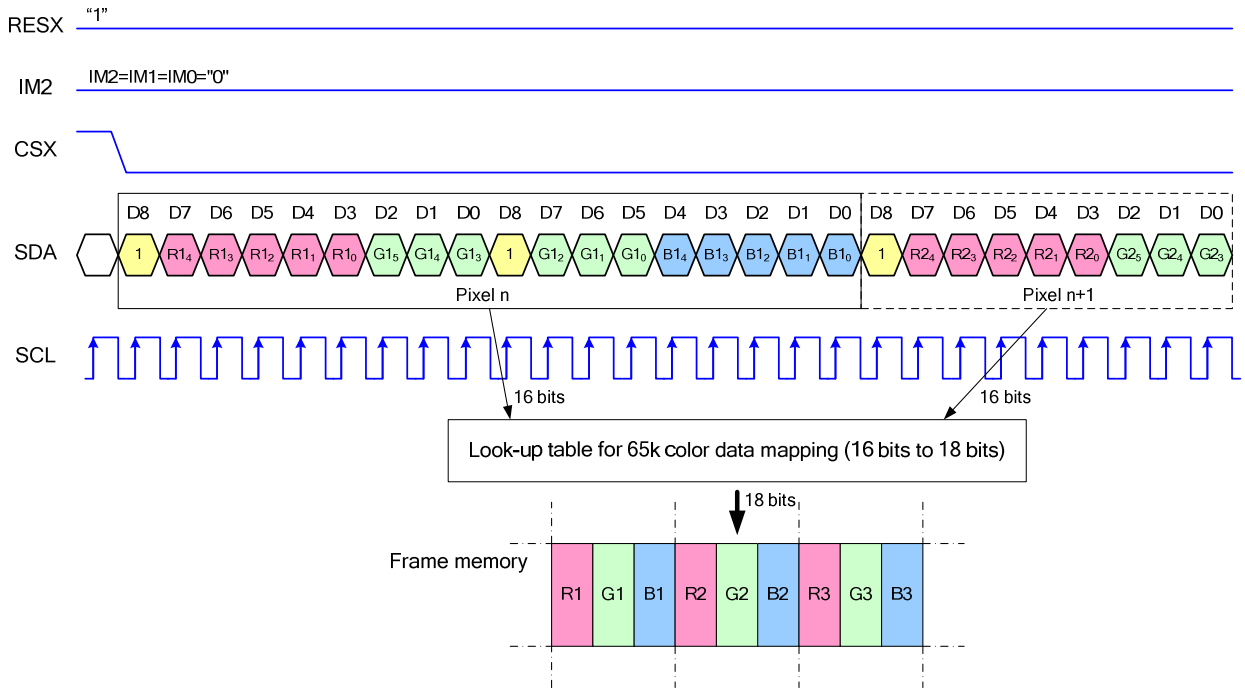
Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

9.8.16 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



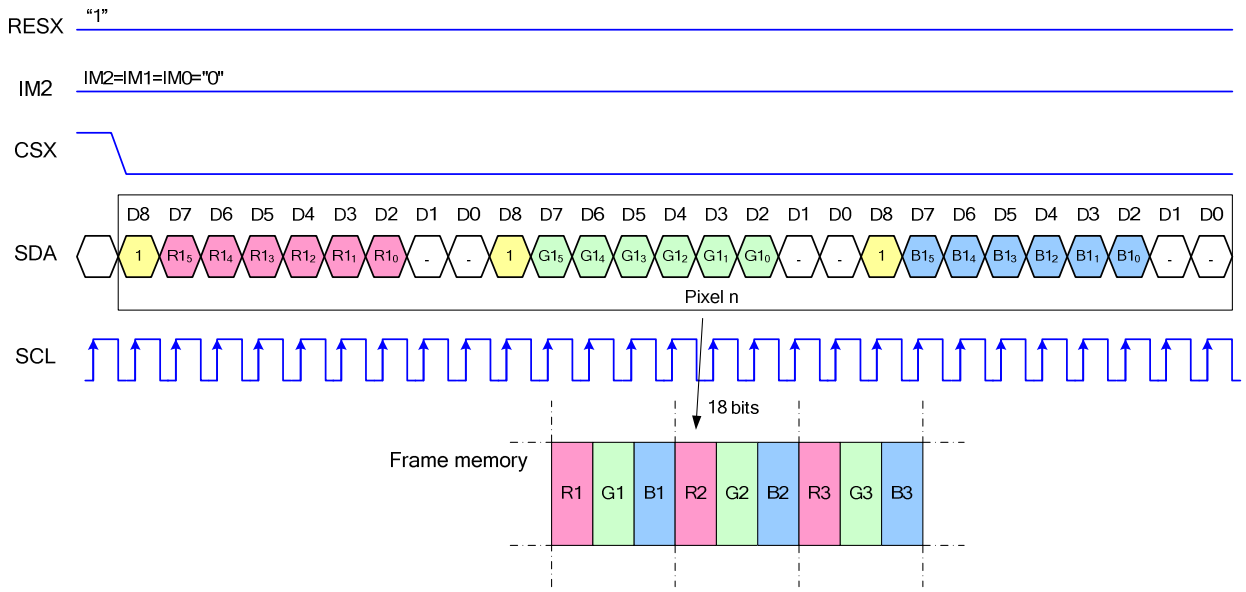
Note 1: Pixel data with the 12-bit color depth information
Note 2: The most significant bits are: Rx3, Gx3 and Bx3
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.17 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.18 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

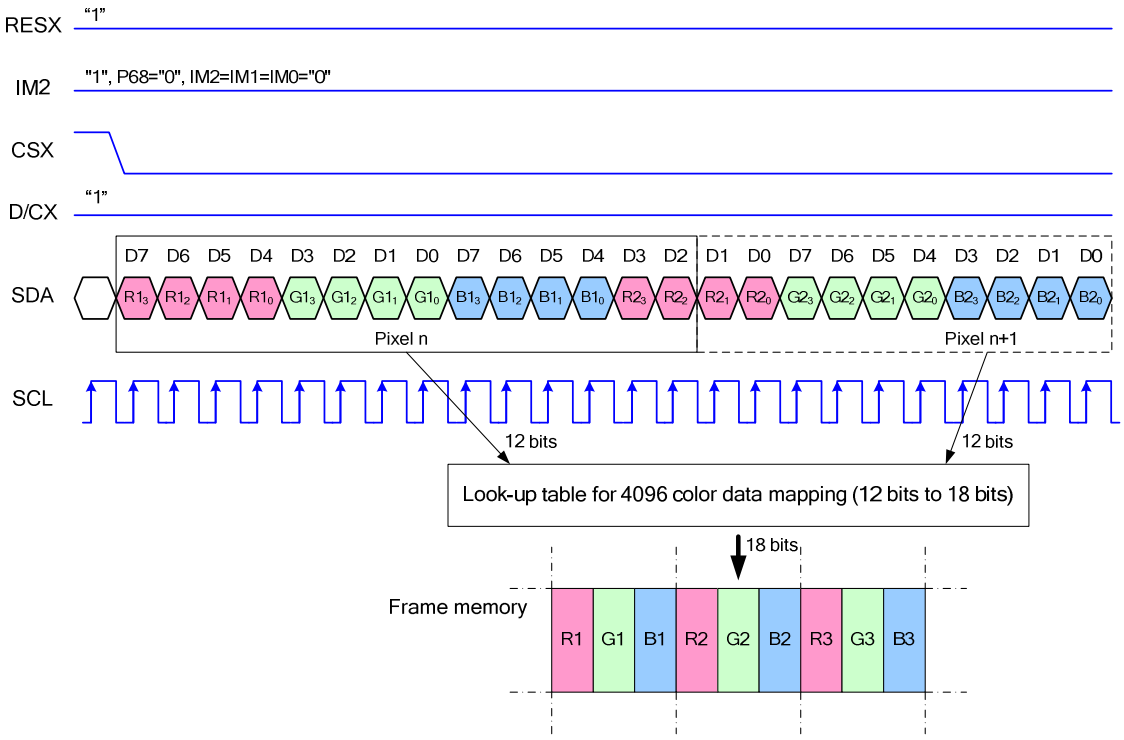


Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.19 4-line serial Interface

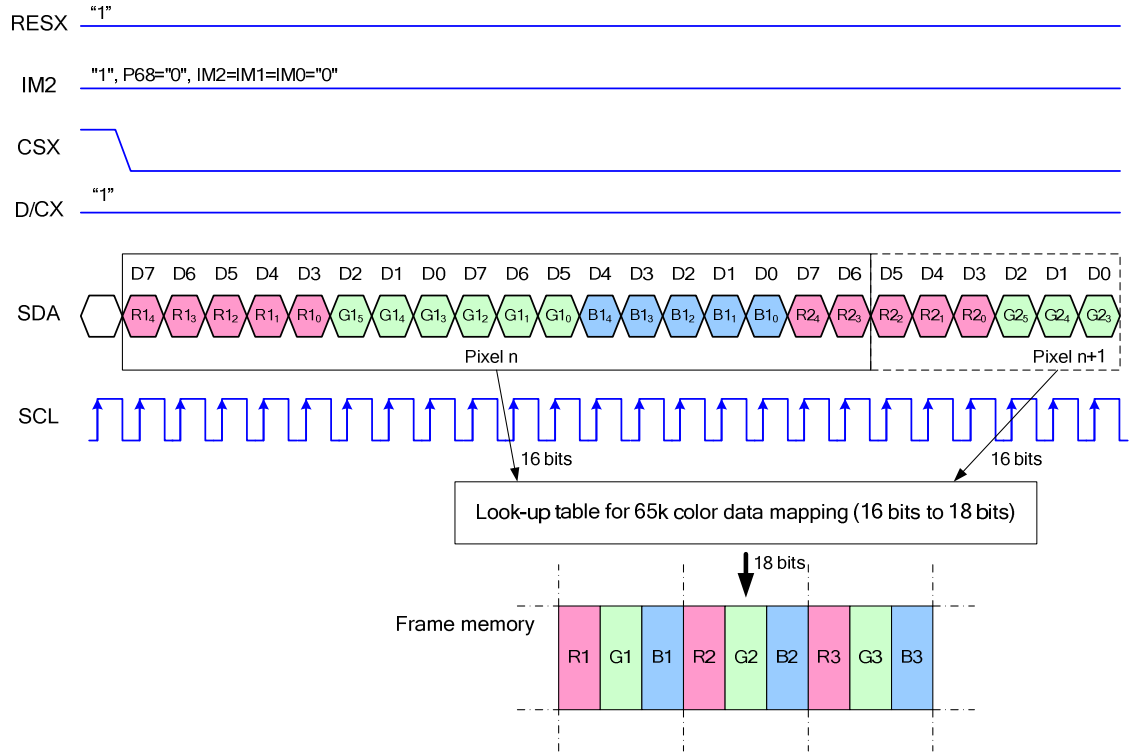
Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

9.8.20 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



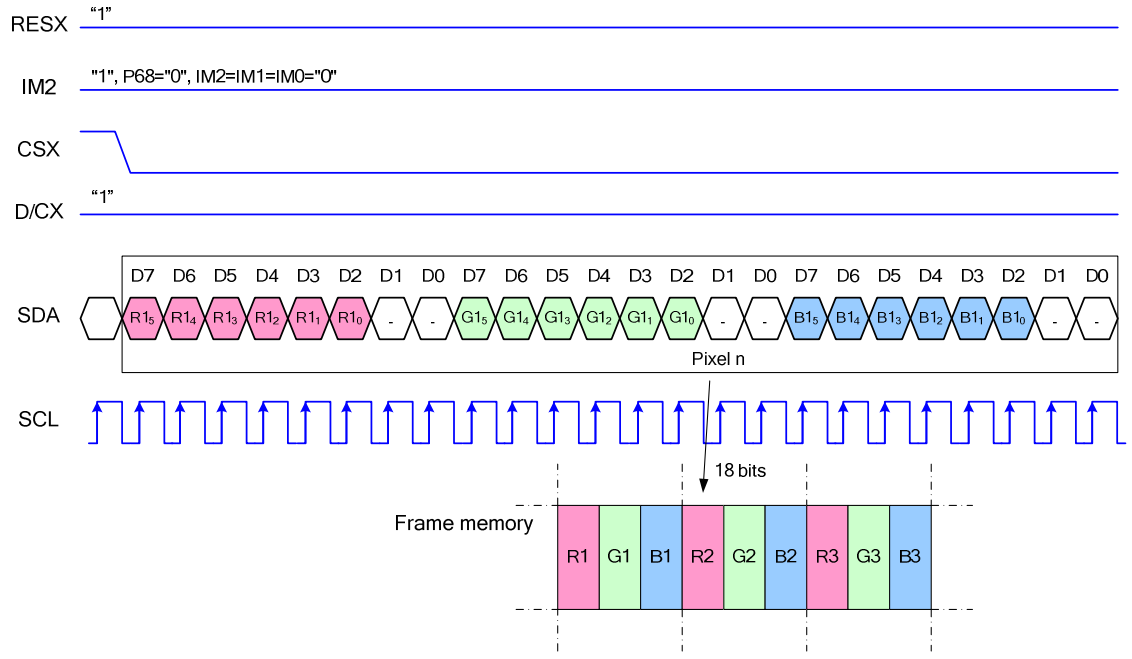
Note 1. pixel data with the 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.21 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



Note 1. pixel data with the 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.22 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



Note 1. pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.9 Display Data RAM

9.9.1 Configuration (GM[1:0] = “00”)

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bit memory allows storing on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

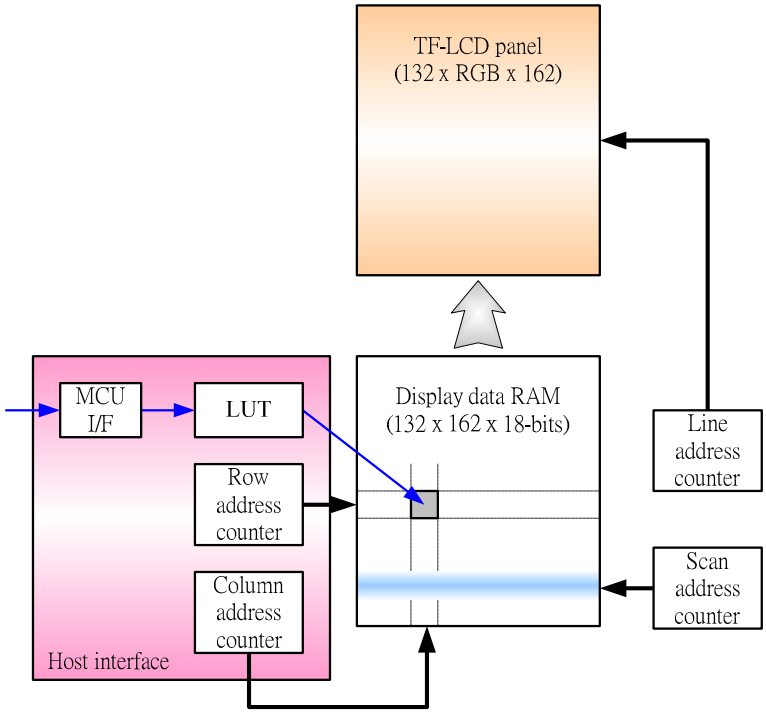
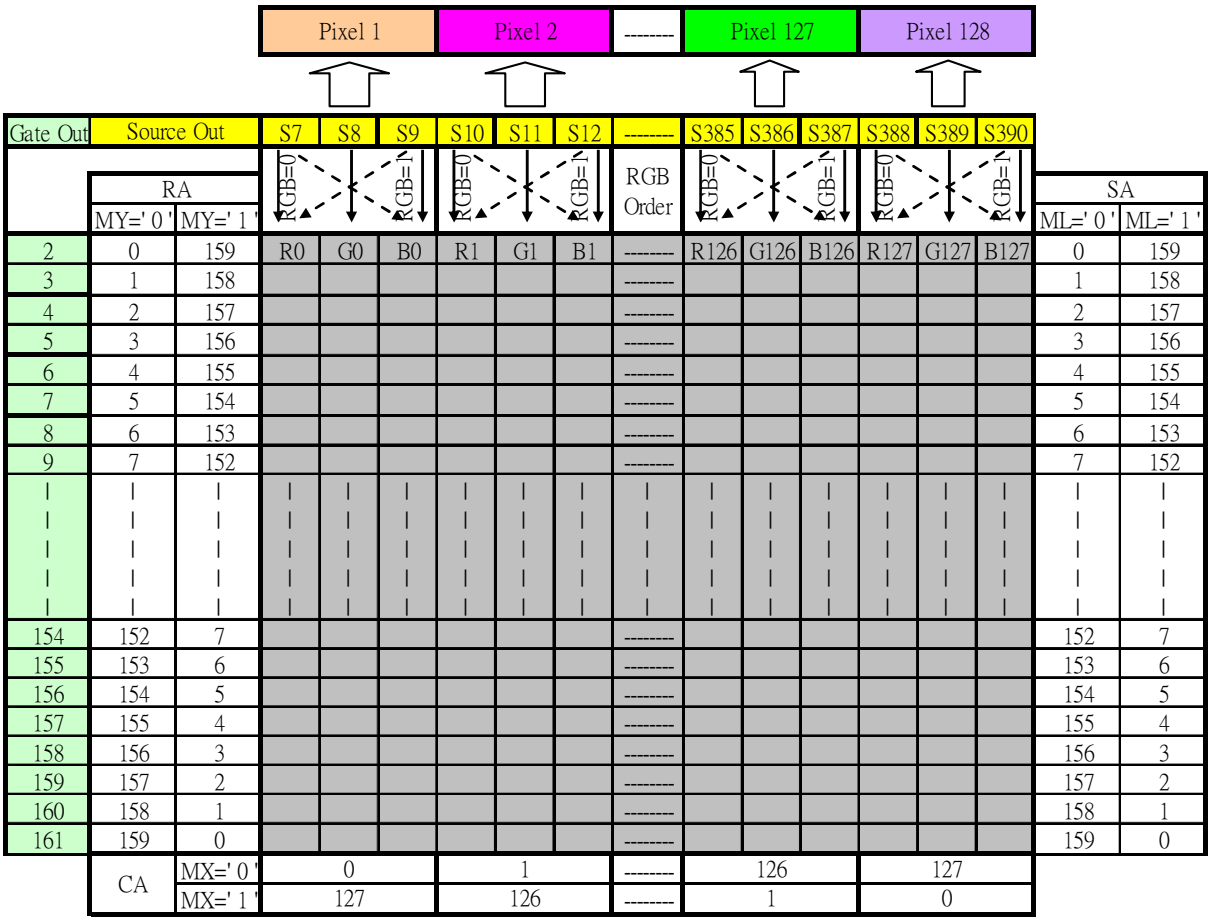


Figure 9.9.1Display data RAM organization

9.9.2 Memory to Display Address Mapping

9.9.3 When using 128RGB x 160 resolution (GM[1:0] = “11”, SMX=SMY=SRGB= ‘0’)



Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.9.4 When using 132RGB x 162 resolution (GM[1:0] = “00”, SMX=SMY=SRGB= ‘0’)

Gate Out	Source Out		S1	S2	S3	S4	S5	S6	--------	S391	S392	S393	S394	S395	S396		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=' 0 '	MY=' 1 '														ML=' 0 '	ML=' 1 '
1	0	161	R0	G0	B0	R1	G1	B1	--------	R131	G131	B131	R132	G132	B132	0	161
2	1	160							--------							1	160
3	2	159							--------							2	159
4	3	158							--------							3	158
5	4	157							--------							4	157
6	5	156							--------							5	156
7	6	155							--------							6	155
8	7	154							--------							7	154
155	154	7							--------							154	7
156	155	6							--------							155	6
157	156	5							--------							156	5
158	157	4							--------							157	4
159	158	3							--------							158	3
160	159	2							--------							159	2
161	160	1							--------							160	1
162	161	0							--------							161	0
	CA	MX=' 0 '	0			1			--------	130			131				
		MX=' 1 '	131			130			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

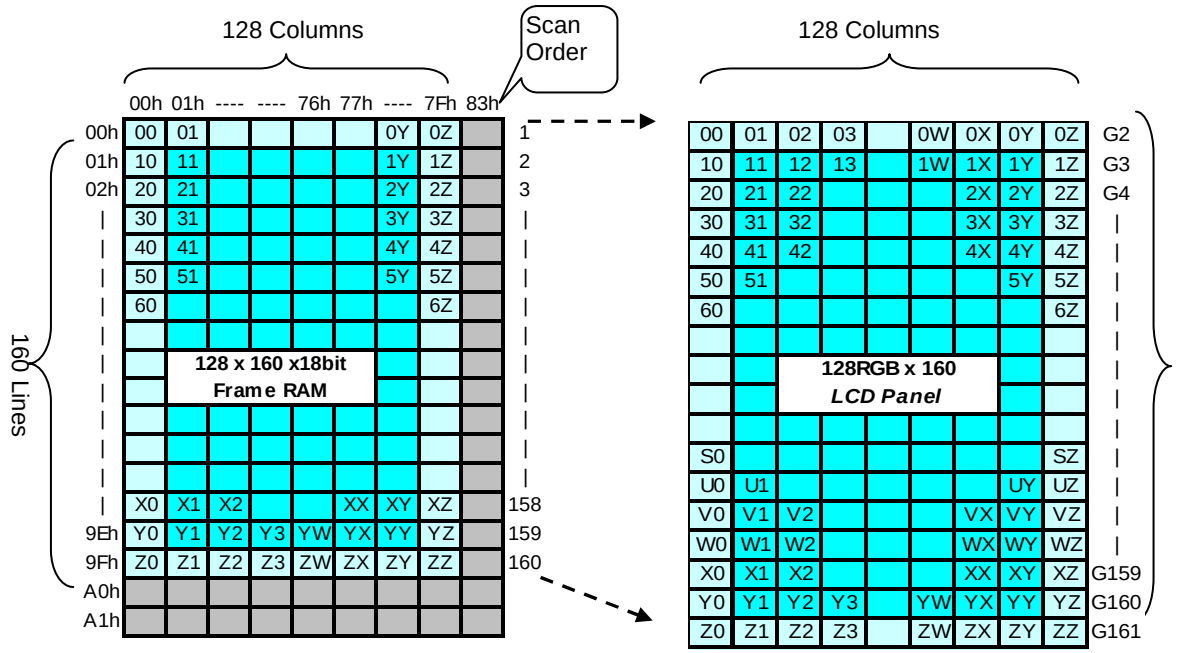
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.9.5 Normal Display On or Partial Mode On

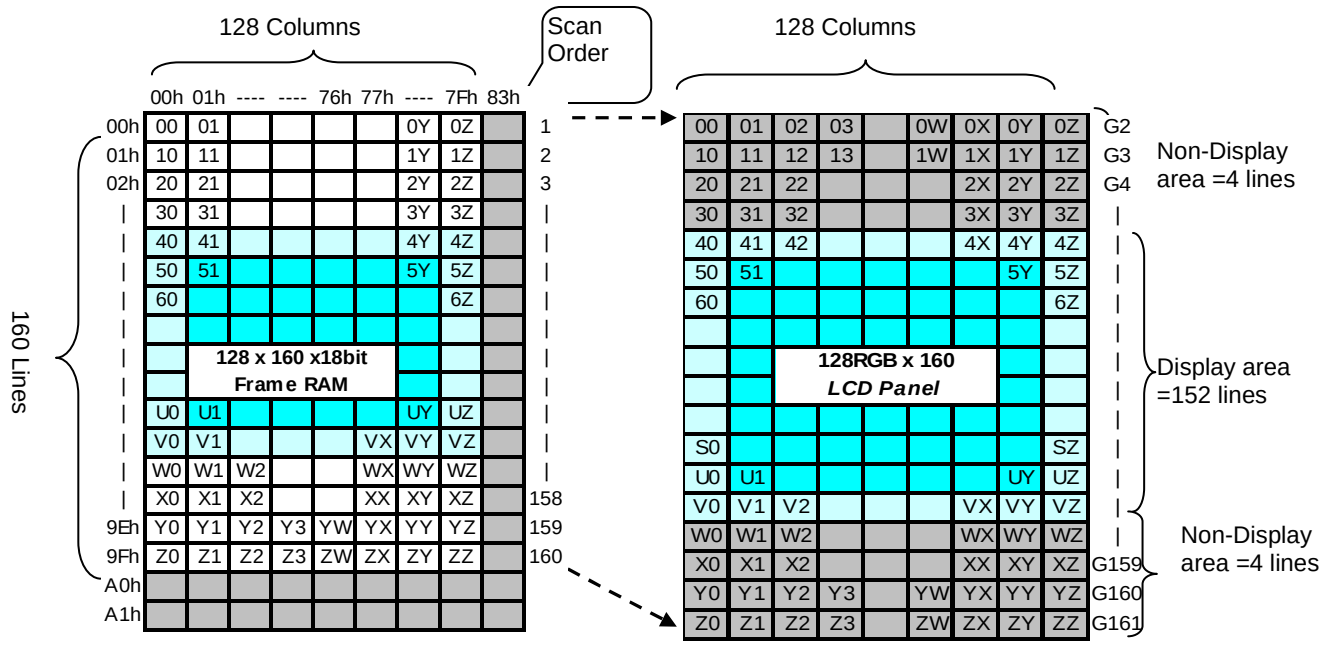
9.9.6 When using 128RGB x 160 resolution (GM[1:0] = “11”)

In this mode, the content of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML=’0’, SMX=SMY=’0’)



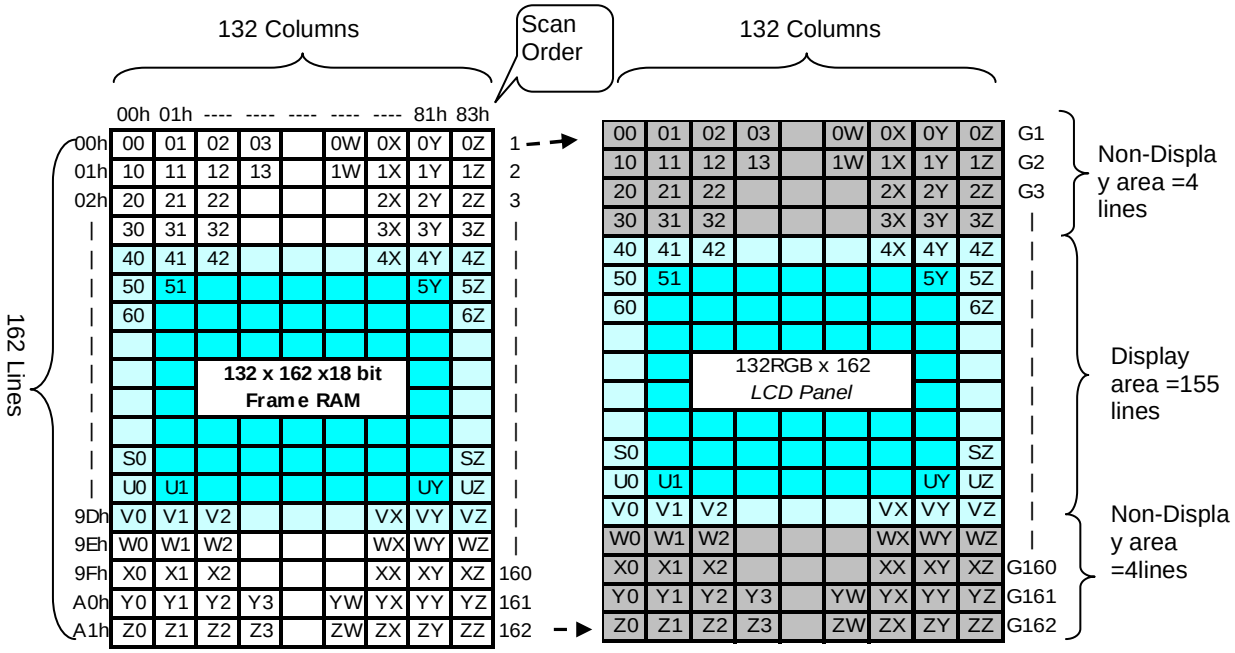
2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MV=ML=’0’ ,SMX=SMY=’0’)



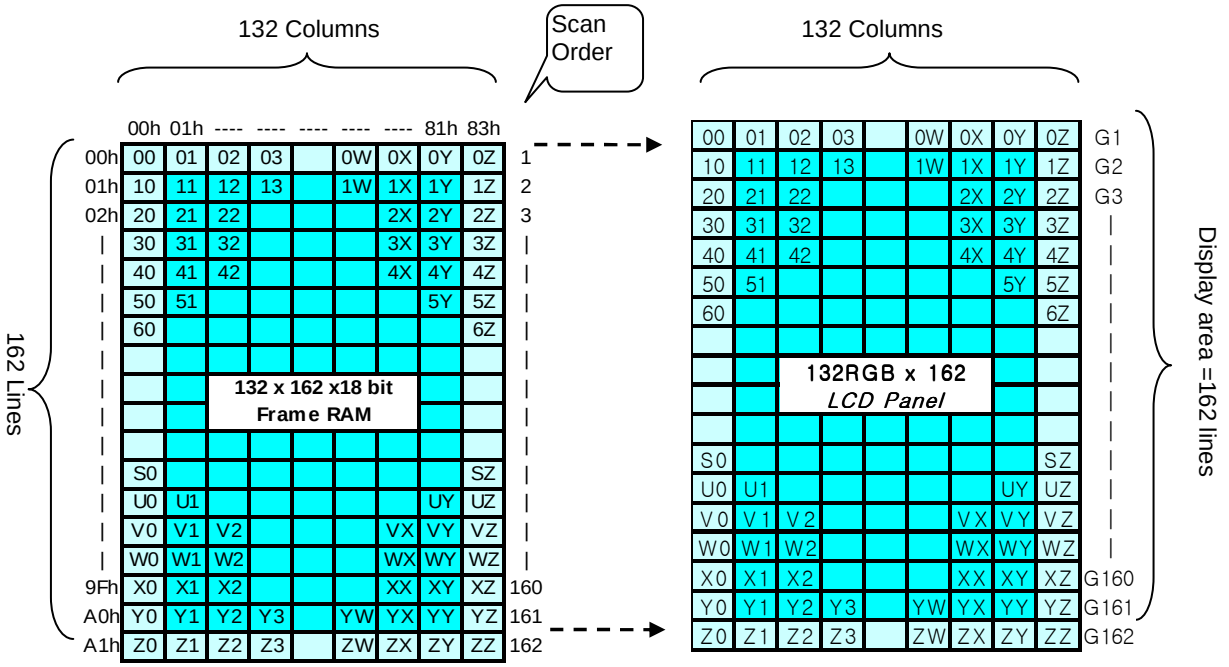
9.9.7 When using 132RGB x 162 resolution (GM[1:0] = “00”)

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0)

1). Example for Normal Display On (MX=MY=ML=’0’, SMX=SMY=’0’)



2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Dh, MX=MV=ML=’0’ ,SMX=SMY=’0’)



9.10 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.
Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET and MADCTL" (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.10 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.11 below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

9.11 Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

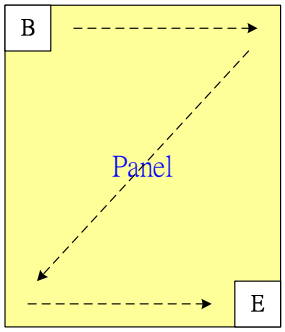


Figure 9.11.1Data streaming order

9.11.1 When 128RGBx160 (GM= “11”)

MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (159-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (127-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (127-Physical Column Pointer)

9.11.2 When 132RGBx162 (GM= “00”)

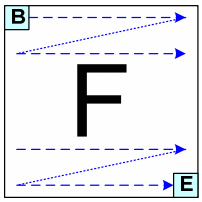
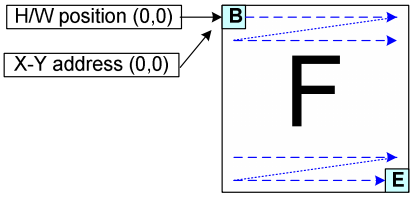
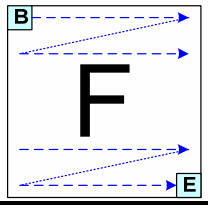
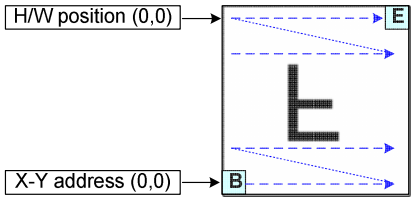
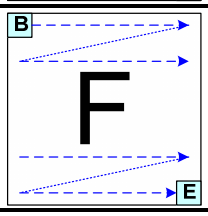
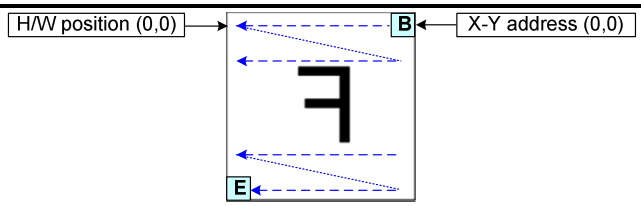
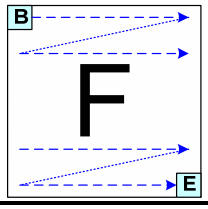
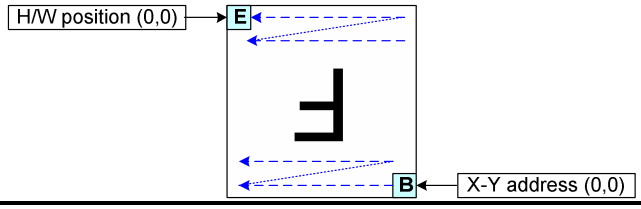
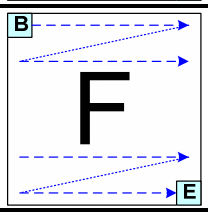
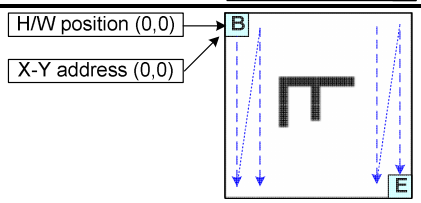
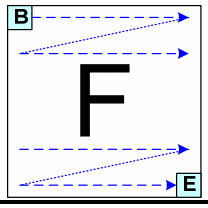
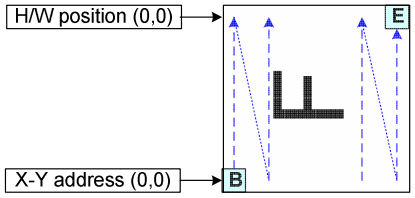
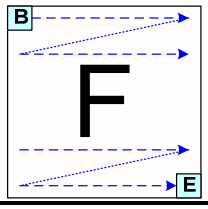
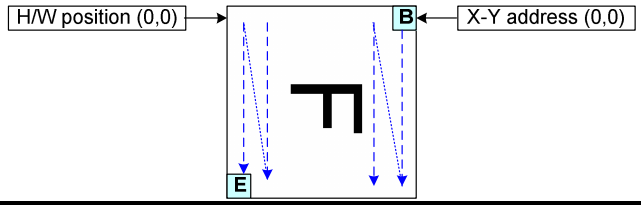
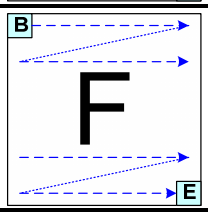
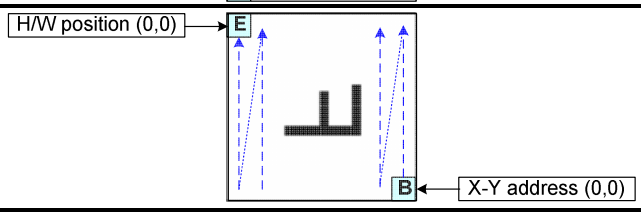
MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161-Physical Row Pointer)
0	1	0	Direct to (131-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (131-Physical Column Pointer)	Direct to (161-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (131-Physical Column Pointer)
1	1	1	Direct to (161-Physical Row Pointer)	Direct to (131-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

9.11.3 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

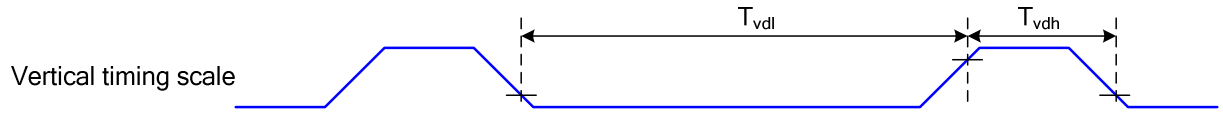
Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

9.12 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

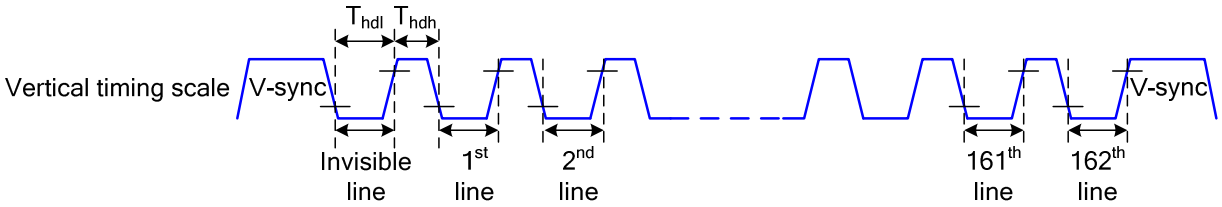
9.12.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

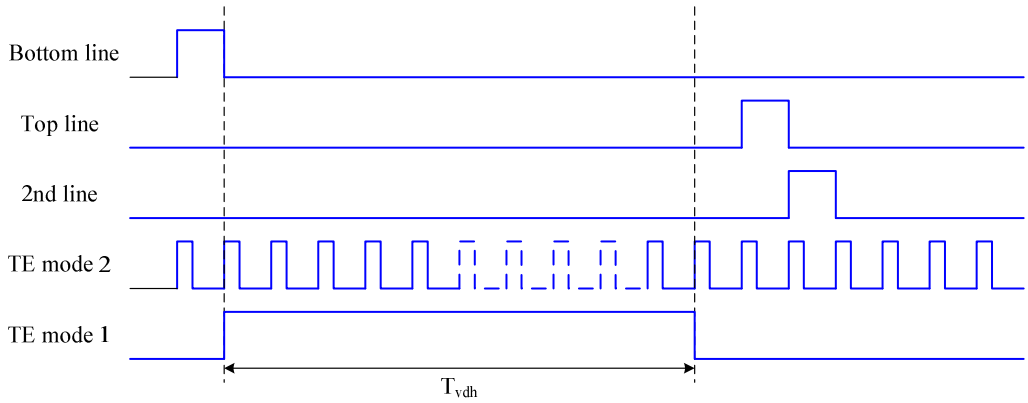


tvdh= The LCD display is not updated from the Frame Memory
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.



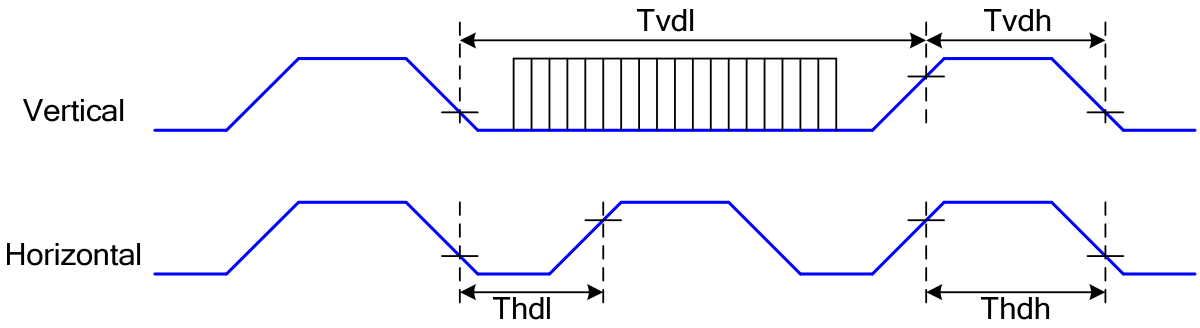
thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

9.12.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

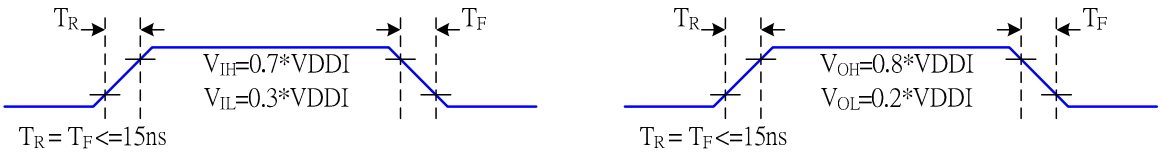


Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	33	-	µs	
thdh	Horizontal Timing Low Duration	25	500	µs	

Table 9.12.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25℃)

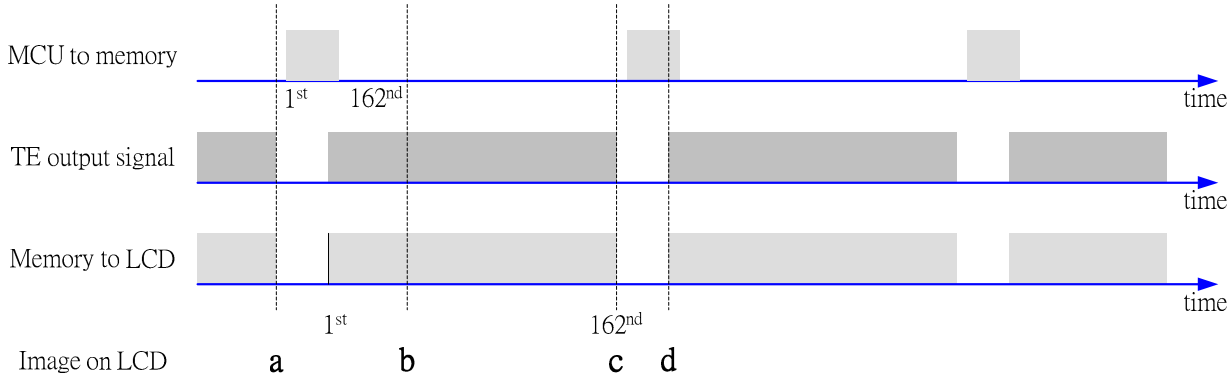
Note: The timings in Table 9.10.1 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

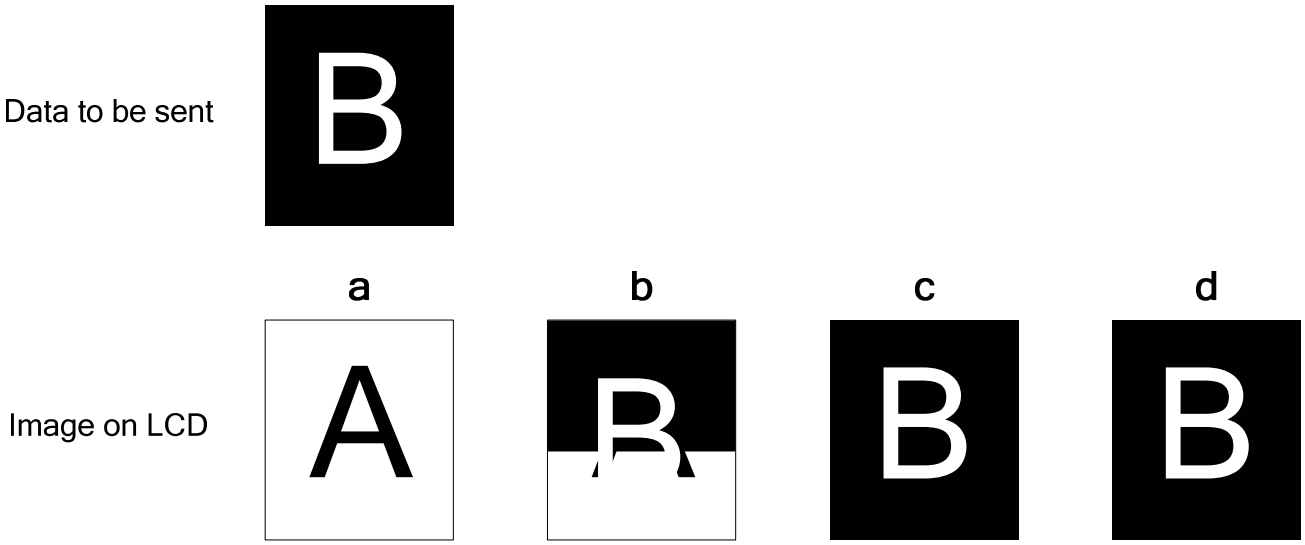


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

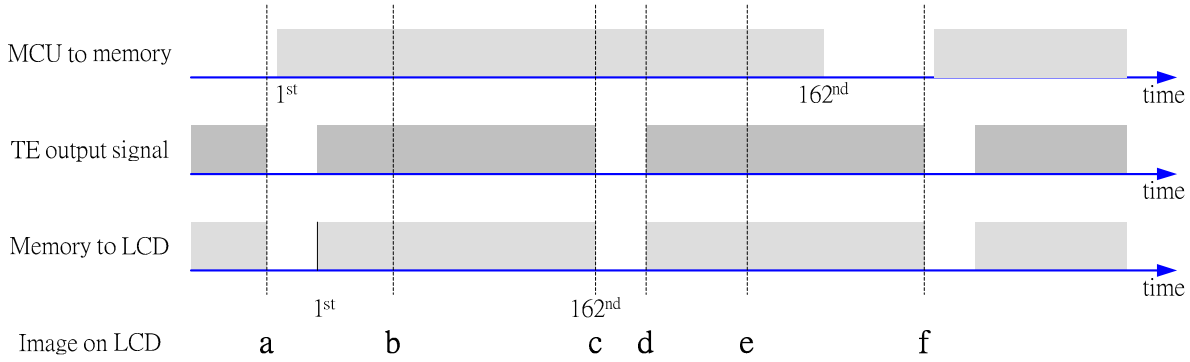
9.12.3 Example 1: MPU Write is faster than panel read



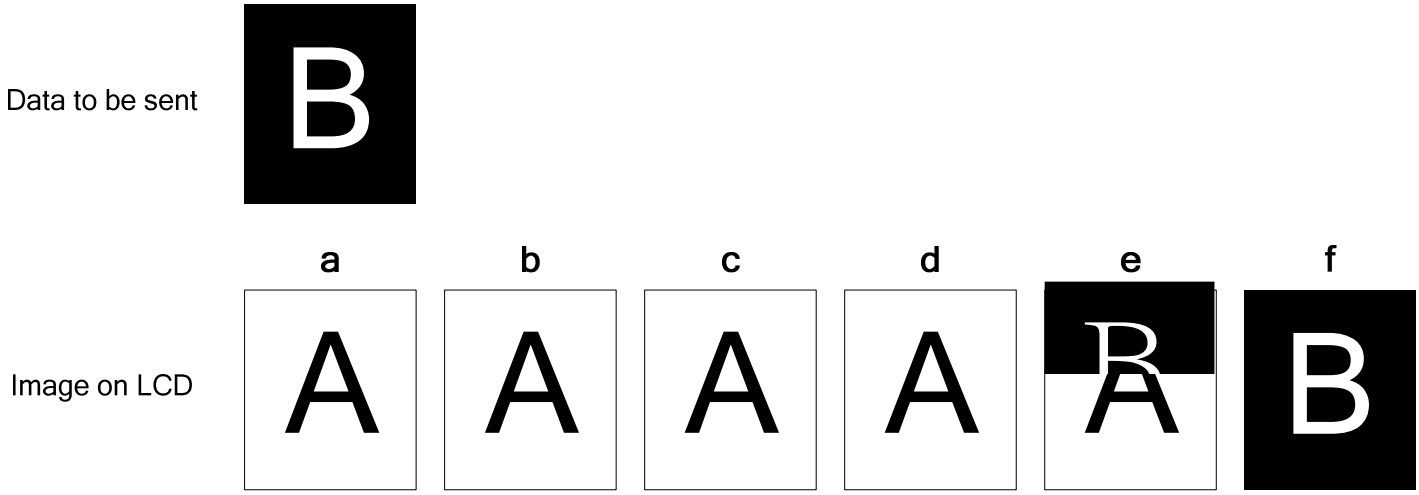
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



9.12.4 Example 2: MPU write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



9.13 Power ON/OFF Sequence

VDD must be powered on before the VDDI.
VDDI must be powered off before the VDD.
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

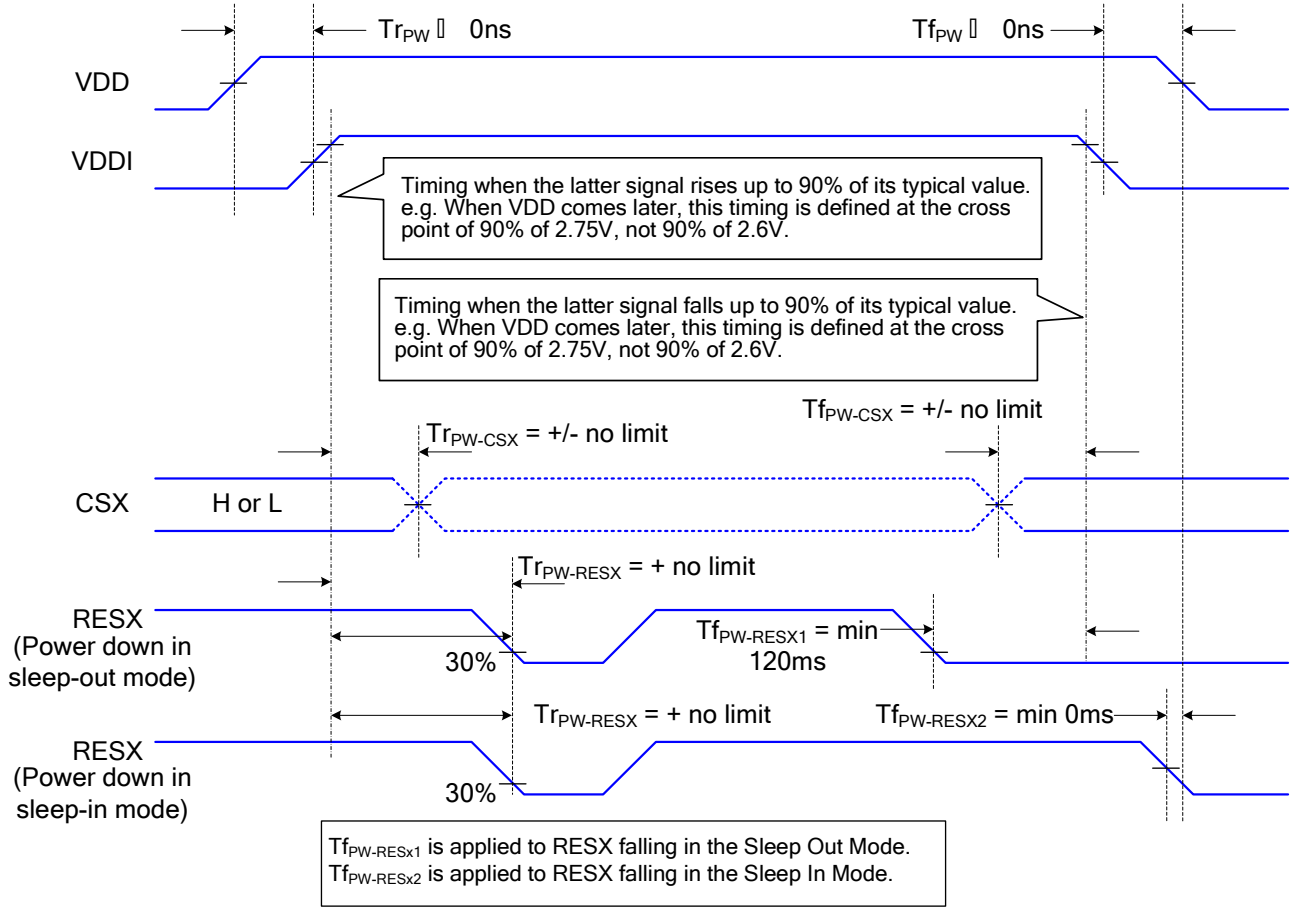
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



9.13.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

9.14 Power Level Definition

9.14.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.
In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used but with 8 colors.

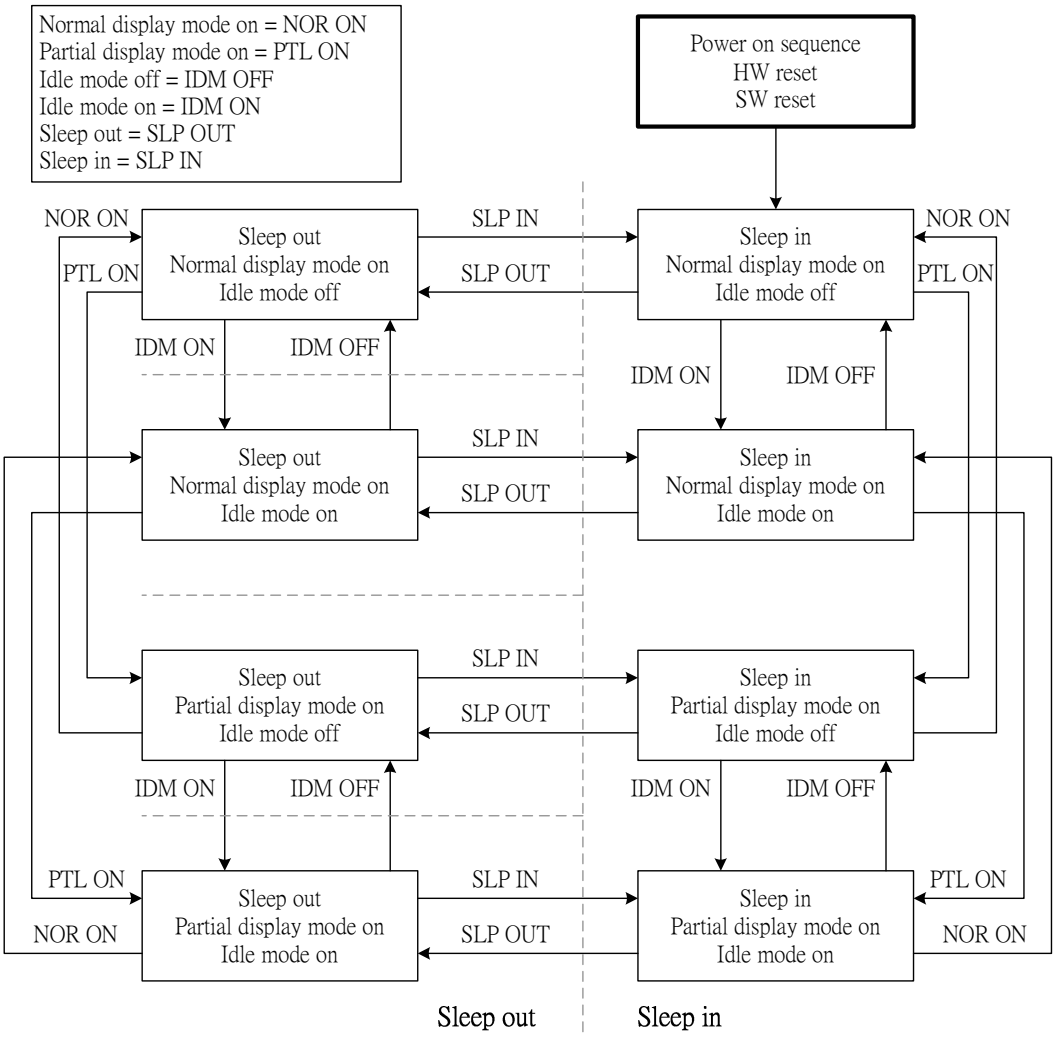
4. Partial Mode On, Idle Mode On, Sleep Out.
In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode
In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode
In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

9.14.2 Power Flow Chart



9.15 Reset Table

9.15.1 Reset Table (Default Value, GM[1:0]="11", 128RGB x 160)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	Random values	Random values	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.15.2 Reset Table (GM[1:0]= “00”, 132RGB x 162)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 00A1h (161d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00A1h	00A1h	00A1h (161d) (when MV=0) 0083h (131d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	Random values	Random values	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00A1h	00A1h	00A1h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.16 Module Input/Output Pins

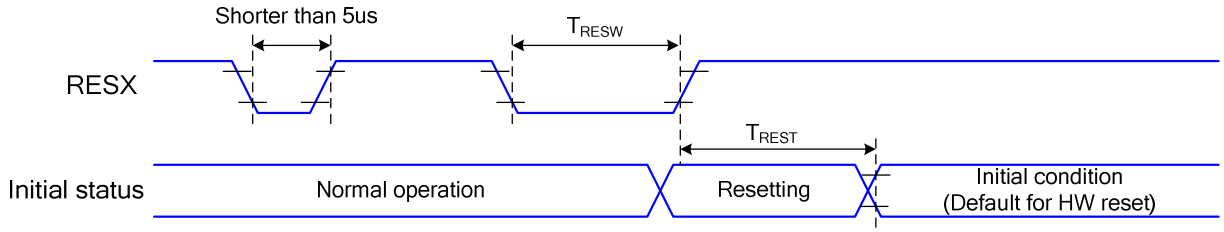
9.16.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 9.14	Input valid	Input valid	Input valid	See 9.14
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D7 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

9.17 Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset pulse duration	10	-	us
	tREST	Reset cancel	-	5	ms
				120	ms

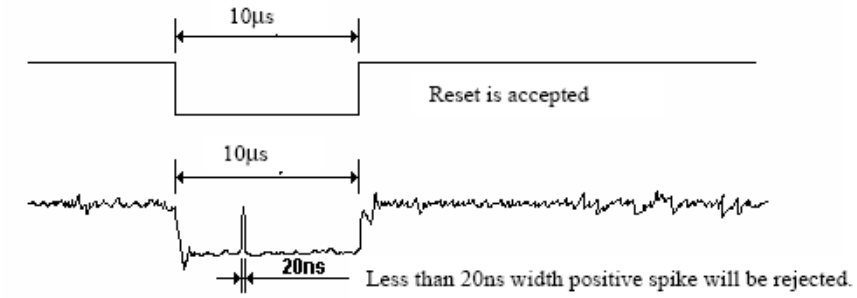
Table 9.17.1 Reset timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9.18 Color Depth Conversion Look Up Tables

9.18.1 65536 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
RED	R005 R004 R003 R002 R001 R000	1	00000
	R015 R014 R013 R012 R011 R010	2	00001
	R025 R024 R023 R022 R021 R020	3	00010
	R035 R034 R033 R032 R031 R030	4	00011
	R045 R044 R043 R042 R041 R040	5	00100
	R055 R054 R053 R052 R051 R050	6	00101
	R065 R064 R063 R062 R061 R060	7	00110
	R075 R074 R073 R072 R071 R070	8	00111
	R085 R084 R083 R082 R081 R080	9	01000
	R095 R094 R093 R092 R091 R090	10	01001
	R105 R104 R103 R102 R101 R100	11	01010
	R115 R114 R113 R112 R111 R110	12	01011
	R125 R124 R123 R122 R121 R120	13	01100
	R135 R134 R133 R132 R131 R130	14	01101
	R145 R144 R143 R142 R141 R140	15	01110
	R155 R154 R153 R152 R151 R150	16	01111
	R165 R164 R163 R162 R161 R160	17	10000
	R175 R174 R173 R172 R171 R170	18	10001
	R185 R184 R183 R182 R181 R180	19	10010
	R195 R194 R193 R192 R191 R190	20	10011
	R205 R204 R203 R202 R201 R200	21	10100
	R215 R214 R213 R212 R211 R210	22	10101
	R225 R224 R223 R222 R221 R220	23	10110
	R235 R234 R233 R232 R231 R230	24	10111
	R245 R244 R243 R242 R241 R240	25	11000
	R255 R254 R253 R252 R251 R250	26	11001
	R265 R264 R263 R262 R261 R260	27	11010
	R275 R274 R273 R272 R271 R270	28	11011
	R285 R284 R283 R282 R281 R280	29	11100
	R295 R294 R293 R292 R291 R290	30	11101
	R305 R304 R303 R302 R301 R300	31	11110
	R315 R314 R313 R312 R311 R310	32	11111

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
GREEN	G005 G004 G003 G002 G001 G000	33	000000
	G015 G014 G013 G012 G011 G010	34	000001
	G025 G024 G023 G022 G021 G020	35	000010
	G035 G034 G033 G032 G031 G030	36	000011
	G045 G044 G043 G042 G041 G040	37	000100
	G055 G054 G053 G052 G051 G050	38	000101
	G065 G064 G063 G062 G061 G060	39	000110
	G075 G074 G073 G072 G071 G070	40	000111
	G085 G084 G083 G082 G081 G080	41	001000
	G095 G094 G093 G092 G091 G090	42	001001
	G105 G104 G103 G102 G101 G100	43	001010
	G115 G114 G113 G112 G111 G110	44	001011
	G125 G124 G123 G122 G121 G120	45	001100
	G135 G134 G133 G132 G131 G130	46	001101
	G145 G144 G143 G142 G141 G140	47	001110
	G155 G154 G153 G152 G151 G150	48	001111
	G165 G164 G163 G162 G161 G160	49	010000
	G175 G174 G173 G172 G171 G170	50	010001
	G185 G184 G183 G182 G181 G180	51	010010
	G195 G194 G193 G192 G191 G190	52	010011
	G205 G204 G203 G202 G201 G200	53	010100

	G215 G214 G213 G212 G211 G210	54	010101
	G225 G224 G223 G222 G221 G220	55	010110
	G235 G234 G233 G232 G231 G230	56	010111
	G245 G244 G243 G242 G241 G240	57	011000
	G255 G254 G253 G252 G251 G250	58	011001
	G265 G264 G263 G262 G261 G260	59	011010
	G275 G 274 G273 G272 G271 G270	60	011011
	G285 G 284 G283 G282 G281 G280	61	011100
	G295 G 294 G293 G292 G291 G290	62	011101
	G305 G 304 G303 G302 G301 G300	63	011110
	G315 G 314 G313 G312 G311 G310	64	011111
	G325 G324 G323 G322 G321 G320	65	100000
	G335 G334 G333 G332 G331 G330	66	100001
	G345 G344 G343 G342 G341 G340	67	100010
	G355 G354 G353 G352 G351 G350	68	100011
	G365 G364 G363 G362 G361 G360	69	100100
	G375 G374 G373 G372 G371 G370	70	100101
	G385 G384 G383 G382 G381 G380	71	100110
	G395 G394 G393 G392 G391 G390	72	100111
	G405 G404 G403 G402 G401 G400	73	101000
	G415 G414 G413 G412 G411 G410	74	101001
	G425 G424 G423 G422 G421 G420	75	101010
	G435 G434 G433 G432 G431 G430	76	101011
	G445 G444 G443 G442 G441 G440	77	101100
	G455 G454 G453 G452 G451 G450	78	101101
	G465 G464 G463 G462 G461 G460	79	101110
	G475 G474 G473 G472 G471 G470	80	101111
	G485 G484 G483 G482 G481 G480	81	110000
	G495 G494 G493 G492 G491 G490	82	110001
	G505 G504 G503 G502 G501 G500	83	110010
	G515 G514 G513 G512 G511 G510	84	110011
	G525 G524 G523 G522 G521 G520	85	110100
	G535 G534 G533 G532 G531 G530	86	110101
	G545 G544 G543 G542 G541 G540	87	110110
	G555 G554 G553 G552 G551 G550	88	110111
	G565 G564 G563 G562 G561 G560	89	111000
	G575 G574 G573 G572 G571 G570	90	111001
	G585 G584 G583 G582 G581 G580	91	111010
	G595 G594 G593 G592 G591 G590	92	111011
	G605 G604 G603 G602 G601 G600	93	111100
	G615 G614 G613 G612 G611 G610	94	111101
	G625 G624 G623 G622 G621 G620	95	111110
	G635 G634 G633 G632 G631 G630	96	111111

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
BLUE	B005 B004 B003 B002 B001 B000	97	00000
	B015 B014 B013 B012 B011 B010	98	00001
	B025 B024 B023 B022 B021 B020	99	00010
	B035 B034 B033 B032 B031 B030	100	00011
	B045 B044 B043 B042 B041 B040	101	00100
	B055 B054 B053 B052 B051 B050	102	00101
	B065 B064 B063 B062 B061 B060	103	00110
	B075 B074 B073 B072 B071 B070	104	00111
	B085 B084 B083 B082 B081 B080	105	01000
	B095 B094 B093 B092 B091 B090	106	01001
	B105 B104 B103 B102 B101 B100	107	01010
	B115 B114 B113 B112 B111 B110	108	01011
	B125 B124 B123 B122 B121 B120	109	01100
	B135 B134 B133 B132 B131 B130	110	01101
	B145 B144 B143 B142 B141 B140	111	01110
	B155 B154 B153 B152 B151 B150	112	01111
	B165 B164 B163 B162 B161 B160	113	10000

	B175 B174 B173 B172 B171 B170	114	10001
	B185 B184 B183 B182 B181 B180	115	10010
	B195 B194 B193 B192 B191 B190	116	10011
	B205 B204 B203 B202 B201 B200	117	10100
	B215 B214 B213 B212 B211 B210	118	10101
	B225 B224 B223 B222 B221 B220	119	10110
	B235 B234 B233 B232 B231 B230	120	10111
	B245 B244 B243 B242 B241 B240	121	11000
	B255 B254 B253 B252 B251 B250	122	11001
	B265 B264 B263 B262 B261 B260	123	11010
	B275 B274 B273 B272 B271 B270	124	11011
	B285 B284 B283 B282 B281 B280	125	11100
	B295 B294 B293 B292 B291 B290	126	11101
	B305 B304 B303 B302 B301 B300	127	11110
	B315 B314 B313 B312 B311 B310	128	11111

9.18.2 4096 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 4k Color (4-bits)
RED	R005 R004 R003 R002 R001 R000	1	0000
	R015 R014 R013 R012 R011 R010	2	0001
	R025 R024 R023 R022 R021 R020	3	0010
	R035 R034 R033 R032 R031 R030	4	0011
	R045 R044 R043 R042 R041 R040	5	0100
	R055 R054 R053 R052 R051 R050	6	0101
	R065 R064 R063 R062 R061 R060	7	0110
	R075 R074 R073 R072 R071 R070	8	0111
	R085 R084 R083 R082 R081 R080	9	1000
	R095 R094 R093 R092 R091 R090	10	1001
	R105 R104 R103 R102 R101 R100	11	1010
	R115 R114 R113 R112 R111 R110	12	1011
	R125 R124 R123 R122 R121 R120	13	1100
	R135 R134 R133 R132 R131 R130	14	1101
	R145 R144 R143 R142 R141 R140	15	1110
	R155 R154 R153 R152 R151 R150	16	1111
	R165 R164 R163 R162 R161 R160	17	Not used
	|	|	
	R315 R314 R313 R312 R311 R310	32	
GREEN	G005 G004 G003 G002 G001 G000	33	0000
	G015 G014 G013 G012 G011 G010	34	0001
	G025 G024 G023 G022 G021 G020	35	0010
	G035 G034 G033 G032 G031 G030	36	0011
	G045 G044 G043 G042 G041 G040	37	0100
	G055 G054 G053 G052 G051 G050	38	0101
	G065 G064 G063 G062 G061 G060	39	0110
	G075 G074 G073 G072 G071 G070	40	0111
	G085 G084 G083 G082 G081 G080	41	1000
	G095 G094 G093 G092 G091 G090	42	1001
	G105 G104 G103 G102 G101 G100	43	1010
	G115 G114 G113 G112 G111 G110	44	1011
	G125 G124 G123 G122 G121 G120	45	1100
	G135 G134 G133 G132 G131 G130	46	1101
	G145 G144 G143 G142 G141 G140	47	1110
	G155 G154 G153 G152 G151 G150	48	1111
	G165 G164 G163 G162 G161 G160	49	Not used
	|	|	
	G635 G634 G633 G632 G631 G630	96	
BLUE	B005 B004 B003 B002 B001 B000	97	0000
	B015 B014 B013 B012 B011 B010	98	0001
	B025 B024 B023 B022 B021 B020	99	0010
	B035 B034 B033 B032 B031 B030	100	0011
	B045 B044 B043 B042 B041 B040	101	0100
	B055 B054 B053 B052 B051 B050	102	0101
	B065 B064 B063 B062 B061 B060	103	0110
	B075 B074 B073 B072 B071 B070	104	0111
	B085 B084 B083 B082 B081 B080	105	1000
	B095 B094 B093 B092 B091 B090	106	1001
	B105 B104 B103 B102 B101 B100	107	1010
	B115 B114 B113 B112 B111 B110	108	1011
	B125 B124 B123 B122 B121 B120	109	1100
	B135 B134 B133 B132 B131 B130	110	1101
	B145 B144 B143 B142 B141 B140	111	1110
	B155 B154 B153 B152 B151 B150	112	1111
	B165 B164 B163 B162 B161 B160	113	Not used
	|	|	
	B315 B314 B313 B312 B311 B310	128	

10 Command

10.1 System function Command List and Description

Table 10.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	10.1.1	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	10.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	10.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	10.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
		1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	10.1.5	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	-	-		-
RDD MADCTL	10.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	-	-		-
RDD COLMOD	10.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0		-
RDDIM	10.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	VSSON	D6	INVON	-	-	GCS2	GCS1	GCS0		-
RDDSM	10.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	TEON	TEM	-	-	-	-	-	-		-

"-": Don't care

Table 10.1.2 System Function command List (2)

Instructio	Refer	D/C	WR	RDX	D17-	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
SLPIN	10.1.10	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	10.1.11	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	10.1.12	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	10.1.13	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	10.1.14	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	10.1.15	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	10.1.16	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	10.1.17	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	10.1.18	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	10.1.19	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦XS≦X
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: S≦XE≦X
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	10.1.20	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦YS≦Y
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end:S≦YE≦Y
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	10.1.21	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RGBSET	10.1.22	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 4k,65k,262k color
		1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000		Red tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red tone “a”
		1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000		Green tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green tone “b”
		1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000		Blue tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue tone “c”
RAMRD	10.1.23	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		Read data

“-“: Don’t care

Table 10.1.3 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PTLAR	10.1.24	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address (0,1,2, ..P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0,1,2, .., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
TEOFF	10.1.25	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.26	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
		1	↑	1	-	-	-	-	-	-	-	-	TEM		Mode1: TEM="0" Mode2: TEM="1"
MADCTL	10.1.27	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-		-
IDMOFF	10.1.28	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	10.1.29	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	10.1.30	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
		1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0		Interface format
RDID1	10.1.31	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	10.1.32	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	10.1.33	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DA to F are for factory use of driver supplier.

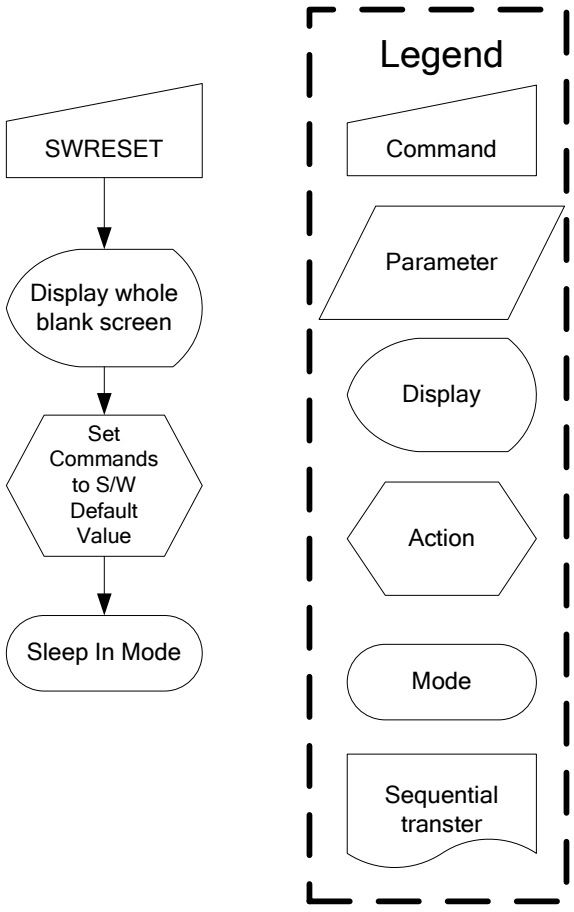
Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).

10.1.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command.												

"-" Don't care

10.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	"-" Don't care -If Software Reset is applied during Sleep In mode, it will be necessary to wait 120msec before sending next command. -The display module loads all default values to the registers during 120msec. -If Software Reset is applied during Sleep Out or Display On Mode, it will be necessary to wait 120msec before sending next command.												
Flow Chart													

10.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rd parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

Description

-This read byte returns 24-bit display identification information.

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

-The 3rd parameter (ID26 to ID20): LCD module/driver version ID

-The 4th parameter (ID37 to UD30): LCD module/driver ID.

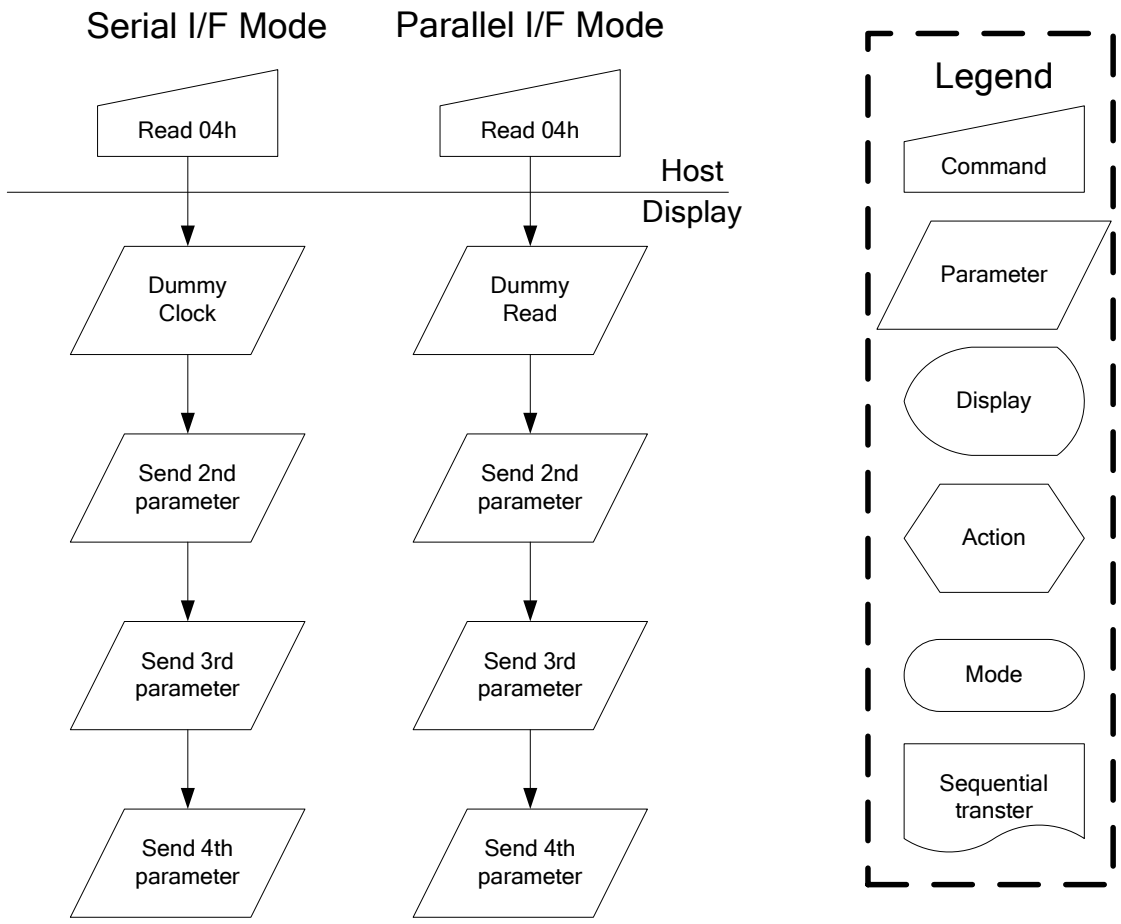
-Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

"-" Don't care

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	-	NV Value	NV Value
S/W Reset	-	NV Value	NV Value
H/W Reset	-	NV Value	NV Value

Flow Chart



10.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th parameter	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th parameter	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0'
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
ST24	For Future Use	'0'
ST23	For Future Use	'0'
IFPF2	Interface Color Pixel Format Definition	"011" = 12-bit / pixel, "101" = 16-bit / pixel, "110" = 18-bit / pixel, others are no define
IFPF1		
IFPF0		
IDMON	Idle Mode On/Off	'1' = On, "0" = Off
PTLON	Partial Mode On/Off	'1' = On, "0" = Off
SLPOUT	Sleep In/Out	'1' = Out, "0" = In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
ST15	Vertical Scrolling Status (Not Used)	'1' = Scroll on,"0" = Scroll off
ST14	Horizontal Scroll Status (Not Used)	'0'
INVON	Inversion Status	'1' = On, "0" = Off
ST12	All Pixels On (Not Used)	'0'
ST11	All Pixels Off (Not Used)	'0'

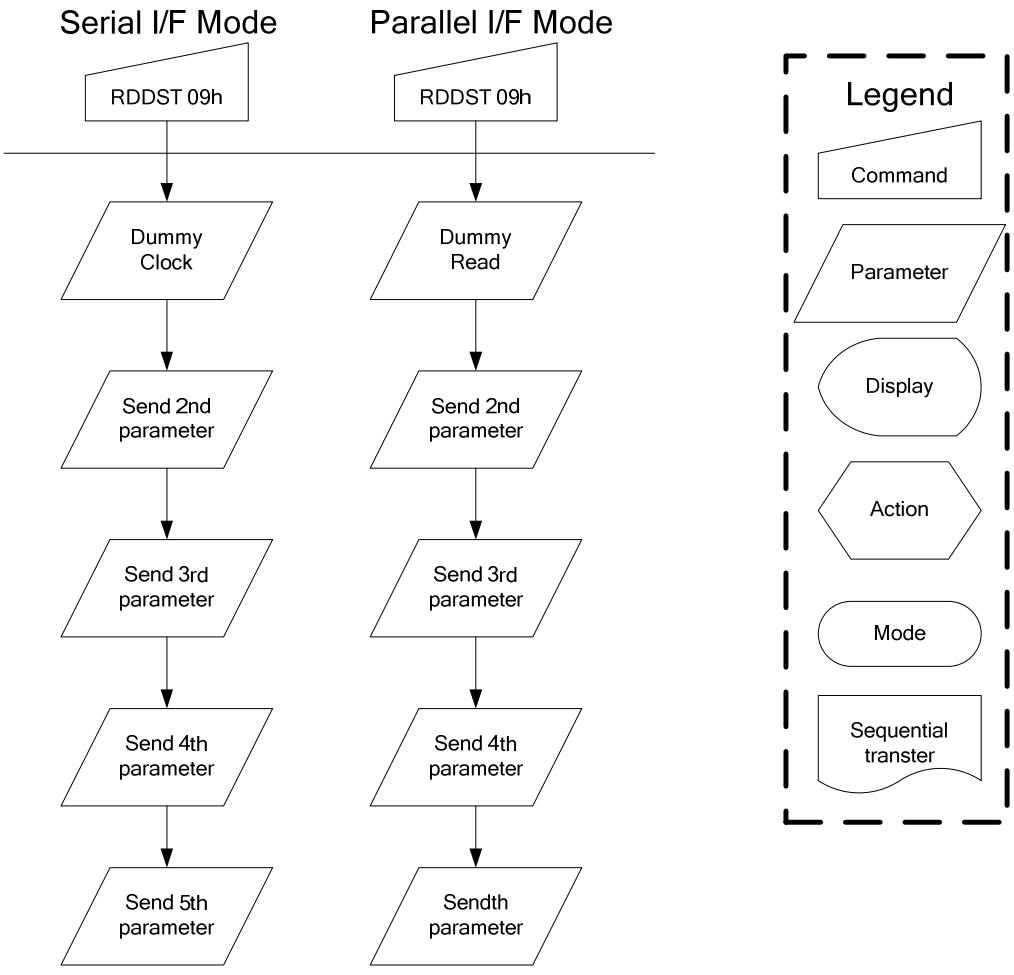
DISON	Display On/Off	'1' = On, "0" = Off
TEON	Tearing effect line on/off	'1' = On, "0" = Off
GCSEL2	Gamma Curve Selection	"000" = GC0
GCSEL1		"001" = GC1
GCSEL0		"010" = GC2 "011" = GC3 "100" to "111" = Not defined
TEM	Tearing effect line mode	'0' = mode1, '1' = mode2
ST4	For Future Use	'0'
ST3	For Future Use	'0'
ST2	For Future Use	'0'
ST1	For Future Use	'0'
ST0	For Future Use	'0'

"-" Don't care

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx0xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart



10.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

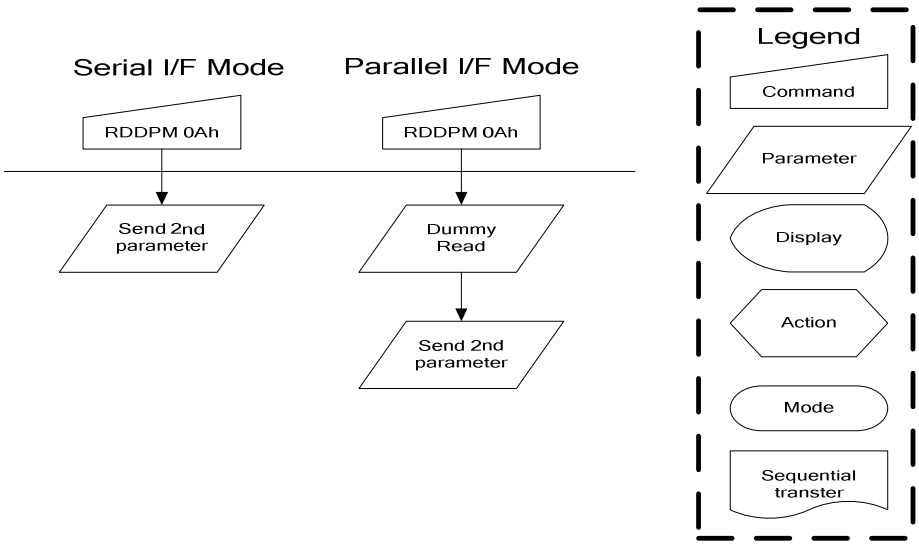
"-" Don't care

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
DISON	Display On/Off	'1' = Display On, '0' = Display Off
D1	Not Used	'0'
D0	Not Used	'0'

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000(08h)
S/W Reset	0000_1000(08h)
H/W Reset	0000_1000(08h)

Flow Chart



10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑		MY	MX	MV	ML	RGB	MH	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

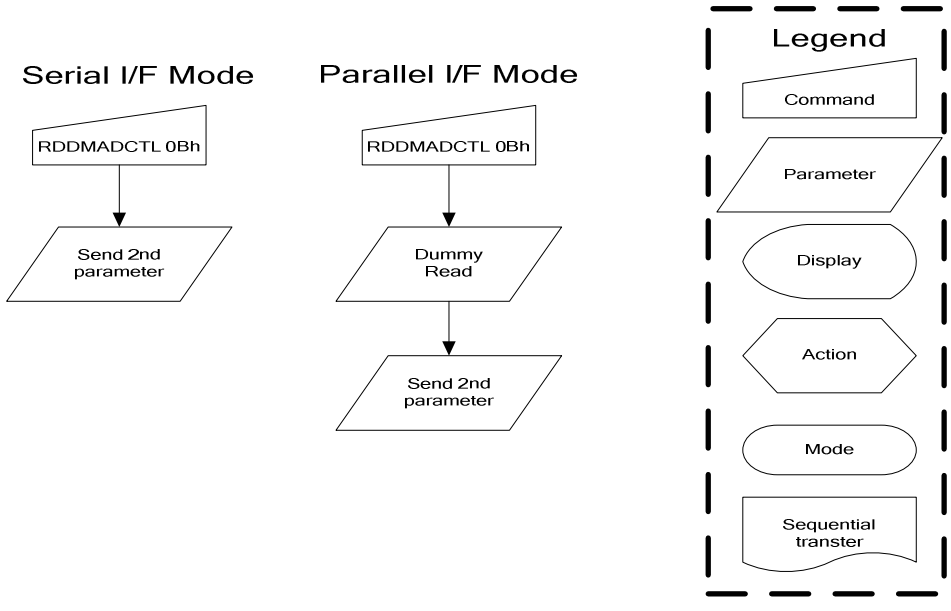
"-" Don't care

Bit	Description	Value
MX	Column Address Order	'1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')
MY	Row Address Order	'1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')
MV	Row/Column Order (MV)	'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)
ML	Vertical Refresh Order	'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom
RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left
D1	Not Used	'0'
D0	Not Used	'0'

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

Flow Chart



10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0	

Description

This command indicates the current status of the display as described in the table below:

IFPF[2:0]	MCU Interface Color Format
011	12-bit/pixel
101	16-bit/pixel
110	18-bit/pixel
111	No used

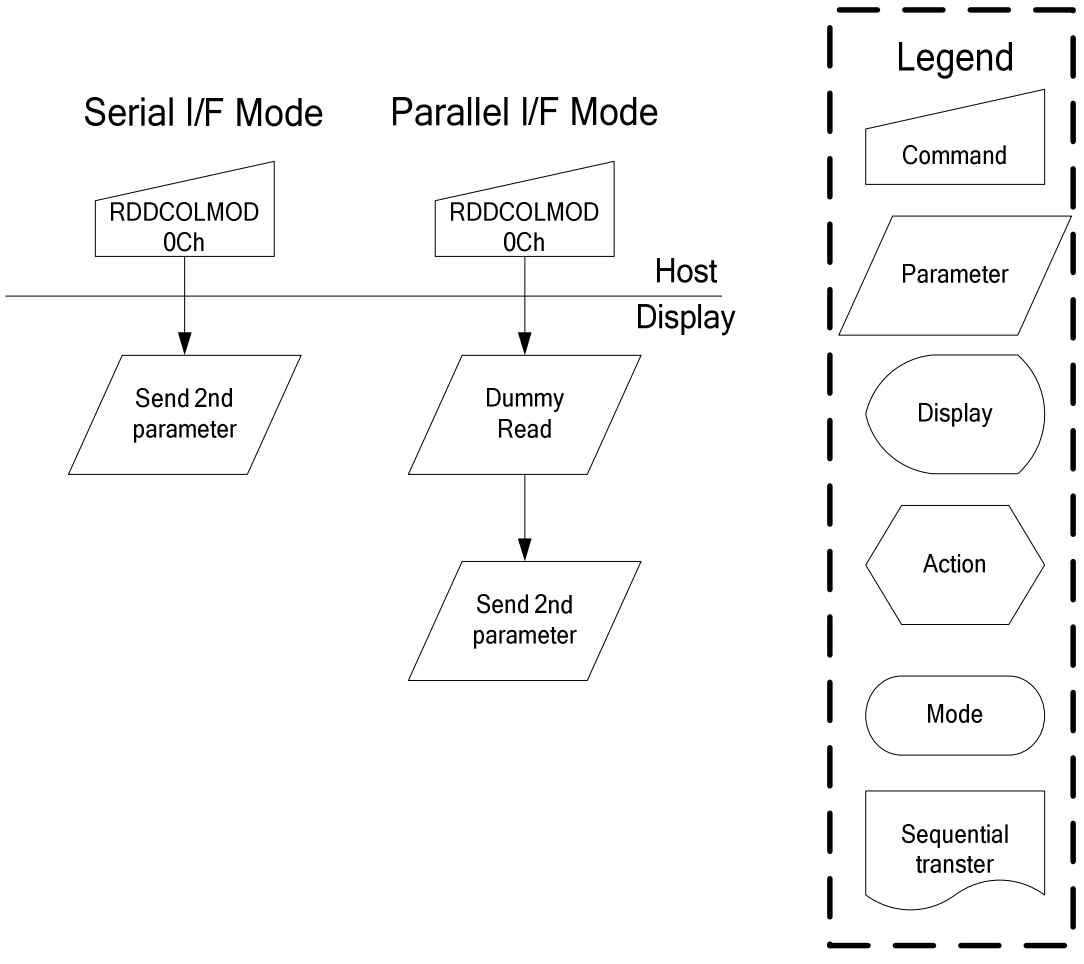
Others are no define and invalid

"-" Don't care

Default

Status	Default Value
	IFPF[2:0]
Power On Sequence	0110 (18 bits/pixel)
S/W Reset	No Change
H/W Reset	0110 (18 bits/pixel)

Flow Chart



10.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (0Dh): Read Display Image Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	

Description

This command indicates the current status of the display as described in the table below:

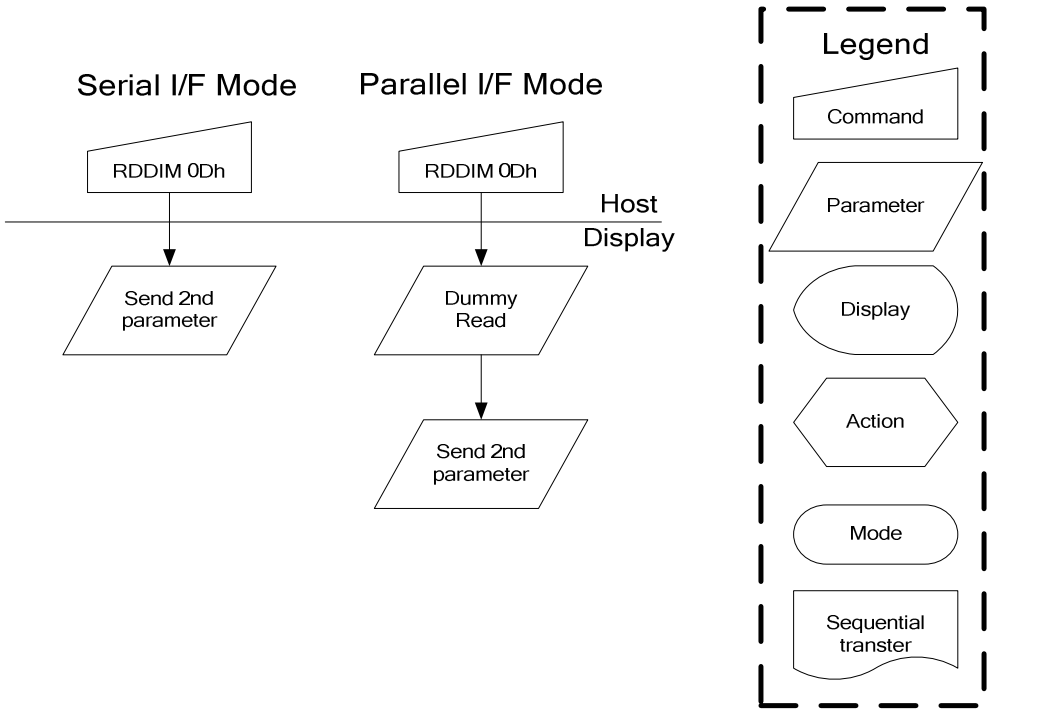
"-" Don't care

Bit	Description	Value
VSSON	Reversed	"0"
D6	Reversed	"0"
INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
GCS2 GCS1 GCS0	Gamma Curve Selection	"000" = GC0, "001" = GC1, "010" = GC2, "011" = GC3, "100" to "111" = Not defined

Default

Status	Default Value(D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



10.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (0Eh): Read Display Signal Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	TEON	TEM	D5	D4	D3	D2	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

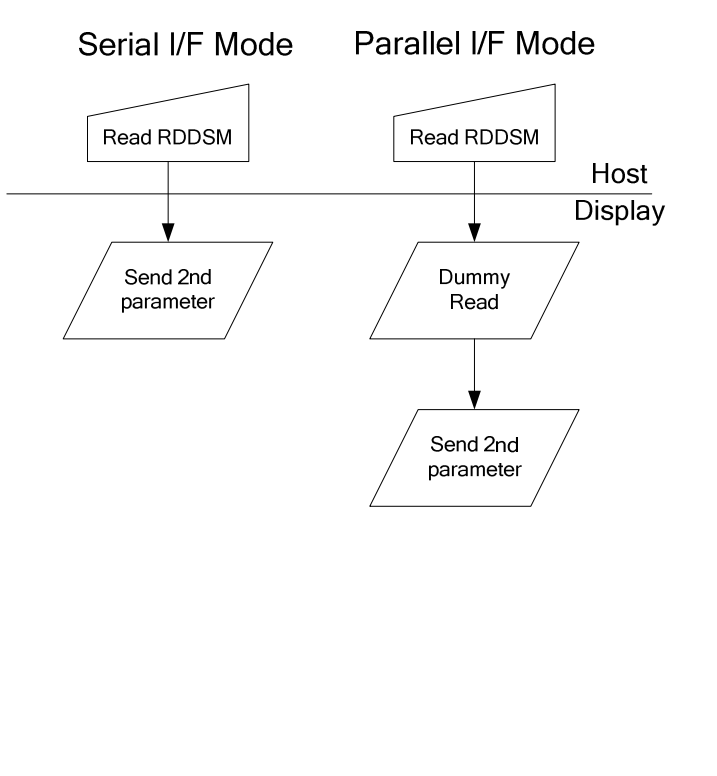
"-" Don't care

Bit	Description	Value
TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
TEM	Tearing effect line mode	"1" = mode2, "0" = mode1
D5	Not Used	"1" = On, "0" = Off
D4	Not Used	"1" = On, "0" = Off
D3	Not Used	"1" = On, "0" = Off
D2	Not Used	"1" = On, "0" = Off
D1	Not Used	"1" = On, "0" = Off
D0	Not Used	"1" = On, "0" = Off

Default

Status	Default Value(D7~D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDSM
Read RDDSM
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

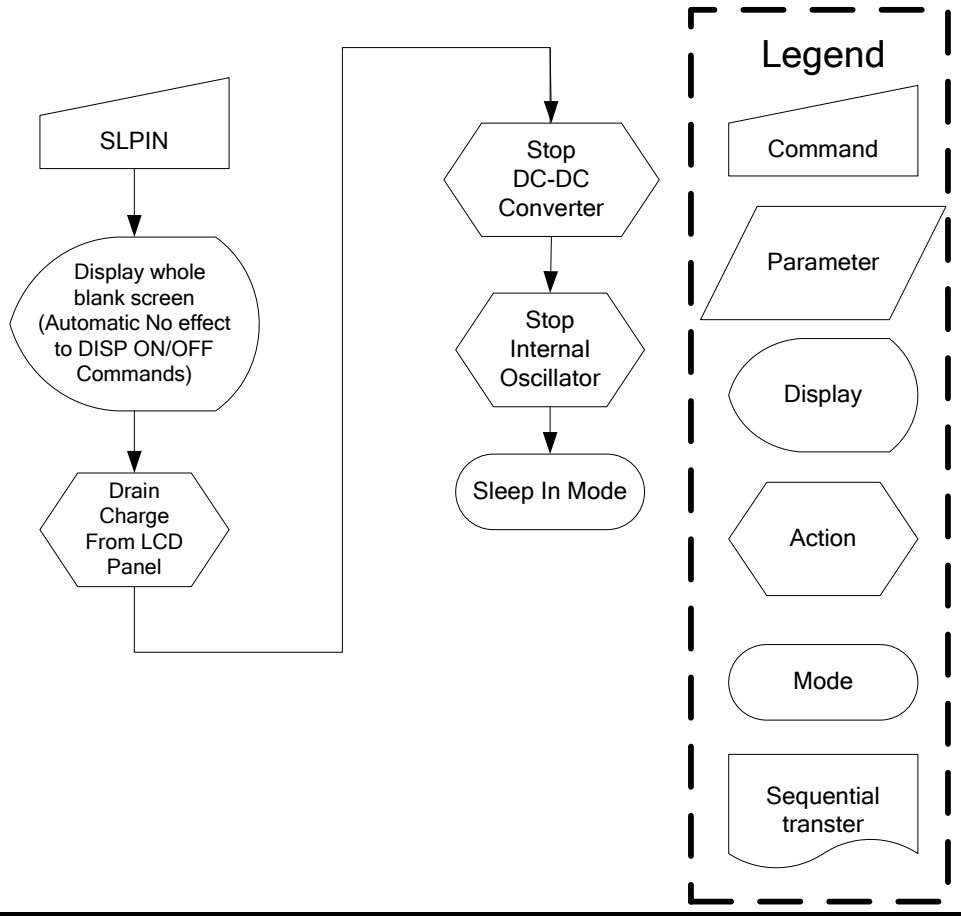
10.1.10 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
Parameter	No Parameter												-
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.												
Restriction	-This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). -When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.												

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart



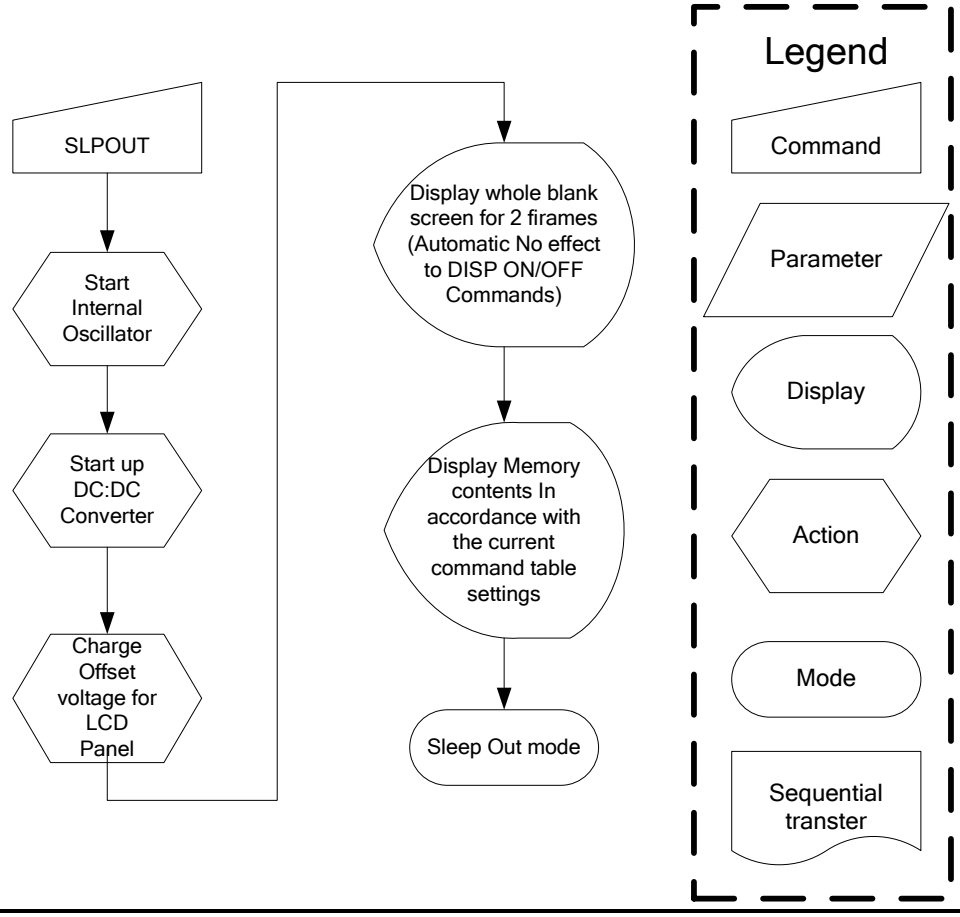
10.1.11 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
Parameter	No Parameter												-
Description	-This command turns off sleep mode. -In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.												
Restriction	-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). -When IC is in Sleep In mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits. -When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command due to the download of default value of registers and the execution of self-diagnostic function.												

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart



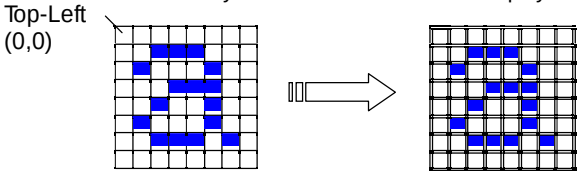
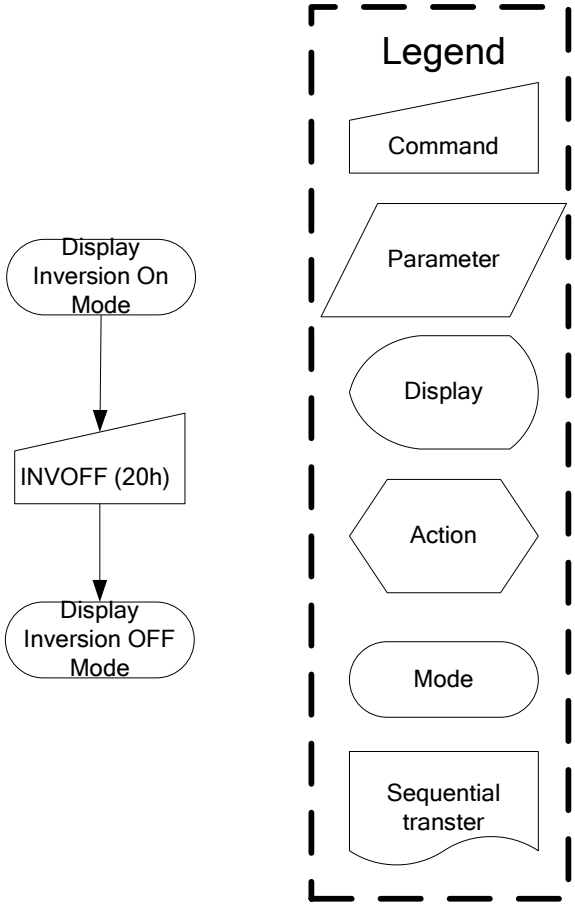
10.1.12 PTLON (12h): Partial Display Mode On

<table>
<tr><th>12H</th><th colspan="13">PTLON (12h): Partial Display Mode On</th></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>PTLON</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(12h)</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)
-To leave Partial mode, the Normal Display Mode On command (13h) should be written.
“-“ Don’t care</td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

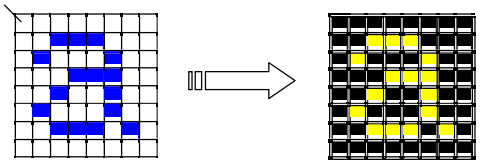
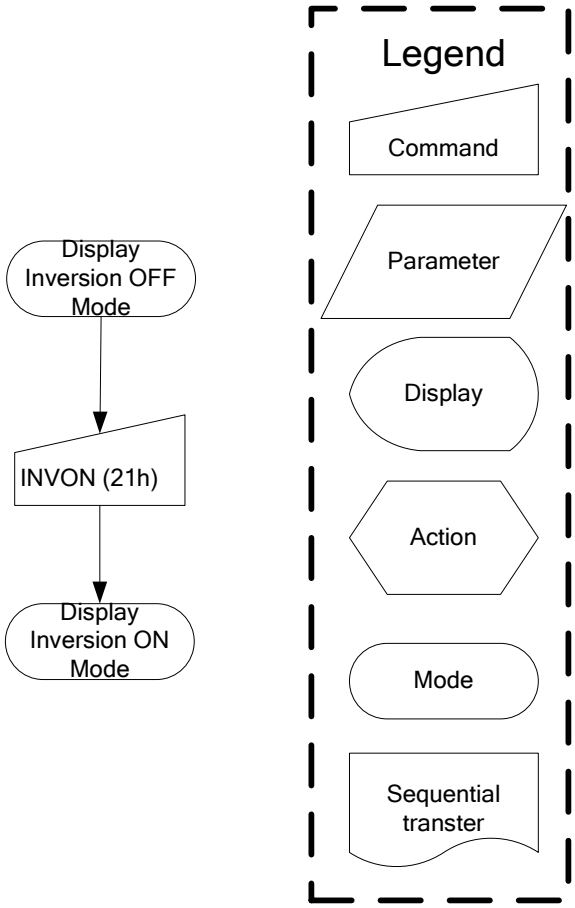
10.1.13 NORON (13h): Normal Display Mode On

<table>
<tr><th>13H</th><th colspan="13">NORON (Normal Display Mode On)</th></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>NORON</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(13h)</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">-This command returns the display to normal mode.
-Normal display mode on means Partial mode off.
-Exit from NORON by the Partial mode On command (12h)
“-“ Don’t care</td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area Definition Descriptions for details of when to use this command</td></tr>
</table>

10.1.14 INVOFF (20h): Display Inversion Off

20H	IVNOFF (Normal Display Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
Parameter	No Parameter												-
Description	-This command is used to recover from display inversion mode. "-" Don't care (Example) Memory Display Top-Left (0,0) 												
Default	Status: Power On Sequence — Default Value: Display Inversion off Status: S/W Reset — Default Value: Display Inversion off Status: H/W Reset — Default Value: Display Inversion off												
Flow Chart													

10.1.15 INVON (21h): Display Inversion On

21H	IVNOFF (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
Parameter	No Parameter												-
Description	-This command is used to enter into display inversion mode -To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. "-" Don't care (Example) Memory Top-Left (0,0) Display 												
Default	Status / Default Value Power On Sequence: Display Inversion off S/W Reset: Display Inversion off H/W Reset: Display Inversion off												
Flow Chart													

10.1.16 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
Parameter	1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0	

Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

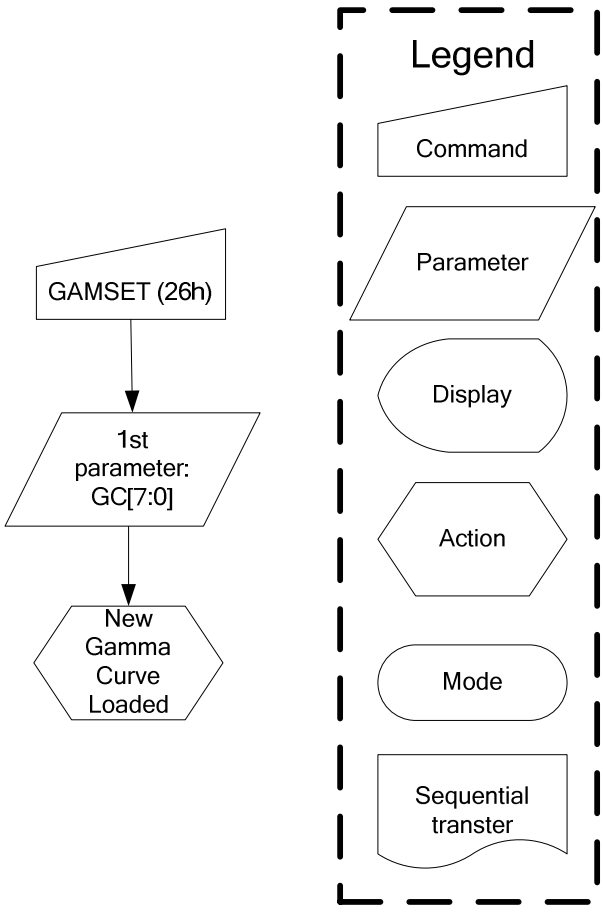
GC [7:0]	Parameter	Curve Selected	
		GS=1	GS=0
01h	GC0	Gamma Curve 1 (G2.2)	Gamma Curve 1 (G1.0)
02h	GC1	Gamma Curve 2 (G1.8)	Gamma Curve 2 (G2.5)
04h	GC2	Gamma Curve 3 (G2.5)	Gamma Curve 3 (G2.2)
08h	GC3	Gamma Curve 4 (G1.0)	Gamma Curve 4 (G1.8)

Note: All other values are undefined.

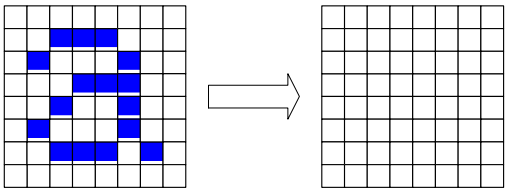
Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



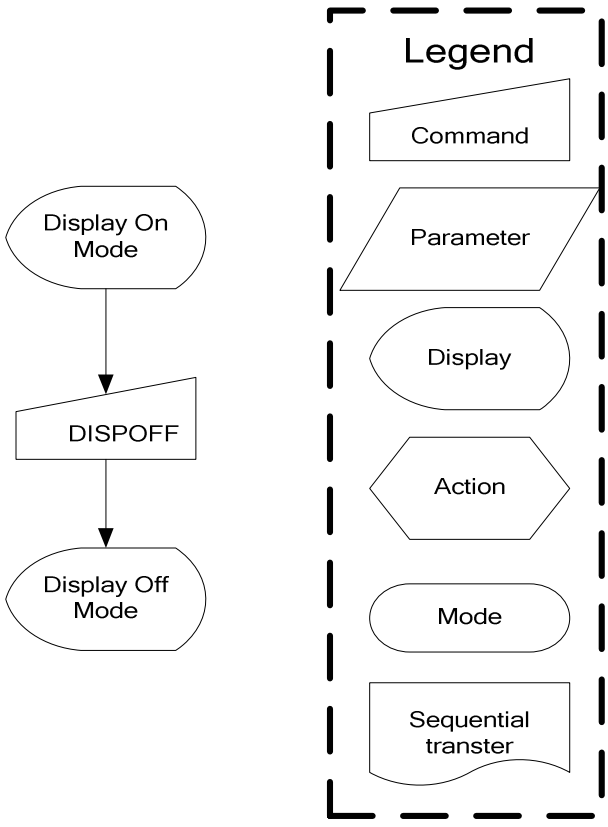
10.1.17 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter												-
Description	- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h) **(Example)** **Memory** **Display** 												

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



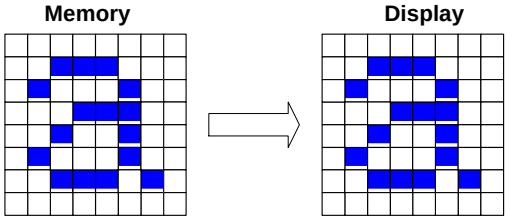
10.1.18 DISPON (29h): Display On

29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
Parameter	No Parameter												-

Description

- This command is used to recover from DISPLAY OFF mode.
- Output from the Frame Memory is enabled.
- This command makes no change of contents of frame memory.
- This command does not change any other status.

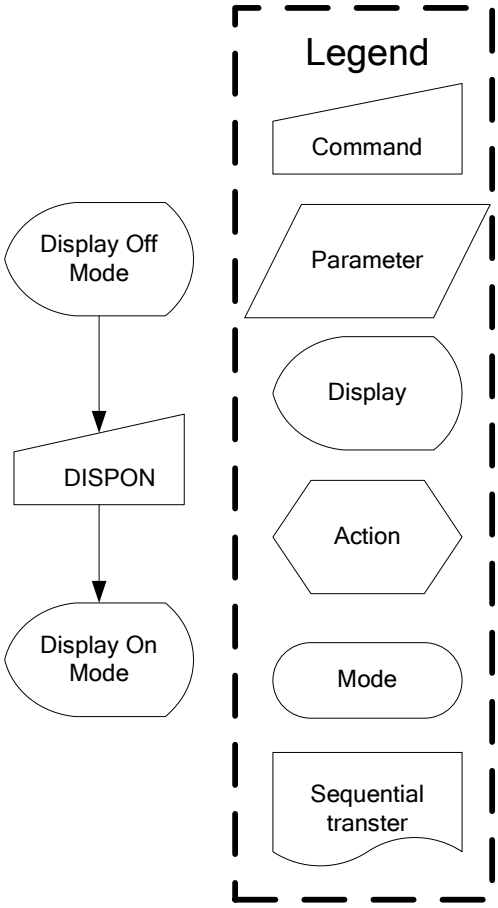
(Example)



Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



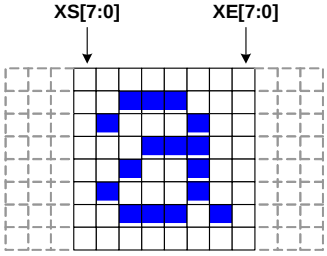
10.1.19 CASET (2Ah): Column Address Set

2AH	CASET(Column Address Set)_												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET(2Ah)	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2nd parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3rd parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

Description

-The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.

-Each value represents one column line in the Frame Memory.



Restriction

XS [15:0] always must be equal to or less than XE [15:0]

When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '11')

(Parameter range: 0 < XS [15:0] < XE [15:0] < 127 (007Fh)): MV="0")

(Parameter range: 0 < XS [15:0] < XE [15:0] < 159 (009Fh)): MV="1")

2. 132X162 memory base (GM = '00')

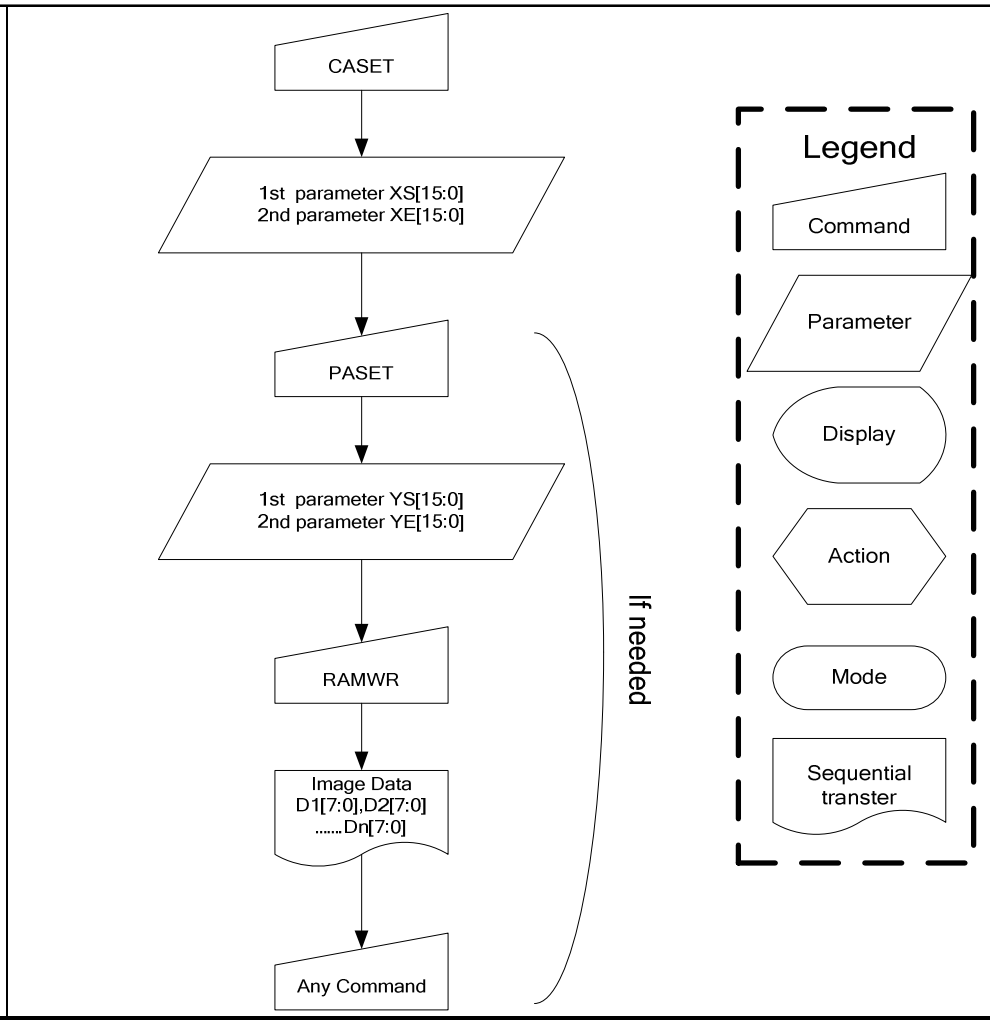
(Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV="0")

(Parameter range: 0 < XS [15:0] < XE [15:0] < 161 (00A1h)): MV="1")

Default

GM Status	Status	Default Value		
		XS [7:0]	XE [7:0] (MV='0 ')	XE [7:0] (MV='1')
GM='11' (128x160 memory base)	Power On Sequence	0000h	007Fh (127)	
	S/W Reset	0000h	007Fh (127)	009Fh (159)
	H/W Reset	0000h	007Fh (127)	
GM='00' (132x162 memory base)	Power On Sequence	0000h	0083h (131)	
	S/W Reset	0000h	0083h (131)	00A1h (161)
	H/W Reset	0000h	0083h (131)	

Flow Chart


CASET
1st parameter XS[15:0]
2nd parameter XE[15:0]
PASET
1st parameter YS[15:0]
2nd parameter YE[15:0]
RAMWR
Image Data
D1[7:0],D2[7:0]
.....Dn[7:0]
Any Command
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

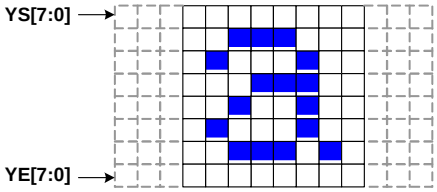
10.1.20 RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET (2Bh)	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

Description

The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes.

Each value represents one column line in the Frame Memory.



Restriction

YS [15:0] always must be equal to or less than YE [15:0]

When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '11')

(Parameter range: 0 < YS [15:0] < YE [15:0] < 159 (009Fh)): MV="0"

(Parameter range: 0 < YS [15:0] < YE [15:0] < 127 (007Fh)): MV="1"

2. 132X162 memory base (GM = '00')

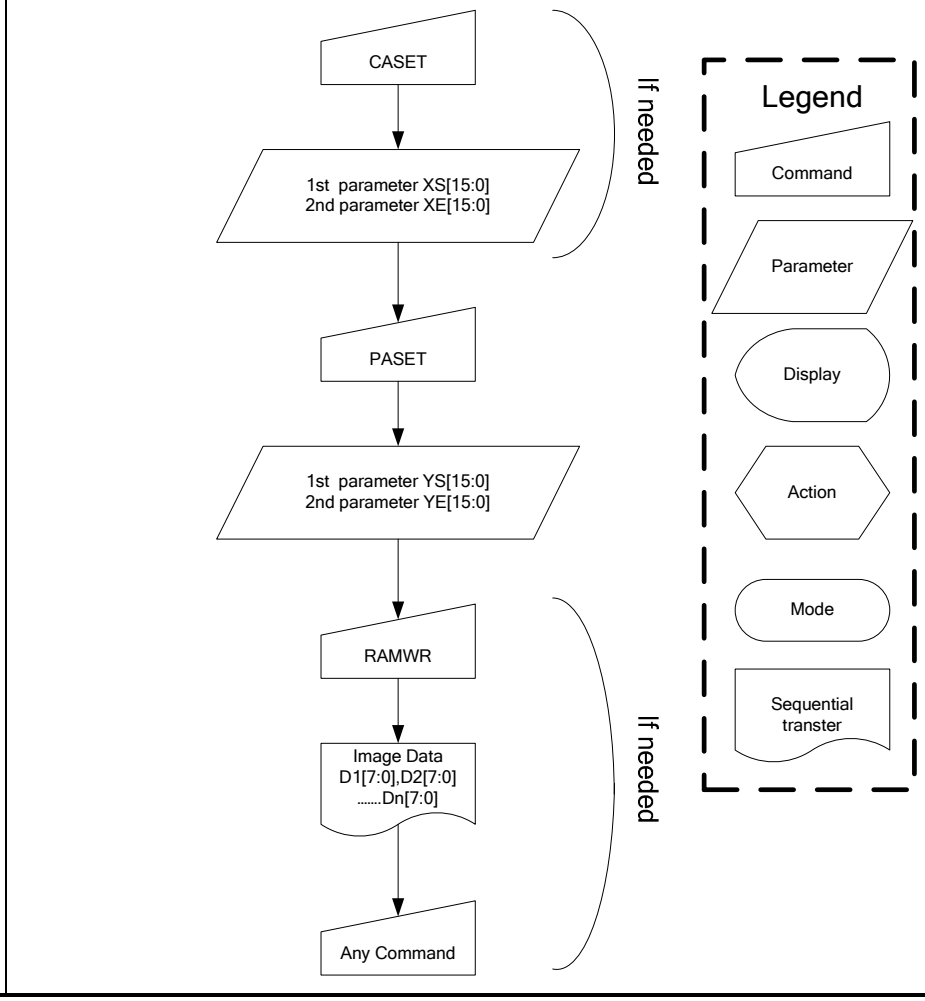
(Parameter range: 0 < YS [15:0] < YE [15:0] < 161 (00A1h)): MV="0"

(Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (0083h)): MV="1"

Default

GM status	Status	Default Value		
		YS [15:0]	YE [15:0] (MV='0 ')	YE [15:0] (MV='1')
GM='11' (128x160 memory base)	Power On Sequence	0000h	009Fh (159)	
	S/W Reset	0000h	009Fh (159)	007Fh (127)
	H/W Reset	0000h	009Fh (159)	
GM='00' (132x162 memory base)	Power On Sequence	0000h	00A1h (161)	
	S/W Reset	0000h	00A1h (161)	0083h (131)
	H/W Reset	0000h	00A1h (161)	

Flow Chart


CASET
1st parameter XS[15:0]
2nd parameter XE[15:0]
PASET
1st parameter YS[15:0]
2nd parameter YE[15:0]
RAMWR
Image Data
D1[7:0],D2[7:0]
.....Dn[7:0]
Any Command
If needed
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

10.1.21 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
|	1	↑	1	|	|	|	|	|	|	|	|	|	
Nth parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	

Description

In all color modes, there is no restriction on length of parameters.

1. 128X160 memory base (GM = '11')

128x160x18-bit memory can be written by this command

Memory range: (0000h, 0000h) -> (007Fh, 09Fh)

2. 132x162 memory base (GM = '00')

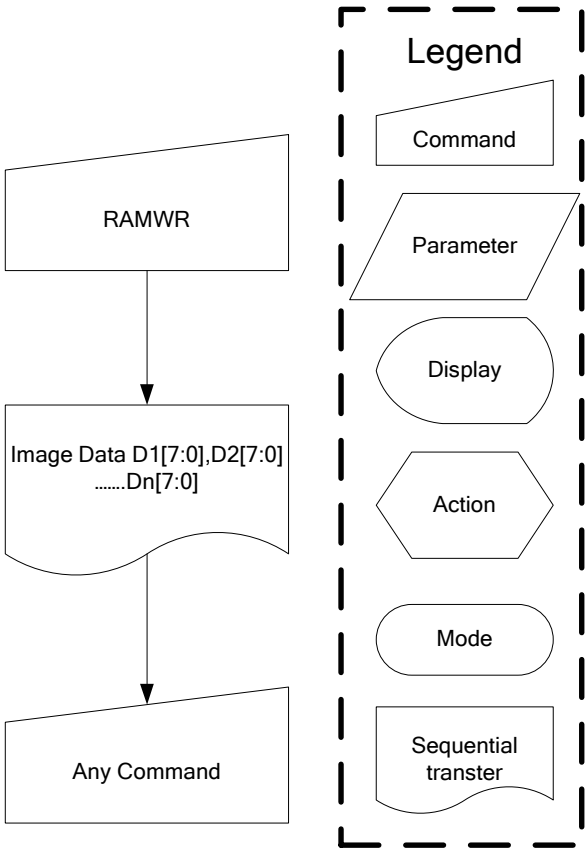
132x162x18-bit memory can be written on this command.

Memory range: (0000h, 0000h) -> (0083h, 00A1h)

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



10.1.22 RGBSET (2Dh): Color Setting for 4K, 65K and 262K

2DH	RGBSET (Color Set for 4K, 65K, 262K and 16.7M)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)
1st parameter	1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000	
|	1	↑	1	-	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	
|	1	↑	1	-	-	-	R315	R314	R313	R312	R311	R310	
|	1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000	
|	1	↑	1	-	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	
|	1	↑	1	-	-	-	G635	G634	G633	G632	G631	G630	
|	1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000	
|	1	↑	1	-	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	
128th parameter	1	↑	1	-	-	-	B315	B314	B313	B312	B311	B310	

Description

This command is used to define the LUT for 12bits-to-16bits / 16-bit-to- 18bits color depth conversations.

128-Bytes must be written to the LUT regardless of the color mode. Only the values in Section 9.18 are referred.

In this condition, 4K-color (4-4-4) and 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table.

This command has no effect on other commands/parameters and Contents of frame memory.

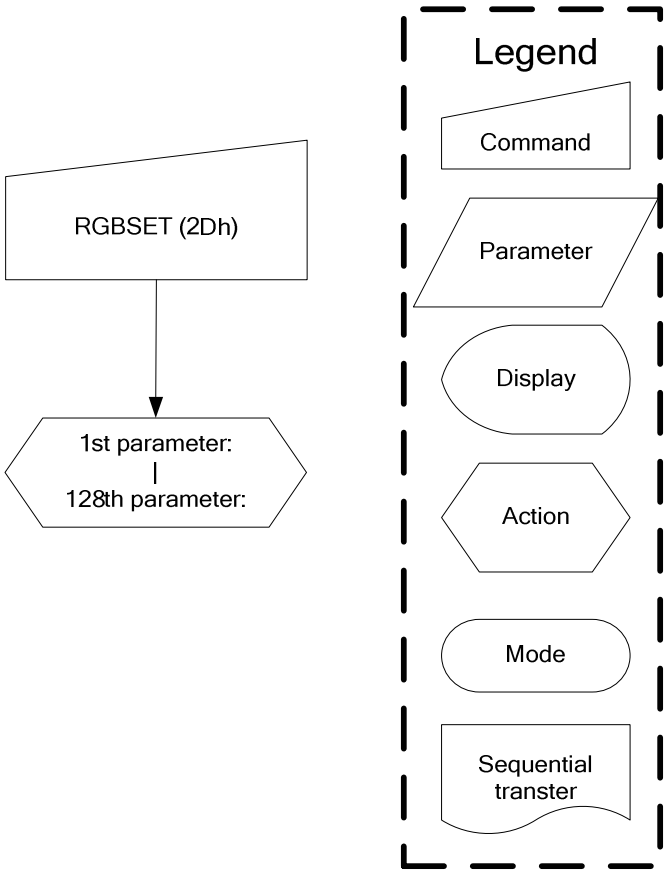
Visible change takes effect next time the Frame Memory is written to.

Do not send any command before the last data is sent or LUT is not defined correctly.

Default

Status	Default Value
Power On Sequence	Random
S/W Reset	Contents of the look-up table protected
H/W Reset	Random

Flow Chart



10.1.23 RAMRD (2Eh): Memory Read

2EH	RAMHD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
|	1	1	↑	|	|	|	|	|	|	|	|	|	
(N+1)th parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	

Description

-This command is used to transfer data from frame memory to MCU.

-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

-The Start Column/Start Row positions are different in accordance with MADCTL setting.

-Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 9.10

-Frame Read can be cancelled by sending any other command.

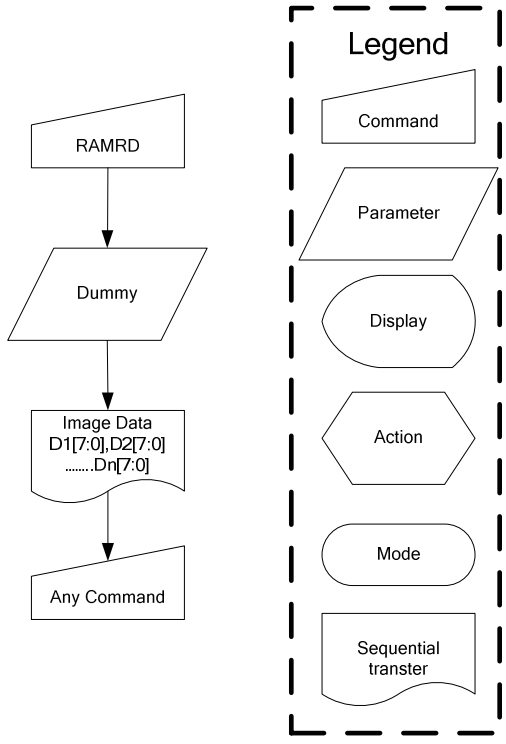
-The data color coding is fixed to 18-bit in reading function. Please see section 9.8 “Data color coding” for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.

Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



10.1.24 PTLAR (30h): Partial Area

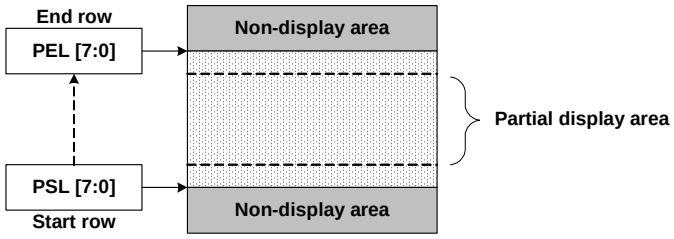
30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2nd parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3rd parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

Description

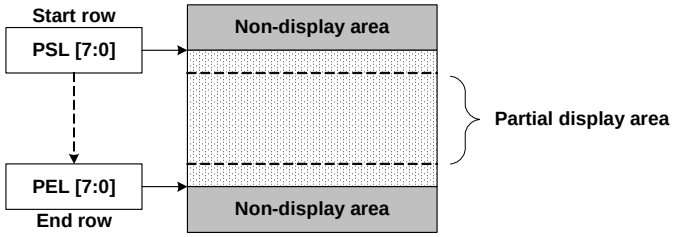
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

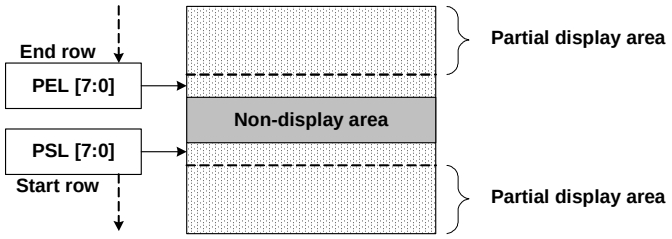
-If End Row > Start Row, when MADCTL ML='0'



-If End Row > Start Row, when MADCTL ML='1'



-If End Row < Start Row, when MADCTL ML='0'

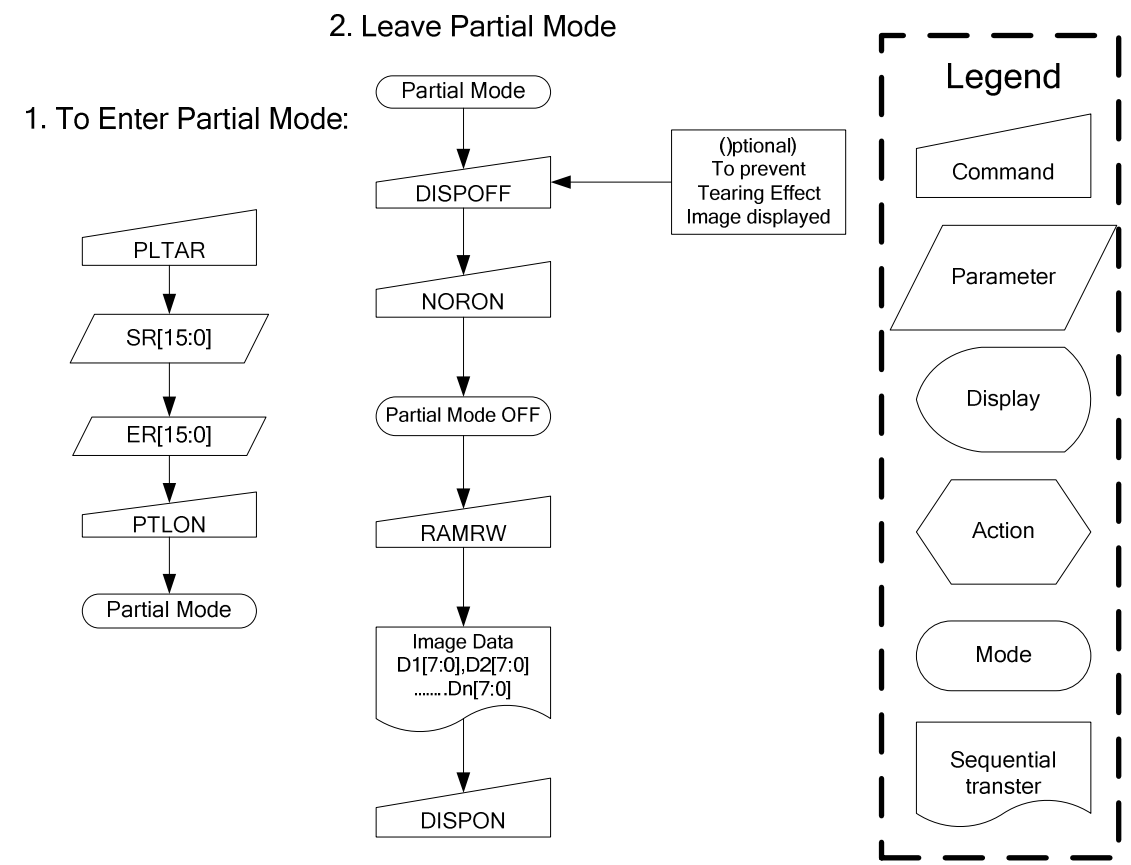


-If End Row = Start Row then the Partial Area will be one row deep.

Default

Status	Default Value		
	PSL [15:0]	PEL [15:0]	
GM[1:0]	"xx"	GM[1:0]="11"	GM[1:0]="00"
Power On Sequence	0000h	009Fh	00A1h
S/W Reset	0000h	009Fh	00A1h
H/W Reset	0000h	009Fh	00A1h

Flow Chart


2. Leave Partial Mode
1. To Enter Partial Mode:
PLTAR
SR[15:0]
ER[15:0]
PTLON
Partial Mode
Partial Mode
DISPOFF
NORON
Partial Mode OFF
RAMRW
Image Data
D1[7:0],D2[7:0]
.....Dn[7:0]
DISPON
()ptional)
To prevent
Tearing Effect
Image displayed
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

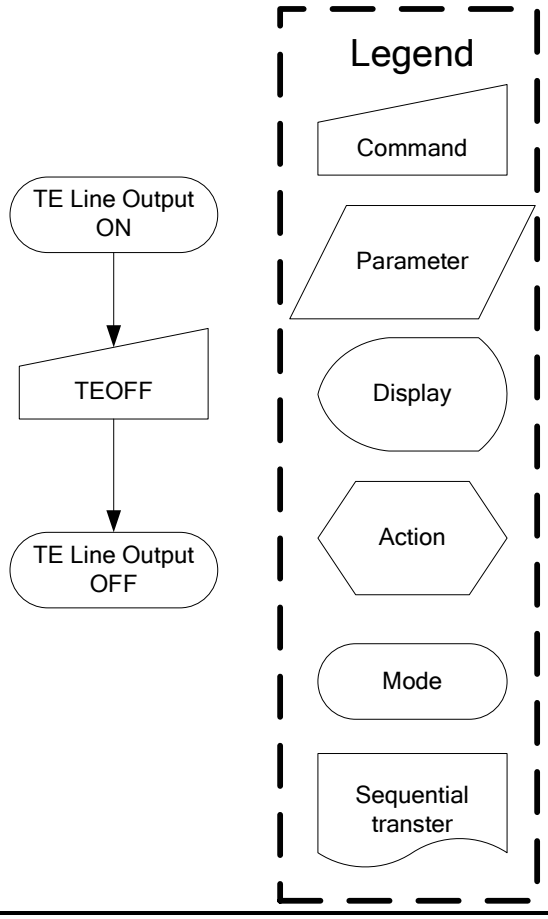
10.1.25 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
Parameter	No Parameter												-
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

Flow Chart



10.1.26 TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	-	0	0	0	0	0	0	0	TEM	

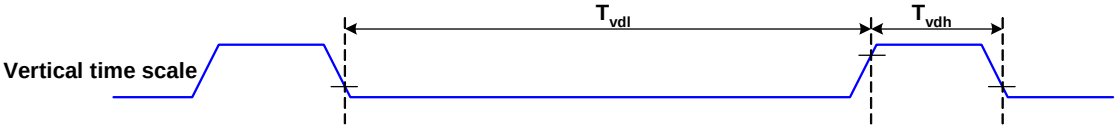
Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

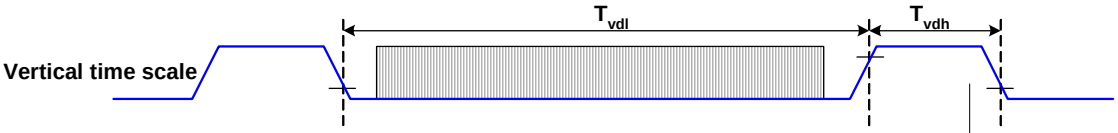
-This output is not affected by changing MADCTL bit ML.

-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:

-When TEM ='0': The Tearing Effect output line consists of V-Blanking information only



-When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information

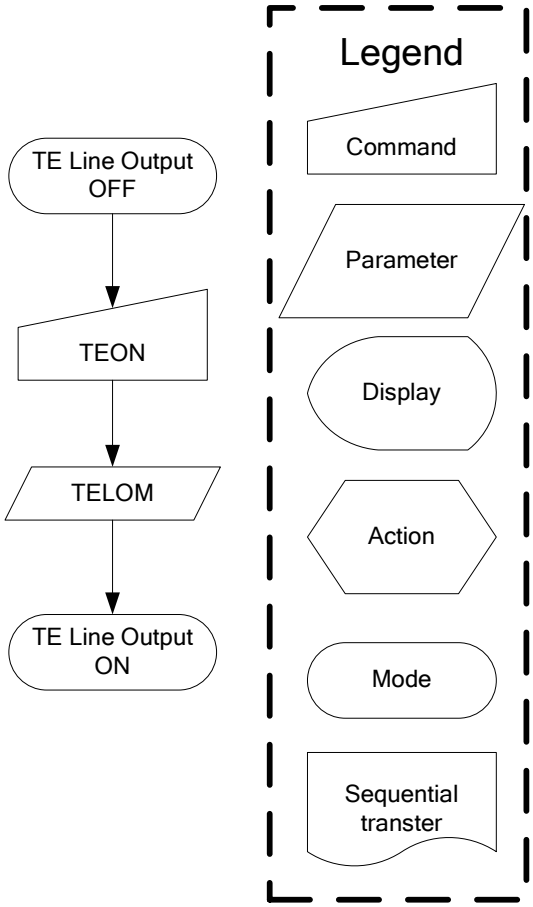


Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Default

Status	Default Value
Power On Sequence	Tearing effect off & TEM=0
S/W Reset	Tearing effect off & TEM=0
H/W Reset	Tearing effect off & TEM=0

Flow Chart



10.1.27 MADCTL (36h): Memory Data Access Control

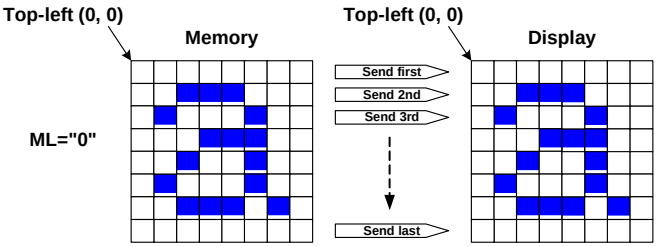
36H	MADCTL (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-	

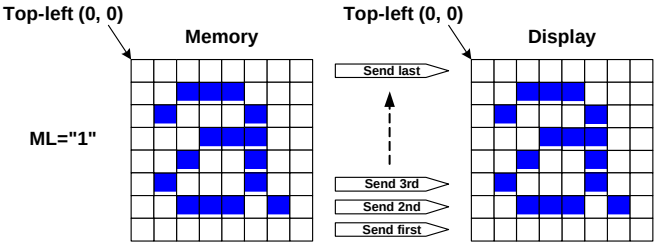
Description

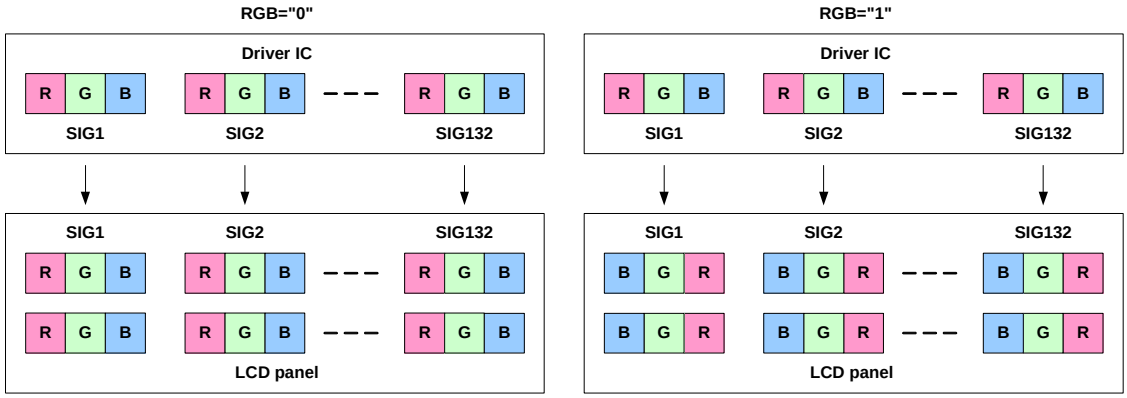
-This command defines read/ write scanning direction of frame memory.

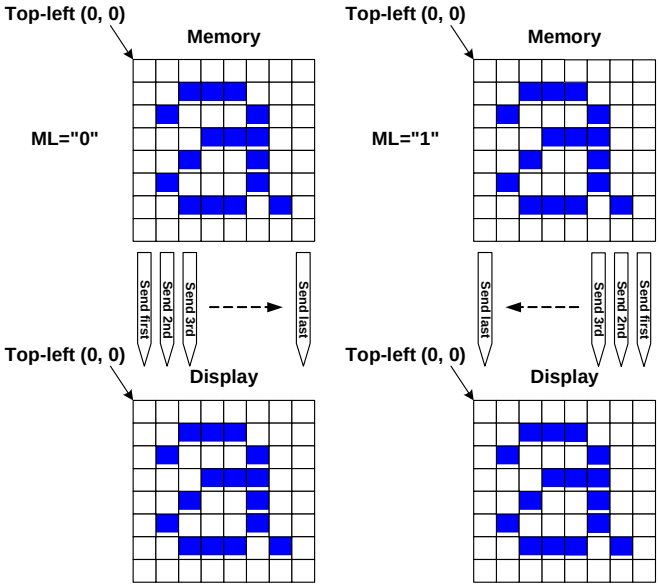
Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)
MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left

-Bit Assignment





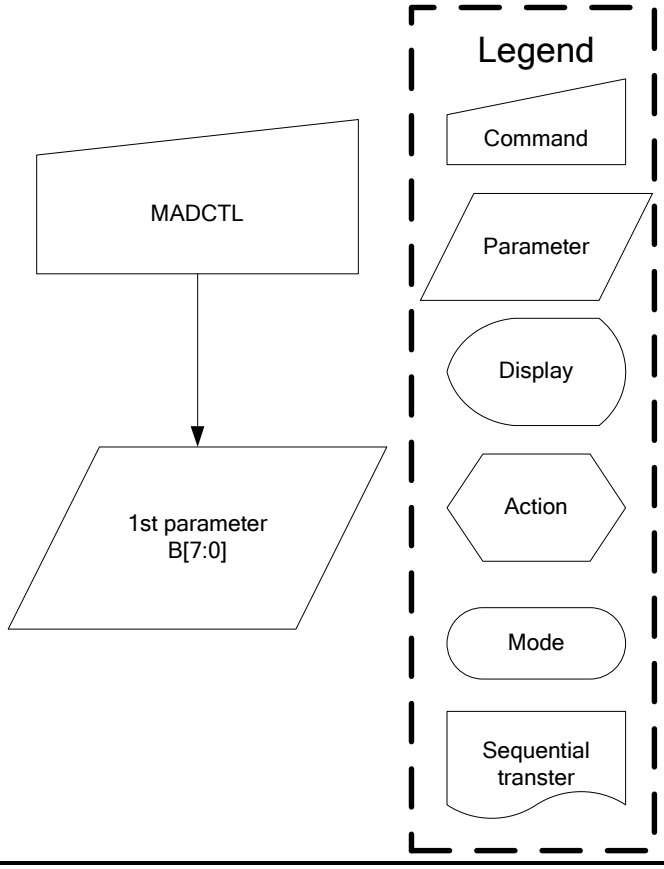




Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0

Flow Chart



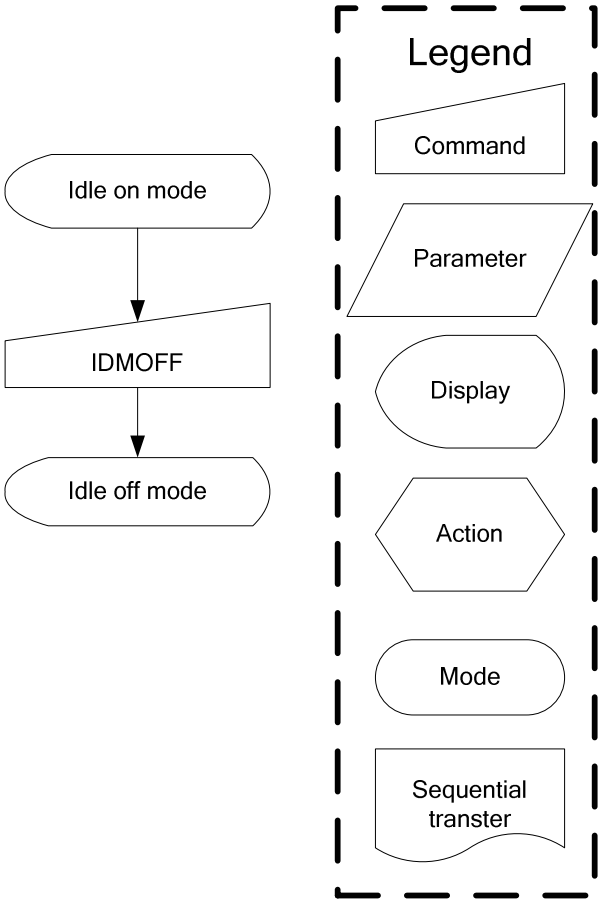
10.1.28 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter												-
Description	-This command is used to recover from Idle mode on. -In the idle off mode, 1. LCD can display 4096, 65k or 262k colors. 2. Normal frame frequency is applied.												

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



10.1.29 IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
Parameter	No Parameter												-

Description

-This command is used to enter into Idle mode on.

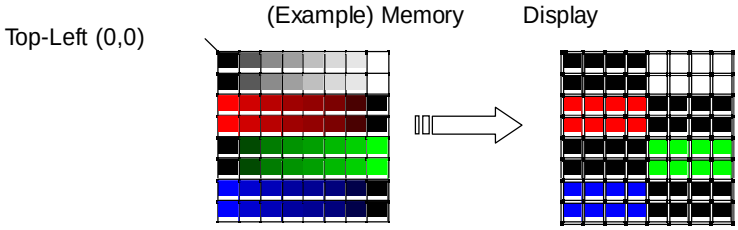
-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.

2. 8-Color mode frame frequency is applied.

3. Exit from IDMON by Idle Mode Off (38h) command



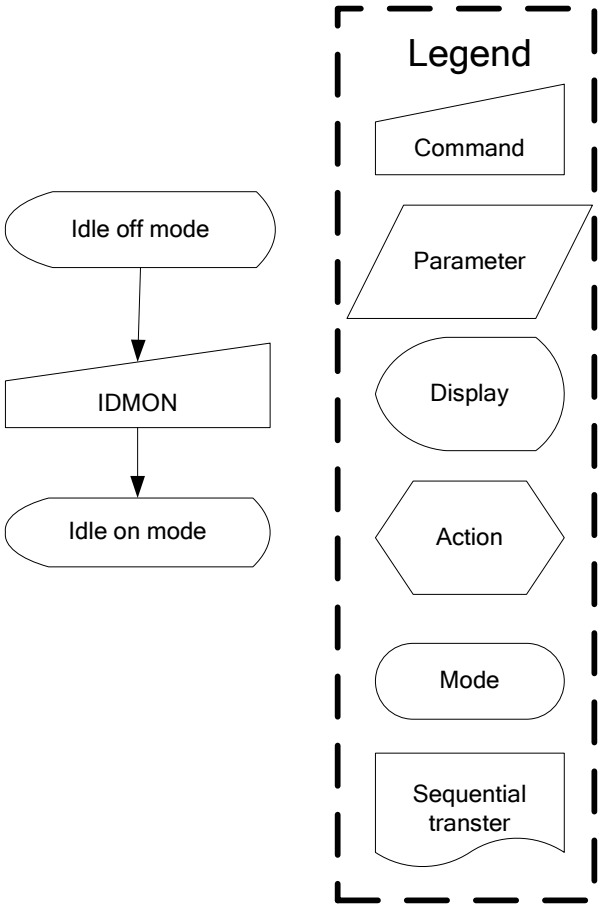
Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart	 Idle off mode IDMON Idle on mode Legend Command Parameter Display Action Mode Sequential transter

10.1.30 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (3Ah): Interface Pixel Format												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0	

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:

IFPF[2:0]		MCU Interface Color Format
011	3	12-bit/pixel
101	5	16-bit/pixel
110	6	18-bit/pixel
111	7	No used

Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

Note2: The Command 3Ah should be set at 55h when writing 16-bit/pixel data into frame memory, but 3Ah should be re-set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.

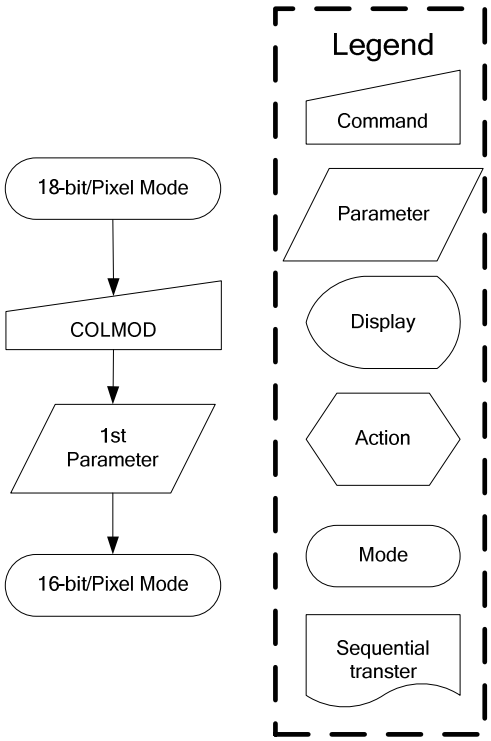
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value	
	IFPF[2:0]	VIPF[3:0]
Power On Sequence	0110(18-bit/Pixel)	0110(18-bit/Pixel)
S/W Reset	No Change	No Change
H/W Reset	0110(18-bit/Pixel)	0110(18-bit/Pixel)

Flow Chart



10.1.31 RDID1 (DAh): Read ID1 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	

Description

-This read byte returns 8-bit LCD module's manufacturer ID

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

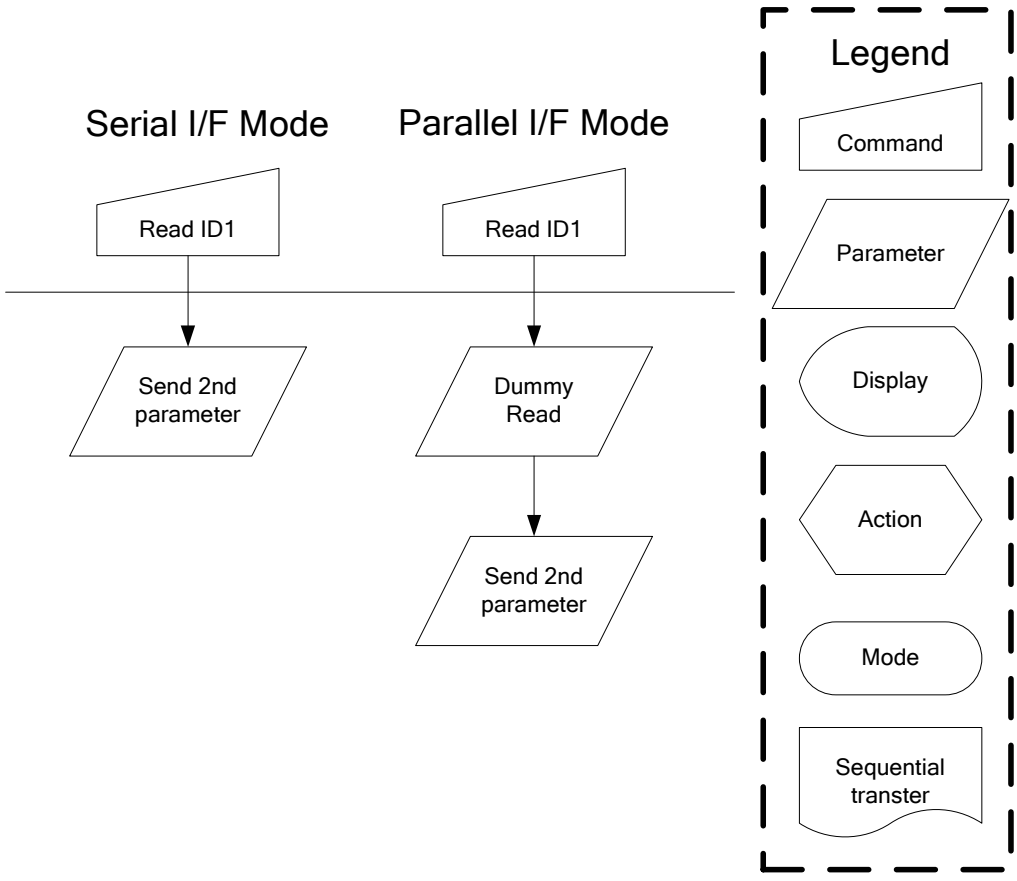
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



10.1.32 RDID2 (DBh): Read ID2 Value

DBH	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

Description

-This read byte returns 8-bit LCD module/driver version ID

-The 1st parameter is dummy data

-The 2nd parameter (ID26 to ID20): LCD module/driver version ID

-Parameter Range: ID=80h to FFh

ID26 to ID20	Version	Changes
80h		
81h		
82h		
83h		

NOTE: See command RDDID (04h), 3rd parameter.

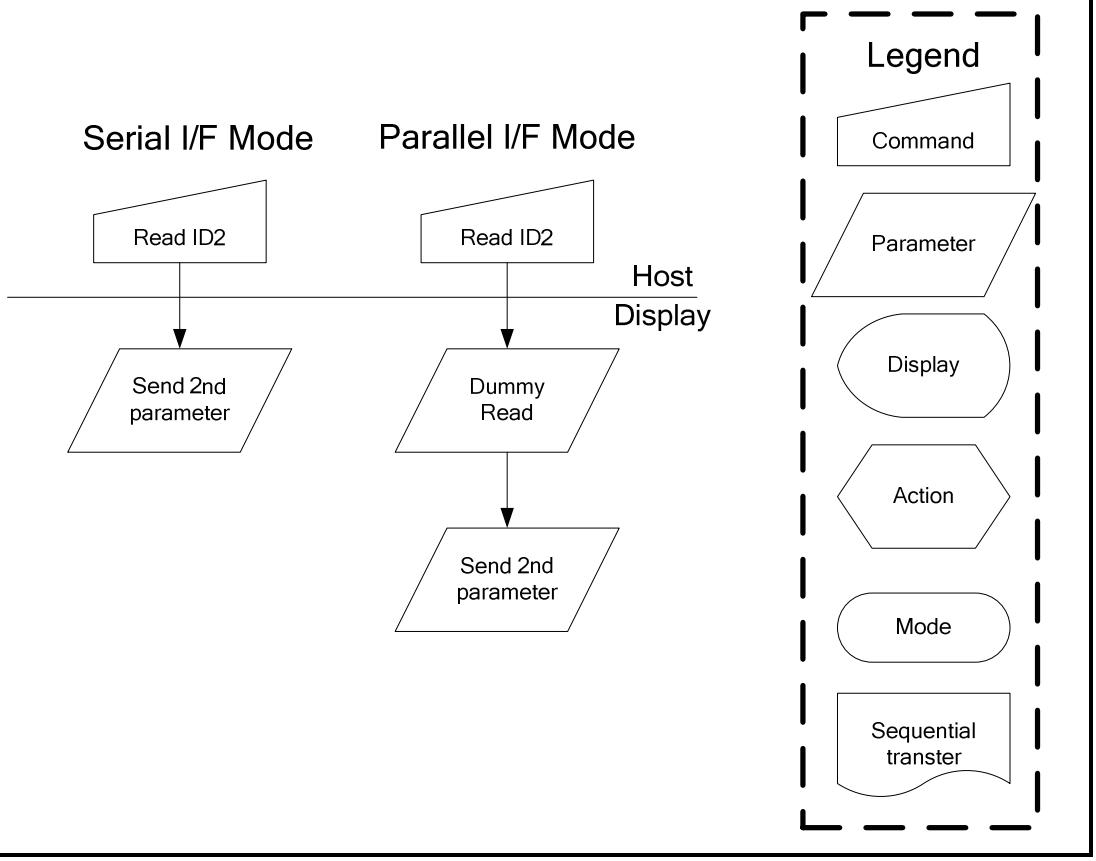
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	NV Value
S/W Reset	NV Value
H/W Reset	NV Value

Flow Chart



10.1.33 RDID3 (DCh): Read ID3 Value

DCH	RDID3 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

Description

-This read byte returns 8-bit LCD module/driver ID.

-The 1st parameter is dummy data

-The 2nd parameter (ID37 to ID30): LCD module/driver ID.

NOTE: See command RDDID (04h), 4th parameter.

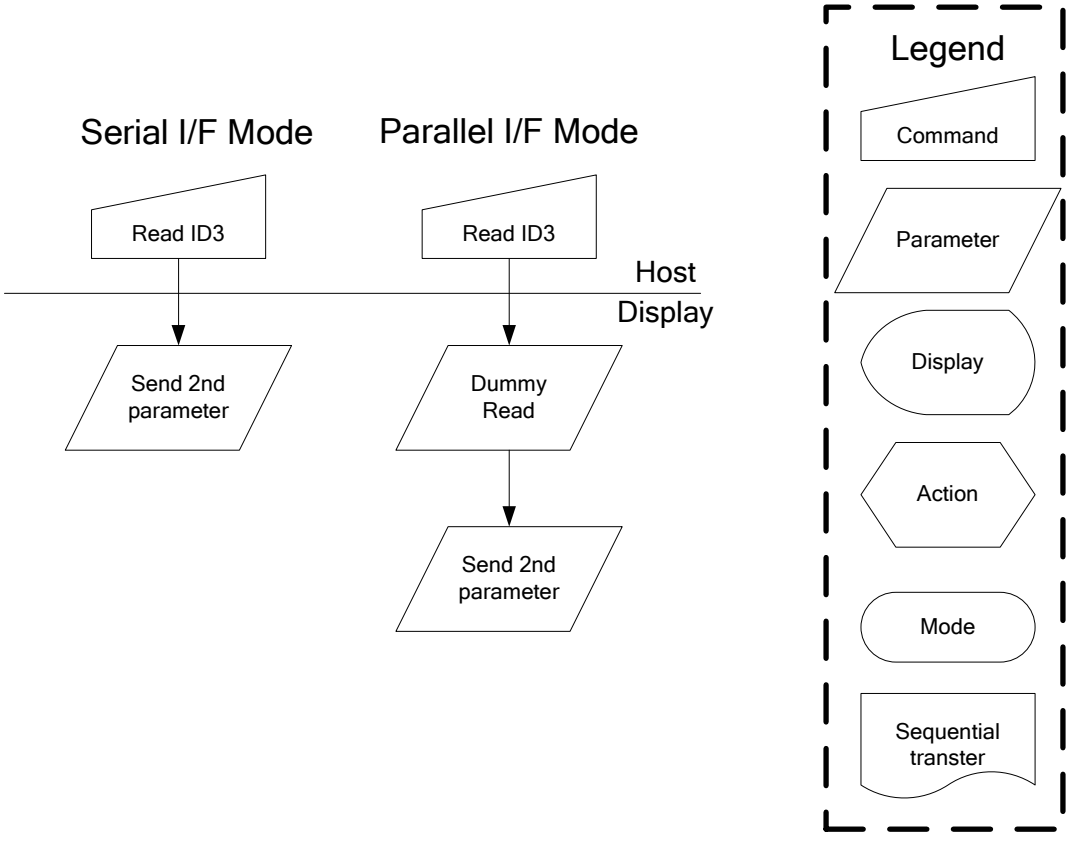
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	NV Value
S/W Reset	NV Value
H/W Reset	NV Value

Flow Chart



10.2 Panel Function Command List and Description

Table 10.2.1 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
FRMCTR1	10.2.1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors)
		1	↑	1	-					RTNA3	RTNA2	RTNA1	RTNA0		RTNA set 1-line period FPA: front porch BPA: back porch
		1	↑	1	-			FPA5	FPA4	FPA3	FPA2	FPA1	FPA0		
		1	↑	1	-			BPA5	BPA4	BPA3	BPA2	BPA1	BPA0		
FRMCTR2	10.2.2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8-colors)
		1	↑	1	-					RTNB3	RTNB2	RTNB1	RTNB0		RTNB: set 1-line period FPB: front porch BPB: back porch
		1	↑	1	-			FPB5	FPB4	FPB3	FPB2	FPB1	FPB0		
		1	↑	1	-			BPB5	BPB4	BPB3	BPB2	BPB1	BPB0		
FRMCTR3	10.2.3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In partial mode + Full colors
		1	↑	1	-					RTNC3	RTNC2	RTNC1	RTNC0		RTNC,RTND: set 1-line period FPC,FPD: front porch BPC,BPD: back porch
		1	↑	1	-			FPC5	FPC4	FPC3	FPC2	FPC1	FPC0		
		1	↑	1	-			BPC5	BPC4	BPC3	BPC2	BPC1	BPC0		
		1	↑	1	-					RTND3	RTND2	RTND1	RTND0		
		1	↑	1	-			FPD5	FPD4	FPD3	FPD2	FPD1	FPD0		
		1	↑	1	-			BPD5	BPD4	BPD3	BPD2	BPD1	BPD0		
INVCTR	10.2.4	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		NLA,NLB,NLC set inversion

Table 10.2.2 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PWCTR1	10.2.5	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	Power control setting
		1	↑	1	-	AVDD[2]	AVDD[1]	AVDD[0]	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0		VRH: Set the GVDD voltage
		1	↑	1	-	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0		
		1	↑	1		MODE[1]	MODE[0]	0	0	0	1	0	0		
PWCTR2	10.2.6	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	Power control setting
		1	↑	1	-	VGH25[1]	VGH25[0]	-	-	VGLSEL[1]	VGLSEL[0]	VGHBT[1]	VGHBT[0]		BT: set VGH/ VGL voltage
PWCTR3	10.2.7	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	In normal mode (Full colors)
		1	↑	1	-	DCA9	DCA8	SAPA2	SAPA1	SAPA0	APA2	APA1	APA0		APA: adjust the operational amplifier DCA: adjust the booster Voltage
					-	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA1	DCA0		
PWCTR4	10.2.8	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)	In Idle mode (8-colors)
		1	↑	1	-	DCB9	DCB8	SAPB2	SAPB1	SAPB0	APB2	APB1	APB0		APB: adjust the operational amplifier DCB: adjust the booster Voltage
					-	DCB7	DCB6	DCB5	DCB4	DCB3	DCB2	DCB1	DCB0		
PWCTR5	10.2.9	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	In partial mode + Full
		1	↑	1	-	DCC9	DCC8	SAPC2	SAPC1	SAPC0	APC2	APC1	APC0		APC: adjust the operational amplifier DCC: adjust the booster circuit for Idle mode
		1	↑	1	-	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0		
VMCTR1	10.2.10	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOM control 1
		1	↑	1	-	-	-	VCOMS5	VCOMS4	VCOMS3	VCOMS2	VCOMS1	VCOMS0		VCOM voltage control
VMOFCTR	10.2.11	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	Set VCOM offset control
		1	↑	1	-	-	-	-	VMF4	VMF3	VMF2	VMF1	VMF0		
WRID2	10.2.12	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	Set LCM version code
		1	↑	1	-	-	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]		

"-": Don't care

Note 1: C0h to C7h are fixed for about power controller

Table 10.2.3 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRID3	10.2.13	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Customer Project code
		1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Set the project code at ID3
NVCTR1	10.2.14	0	↑	1	-	1	1	0	1	1	0	0	1	(D9)	NVM control status
		1	↑	1	-	0	VMF _EN	ID2 _EN	0	0	0	0	EXT_ R		
NVCTR2	10.2.15	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	NVM Read Command
		1	↑	1	-	1	0	1	0	0	1	0	1	A5	Action code
NVCTR3	10.2.16	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	NVM Write Command
		1	↑	1	-	NVM_ IB7	NVM _ IB6	NVM _ IB5	NVM _ IB4	NVM _ IB3	NVM _ IB2	NVM _ IB1	NVM _ IB0		
		1	↑	1	-	NVM _ CMD7	NVM _ CMD6	NVM _ CMD5	NVM _ CMD4	NVM _ CMD3	NVM _ CMD2	NVM _ CMD1	NVM _ CMD0		
		1	↑	1	-	1	0	1	0	0	1	0	1	A5	

"-": Don't care

Note 1: The D1h to D3h registers are fixed for about ID code setting.

Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

Table 10.2.4 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
GAMCTRP1	10.2.17	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set
		1	↑	1	-	---	---	VRFP[5]	VRFP[4]	VRFP[3]	VRFP[2]	VRFP[1]	VRF0P[0]		Gamma adjustment (+ polarity)
		1	↑	1	-	---	---	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]		
		1	↑	1	-	---	---	PKP0[5]	PKP0[4]	PKP0[3]	PKP0[2]	PKP0[1]	PKP0[0]		
		1	↑	1	-	---	---	PKP1[5]	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]		
		1	↑	1	-	---	---	PKP2[5]	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]		
		1	↑	1	-	---	---	PKP3[5]	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]		
		1	↑	1	-	---	---	PKP4[5]	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]		
		1	↑	1	-	---	---	PKP5[5]	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]		
		1	↑	1	-	---	---	PKP6[5]	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]		
		1	↑	1	-	---	---	PKP7[5]	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]		
		1	↑	1	-	---	---	PKP8[5]	PKP8[4]	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]		
		1	↑	1		---	---	PKP9[5]	PKP9[4]	PKP9[3]	PKP9[2]	PKP9[1]	PKP9[0]		
		1	↑	1	-	---	---	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]		
		1	↑	1	-	---	---	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]		
		1	↑	1		---	---	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]		
		1	↑	1	-	---	---	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]		
GAMCTRN1	10.2.18	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set
		1	↑	1	-	---	---	VRF0N[5]	VRF0N[4]	VRF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]		Gamma adjustment (- polarity)
		1	↑	1	-	---	---	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]		
		1	↑	1	-	---	---	PKN0[5]	PKN0[4]	PKN0[3]	PKN0[2]	PKN0[1]	PKN0[0]		
		1	↑	1	-	---	---	PKN1[5]	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]		
		1	↑	1	-	---	---	PKN2[5]	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]		
		1	↑	1	-	---	---	PKN3[5]	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]		
		1	↑	1	-	---	---	PKN4[5]	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]		
		1	↑	1	-	---	---	PKN5[5]	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]		
		1	↑	1	-	---	---	PKN6[5]	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]		
		1	↑	1	-	---	---	PKN7[5]	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]		
		1	↑	1	-	---	---	PKN8[5]	PKN8[4]	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]		
		1	↑	1	-	---	---	PKN9[5]	PKN9[4]	PKN9[3]	PKN9[2]	PKN9[1]	PKN9[0]		
		1	↑	1	-	---	---	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]		
		1	↑	1	-	---	---	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]		
		1	↑	1	-	---	---	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]		
		1	↑	1	-	---	---	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]		

"-": Don't care

Note 1: E0-E1 registers are fixed for adjusting Gamma

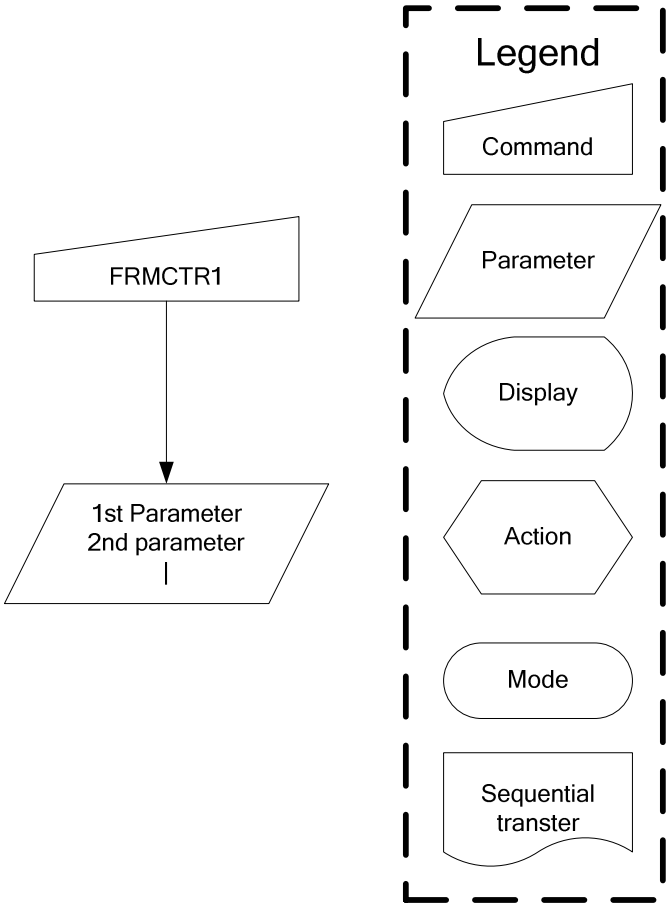
10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	-	-	-	-	-	RTNA3	RTNA2	RTNA1	RTNA0	
2nd parameter	1	↑	1	-	-	-	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	
3rd parameter	1	↑	1	-	-	-	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	
Description	-Set the frame frequency of the full colors normal mode. - Frame rate=fosc/((RTNA x 2 + 40) x (LINE + FPA + BPA)) -fosc = 625kHz												

Default

Status	Default Value	
	GM[1:0] = “00”	GM[1:0] = “11”
Power On Sequence	01h/2Ch/2Dh	01h/2Ch/2Bh
S/W Reset	01h/2Ch/2Dh	01h/2Ch/2Bh
H/W Reset	01h/2Ch/2Dh	01h/2Ch/2Bh

Flow Chart



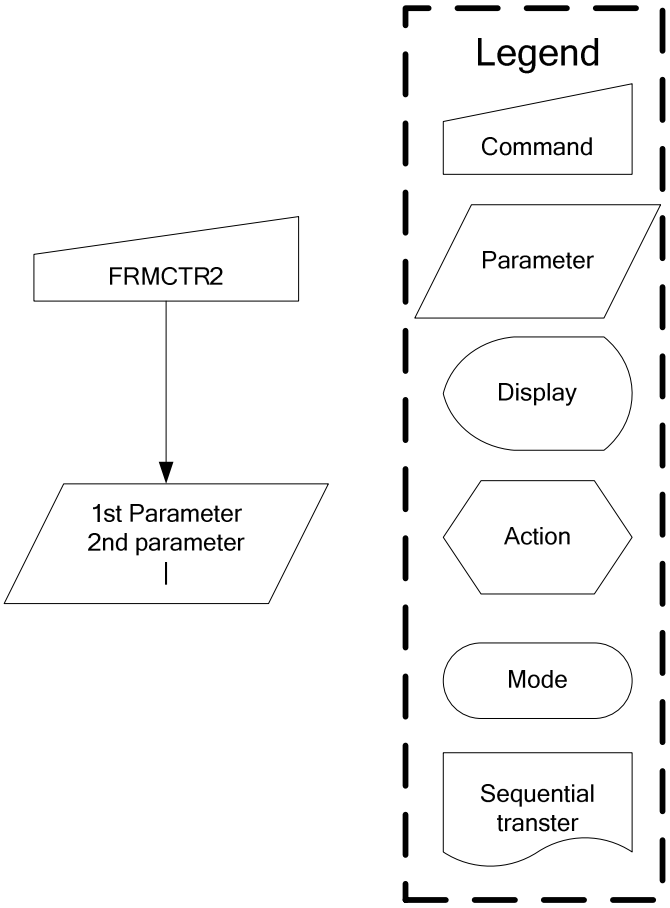
10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	-	-	-	-	-	RTNB3	RTNB2	RTNB1	RTNB0	
2nd parameter	1	↑	1	-	-	-	FPB5	FPB4	FPB3	FPB2	FPB1	FPB0	
3rd parameter	1	↑	1	-	-	-	BPB5	BPB4	BPB3	BPB2	BPB1	BPB0	
Description	-Set the frame frequency of the Idle mode. - Frame rate=fosc/((RTNB x 2 + 40) x (LINE + FPB + BPB)) -fosc = 625kHz												

Default

Status	Default Value	
	GM[1:0] = “00”	GM[1:0] = “11”
Power On Sequence	01h/2Ch/2Dh	01h/2Ch/2Bh
S/W Reset	01h/2Ch/2Dh	01h/2Ch/2Bh
H/W Reset	01h/2Ch/2Dh	01h/2Ch/2Bh

Flow Chart



10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H	FRMCTR3 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3
1st parameter	1	↑	1	-	-	-	-	-	RTNC	RTNC	RTNC	RTNC	
2nd parameter	1	↑	1	-	-	-	FPC5	FPC4	FPC3	FPC2	FPC1	FPC0	
3rd parameter	1	↑	1	-	-	-	BPC5	BPC4	BPC3	BPC2	BPC1	BPC0	
4th parameter	1	↑	1	-	-	-	-	-	RTND	RTND	RTND	RTND	
5th parameter	1	↑	1	-	-	-	FPD5	FPD4	FPD3	FPD2	FPD1	FPD0	
6th parameter	1	↑	1	-	-	-	BPD5	BPD4	BPD3	BPD2	BPD1	BPD0	

Description

-Set the frame frequency of the Partial mode/ full colors.

- 1st parameter to 3rd parameter are used in dot inversion mode.

- 4th parameter to 6th parameter are used in line inversion mode.

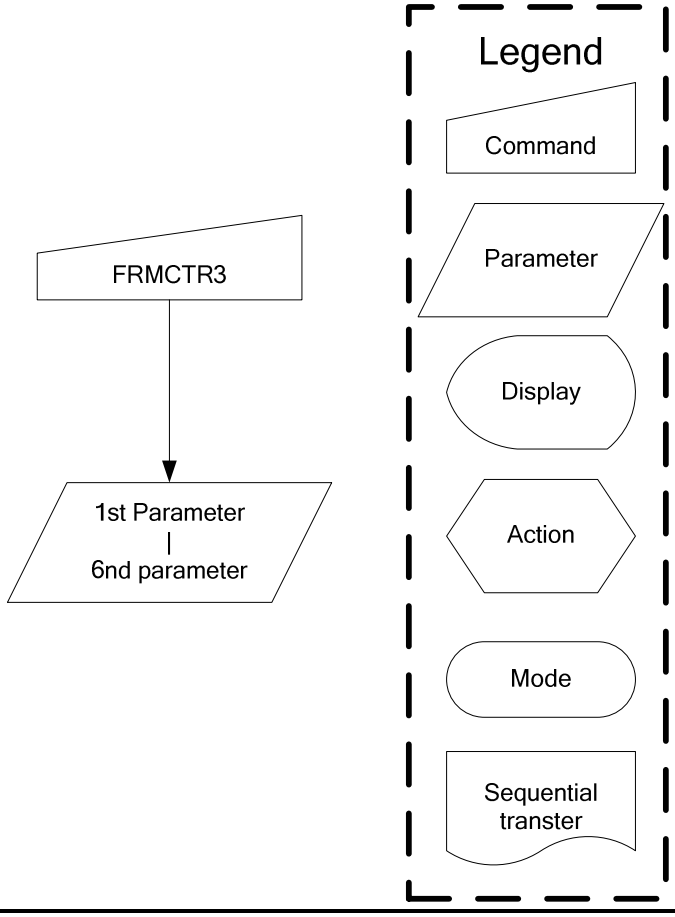
- Frame rate=fosc/((RTNC x 2 + 40) x (LINE + FPC + BPC))

-fosc = 625kHz

Default

Status	Default Value	
	GM[1:0] = “00”	GM[1:0] = “11”
Power On Sequence	01h/2Ch/2Dh/01h/2Ch/2Dh	01h/2Ch/2Bh/01h/2Ch/2Bh
S/W Reset	01h/2Ch/2Dh/01h/2Ch/2Dh	01h/2Ch/2Bh/01h/2Ch/2Bh
H/W Reset	01h/2Ch/2Dh/01h/2Ch/2Dh	01h/2Ch/2Bh/01h/2Ch/2Bh

Flow Chart



10.2.4 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	

Description

-Display Inversion mode control

-NLA: Inversion setting in full colors normal mode (Normal mode on)

NLA	Inversion setting in full Colors normal mode
0	Dot Inversion
1	Line Inversion

-NLB: Inversion setting in Idle mode (Idle mode on)

NLB	Inversion setting in Idle mode
0	Dot Inversion
1	Line Inversion

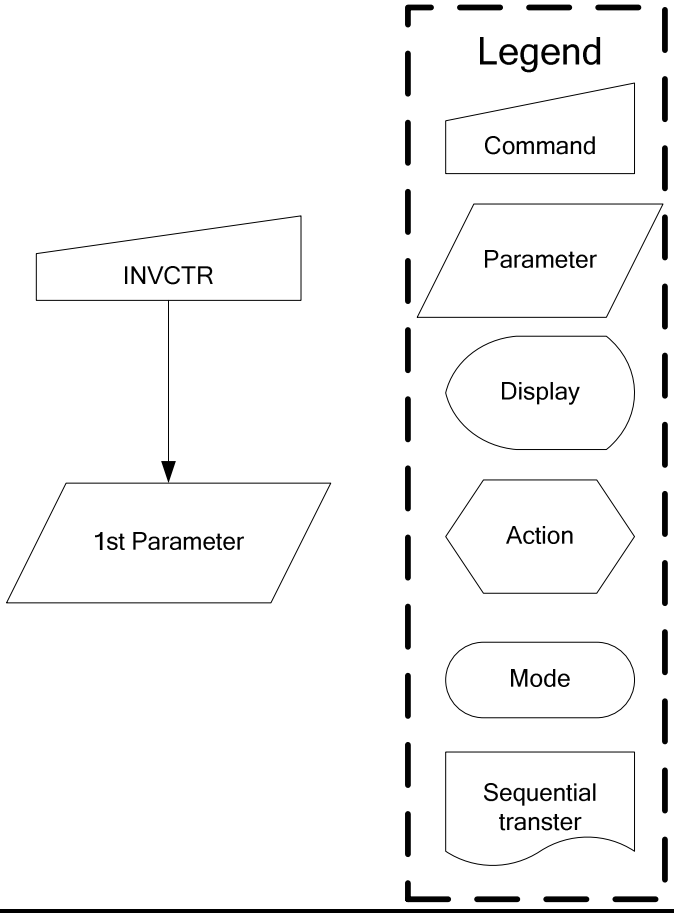
-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLC	Inversion setting in full Colors partial mode
0	Dot Inversion
1	Line Inversion

Default

Status	Default Value
	B4h
Power On Sequence	03h
S/W Reset	03h
H/W Reset	03h

Flow Chart



10.2.5 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	-	AVDD[2]	AVDD[1]	AVDD[0]	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0	
2nd parameter	1	↑	1	-	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	
3rd parameter	1	↑	1	-	MODE[1]	MODE[0]	0	0	0	1	0	0	

Description

AVDD[2:0]	AVDD
000	4.5
001	4.6
010	4.7
011	4.8
100	4.9
101	5
110	5.1
111	Don't use this setting, reserve for testing.

MODE[1:0]	FUNCTION
00	2X
01	3X
10	AUTO
11	3X

VRHP[4:0]	GVDD	VRHN[4:0]	GVCL
00000	4.7	00000	-4.7
00001	4.65	00001	-4.65
00010	4.6	00010	-4.6
00011	4.55	00011	-4.55
00100	4.5	00100	-4.5
00101	4.45	00101	-4.45
00110	4.4	00110	-4.4
00111	4.35	00111	-4.35
01000	4.3	01000	-4.3
01001	4.25	01001	-4.25
01010	4.2	01010	-4.2
01011	4.15	01011	-4.15
01100	4.1	01100	-4.1
01101	4.05	01101	-4.05
01110	4	01110	-4
01111	3.95	01111	-3.95
10000	3.9	10000	-3.9
10001	3.85	10001	-3.85
10010	3.8	10010	-3.8
10011	3.75	10011	-3.75
10100	3.7	10100	-3.7
10101	3.65	10101	-3.65
10110	3.6	10110	-3.6
10111	3.55	10111	-3.55
11000	3.5	11000	-3.5
11001	3.45	11001	-3.45
11010	3.4	11010	-3.4
11011	3.35	11011	-3.35
11100	3.3	11100	-3.3
11101	3.25	11101	-3.25
11110	3.2	11110	-3.2
11111	3.15	11111	-3.15

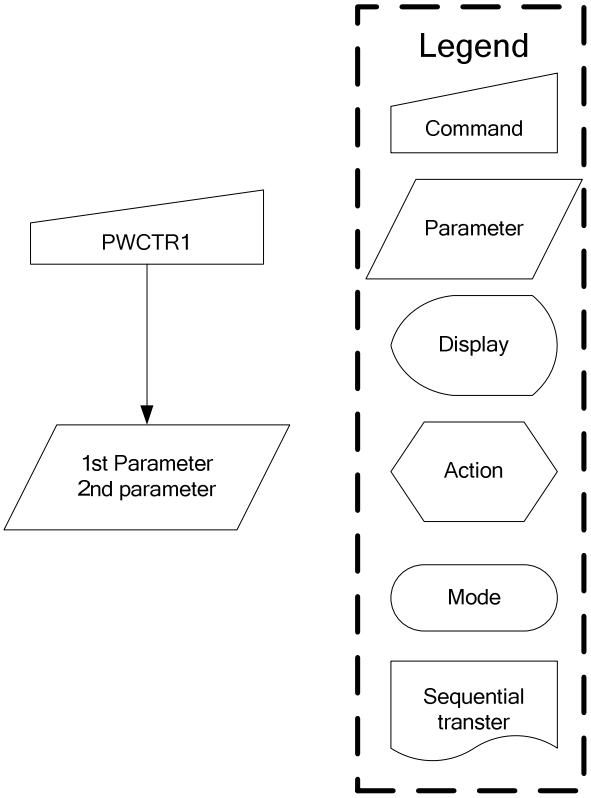
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C0h
Power On Sequence	82h/02h/84h
S/W Reset	82h/02h/84h
H/W Reset	82h/02h/84h

Flow Chart



10.2.6 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	↑	1		VGH25[1]	VGH25[0]	-	-	VGLSEL[1]	VGLSEL[0]	VGHBT[1]	VGHBT[0]	

Description

-Set the VGH and VGL supply power level

VGH25[1:0]	V25
00	2.1
01	2.2
10	2.3
11	2.4

VGHBT[1:0]	VGH
00	2*AVDD+VGH25
01	3*AVDD
10	3*AVDD+VGH25
11	Don't use this setting, reserve for testing.

VGLSEL[1:0]	VGL
00	-7.5
01	-10
10	-12.5
11	-13

Restriction

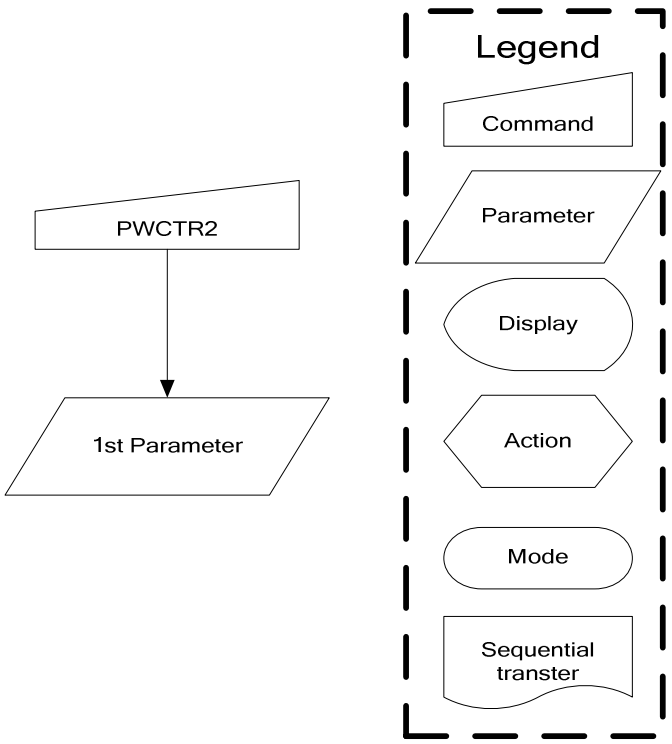
-The deviation value of VGH/ VGL between with Measurement and Specification: Max <= 1V
-VGH-VGL <= 32V

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C1h
Power On Sequence	C5h
S/W Reset	C5h
H/W Reset	C5h

Flow Chart	

PWCTR2
1st Parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

10.2.7 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st parameter	1	↑	1	-	DCA9	DCA8	SAPA2	SAPA1	SAPA0	APA2	APA1	APA0	
2nd parameter	1	↑	1	-	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA1	DCA0	

Description

-Set the amount of current in Operational amplifier in normal mode/full colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

SAP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

-Set the Booster circuit Step-up cycle in Normal mode/ full colors.

	DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]
00	BCLK/1	BCLK/1	BCLK/1	BCLK/1	BCLK/1
01	BCLK/1.5	BCLK/1.5	BCLK/1.5	BCLK/1.5	BCLK/1.5
10	BCLK/2	BCLK/2	BCLK/2	BCLK/2	BCLK/2
11	BCLK/4	BCLK/4	BCLK/4	BCLK/4	BCLK/4

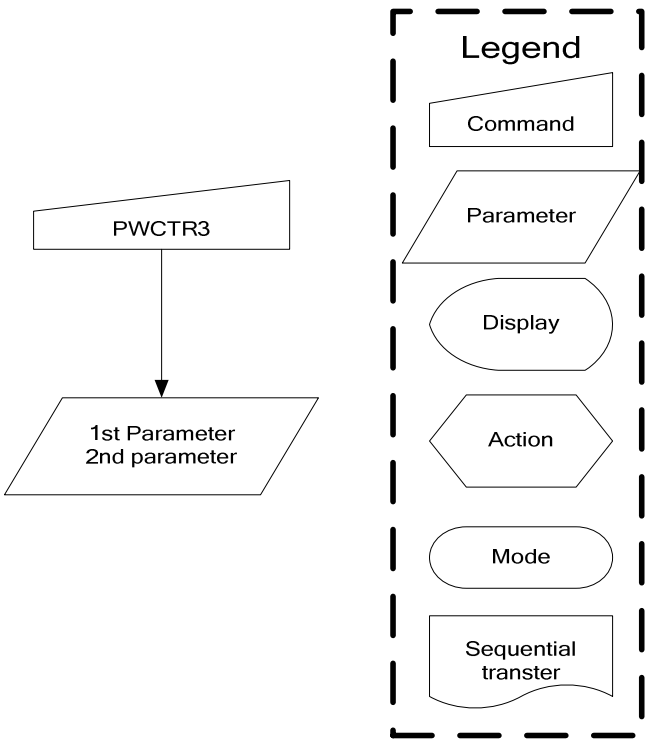
Note: BCLK is Clock frequency for Booster circuit

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C2h
Power On Sequence	0Ah/00h
S/W Reset	0A h/00h
H/W Reset	0A h/00h

Flow Chart	 PWCTR3 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transter

10.2.8 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st parameter	1	↑	1	-	DCB9	DCB8	SAPB2	SAPB1	SAPB0	APB2	APB1	APB0	
2nd parameter	1	↑	1	-	DCB7	DCB6	DCB5	DCB4	DCB3	DCB2	DCB1	DCB0	

Description

-Set the amount of current in Operational amplifier in Idle mode/8 colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

SAP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

-Set the Booster circuit Step-up cycle in Idle mode/8 colors.

	DCB[9:8]	DCB[7:6]	DCB[5:4]	DCB[3:2]	DCB[1:0]
00	BCLK/1	BCLK/1	BCLK/1	BCLK/1	BCLK/1
01	BCLK/1.5	BCLK/1.5	BCLK/1.5	BCLK/1.5	BCLK/1.5
10	BCLK/2	BCLK/2	BCLK/2	BCLK/2	BCLK/2
11	BCLK/4	BCLK/4	BCLK/4	BCLK/4	BCLK/4

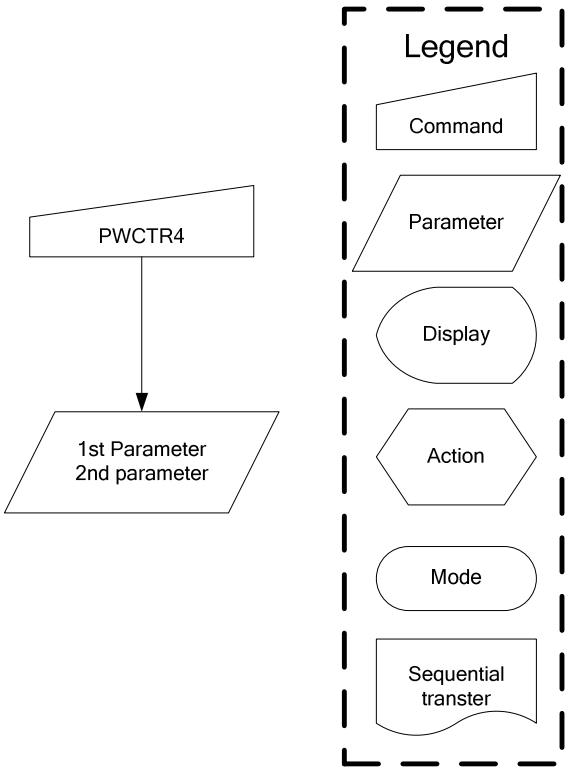
Note: BCLK is Clock frequency for Booster circuit

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C3h
Power On Sequence	8Ah/2Eh
S/W Reset	8Ah/2Eh
H/W Reset	8Ah/2Eh

Flow Chart	 PWCTR4 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transter

10.2.9 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st parameter	1	↑	1	-	DCC9	DCC8	SAPC2	SAPC1	SAPC0	APC2	APC1	APC0	
2nd parameter	1	↑	1	-	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0	

Description

-Set the amount of current in Operational amplifier in Partial mode/ full-colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

SAP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

	DCC[9:8]	DCC[7:6]	DCC[5:4]	DCC[3:2]	DCC[1:0]
00	BCLK/1	BCLK/1	BCLK/1	BCLK/1	BCLK/1
01	BCLK/1.5	BCLK/1.5	BCLK/1.5	BCLK/1.5	BCLK/1.5
10	BCLK/2	BCLK/2	BCLK/2	BCLK/2	BCLK/2
11	BCLK/4	BCLK/4	BCLK/4	BCLK/4	BCLK/4

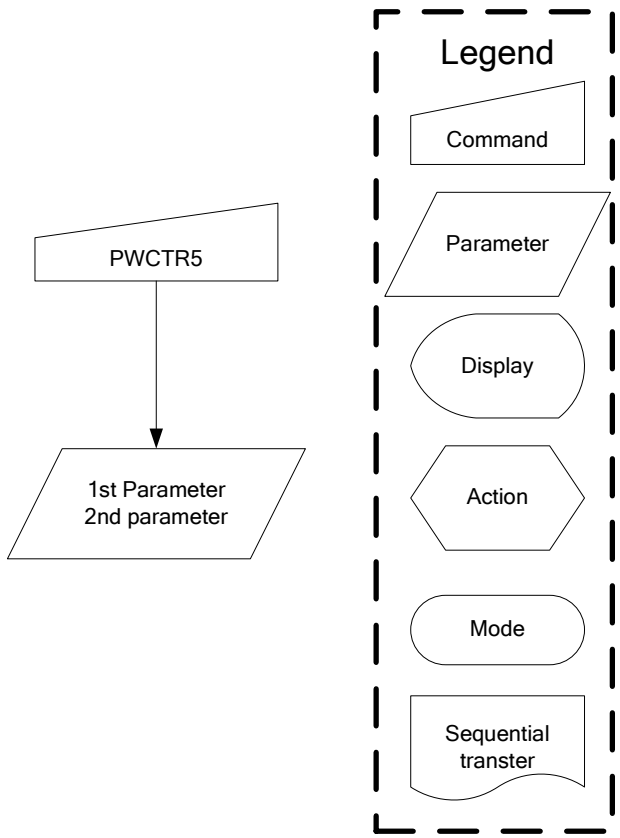
Note: BCLK is Clock frequency for Booster circuit

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C4h
Power On Sequence	8Ah/AAh
S/W Reset	8Ah/AAh
H/W Reset	8Ah/AAh

Flow Chart	 PWCTR5 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transter

10.2.10 VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st parameter	1	↑	1	-	-	-	VCOMS5	VCOMS 4	VCOMS 3	VCOMS 2	VCOMS 1	VCOMS 0	

Description

VCOM voltage setting.

	VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM
0	000000	-0.425	16	010000	-0.825	32	100000	-1.225	48	110000	-1.625
1	000001	-0.45	17	010001	-0.85	33	100001	-1.25	49	110001	-1.65
2	000010	-0.475	18	010010	-0.875	34	100010	-1.275	50	110010	-1.675
3	000011	-0.5	19	010011	-0.9	35	100011	-1.3	51	110011	-1.7
4	000100	-0.525	20	010100	-0.925	36	100100	-1.325	52	110100	-1.725
5	000101	-0.55	21	010101	-0.95	37	100101	-1.35	53	110101	-1.75
6	000110	-0.575	22	010110	-0.975	38	100110	-1.375	54	110110	-1.775
7	000111	-0.6	23	010111	-1	39	100111	-1.4	55	110111	-1.8
8	001000	-0.625	24	011000	-1.025	40	101000	-1.425	56	111000	-1.825
9	001001	-0.65	25	011001	-1.05	41	101001	-1.45	57	111001	-1.85
10	001010	-0.675	26	011010	-1.075	42	101010	-1.475	58	111010	-1.875
11	001011	-0.7	27	011011	-1.1	43	101011	-1.5	59	111011	-1.9
12	001100	-0.725	28	011100	-1.125	44	101100	-1.525	60	111100	-1.925
13	001101	-0.75	29	011101	-1.15	45	101101	-1.55	61	111101	-1.95
14	001110	-0.775	30	011110	-1.175	46	101110	-1.575	62	111110	-1.975
15	001111	-0.8	31	011111	-1.2	47	101111	-1.6	63	111111	-2

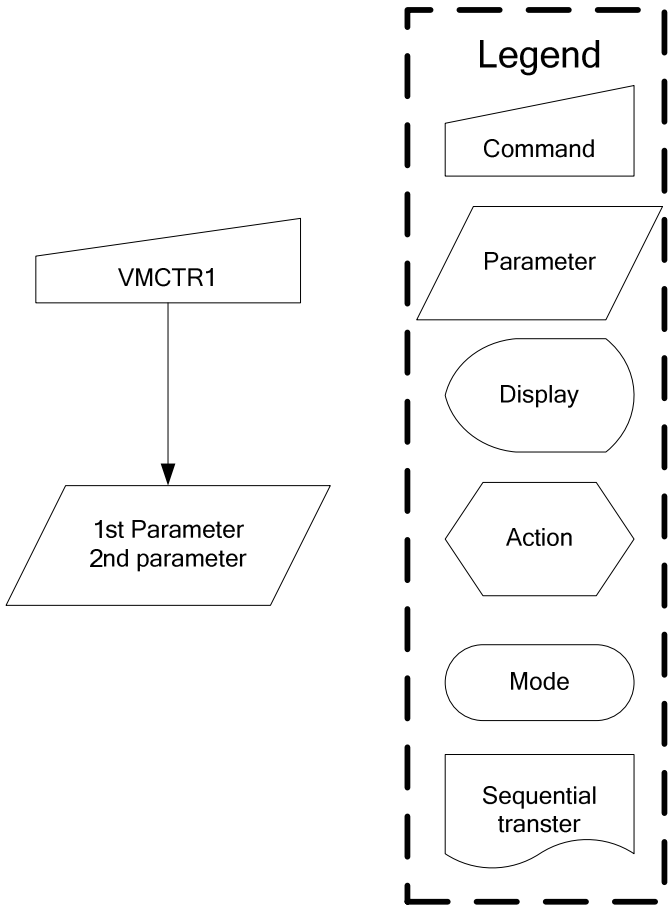
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C5h
Power On Sequence	04h
S/W Reset	04h
H/W Reset	04h

Flow Chart


VMCTR1
1st Parameter
2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

10.2.11 VMOFCTR (C7h): VCOM Offset Control

C7H	VMOFCTR (VCOM Offset Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VMOFCTR	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
Parameter	1	↑	1	-	-	-	-	VMF4	VMF3	VMF2	VMF1	VMF0	

Description

-Set VCOM Voltage level for reduce the flicker issue

-Before use command 0xC7, the bit VMF_EN of command 0xD9 must be enabled (set to 1).

VMF[4]	VMF[3:0]	VCOM Output Level
0	0000	"VCOMS"-16d
0	0001	"VCOMS"-15d
0	|	|
0	1110	"VCOMS"-2d
0	1111	"VCOMS"-1d
1	0000	"VCOMS"
1	0001	"VCOMS"+1d
1	0010	"VCOMS"+2d
1	|	|
1	1110	"VCOMS"+14d
1	1111	"VCOMS"+15d

- 1d=25mV, 2d=50mV 3d=75mv....

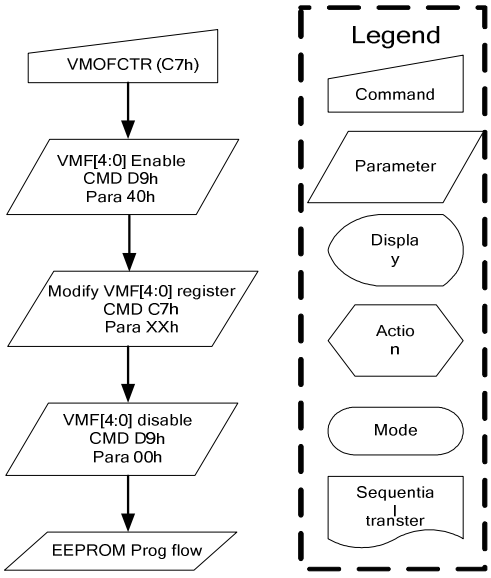
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

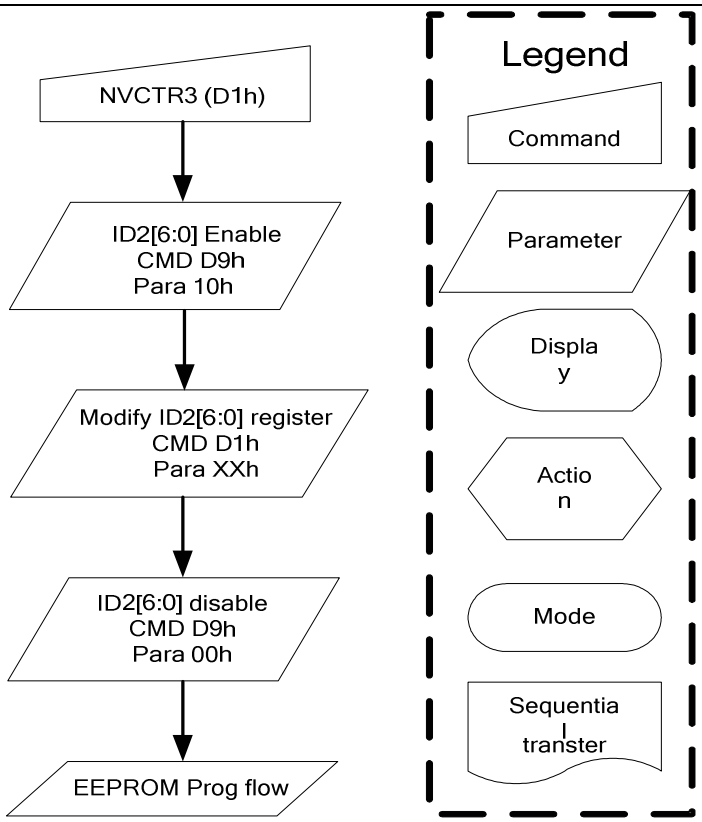
Default

Status	Default Value
	C7h
Power On Sequence	10h
S/W Reset	10h
H/W Reset	10h

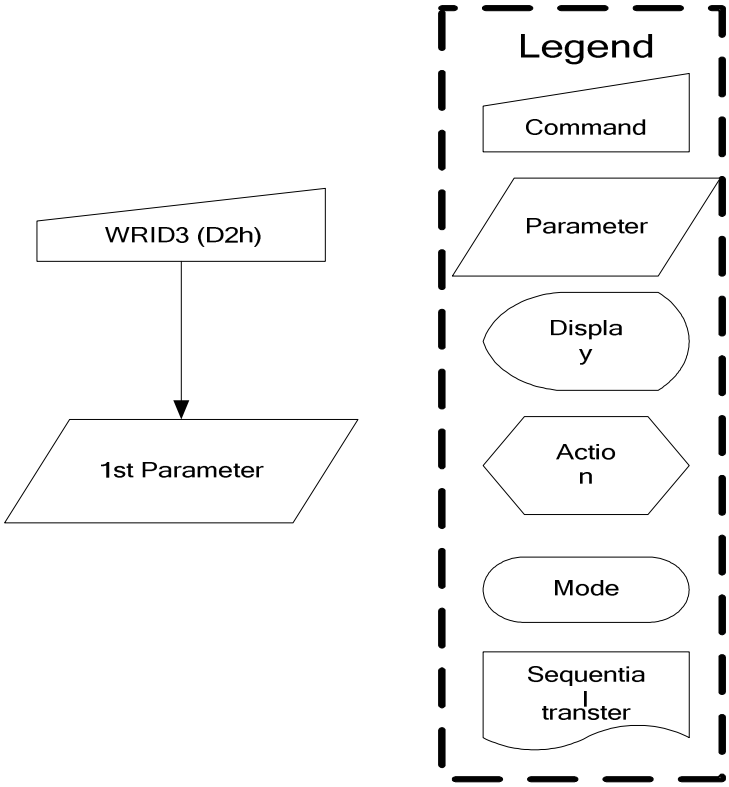
Flow Chart



10.2.12 WRID2 (D1h): Write ID2 Value

D1H	WRID2 (Write ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
Parameter	1	↑	1	-	-	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
Description	-Write 7-bit data of LCD module version to save it to NVM. -The parameter ID2[6:0] is LCD Module version ID.												
Flow Chart													

10.2.13 WRID3 (D2h): Write ID3 Value

D2H	WRID3 (Write ID3 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
Parameter	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
Description	-Write 8-bit data of project code module to save it to NVM. -The parameter ID3[7:0] is product project ID.												
Flow Chart													

10.2.14 NVFCTR1 (D9h): NVM Control Status

D9H	NVFCTR1 (NV Memory Function Controller 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR1	0	↑	1	-	1	1	0	0	1	0	0	1	(D9h)
parameter	1	1	↑	-	0	VMF_EN	ID2_EN	0	0	0	0	EXT_R	

Description

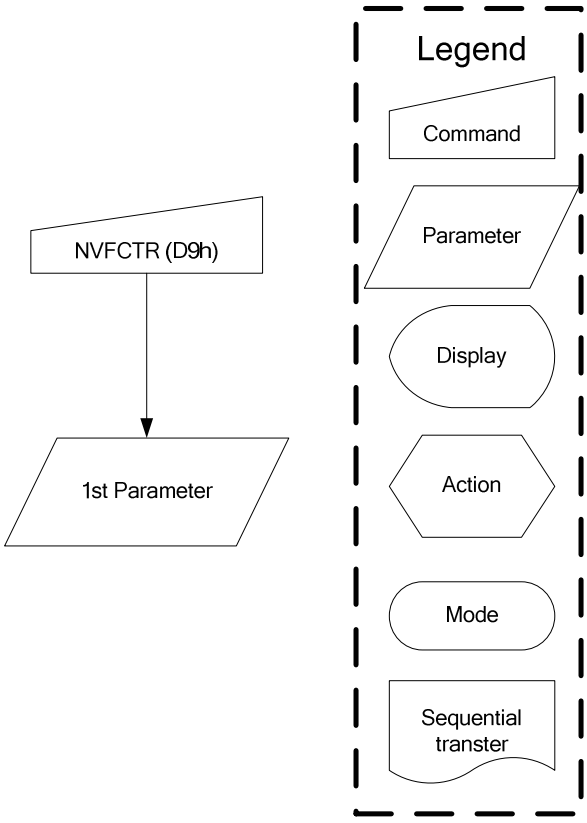
-NVM control status

Bit	Value
VMF_EN	"1" = Command C7h enable ; "0" = Command C7h disable
ID2_EN	"1" = Command D1h enable ; "0" = Command D1h disable
EXT_R	Read: extension command status, "1" for enable, "0" for disable. Write: Don't care

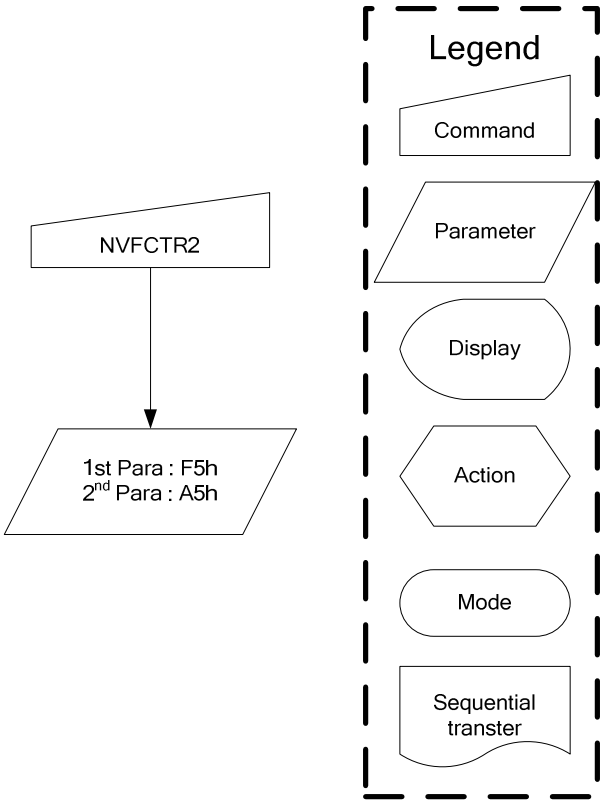
Default

Status	Default Value
	D9h
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

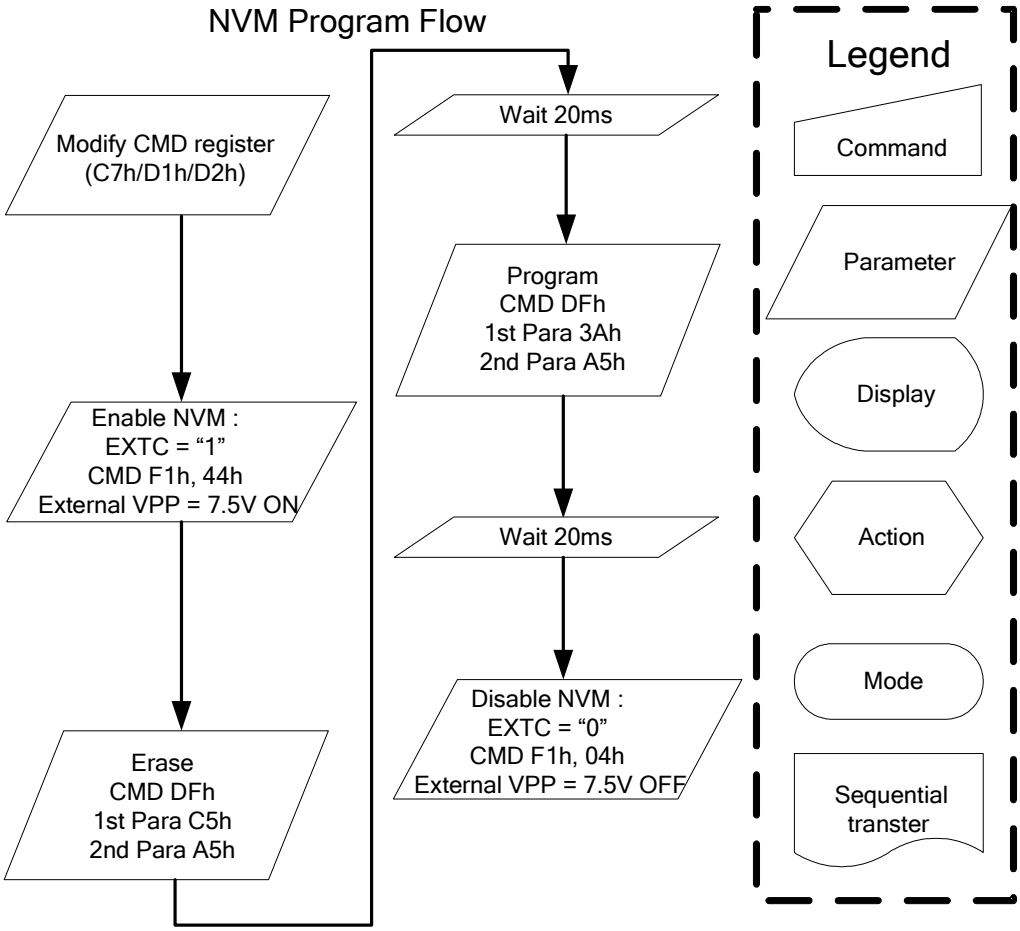
Flow Chart



10.2.15 NVFCTR2 (DEh): NVM Read Command

DEH	NVFCTR1 (NV Memory Function Controller 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR2	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)
1st parameter	1	↑	1		1	1	1	1	0	1	0	1	F5
2nd parameter	1	↑	1		1	0	1	0	0	1	0	1	A5
Description	NVM Read Command *NOTE: "-" Don't care*												
Flow Chart													

10.2.16 NVFCTR3 (DFh): NVM Write Command

DFH	NVFCTR1 (NV Memory Function Controller 3												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR1	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1st parameter	1	↑	1		NVM_CMD7	NVM_CMD6	NVM_CMD5	NVM_CMD4	NVM_CMD3	NVM_CMD2	NVM_CMD1	NVM_CMD0	
2nd parameter	1	↑	1		1	0	1	0	0	1	0	1	A5
Description	-NVM Write Command -NVM_CMD[7:0] : Select to Program/Erase ; Program command : 3Ah ; Erase command : C5h *NOTE: "-" Don't care*												
Flow Chart													

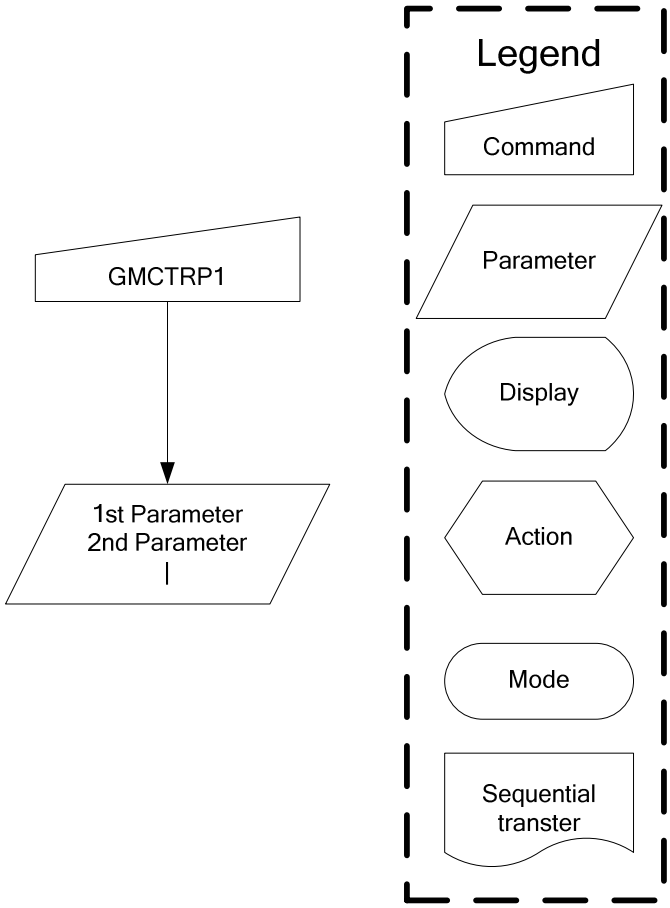
10.2.17 GMCTRP1 (E0h): Gamma ('+'polarity) Correction Characteristics Setting

E0H	GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st parameter	1	↑	1	-	-	-	VRF0P[5]	VRF0P[4]	VF0P[3]	VRF0P[2]	VRF0P[1]	VRF0P[0]	
2nd parameter	1	↑	1	-	-	-	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]	
3rd parameter	1	↑	1	-	-	-	PK0P[5]	PK0P[4]	PK0P[3]	PK0P[2]	PK0P[1]	PK0P[0]	
4th parameter	1	↑	1	-	-	-	PK1P[5]	PK1P[4]	PK1P[3]	PK1P[2]	PK1P[1]	PK1P[0]	
5th parameter	1	↑	1	-	-	-	PK2P[5]	PK2P[4]	PK2P[3]	PK2P[2]	PK2P[1]	PK2P[0]	
6th parameter	1	↑	1	-	-	-	PK3P[5]	PK3P[4]	PK3P[3]	PK3P[2]	PK3P[1]	PK3P[0]	
7th parameter	1	↑	1	-	-	-	PK4P[5]	PK4P[4]	PK4P[3]	PK4P[2]	PK4P[1]	PK4P[0]	
8th parameter	1	↑	1	-	-	-	PK5P[5]	PK5P[4]	PK5P[3]	PK5P[2]	PK5P[1]	PK5P[0]	
9th parameter	1	↑	1	-	-	-	PK6P[5]	PK6P[4]	PK6P[3]	PK6P[2]	PK6P[1]	PK6P[0]	
10th parameter	1	↑	1	-	-	-	PK7P[5]	PK7P[4]	PK7P[3]	PK7P[2]	PK7P[1]	PK7P[0]	
11th parameter	1	↑	1	-	-	-	PK8P[5]	PK8P[4]	PK8P[3]	PK8P[2]	PK8P[1]	PK8P[0]	
12th parameter	1	↑	1	-	-	-	PK9P[5]	PK9P[4]	PK9P[3]	PK9P[2]	PK9P[1]	PK9P[0]	
13th parameter	1	↑	1	-	-	-	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]	
14th parameter	1	↑	1	-	-	-	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]	
15th parameter	1	↑	1	-	-	-	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]	
16th parameter	1	↑	1	-	-	-	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]	

Description

Register Group	Positive Polarity	Set-up Contents
High level adjustment	VRF0P[5:0]	Variable resistor VRHP
Mid level adjustment	SELV0P[5:0]	The voltage of V0 grayscale is selected by the 64 to 1 selector
	SELV1P[5:0]	The voltage of V1 grayscale is selected by the 64 to 1 selector
	PK0P[5:0]	The voltage of V3 grayscale is selected by the 64 to 1 selector
	PK1P[5:0]	The voltage of V4 grayscale is selected by the 64 to 1 selector
	PK2P[5:0]	The voltage of V12 grayscale is selected by the 64 to 1 selector
	PK3P[5:0]	The voltage of V20 grayscale is selected by the 64 to 1 selector
	PK4P[5:0]	The voltage of V28 grayscale is selected by the 64 to 1 selector
	PK5P[5:0]	The voltage of V36 grayscale is selected by the 64 to 1 selector
	PK6P[5:0]	The voltage of V44 grayscale is selected by the 64 to 1 selector
	PK7P[5:0]	The voltage of V52 grayscale is selected by the 64 to 1 selector
	PK8P[5:0]	The voltage of V56 grayscale is selected by the 64 to 1 selector
	PK9P[5:0]	The voltage of V60 grayscale is selected by the 64 to 1 selector
	SELV62P[5:0]	The voltage of V62 grayscale is selected by the 64 to 1 selector
	SELV63P[5:0]	The voltage of V63 grayscale is selected by the 64 to 1 selector
Low level adjustment	VOS0P[5:0]	Variable resistor VRLP

Flow Chart

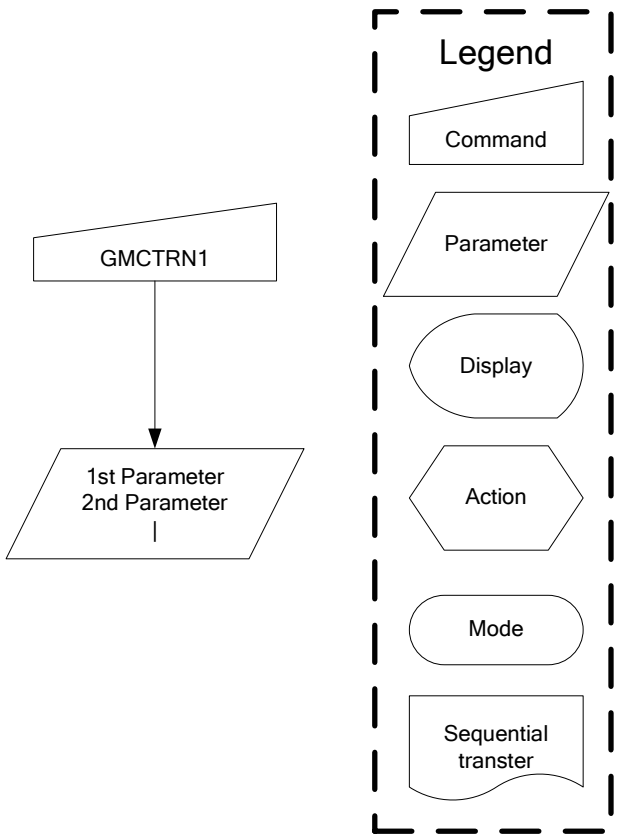

GMCTRP1
1st Parameter
2nd Parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

10.2.18 GMCTRN1 (E1h): Gamma '-'polarity Correction Characteristics Setting

E1H	GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1st parameter	1	↑	1	-	-	-	VRF0N[5]	VRF0N[4]	VF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]	
2nd parameter	1	↑	1	-	-	-	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]	
3rd parameter	1	↑	1	-	-	-	PK0N[5]	PK0N[4]	PK0N[3]	PK0N[2]	PK0N[1]	PK0N[0]	
4th parameter	1	↑	1	-	-	-	PK1N[5]	PK1N[4]	PK1N[3]	PK1N[2]	PK1N[1]	PK1N[0]	
5th parameter	1	↑	1	-	-	-	PK2N[5]	PK2N[4]	PK2N[3]	PK2N[2]	PK2N[1]	PK2N[0]	
6th parameter	1	↑	1	-	-	-	PK3N[5]	PK3N[4]	PK3N[3]	PK3N[2]	PK3N[1]	PK3N[0]	
7th parameter	1	↑	1	-	-	-	PK4N[5]	PK4N[4]	PK4N[3]	PK4N[2]	PK4N[1]	PK4N[0]	
8th parameter	1	↑	1	-	-	-	PK5N[5]	PK5N[4]	PK5N[3]	PK5N[2]	PK5N[1]	PK5N[0]	
9th parameter	1	↑	1	-	-	-	PK6N[5]	PK6N[4]	PK6N[3]	PK6N[2]	PK6N[1]	PK6N[0]	
10th parameter	1	↑	1	-	-	-	PK7N[5]	PK7N[4]	PK7N[3]	PK7N[2]	PK7N[1]	PK7N[0]	
11th parameter	1	↑	1	-	-	-	PK8N[5]	PK8N[4]	PK8N[3]	PK8N[2]	PK8N[1]	PK8N[0]	
12th parameter	1	↑	1	-	-	-	PK9[5]	PK9N[4]	PK9N[3]	PK9N[2]	PK9N[1]	PK9N[0]	
13th parameter	1	↑	1	-	-	-	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]	
14th parameter	1	↑	1	-	-	-	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]	
15th parameter	1	↑	1	-	-	-	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]	
16th parameter	1	↑	1	-	-	-	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]	

Description

Register Group	Negative Polarity	Set-up Contents
High level adjustment	VRF0N[5:0]	Variable resistor VRHN
Mid level adjustment	SELV0N[5:0]	The voltage of V0 grayscale is selected by the 64 to 1 selector
	SELV1N[5:0]	The voltage of V1 grayscale is selected by the 64 to 1 selector
	PK0N[5:0]	The voltage of V3 grayscale is selected by the 64 to 1 selector
	PK1N[5:0]	The voltage of V4 grayscale is selected by the 64 to 1 selector
	PK2N[5:0]	The voltage of V12 grayscale is selected by the 64 to 1 selector
	PK3N[5:0]	The voltage of V20 grayscale is selected by the 64 to 1 selector
	PK4N[5:0]	The voltage of V28 grayscale is selected by the 64 to 1 selector
	PK5N[5:0]	The voltage of V36 grayscale is selected by the 64 to 1 selector
	PK6N[5:0]	The voltage of V44 grayscale is selected by the 64 to 1 selector
	PK7N[5:0]	The voltage of V52 grayscale is selected by the 64 to 1 selector
	PK8N[5:0]	The voltage of V56 grayscale is selected by the 64 to 1 selector
	PK9N[5:0]	The voltage of V60 grayscale is selected by the 64 to 1 selector
	SELV62N[5:0]	The voltage of V62 grayscale is selected by the 64 to 1 selector
	SELV63N[5:0]	The voltage of V63 grayscale is selected by the 64 to 1 selector
Low level adjustment	VOS0N[5:0]	Variable resistor VRLN

Flow Chart	 GMCTRN1 1st Parameter 2nd Parameter Legend Command Parameter Display Action Mode Sequential transter

11 Power Structure

11.1 Driver IC Operating Voltage Specification

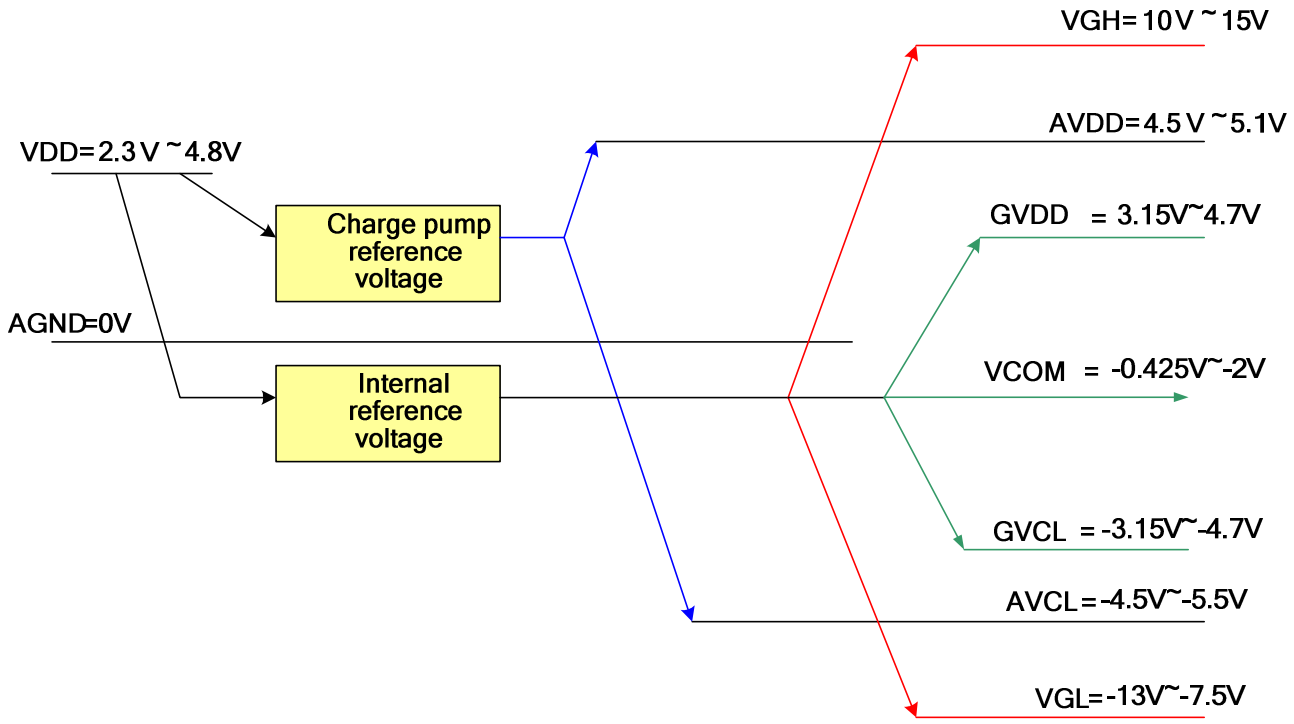
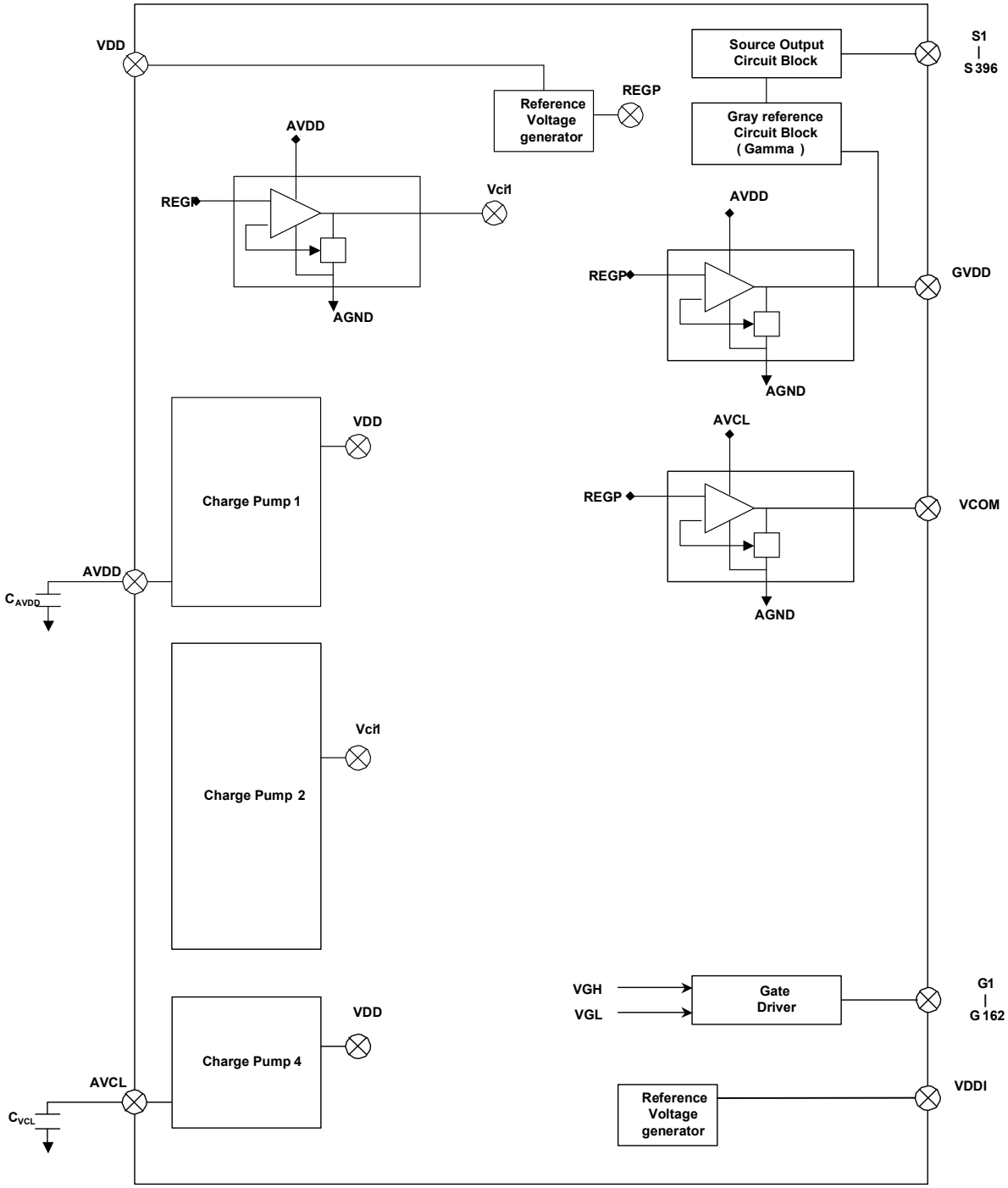


Fig 11.1.1 Power Booster Level

11.2 Power Booster Circuit



11.2.1 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Rated (Min) Voltage	Typical capacitance value
AVDD	Connect to Capacitor: AVDD -------||-------- GND	6.3V	1.0 uF
AVCL	Connect to Capacitor: AVCL -------||-------- GND	6.3V	1.0 uF

12 Gamma structure

12.1 TRUCTURE OF GRAYSCALE AMPLIFIER

16 voltage levels (VIN0-VIN15) between GVDD and VSS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.

12.2 Gamma Voltage Formula (Positive/ Negative Polarity)

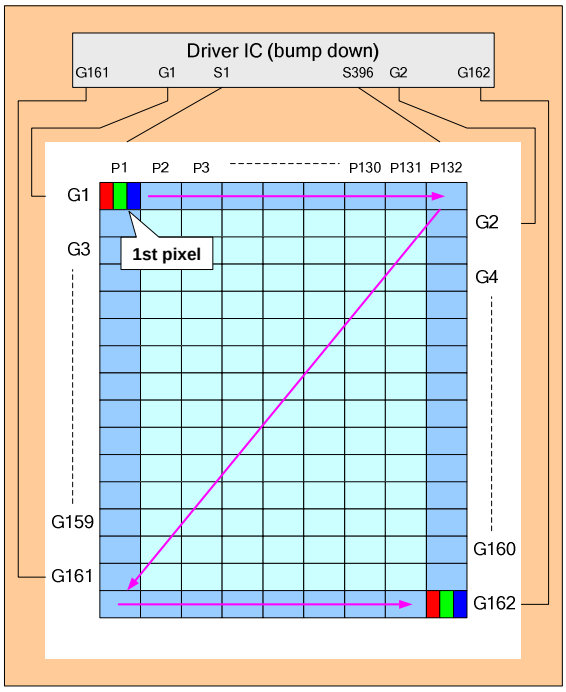
Gray Level	Voltage Formula (Positive)	Voltage Formula (Negative)
0	VINP0	VINP0
1	VINP1	VINP1
2	VINP2	VINP2
3	VINP3	VINP3
4	VINP4	VINP4
5	V4-(V4-V12)*(4/32)	V4-(V4-V12)*(4/32)
6	V4-(V4-V12)*(8/32)	V4-(V4-V12)*(8/32)
7	V4-(V4-V12)*(12/32)	V4-(V4-V12)*(12/32)
8	V4-(V4-V12)*(16/32)	V4-(V4-V12)*(16/32)
9	V4-(V4-V12)*(20/32)	V4-(V4-V12)*(20/32)
10	V4-(V4-V12)*(24/32)	V4-(V4-V12)*(24/32)
11	V4-(V4-V12)*(28/32)	V4-(V4-V12)*(28/32)
12	VINP5	VINP5
13	V12-(V12-V20)*(4/32)	V12-(V12-V20)*(4/32)
14	V12-(V12-V20)*(8/32)	V12-(V12-V20)*(8/32)
15	V12-(V12-V20)*(12/32)	V12-(V12-V20)*(12/32)
16	V12-(V12-V20)*(16/32)	V12-(V12-V20)*(16/32)
17	V12-(V12-V20)*(20/32)	V12-(V12-V20)*(20/32)
18	V12-(V12-V20)*(24/32)	V12-(V12-V20)*(24/32)
19	V12-(V12-V20)*(28/32)	V12-(V12-V20)*(28/32)
20	VINP6	VINP6
21	V20-(V20-V28)*(4/32)	V20-(V20-V28)*(4/32)
22	V20-(V20-V28)*(8/32)	V20-(V20-V28)*(8/32)
23	V20-(V20-V28)*(12/32)	V20-(V20-V28)*(12/32)
24	V20-(V20-V28)*(16/32)	V20-(V20-V28)*(16/32)
25	V20-(V20-V28)*(20/32)	V20-(V20-V28)*(20/32)
26	V20-(V20-V28)*(24/32)	V20-(V20-V28)*(24/32)
27	V20-(V20-V28)*(28/32)	V20-(V20-V28)*(28/32)
28	VINP7	VINP7
29	V28-(V28-V36)* (4/32)	V28-(V28-V36)* (4/32)
30	V28-(V28-V36)* (8/32)	V28-(V28-V36)* (8/32)
31	V28-(V28-V36)* (12/32)	V28-(V28-V36)* (12/32)
32	V28-(V28-V36)* (16/32)	V28-(V28-V36)* (16/32)
33	V28-(V28-V36)* (20/32)	V28-(V28-V36)* (20/32)
34	V28-(V28-V36)* (24/32)	V28-(V28-V36)* (24/32)
35	V28-(V28-V36)* (28/32)	V28-(V28-V36)* (28/32)

36	VINP8	VINP8
37	V36-(V36-V44)*(4/32)	V36-(V36-V44)*(4/32)
38	V36-(V36-V44)*(8/32)	V36-(V36-V44)*(8/32)
39	V36-(V36-V44)*(12/32)	V36-(V36-V44)*(12/32)
40	V36-(V36-V44)*(16/32)	V36-(V36-V44)*(16/32)
41	V36-(V36-V44)*(20/32)	V36-(V36-V44)*(20/32)
42	V36-(V36-V44)*(24/32)	V36-(V36-V44)*(24/32)
43	V36-(V36-V44)*(28/32)	V36-(V36-V44)*(28/32)
44	VINP9	VINP9
45	V44-(V44-V52)*(4/32)	V44-(V44-V52)*(4/32)
46	V44-(V44-V52)*(8/32)	V44-(V44-V52)*(8/32)
47	V44-(V44-V52)*(12/32)	V44-(V44-V52)*(12/32)
48	V44-(V44-V52)*(16/32)	V44-(V44-V52)*(16/32)
49	V44-(V44-V52)*(20/32)	V44-(V44-V52)*(20/32)
50	V44-(V44-V52)*(24/32)	V44-(V44-V52)*(24/32)
51	V44-(V44-V52)*(28/32)	V44-(V44-V52)*(28/32)
52	VINP10	VINP10
53	V52-(V52-V56)*(1/4)	V52-(V52-V56)*(1/4)
54	V52-(V52-V56)*(2/4)	V52-(V52-V56)*(2/4)
55	V52-(V52-V56)*(3/4)	V52-(V52-V56)*(3/4)
56	VINP11	VINP11
57	V56-(V56-V60)*(1/4)	V56-(V56-V60)*(1/4)
58	V56-(V56-V60)*(2/4)	V56-(V56-V60)*(2/4)
59	V56-(V56-V60)*(3/4)	V56-(V56-V60)*(3/4)
60	VINP12	VINP12
61	VINP13	VINP13
62	VINP14	VINP14
63	VINP15	VINP15

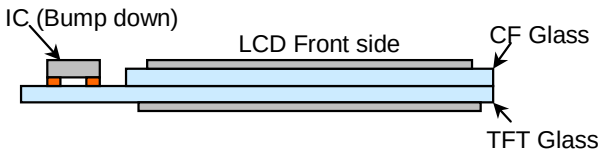
13 Example Connection with Panel direction and Different Resolution

13.1 Application of connection with panel direction

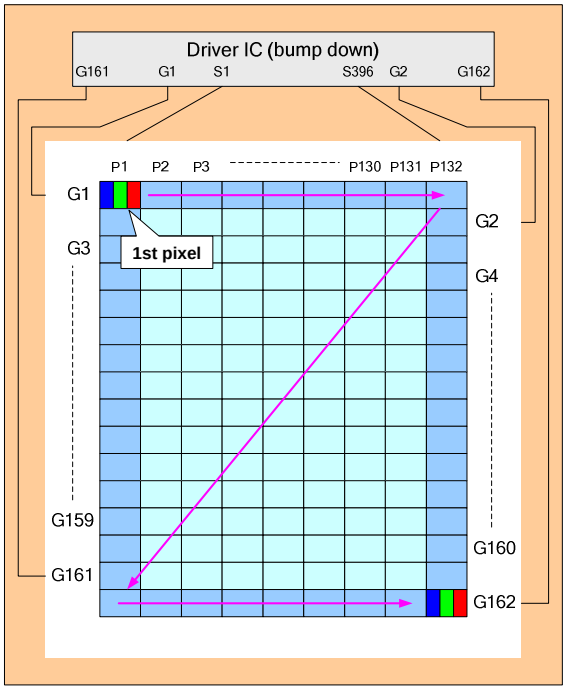
Case 1: (This is default case)
- 1st Pixel is at Left Top of the panel
- RGB filter order = RGB



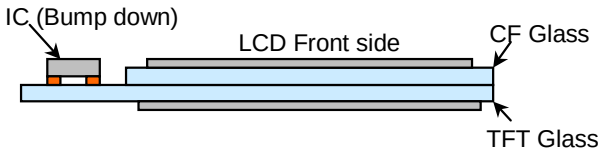
- Direction default setting (H/W)
SMX = '0'
SMY = '0'
SRGB = '0'
S1 = Filter R
S2 = Filter G
S3 = Filter B
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



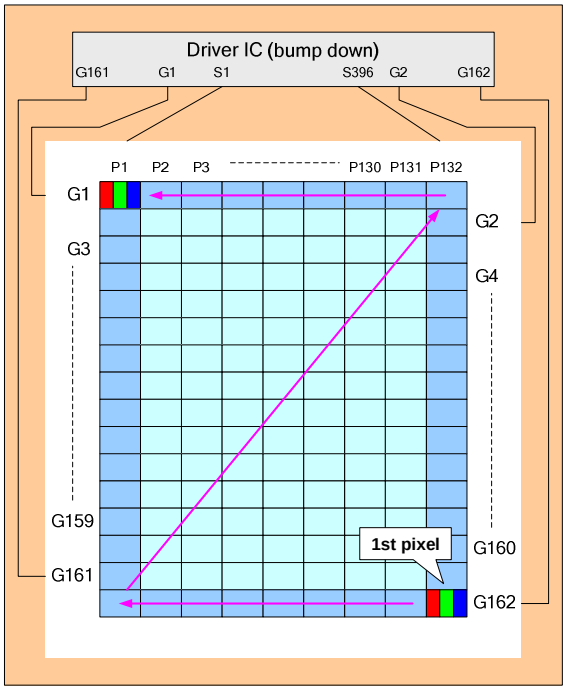
Case 2:
- 1st Pixel is at Left Top of the panel
- RGB filter order = BGR



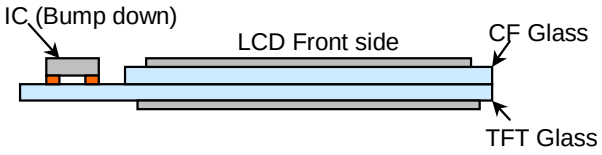
- Direction default setting (H/W)
SMX = '0'
SMY = '0'
SRGB = '1'
S1 = Filter B
S2 = Filter G
S3 = Filter R
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



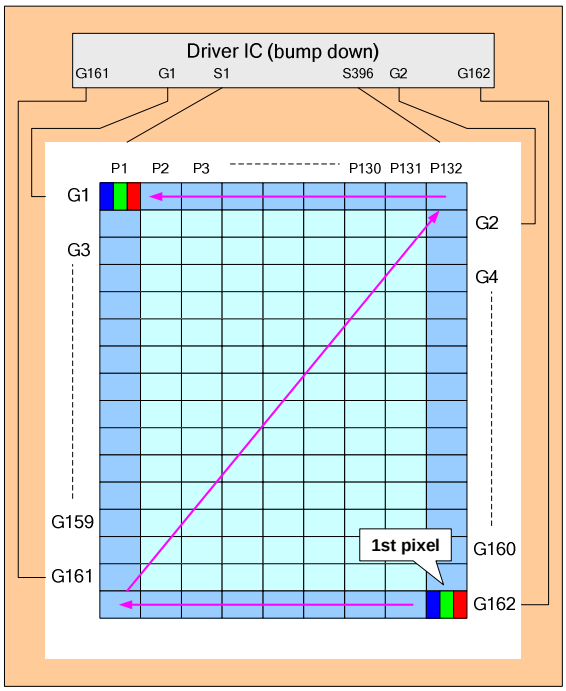
Case 3:
- 1st Pixel is at Right Bottom of the panel
- RGB filter order = RGB



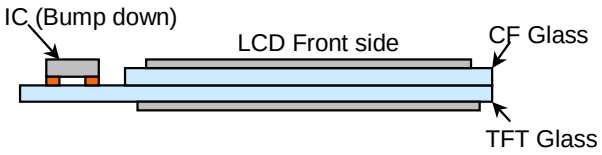
- Direction default setting (H/W)
SMX = '1'
SMY = '1'
SRGB = '0'
S1 = Filter R
S2 = Filter G
S3 = Filter B
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



Case 4:
- 1st Pixel is at Right Bottom of the panel
- RGB filter order = BGR



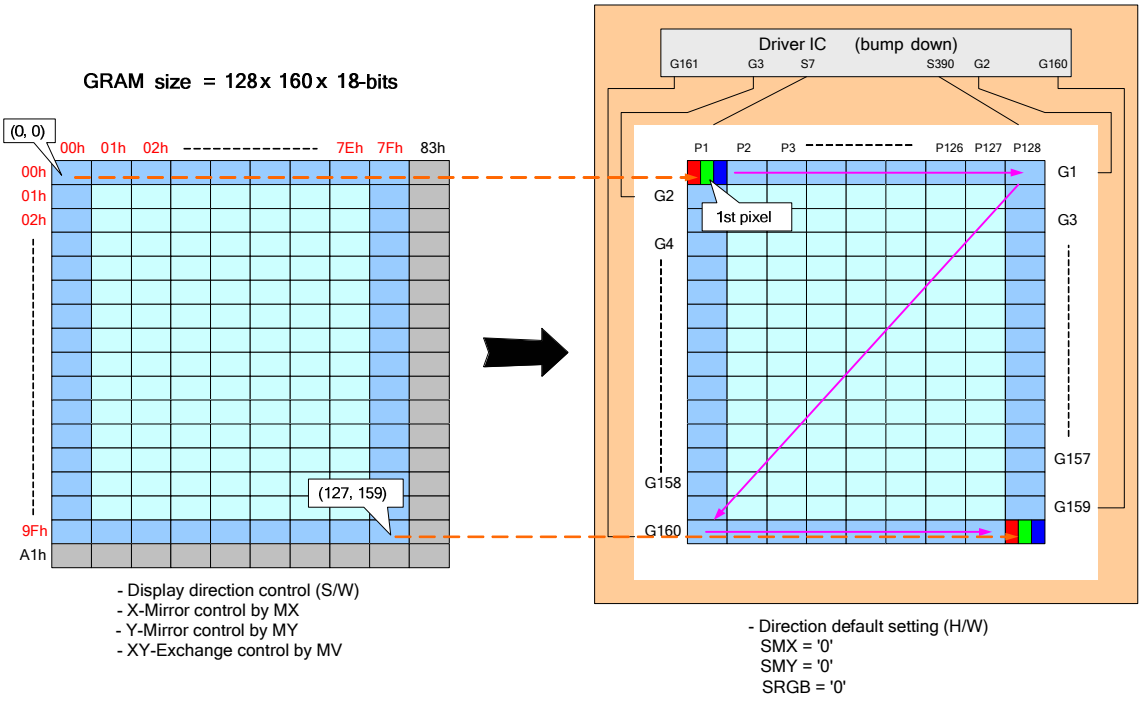
- Direction default setting (H/W)
SMX = '1'
SMY = '1'
SRGB = '1'
S1 = Filter B
S2 = Filter G
S3 = Filter R
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



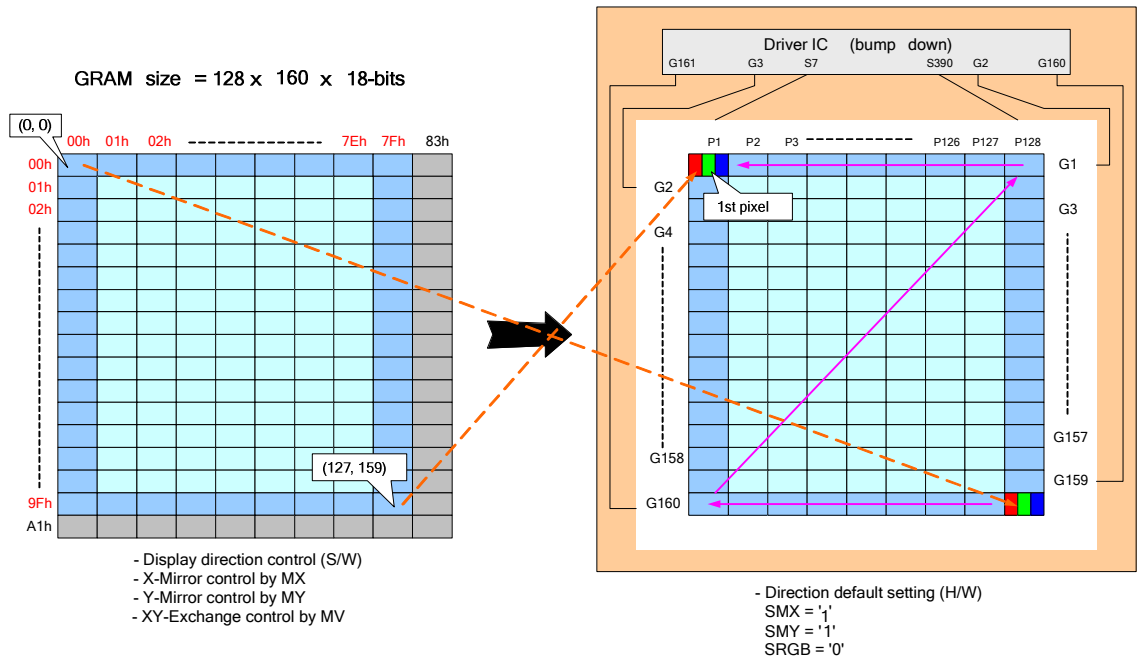
13.2 Application of connection with Different resolution

Case1 of Resolution (128RGB x 160) (GM[1:0] = “11”)
RAM size=128 x 160 x 18-bit (Used)
Display size = 128RGB x 160

1). Example for SMX=SMY=’0’

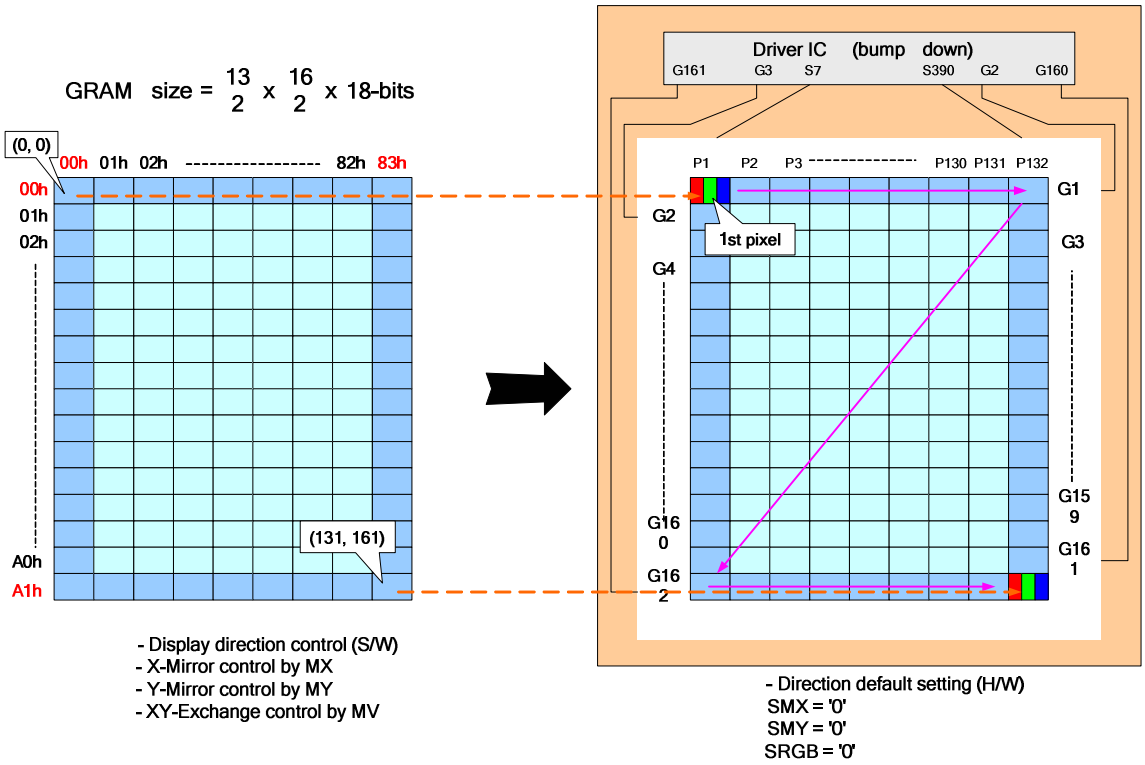


2). Example for SMX=SMY=’1’

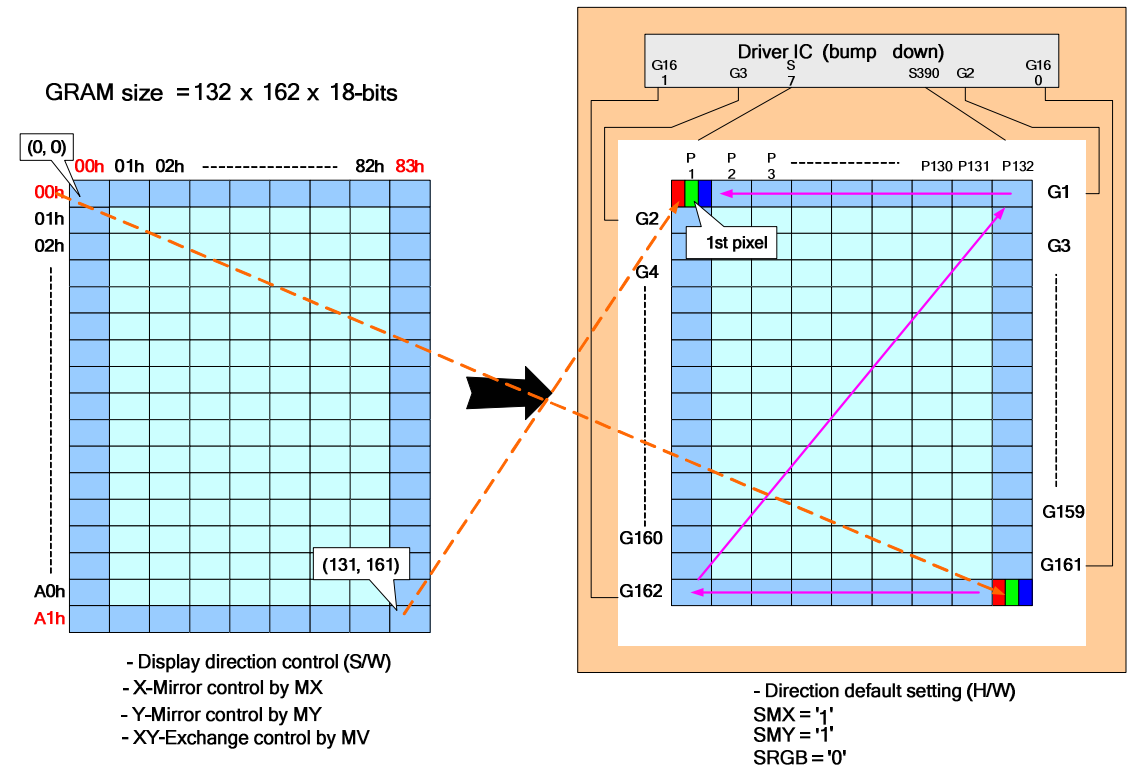


Case2 of Resolution (132RGB x 162) (GM[1:0] = “00”)
RAM size=132 x 162 x 18-bit (Used)
Display size = 132RGB x 162

1). Example for SMX=SMY=’0’



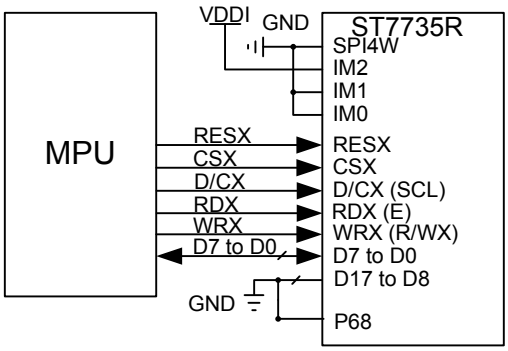
2). Example for SMX=SMY=’1’



13.3 Microprocessor Interface applications

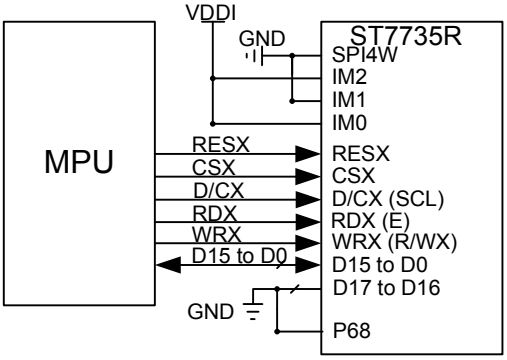
13.3.1 8080-Series MCU Interface for 8-bit data bus (P68=0, IM2, IM1, IM0="100")

80 Serial MPU 8-Bit Bus



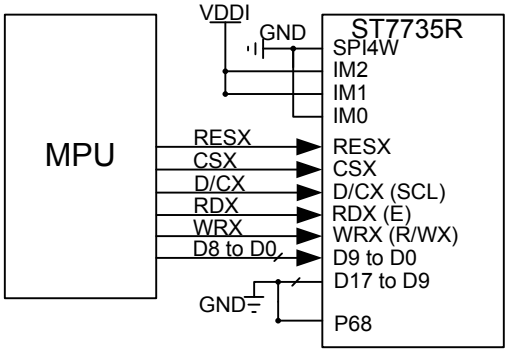
13.3.2 8080-Series MCU Interface for 16-bit data bus (P68=0, IM2, IM1, IM0="101")

80 Serial MPU 16-Bit Bus

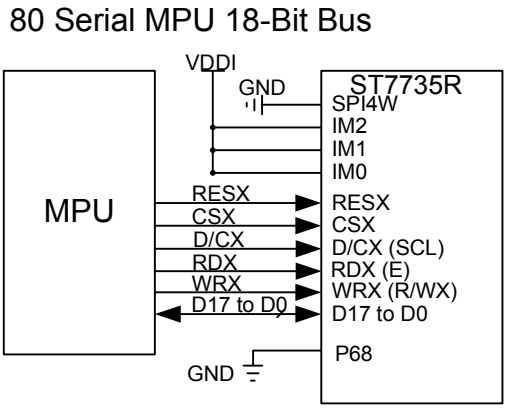


13.3.3 8080-Series MCU Interface for 9-bit data bus (P68=0, IM2, IM1, IM0="110")

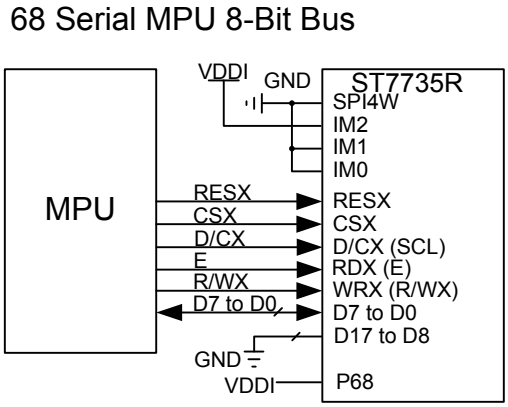
80 Serial MPU 9-Bit Bus



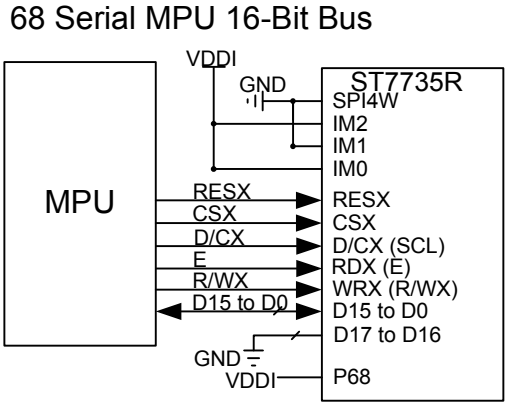
13.3.4 8080-Series MCU Interface for 18-bit data bus (P68=0, IM2, IM1, IM0="111")



13.3.5 6800-Series MCU Interface for 8-bit data bus (P68=1, IM2, IM1, IM0="100")

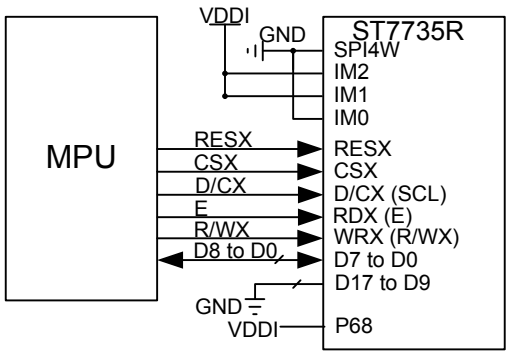


13.3.6 6800-Series MCU Interface for 16-bit data bus (P68=1, IM2, IM1, IM0="101")



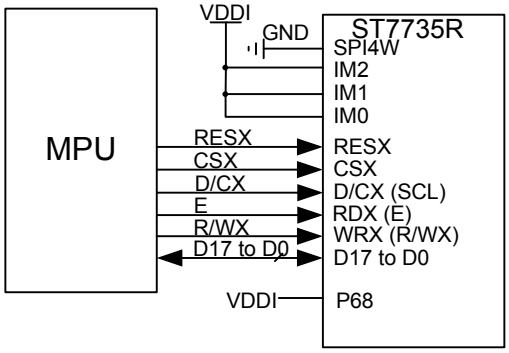
13.3.7 6800-Series MCU Interface for 9-bit data bus (P68=1, IM2, IM1, IM0=”110”)

68 Serial MPU 9-Bit Bus



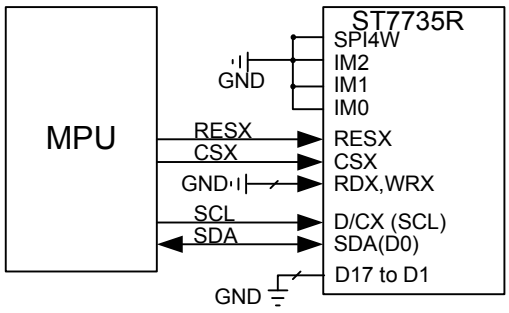
13.3.8 6800-Series MCU Interface for 18-bit data bus (P68=1, IM2, IM1, IM0=”111”)

68 Serial MPU 18-Bit Bus



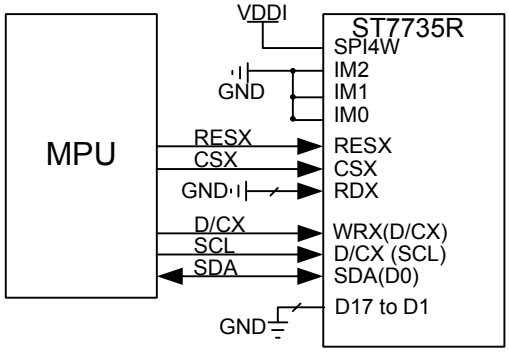
13.3.9 3-Line serial MCU Interface (IM2, IM1, IM0=”000”, SPI4W=0)

3-Pin Serial Mode



13.3.10 4-Line serial MCU Interface (IM2, IM1, IM0=”000”, SPI4W=1)

4-Pin Serial Mode



14 Revision History

ST7735R Specification Revision History		
Version	**Date**	**Description**
V0.1	2009/07/10	First issue.
V0.2	2009/08/05	Modify VGH, VGL PAD location (P7) Add TESEL pin description. (P16) Modify command DFh (P147) Modify AVDD range 4.5~5.1 (P152)