

COMSM1302

Overview of Computer Architecture

Lecture 6

Memory (SRAM, DRAM)

In this lecture

Foundations

- Data representation, logic, Boolean algebra.

Building blocks

- Transistors, transistor based logic, simple devices, storage.

Modules

- **Memory**, simple controllers, FSMs, processors and execution.

Programming

- Machine code, assembly, high-level languages, compilers.

Wrap-up

- Operating systems, energy aware computing.



In this lecture

- Memory, the abstract view.
 - The top-level view of how we use memory.
- Two types of memory cell.
 - SRAM
 - used on-chip, e.g. cache
 - DRAM
 - used off-chip, e.g. main memory
- Practical aspects.



Source: https://en.wikipedia.org/wiki/Random-access_memory



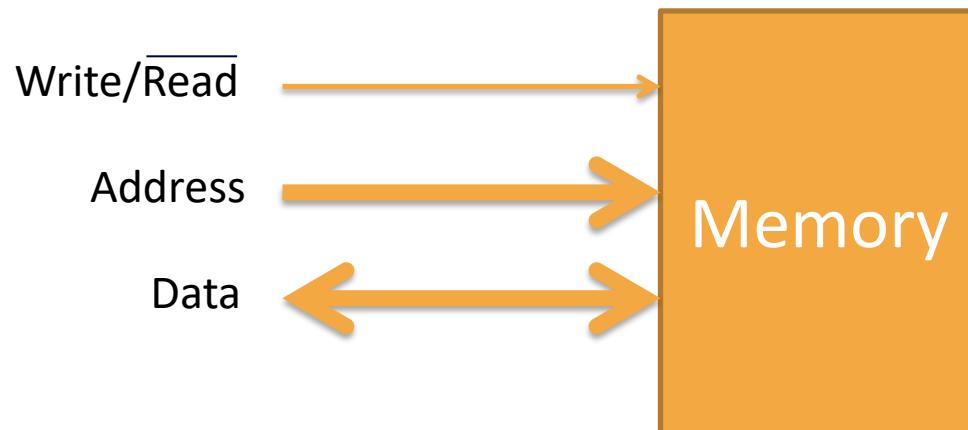
Memory, the abstract view

- We are already familiar with latches and flip-flops.
 - Level and edge sensitive devices for storing data.
- But there are better ways of building large banks of memory.
 - Essential to building a complex processor that performs well.



Memory, the abstract view

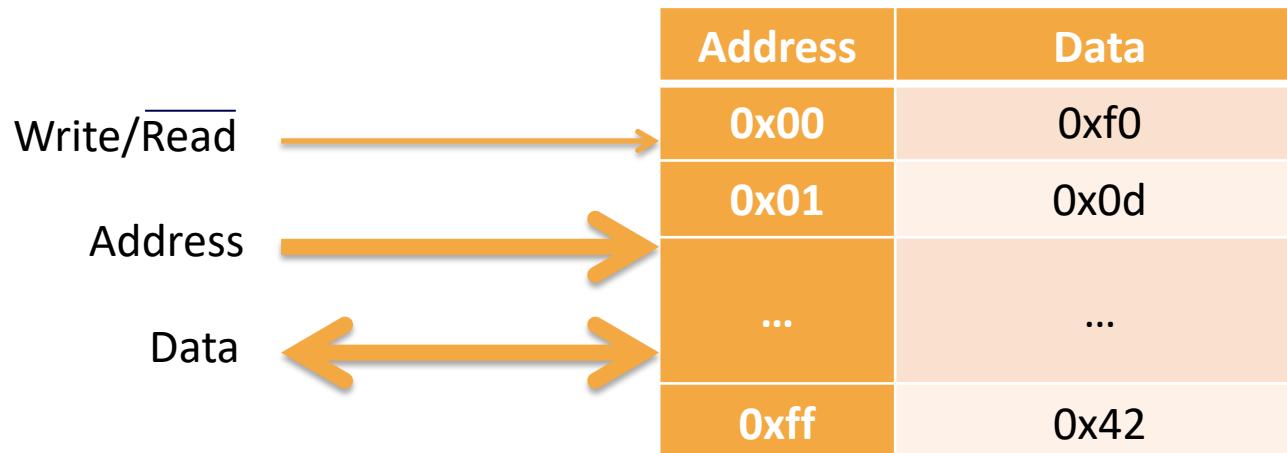
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Memory, the abstract view

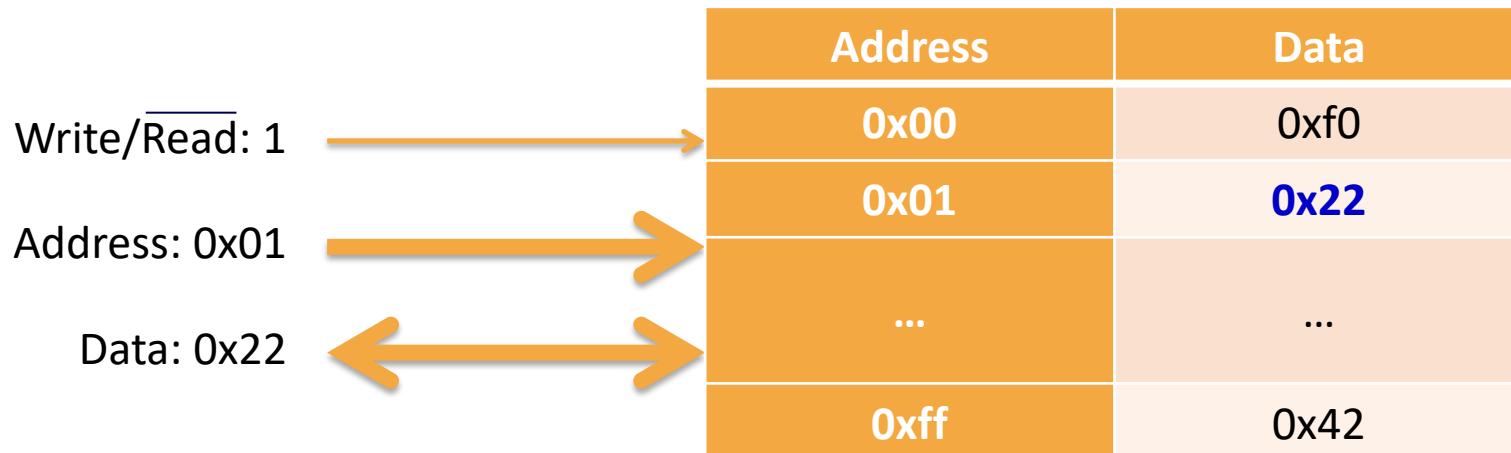


- A memory is like a series of pigeon holes (message boxes).
 - The **number** of pigeon holes **is limited**.
 - Each pigeon hole can contain a **fixed amount of data**.
 - We can **look at the contents** of a pigeon hole.
 - Or we can **replace the contents** with something new.



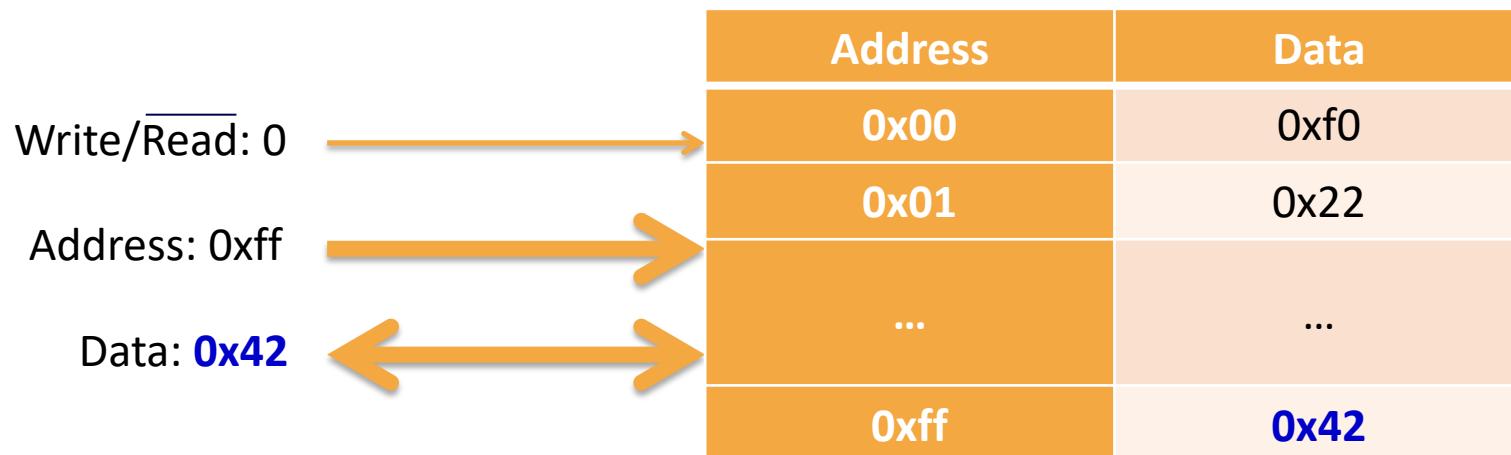
Writing to memory

- Set the control signal to 1 (write).
- Set the address wires to the location we want to use.
- Set the data wires to the value we want to store.
- Hold for the required time (clock edge).

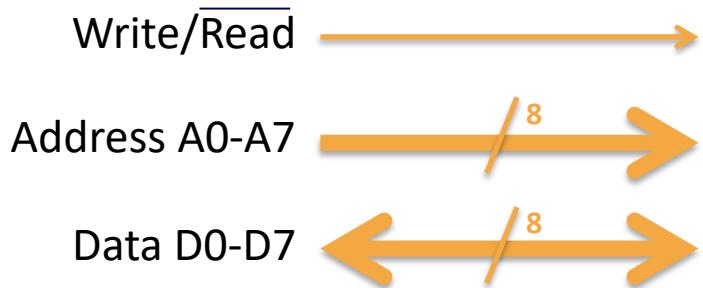


Reading from memory

- Set the control signal to 0 (read).
- Set the address wires to the location we want to read.
- Hold for the required time.
- Data from the requested address appears on the data wires.



Signals, buses, directions



- Groups of wires serving the same purpose (e.g. address, data) can be combined.
 - The number of wires in a group may be denoted with a slash and number.
 - Or by other appropriate labelling.
- Signals may be *driven* (controlled, asserted) in one direction, or more.
 - Arrowheads indicate this.
- A group of signals is called a **bus**, e.g. **address bus or data bus**.





Random-access memory (RAM)

- ***Random access*** means that each memory cell can be read or written to in any order, no matter which cell was last accessed.
- Going back to single bits, what do we need in a RAM?
 - Data retention: **Keep** current value.
 - Data write: **Update** with a new value.
 - Data read: Present the stored value **when requested**.
- To provide a useful amount of storage we also need lots and **lots of memory cells**.



- Static Random Access Memory
 - Write a value to an SRAM cell, it **stays there** for **as long as power is supplied** to the cell.
- An SRAM module comprises:
 - The SRAM **cells**, units of storage
 - Surrounding **control logic** to allow updating and retrieving data from specified groups of cells.



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INDIVIDUAL MEMORY CELLS

SRAM cell

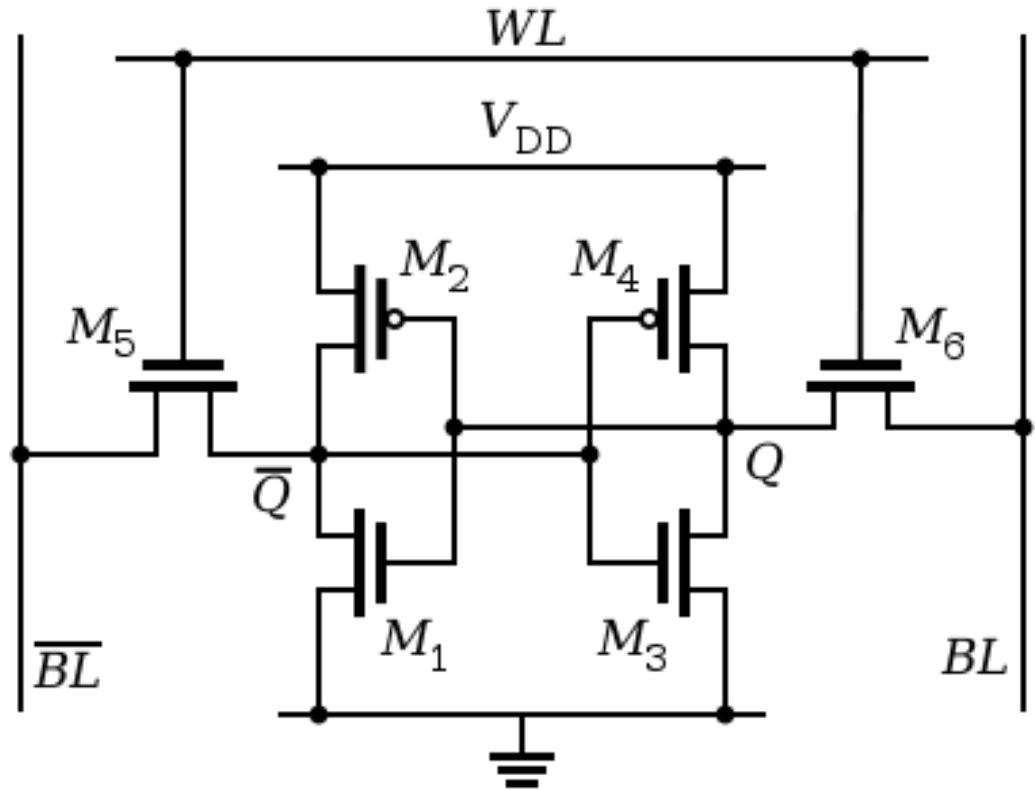
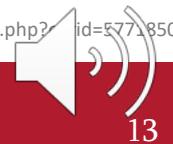


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SRAM cell

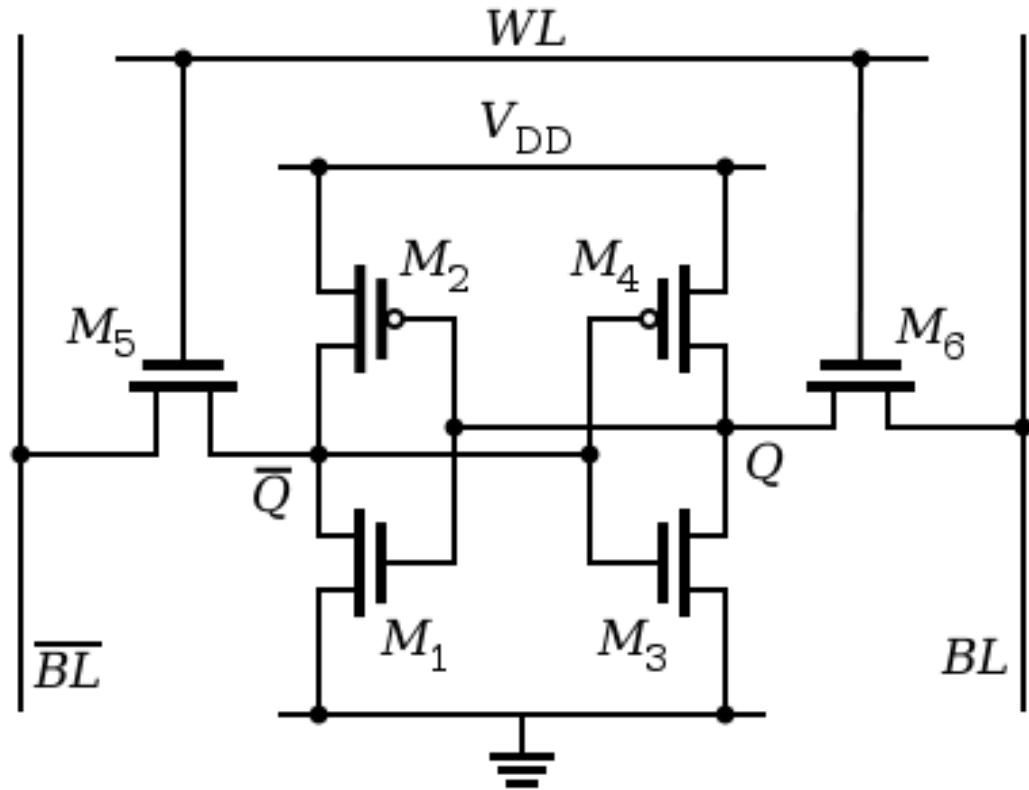
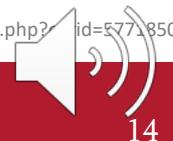
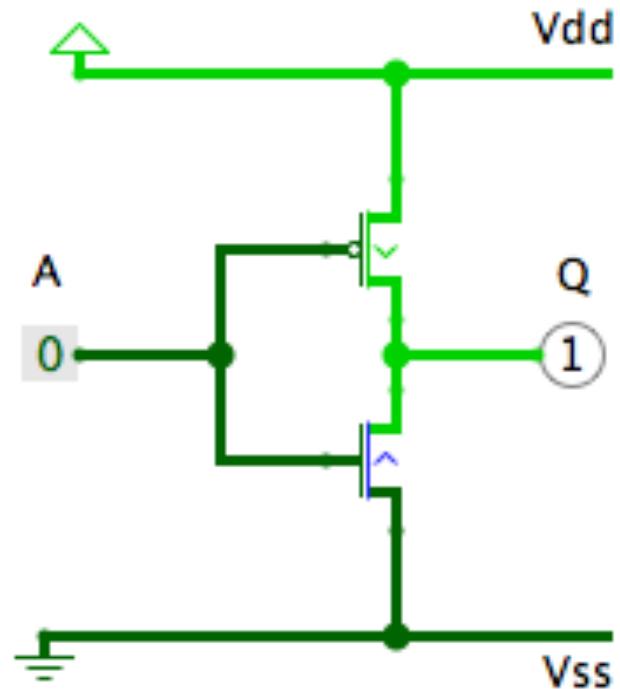
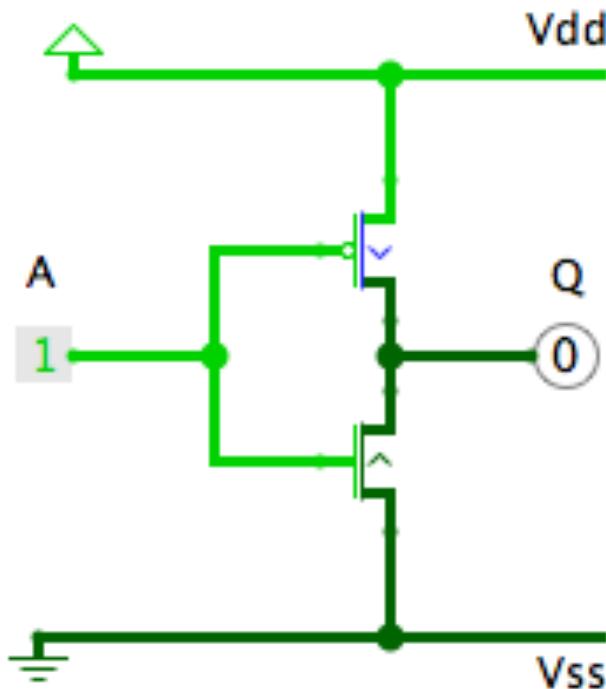


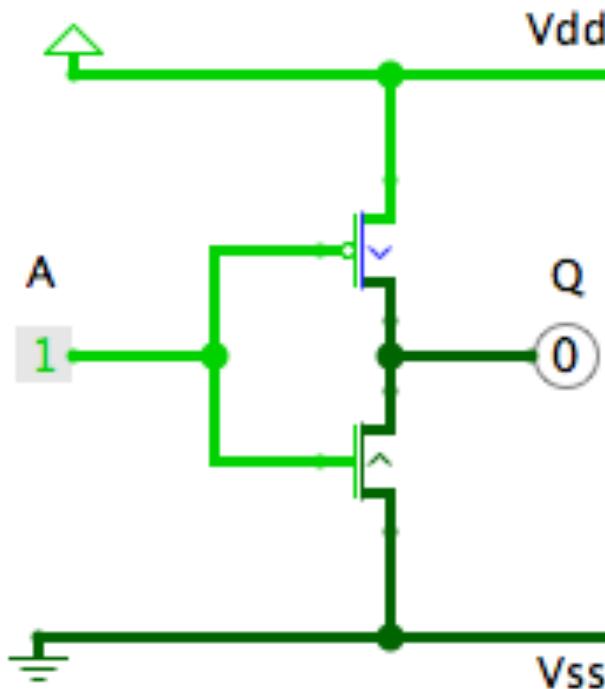
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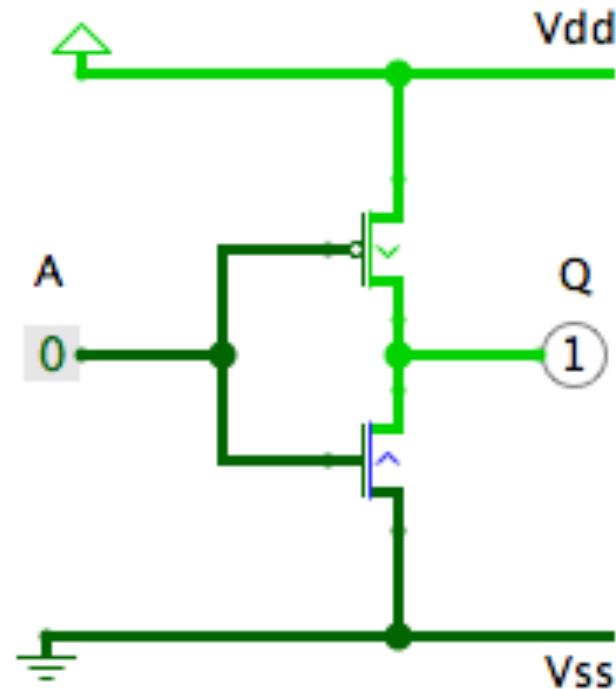
Can you find these?



The COMS inverter



NOT



NOT



SRAM cell

- Two inverters (NOT-gates)
- Two nMOS transistors and some signals
 - M5, M6 used for access
 - WL controls access
- Power

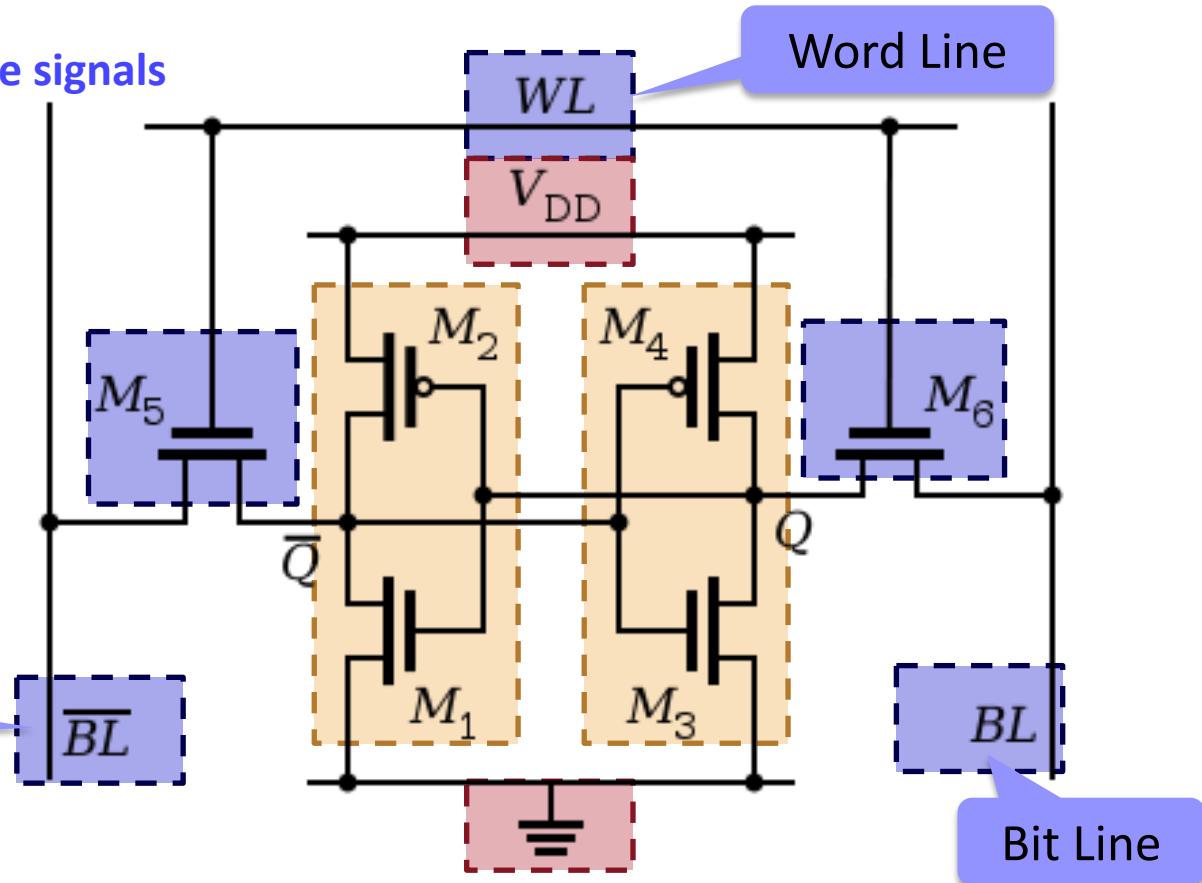


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SRAM cell

μ

- Two inverters (NOT-gates) based on transistors M1-M4

- Two nMOS transistors and some signals

- M5, M6 used for access
- WL controls access

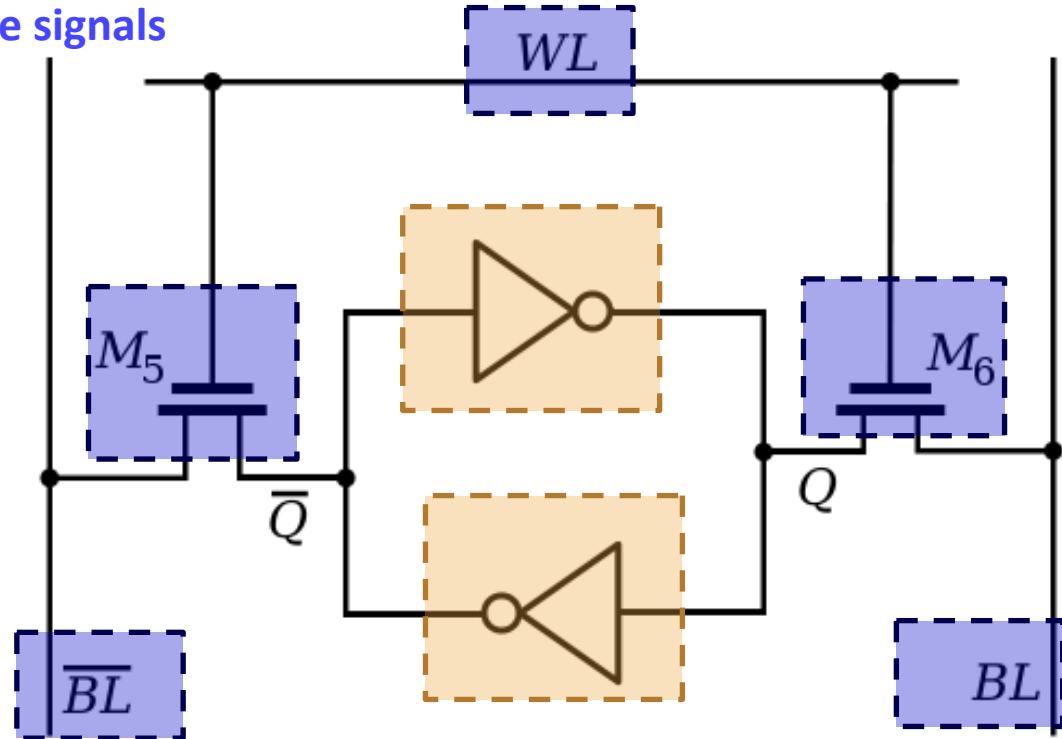
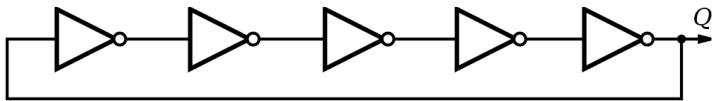


Image by Crystallizedcarbon, Inductiveload - Own work Based on File:SRAM Cell (6 Transistors).svg by Inductiveload, CC BY-SA 4.0, <https://commons.wikimedia.org/w/index.php?curid=35720494>



Cross-coupled inverters: Storage

- Remember the **Ring Oscillator**?
 - It needed an **odd-number of inverters**.
 - What happens with an **even number of inverters**?

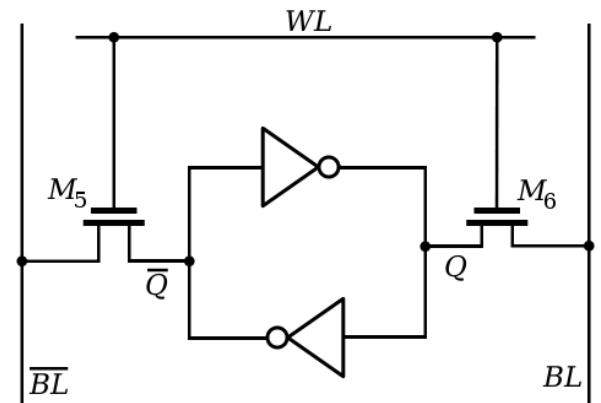
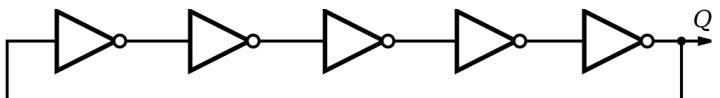




Cross-coupled inverters: Storage



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 - What happens with an **even number of inverters**?
 - Two cross-coupled inverters are central to the memory cell.
 - Simple inverter loop creates a *bi-stable* circuit.
 - Two stable states: $Q=1$ and $Q'=0$
 $Q=0$ and $Q'=1$





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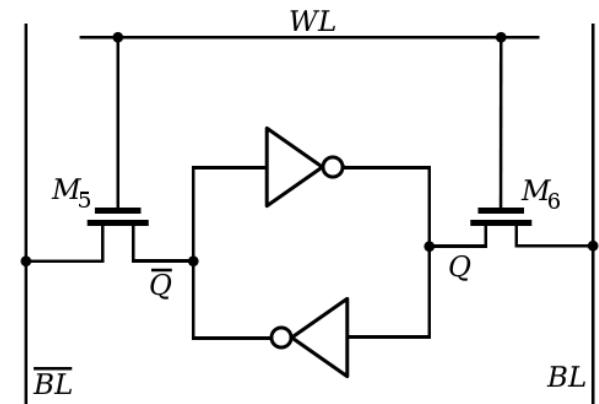
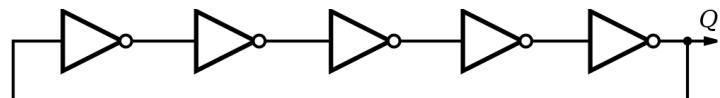
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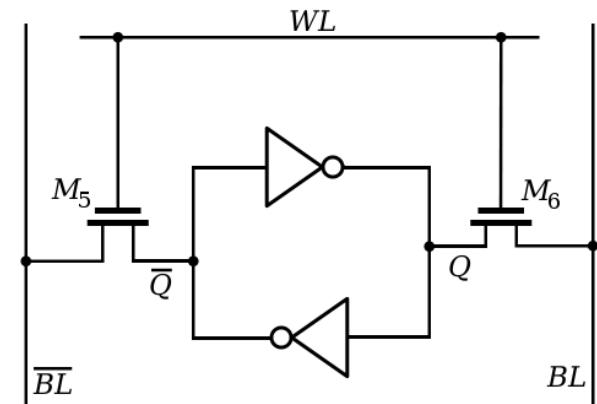
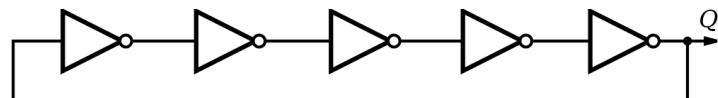
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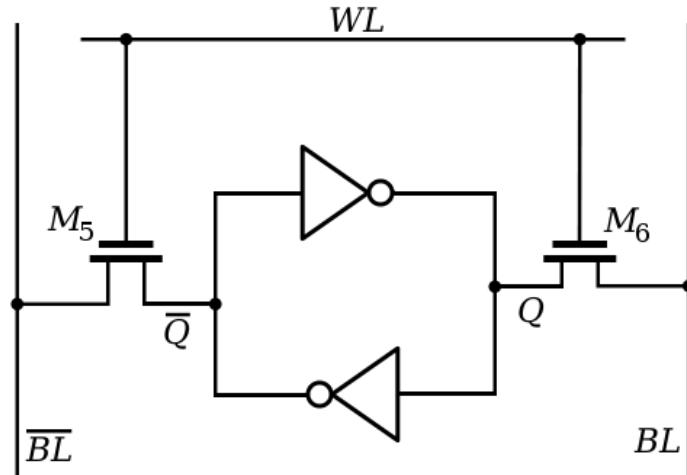
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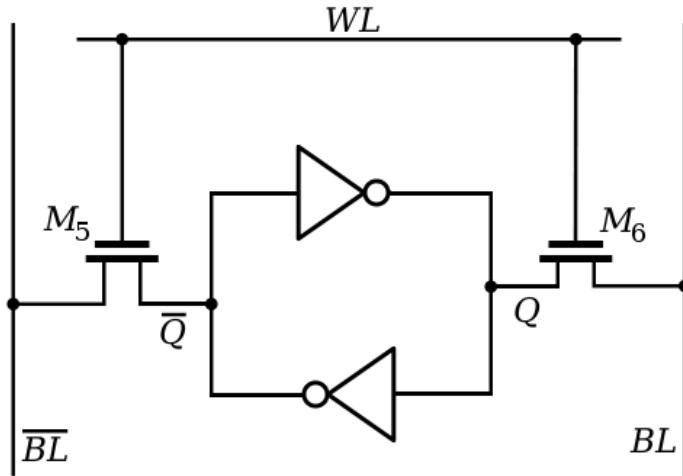
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SRAM reading



SRAM reading



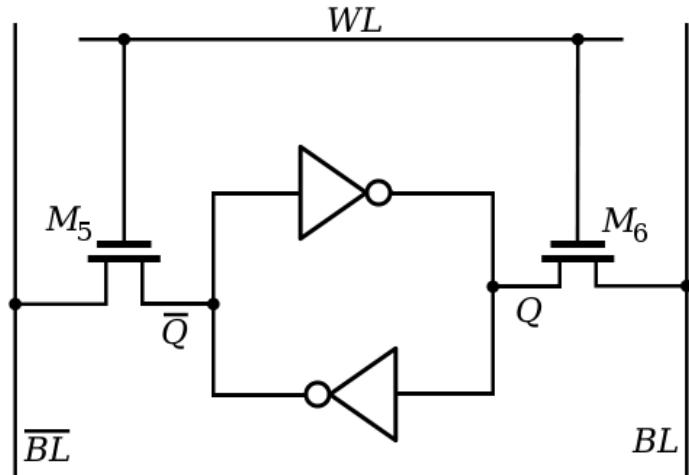
Read Q

Set BL and BL' both to a threshold voltage greater 0 and less than 1
(pre-charge)

Set WL to 1

BL = Q, BL' = Q'

SRAM writing



Write nQ

Set $BL = nQ$
 $BL' = nQ'$

Set WL to 1

$Q = nQ$
 $Q' = nQ'$



SRAM cell remarks

- More complicated conceptually than a flip-flop or latch.
 - Pre-charge.
 - Read/write on same wires.
- Only uses **6 transistors**.
 - Flip-flop can use between **12 and 30 transistors**.
 - 6T SRAM (standard SRAM cell).
 - There are other SRAM variants.
 - 4T SRAM.



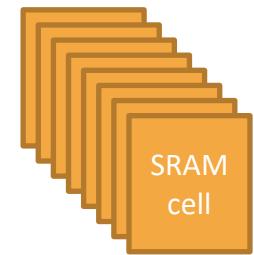
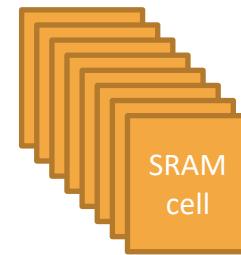
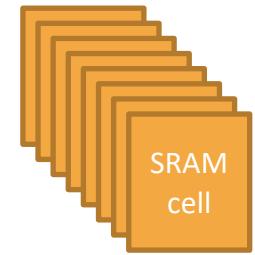
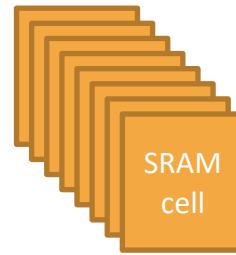


BUILDING A MEMORY FROM INDIVIDUAL CELLS



Building a memory from cells

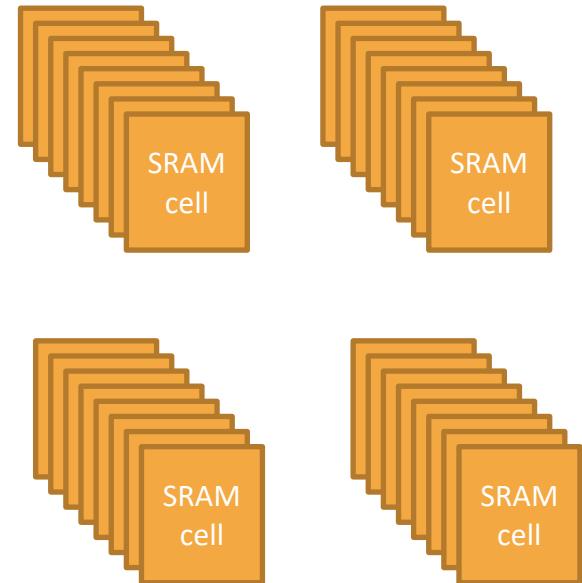
- How many bits per memory location (pigeon hole)?
 - One memory cell per bit
 - Each cell will read/write using the bit lines (BL and BL').
 - Multiple cells connected together can be addressed simultaneously to give one addressable memory location.





Building a memory from cells

- How many bits per memory location (pigeon hole)?
 - One memory cell per bit
 - Each cell will read/write using the bit lines (BL and BL').
 - Multiple cells connected together can be addressed simultaneously to give one addressable memory location.
- Control logic around the cells
 - determines which cells are being addressed, i.e. receive the WL signal,
 - ensures BL/BL' are driven correctly, and
 - decodes addresses.





Each SRAM cell is now a Bitcell

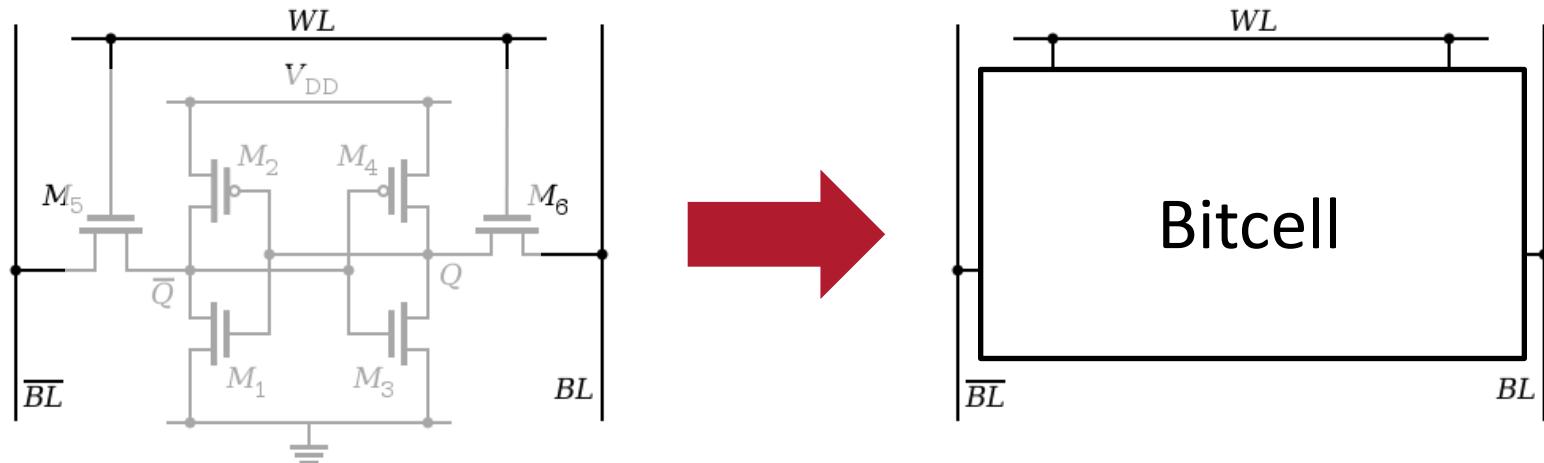
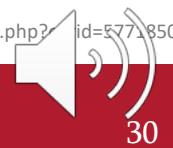
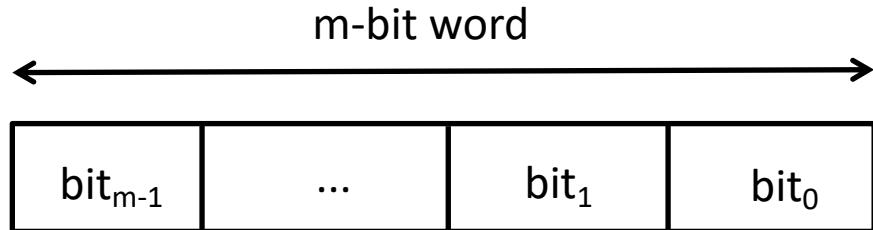


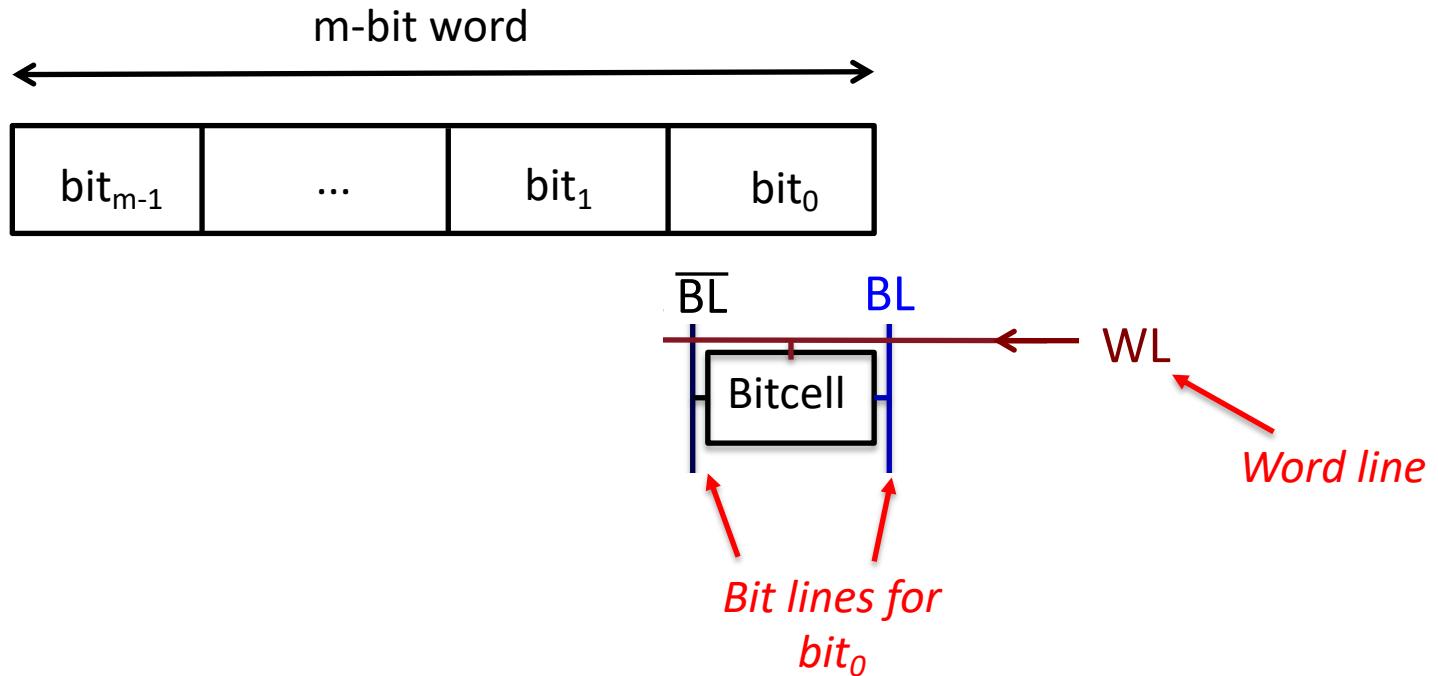
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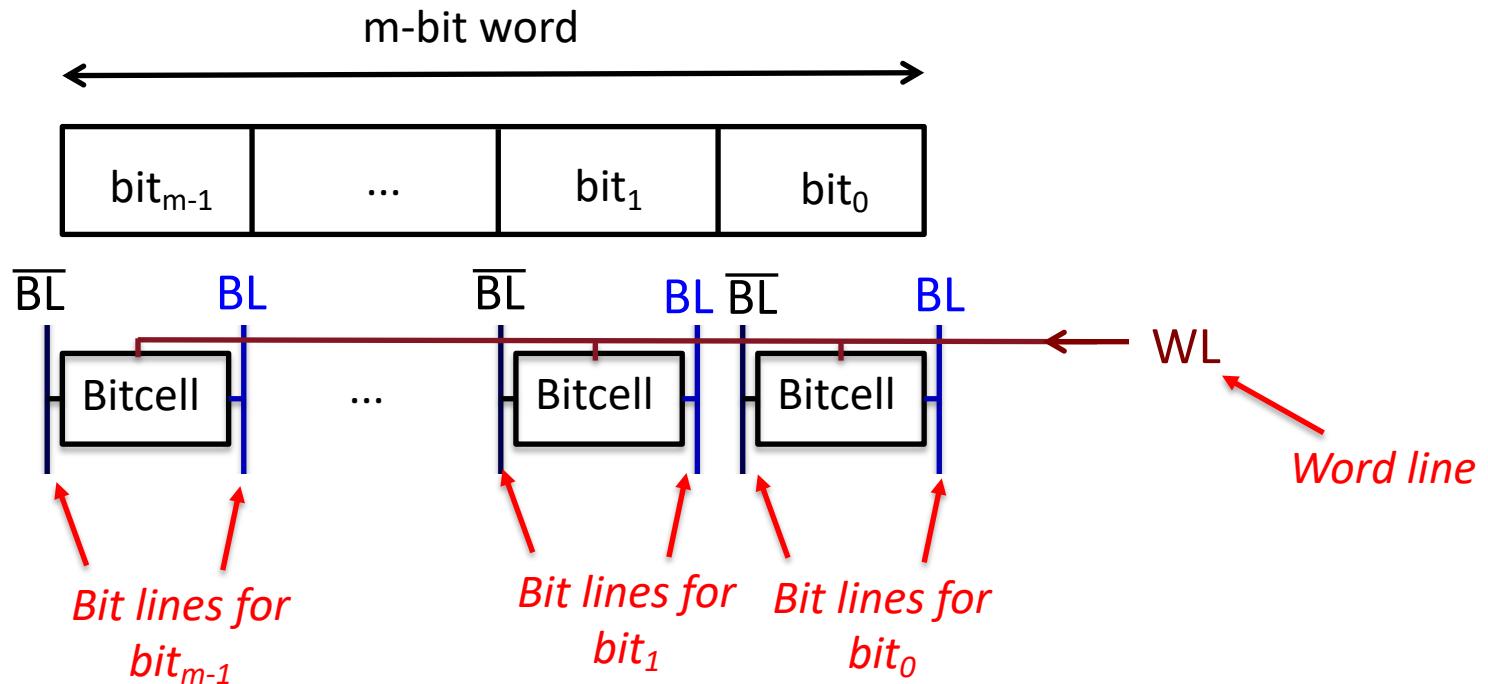
SRAM memory “Word”



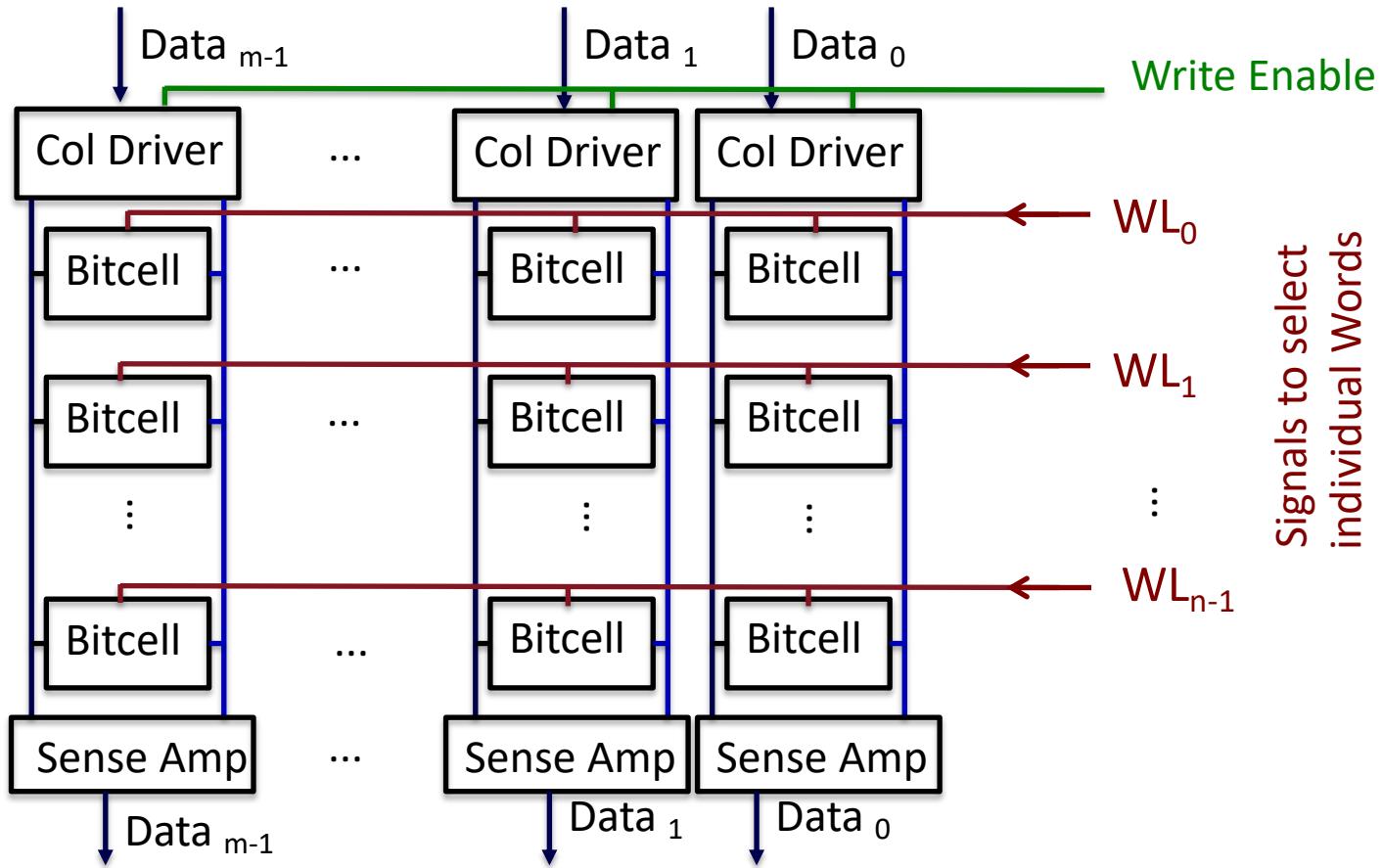
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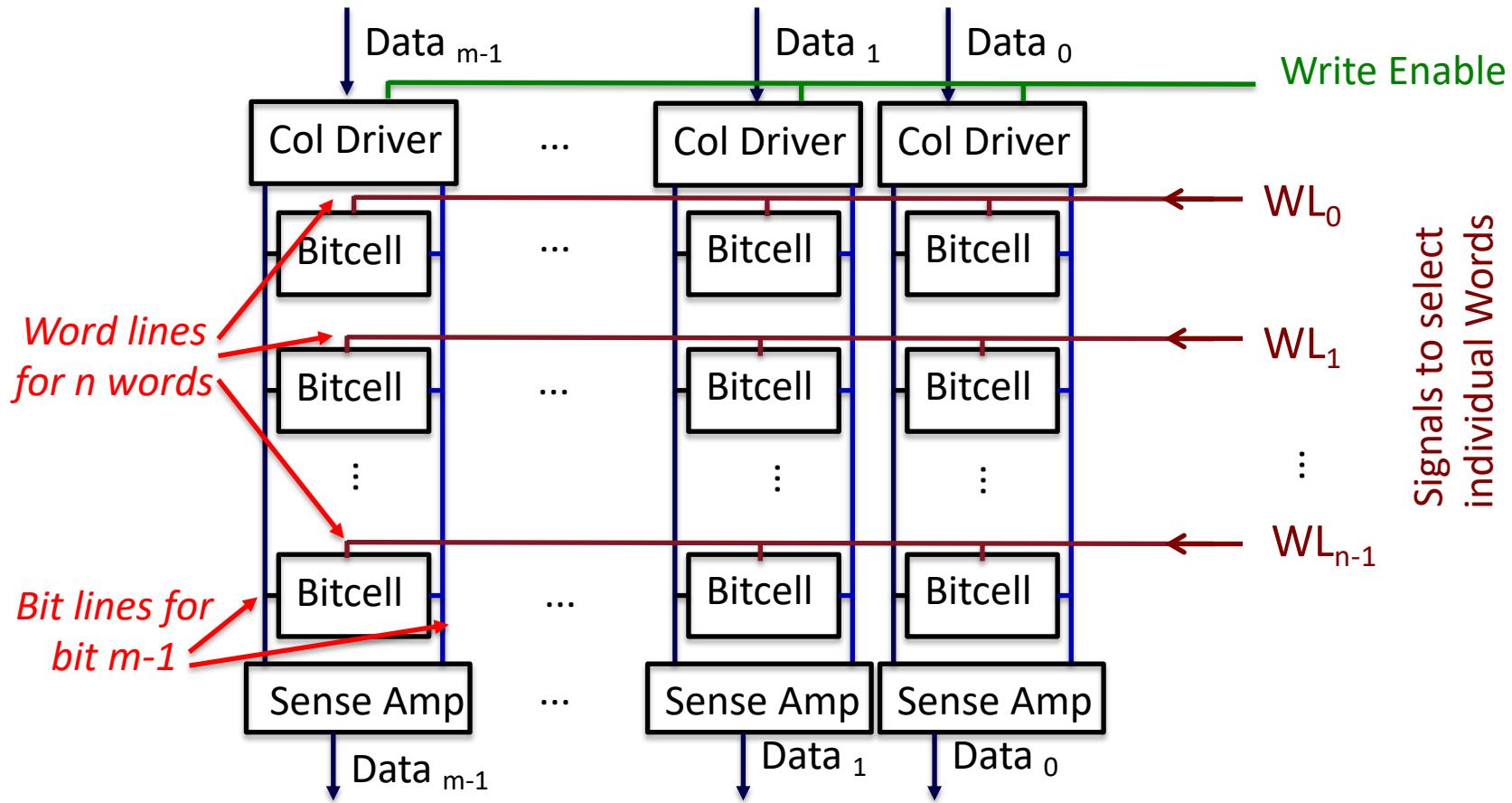
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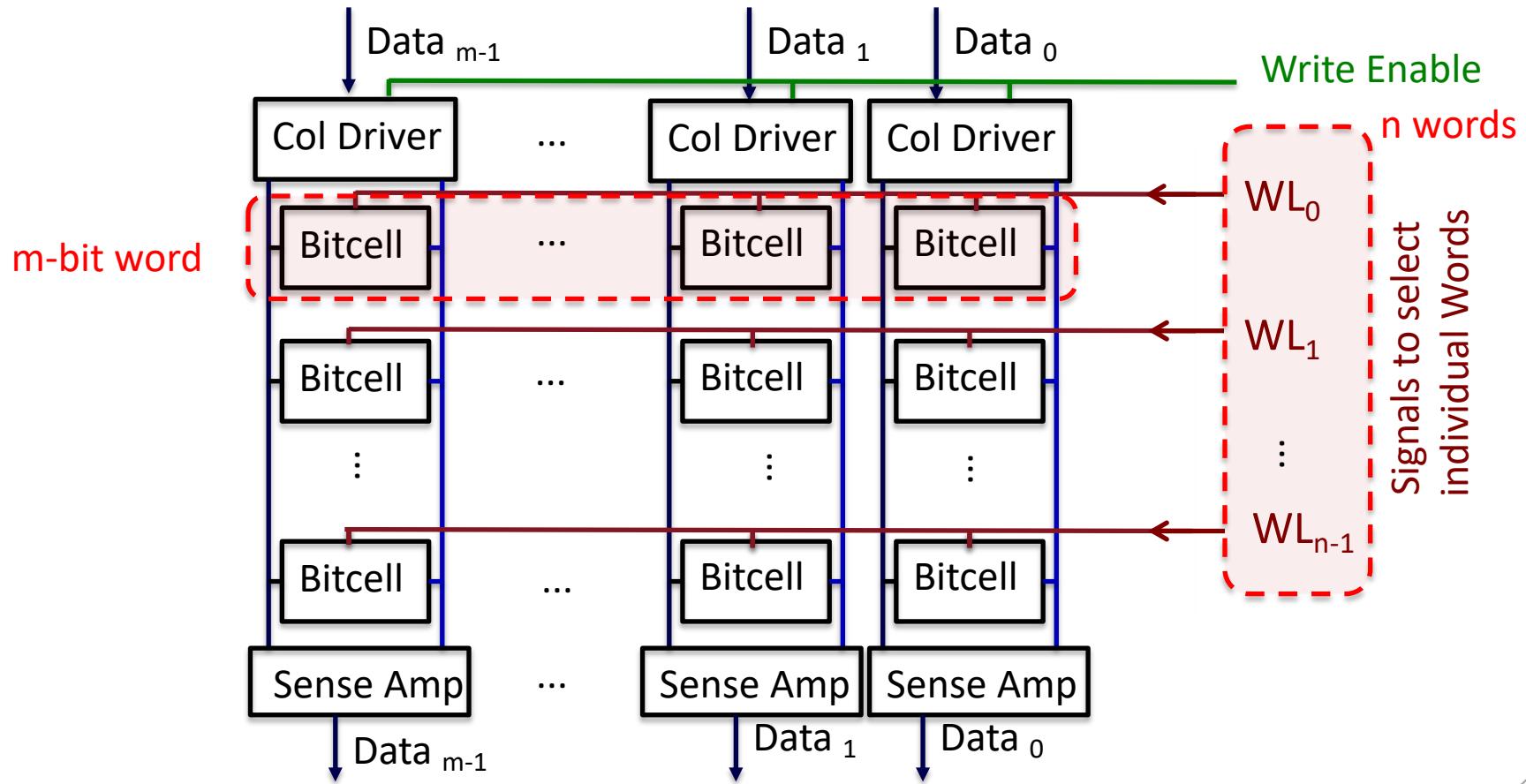
SRAM memory organization



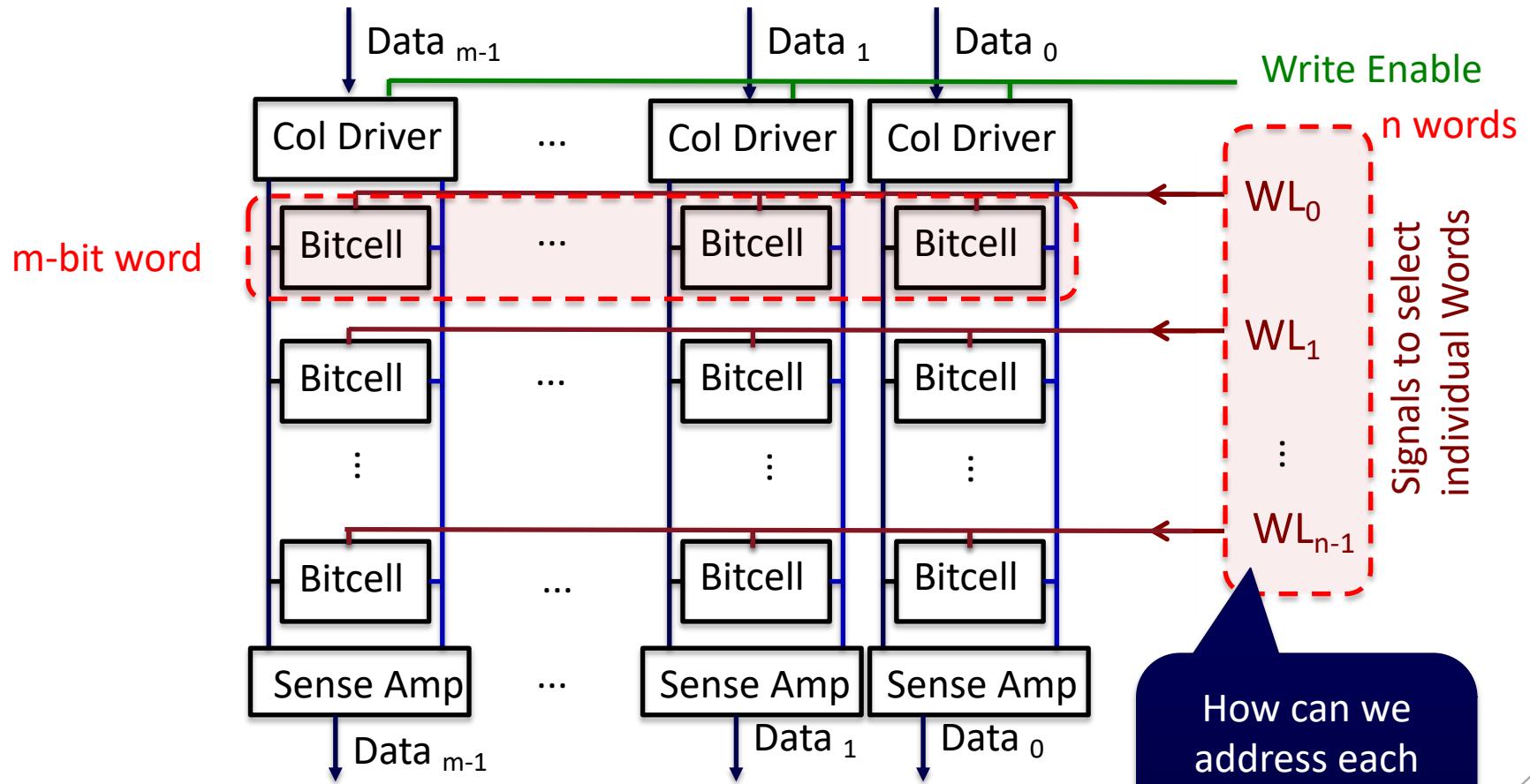
SRAM memory organization



SRAM memory organization

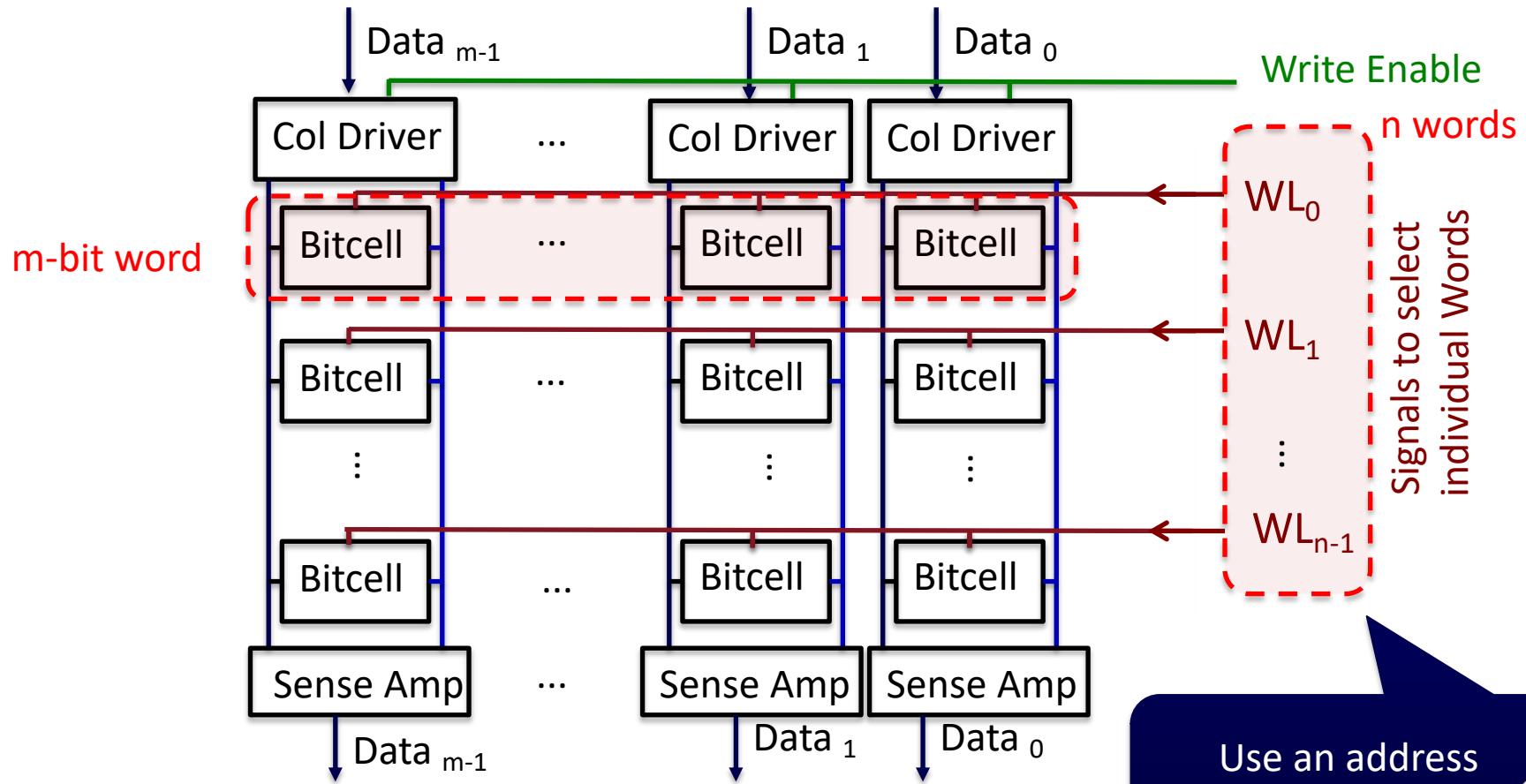


SRAM memory organization

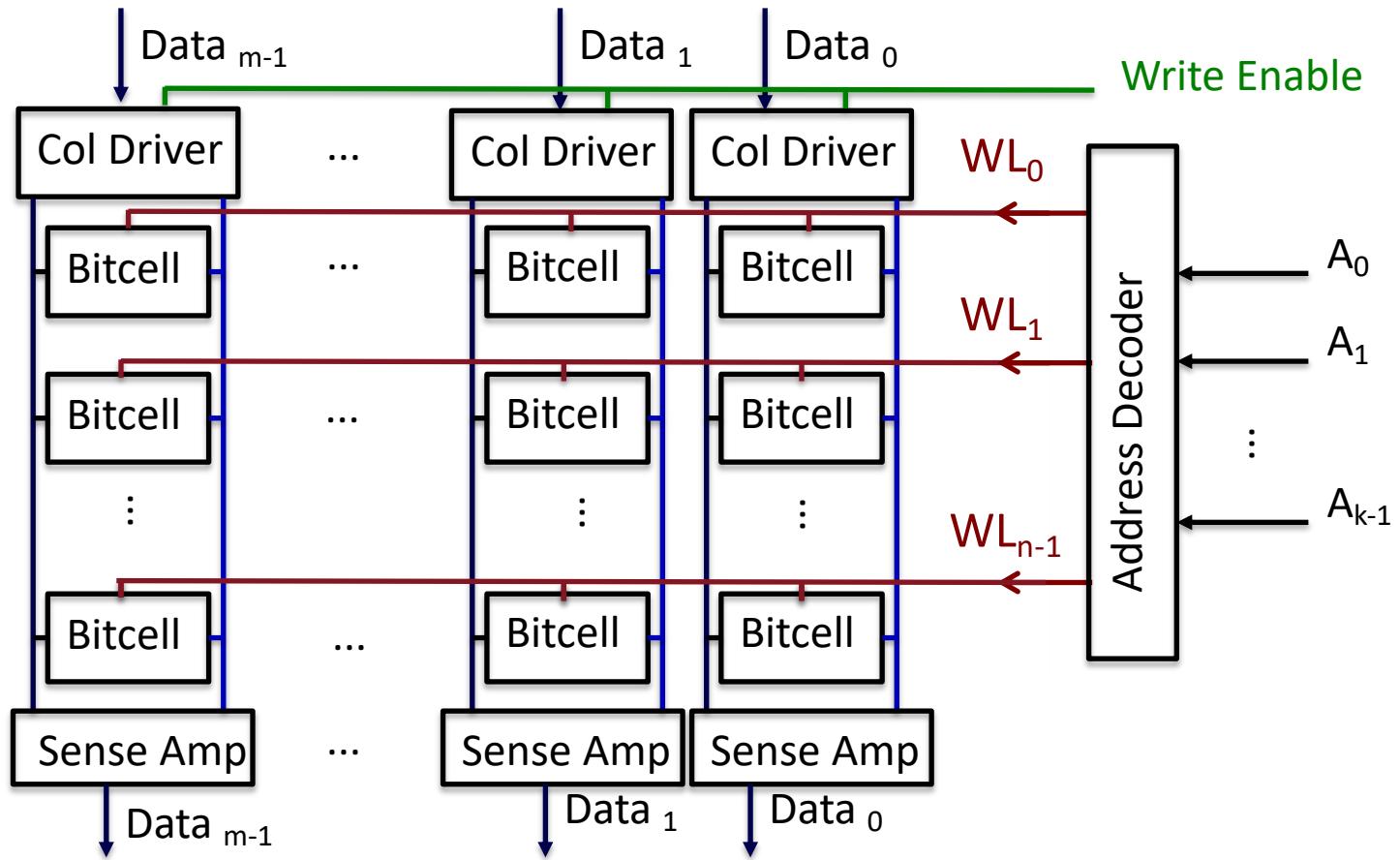


How can we
address each
Word Line
individually?

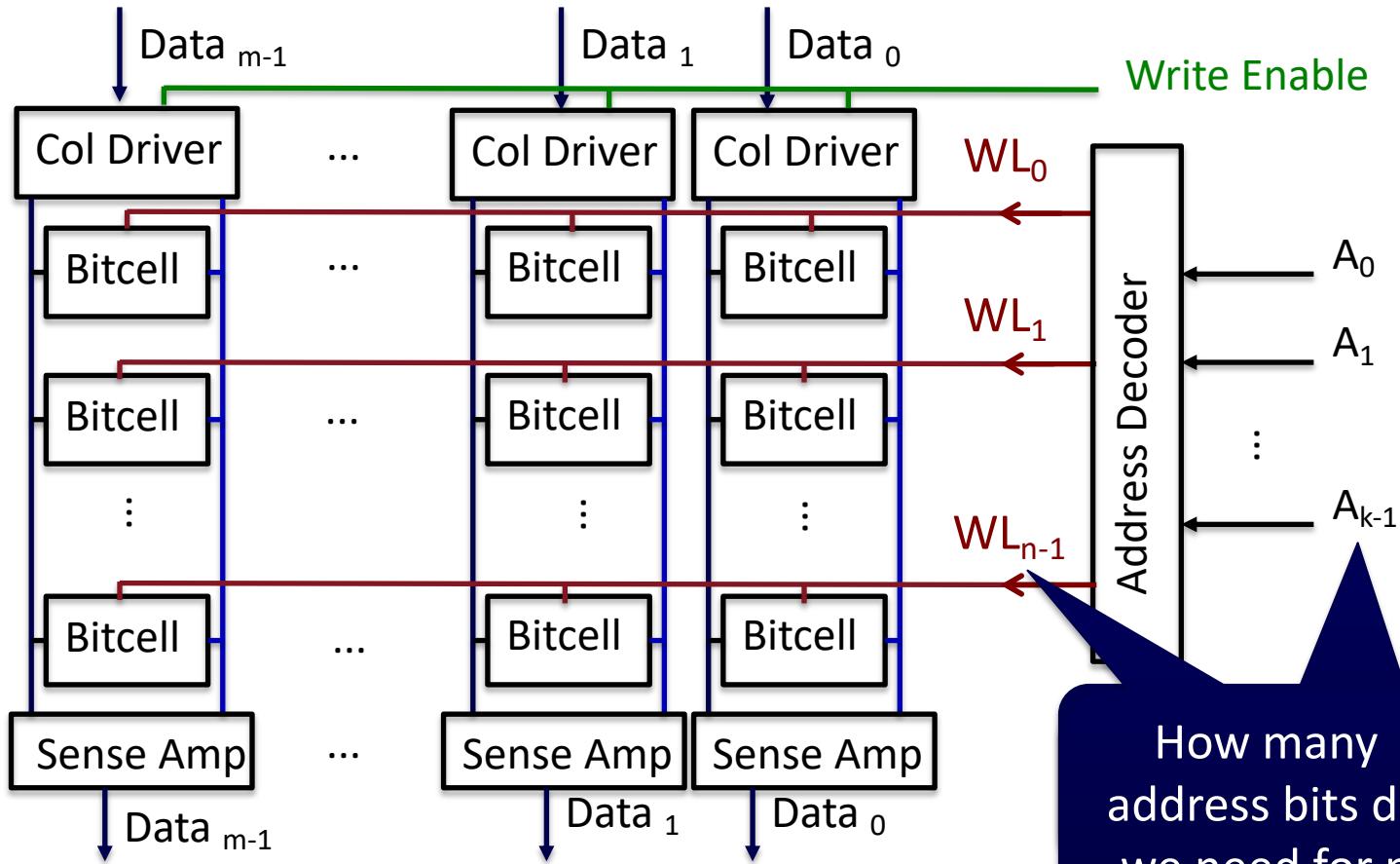
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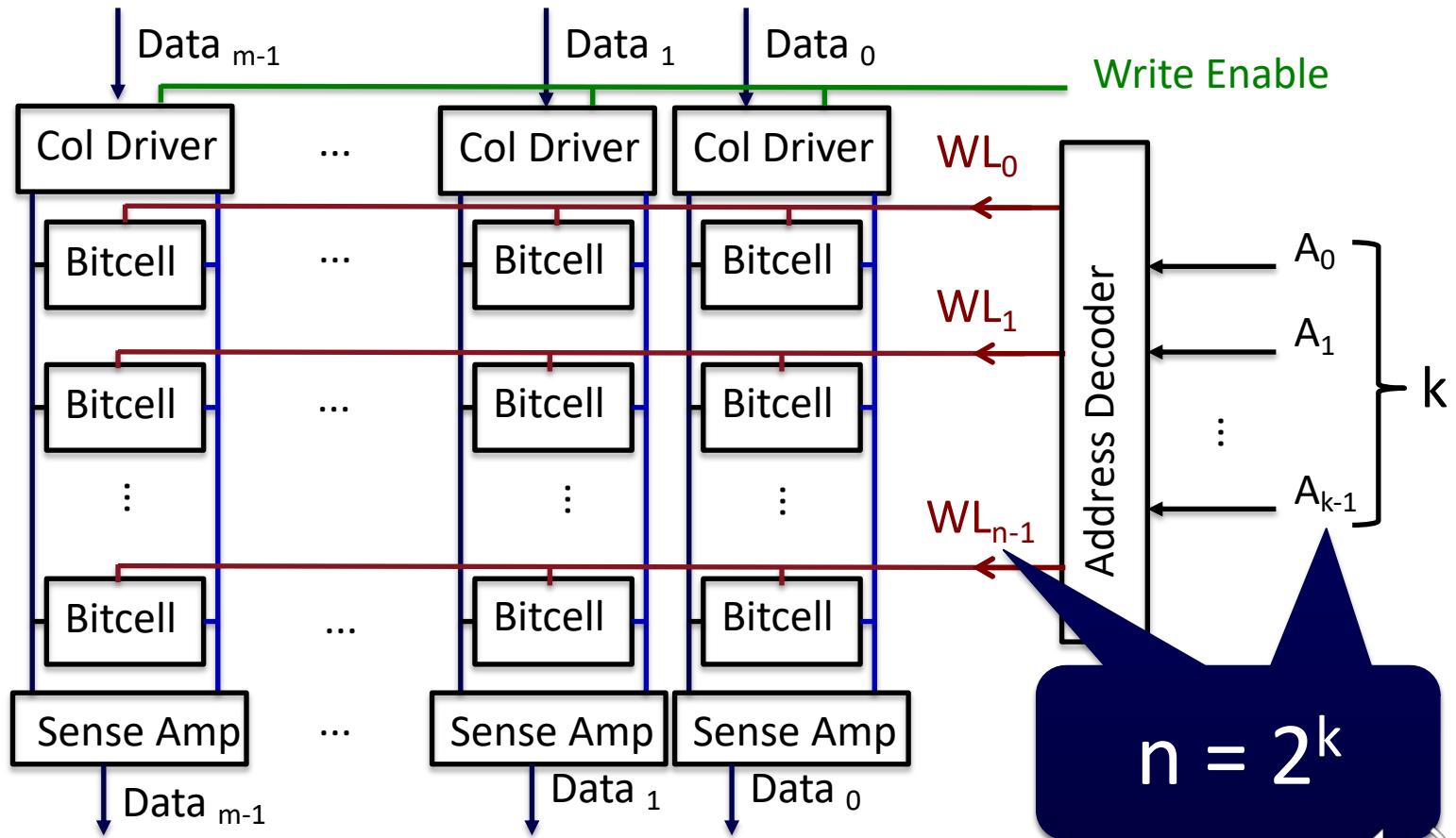
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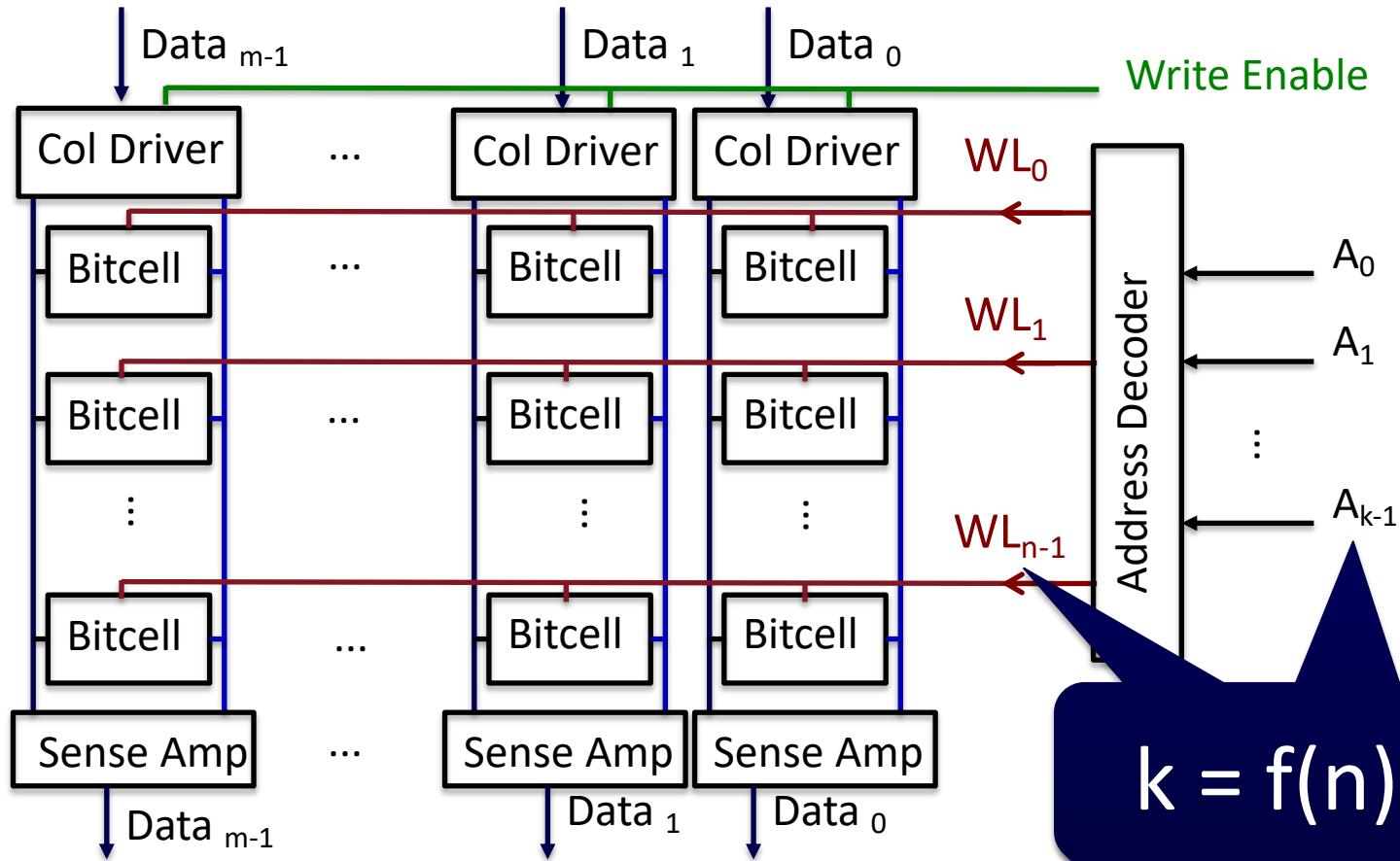
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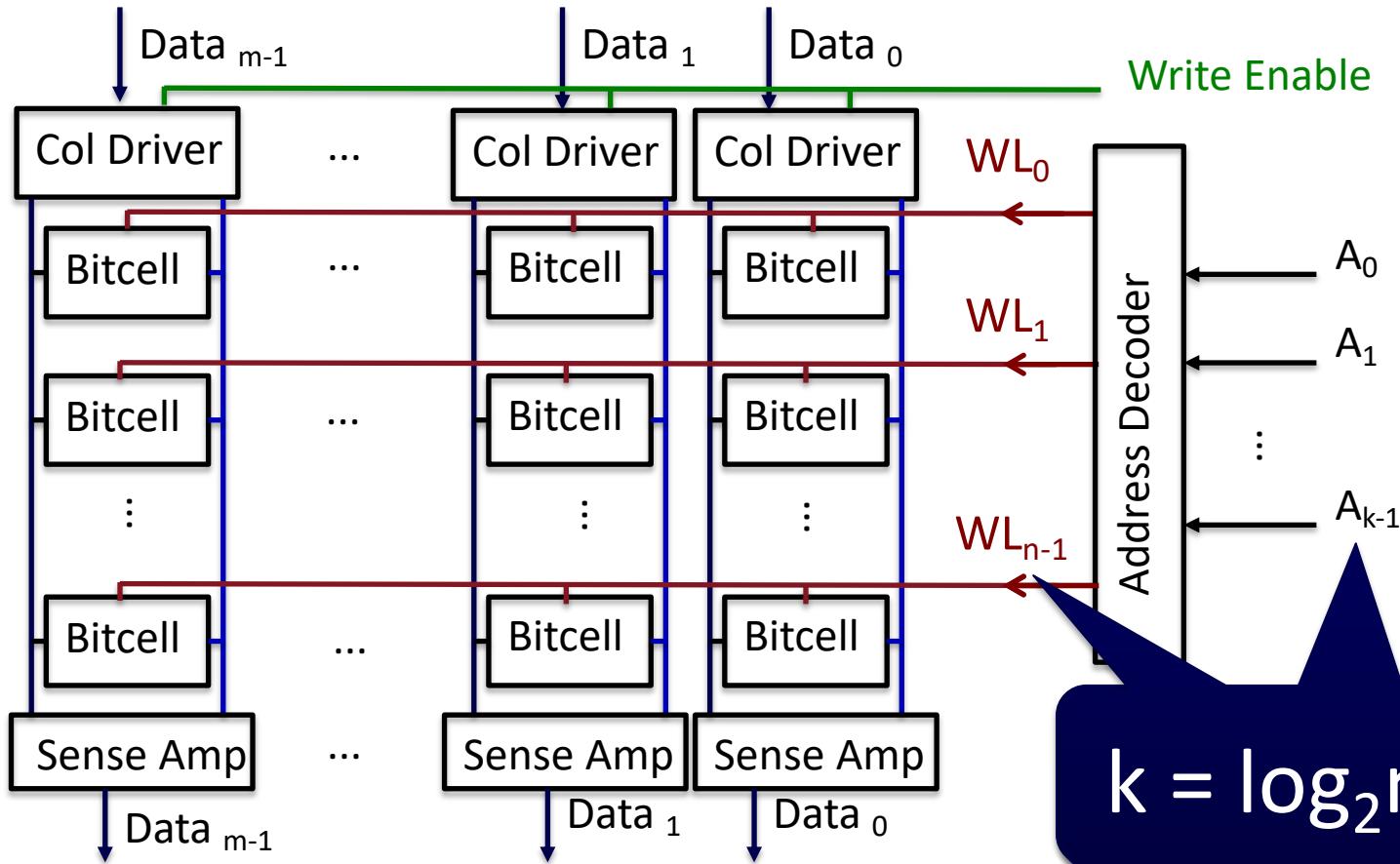
SRAM memory organization



SRAM memory organization



SRAM memory organization



Logarithms...some revision

How can you calculate $\log_2 a$ on your calculator?

$$\log_2 a = ?$$

$$\log_b a = \frac{\log_c a}{\log_c b}$$

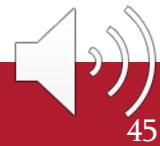
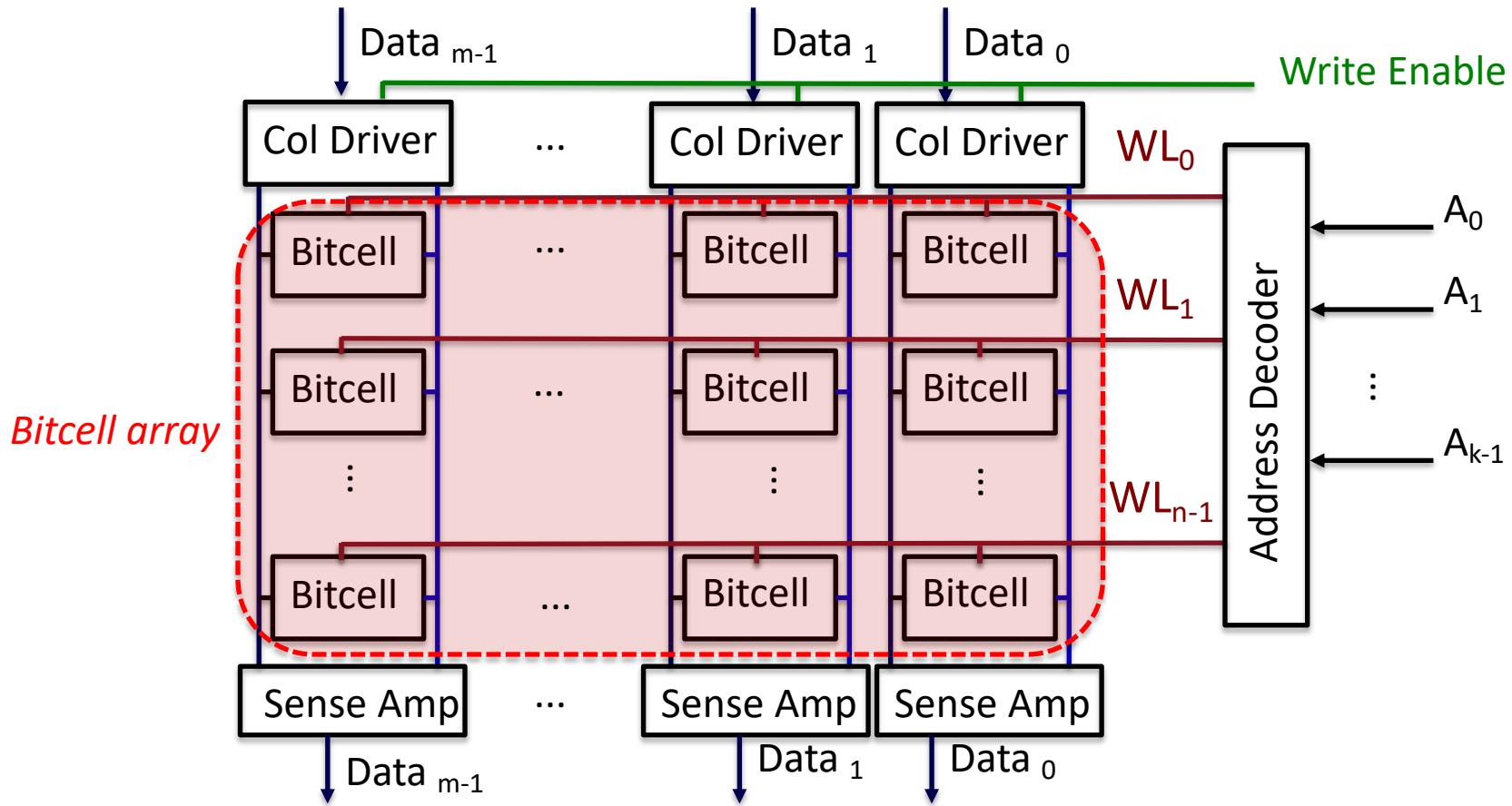
$$\log_2 a = \frac{\ln a}{\ln 2}$$

$$\log_2 a = \frac{\log_{10} a}{\log_{10} 2}$$

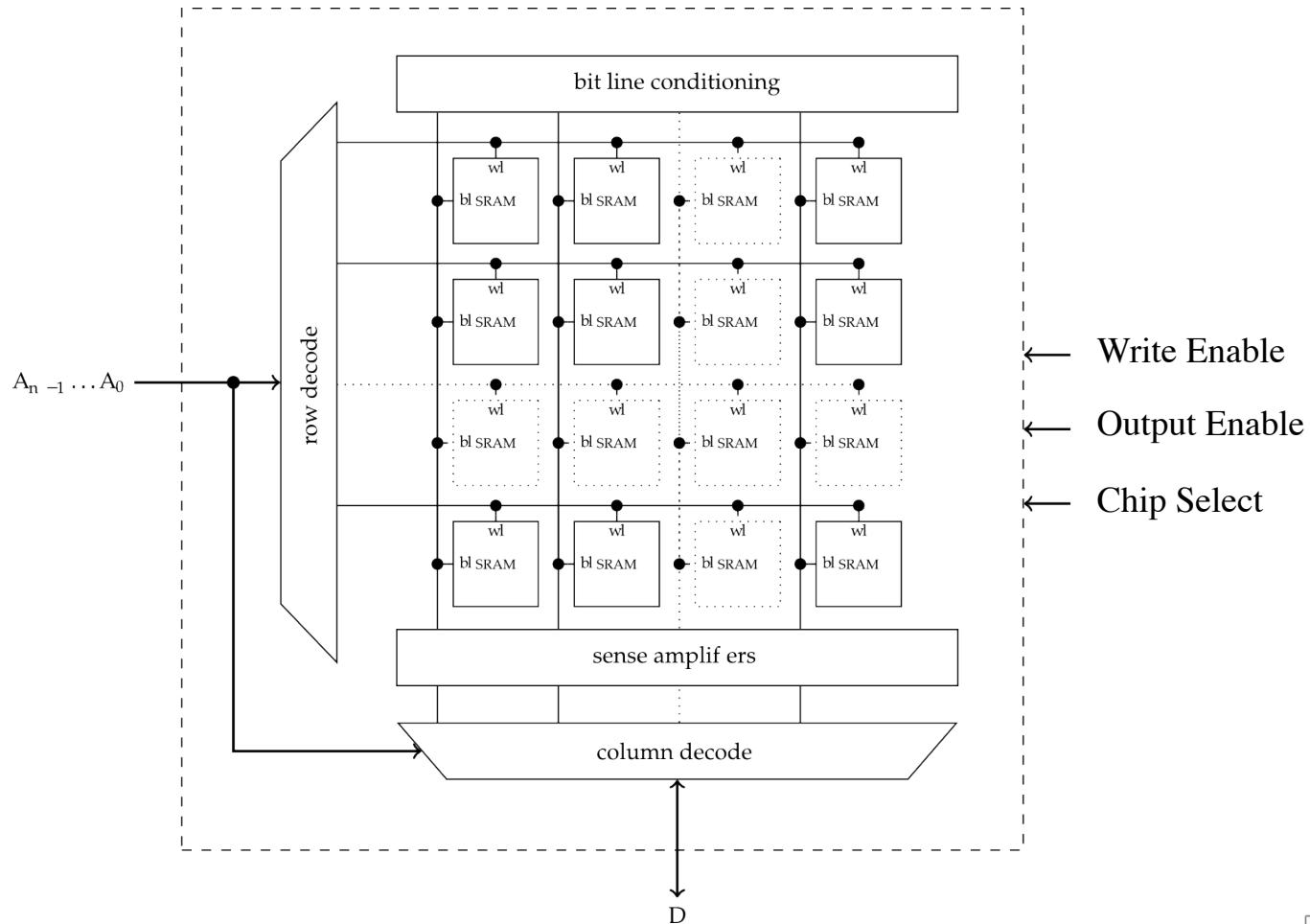
So how many address bits do we need for 64 words, and how many for 100 words?



SRAM memory organization



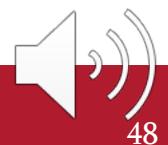
SRAM memory layout



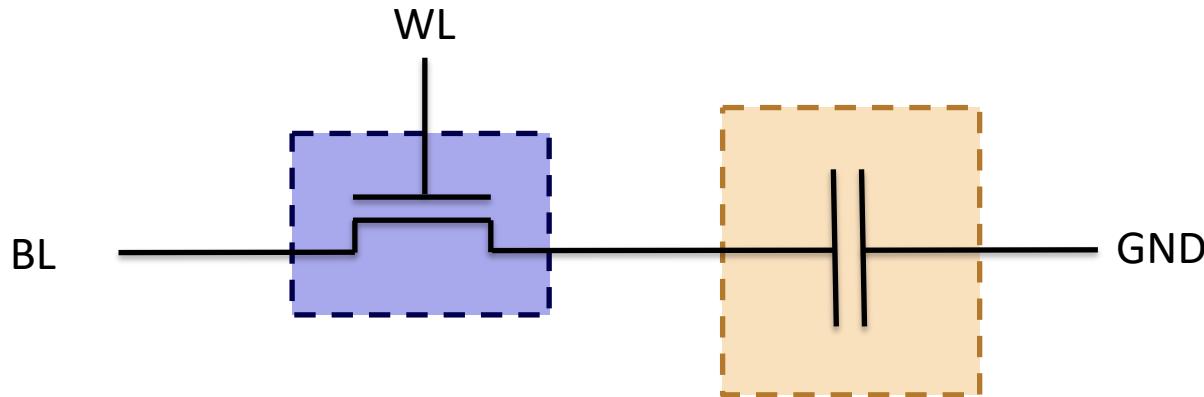
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DRAM

- Dynamic Random Access Memory
 - Write a value to a DRAM cell, it **stays there** for **a short period of time**, until the contents need to be **refreshed**.
- A DRAM chip comprises:
 - The DRAM cells, units of storage.
 - Surrounding control logic to allow updating and retrieving data from specified groups of cells.
 - A **separate controller** is needed to keep the DRAM refreshed.



DRAM cell



- A **capacitor** can be charged to store a '1', or discharged to store a '0'.
- A **transistor** allows us to read the current value, or charge/discharge it.
 - Turning the transistor on will make the capacitor discharge a little.
 - Even when off, the transistor **leaks** current, hence the need to refresh periodically, **even if we don't access a cell**.



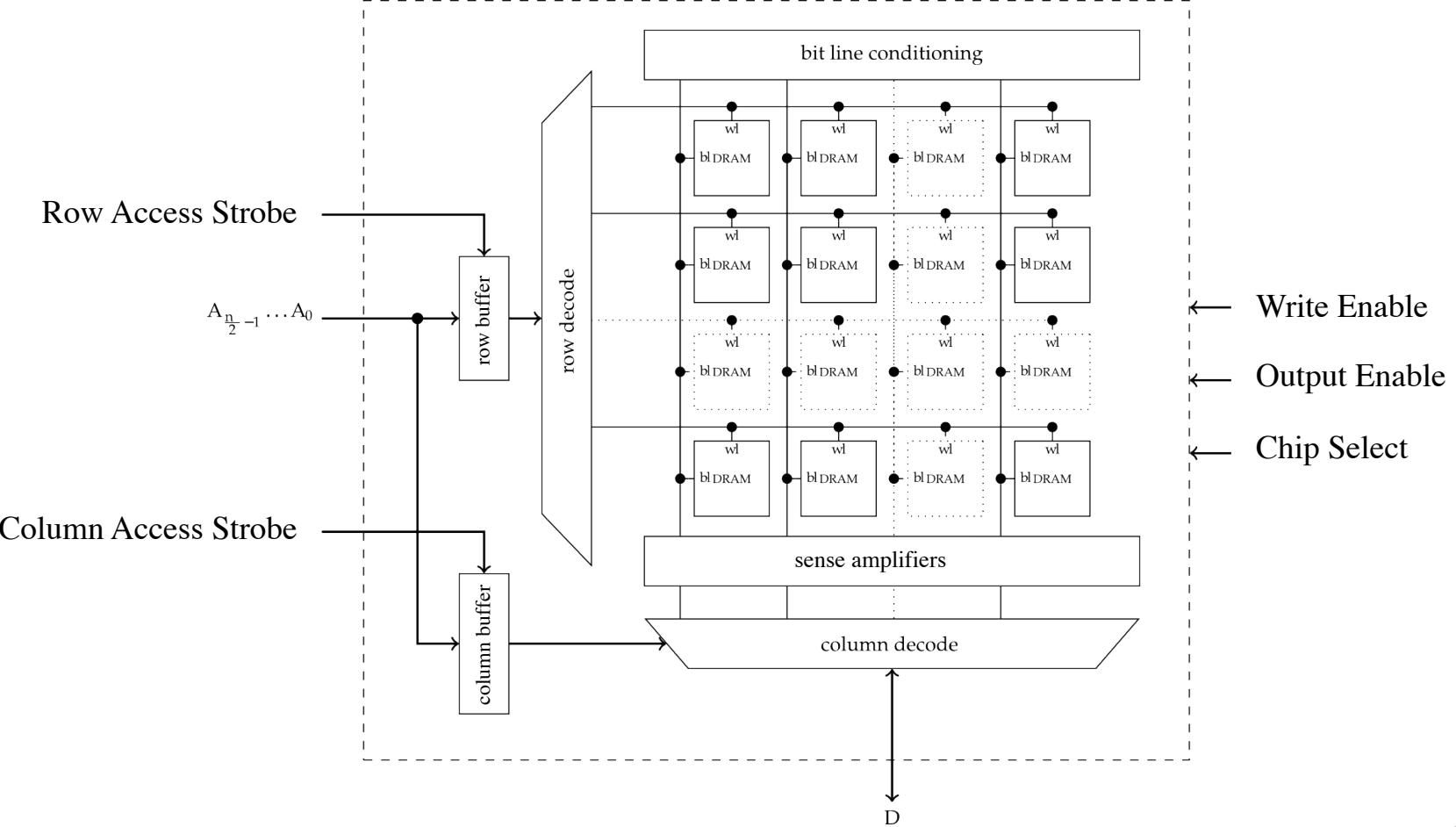
DRAM Read/Write - Refresh

Different DRAM refresh methods:

- Use a counter to hold the row (number) to be refreshed next
 - Some DRAM chips contain a counter
 - Some DRAM chips use **peripheral refresh logic** that includes a counter
- **DRAM cells** are typically organized in a *square* collection of capacitors.
- **DRAM cell in READ state:**
 - an entire row is read out and the refresh is written back
- **DRAM cell in WRITE state:**
 - a whole row is “read” out, *one value is changed*, and
 - then the whole row is written back
- DRAM access time ~50-150 ns (SRAM is ~ one order of magnitude faster!)



DRAM array



DRAM Refresh



JEDEC (<https://www.jedec.org/>) standardizes the **maximum time interval between refresh operations** for each DRAM technology.

- Measured in ms (10^{-3}), μs (10^{-6}) or ns (10^{-9})
- Manufacturers specify that *each row* must be refreshed every 64 ms or less, as defined by the JEDEC standard.

**JEDEC
STANDARD**

DDR2 SDRAM SPECIFICATION

JESD79-2B

(Revision of JESD79-2A)

January 2005

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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DRAM Refresh

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Electrical characteristics & AC timing for DDR2-400/533/667/800 - absolute specification

(T_{OPER} ; $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$)

Table 39 — Refresh parameters by device density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units	Note
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns	1
Average periodic refresh interval	tREFI	$0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	7.8	7.8	7.8	7.8	7.8	μs	1
		$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	3.9	3.9	3.9	3.9	3.9	μs	1, 2

NOTE 1 If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

NOTE 3 This is an optional feature. For detailed information, please refer to “operating temperature condition” chapter in this spec



DRAM Refresh

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If refresh is staggered “one-row-at-a-time” over 64 ms, then a system with $2^{13} = 8192$ rows would require a refresh of one row every 7.8 μ s, i.e. $64 \text{ ms}/8192 \text{ rows} = 0.007812 \text{ ms/row}$.

Electrical characteristics

**JEDEC
STANDARD**

DDR2 SDRAM SPECIFICATION

JESD79-2B

(Revision of JESD79-2A)

January 2005

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ification

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DRAM Refresh

JEDEC[®]

Global Standards for the Microelectronics Industry

**JEDEC
STANDARD**

DDR2 SDRAM SPECIFICATION

JESD79-2B

(Revision of JESD79-2A)

January 2005

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

EIA
Electronic Industries Alliance

JEDEC (<https://www.jedec.org/>) standardizes the **maximum time interval between refresh operations** for each DRAM technology.

- Measured in ms (10^{-3}), μ s (10^{-6}) or ns (10^{-9})
- Manufacturers specify that *each row* must be refreshed every 64 ms or less, as defined by the JEDEC standard.

Electrical characteristics & AC timing for DDR2-400/533/667/800 - absolute specification

(T_{OPER} ; $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$)

Table 39 — Refresh parameters by device density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units	Note
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns	1
Average periodic refresh interval	tREFI	$0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	7.8	7.8	7.8	7.8	7.8	μs	1
		$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	3.9	3.9	3.9	3.9	3.9	μs	1, 2

NOTE 1 If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

NOTE 3 This is an optional feature. For detailed information, please refer to “operating temperature condition” chapter in this spec



Remarks about DRAM

- Controlling DRAM is relatively complex.
 - A DRAM controller must occasionally access each row to refresh it, regardless of whether anything wanted to read/write it.
 - Timing of refresh is very important.
- DRAM is **very dense**.
 - In 2014, **~100 million bits per square millimetre...**
 - Or several gigabytes in a single chip, the size of a fingernail.



MEMORY ORGANISATION



Memory arrangement

- Two important parameters affect memory arrangement.
 - Addressing width
 - Data width
- Q1: A memory chip has 8 address bits. How many locations can it support?
- Q2: What data capacity does the chip have?





Memory arrangement

- A1:
 - $2^8 = 256$
 - There are 256 addressable locations
- A2:
 - What data capacity does the chip have?
 - We don't have enough information!
 - We know how many locations there are, but not how big they are.





Memory arrangement

- Q3: A memory chip has 8 address bits and 8-bit data. What is its capacity?



Memory arrangement

- Q3: A memory chip has 8 address bits and 8-bit data. What is its capacity?
 - $2^8 = 256$ locations, each 8 bit wide = 2^{11} bit = 2048 bit
 - $2^8 = 256$ locations, each **1 Byte** wide = 256 Bytes





Memory arrangement

- Q3: A memory chip has 8 address bits and 8-bit data. What is its capacity?
 - $2^8 = 256$ locations, each 8 bit wide = 2^{11} bit = 2048 bit
 - $2^8 = 256$ locations, each 1 Byte wide = 256 Bytes
- Q4: A memory chip has 7 address bits and 16-bit data. What is its capacity?
 - $2^7 = 128$ locations, each 16 bit wide = 2048 bit
 - $2^7 = 128$ locations, each **2 Byte** wide = 256 Bytes





Same capacity, different layout

Address A0-A2	Data D0-7
0x0	0xAB
0x1	0xCD
0x2	0xAB
0x3	0xCD
0x4	0xAB
0x5	0xCD
0x6	0xAB
0x7	0xCD
Total memory:	8 bytes

3 bit address

8 bit data

8 individually
addressable bytes



Same capacity, different layout



Address A0-A2	Data D0-7
0x0	0xAB
0x1	0xCD
0x2	0xAB
0x3	0xCD
0x4	0xAB
0x5	0xCD
0x6	0xAB
0x7	0xCD
Total memory:	8 bytes

Address A0-A1	Data D0-D7	Data D8-D15
0x0	0xAB	0xCD
0x1	0xAB	0xCD
0x2	0xAB	0xCD
0x3	0xAB	0xCD
Total memory:	8 bytes	

4 individually addressable locations, each 2 bytes wide





Same capacity, different layout



Address A0-A2	Data D0-7
0x0	0xAB
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0x2	0xAB
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0x2	0xAB	0xCD
0x3	0xAB	0xCD
Total memory:	8 bytes	

The wider memory has 2x data signals, one less address signal.





Memory arrangement

- To fully understand a memory structure, we need to know:
 - How many **address bits** there are
 - How **wide** the data bus is
 - At what resolution the addressing takes place
 - Bytes, 16-bits, 32-bits, etc...
 - Typically the data width = resolution.
- Datasheets will often describe the layout in terms of the number of locations and the data width:
 - 64K x 32 bit





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 - Typically the data width = resolution.
- Datasheets will often describe the layout in terms of the number of locations and the data width, e.g.:
 - 64K x 32 bit
 - Remember: K is used for 2^{10} , i.e. $64K = 64 \times 1024 = 65536$





CY14E256LA

256-Kbit (32 K × 8) nvSRAM

Features

- 25 ns and 45 ns access times
- Internally organized as 32 K × 8 (CY14E256LA)
- Hands-off automatic STORE on power-down with only a small capacitor
- STORE to QuantumTrap nonvolatile elements initiated by software, device pin, or autostore on power-down
- RECALL to SRAM initiated by software or power-up
- Infinite read, write, and RECALL cycles
- 1 million STORE cycles to QuantumTrap
- 20-year data retention
- Single 5 V ± 10% operation
- Industrial temperature
- 44-pin thin small-outline package (TSOP) Type II and 32-pin small-outline integrated circuit (SOIC) package
- Pb-free and restriction of hazardous substances (RoHS) compliant

Functional Description

The Cypress CY14E256LA is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 32 KB. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click [here](#).



Memory datasheet

- 32K x 8-bit
 - How much total memory?

256-Kbit (32 K × 8) nvSRAM

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- 25 ns and 45 ns access times
- Internally organized as 32 K × 8 (CY14E256LA)
- Hands-off automatic STORE on power-down with only a small address change
- STORE to QuantumTap nonvolatile elements initiated by software, device pins, or software on power-down
- RECALL from QuantumTap to volatile or power-up
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- 1 million STORE cycles to QuantumTap
- 20-year data retention
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Functional Description

The Cypress CY14E256LA is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 32 K × 8 bits. The CY14E256LA incorporates QuantumTap technology, producing the world's first nonvolatile SRAM. This allows the device to do a fast read and write cycles, while independent nonvolatile data is stored in the background. The STORE operation moves data from the SRAM to the nonvolatile elements (the STORE operation takes place automatically at power-down. On power-up, data is moved back from the nonvolatile memory. Both the STORE and RECALL operations are also triggered by software).

For a complete list of related documentation, click [here](#).



Memory datasheet

- 32K x 8-bit
 - How much total memory?
 - $32 \times 1024 \times 8 \text{ bit} = 32 \times 8 \times 1024 \text{ bit} = 32 \times 8 \text{ Kbit} = 256 \text{ Kbit}$

<p>Features</p> <ul style="list-style-type: none"> ■ 25 ns and 45 ns access times ■ Internally organized as 32 K × 8 (CY14E256LA) ■ Hands-off automatic STORE on power-down with only a small dataset loss ■ STORE to QuantumTap nonvolatile elements initiated by software, device pins, or software on power-down ■ RECALL from QuantumTap to volatile SRAM on power-up ■ Infinite read, write, and RECALL cycles ■ 1 million STORE cycles to QuantumTap ■ 20-year data retention ■ Single 5 V ± 10% operation ■ Industrial temperature ■ 44-pin thin lead-frame package (TSSOP) Type II and 32-pin small-outline integrated circuit (SOIC) package ■ Pb-Free and restriction of hazardous substances (RoHS) compliant 	<p>Functional Description</p> <p>The Cypress CY14E256LA is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 32 K × 8 bits. The CY14E256LA incorporates QuantumTap technology, producing the world's first nonvolatile SRAM. It can store data in nonvolatile data cells during power-down, and automatically recall data from the SRAM to the nonvolatile elements (the STORE operation takes place automatically at power-down). On power-up, data is recalled from the nonvolatile memory. Both the STORE and RECALL operations are triggered by software.</p> <p>For a complete list of related documentation, click here.</p>
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CY14E256LA

256-Kbit (32 K × 8) nvSRAM

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– How much total memory?

- $32 \times 1024 \times 8 \text{ bit} = 32 \times 8 \times 1024 \text{ bit} = 32 \times 8 \text{ Kbit} = 256 \text{ Kbit}$
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– How much total memory?

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- $32\text{K} \times 8 \text{ bit} = 32\text{KB}$

Remember: 8 bit = 1 Byte

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CY14E256LA

256-Kbit (32 K × 8) nvSRAM

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 - $2^5 \times 2^{10} \times 2^3 \text{ bit} = 2^{18} \text{ bit} = 2^8 \times 2^{10} \text{ bit} = 256 \text{ Kbit}$
 - 32K x 8 bit = 32KB
 - How many address bits?
 - $32K = 32 \times 1024 = 32768$ (locations)

256-Kbit (32 K × 8) nvSRAM

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- $\log_2 32768 = 15$

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CY14E256LA

256-Kbit (32 K × 8) nvSRAM



Memory datasheet



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CY14E256LA

256-Kbit (32 K × 8) nvSRAM

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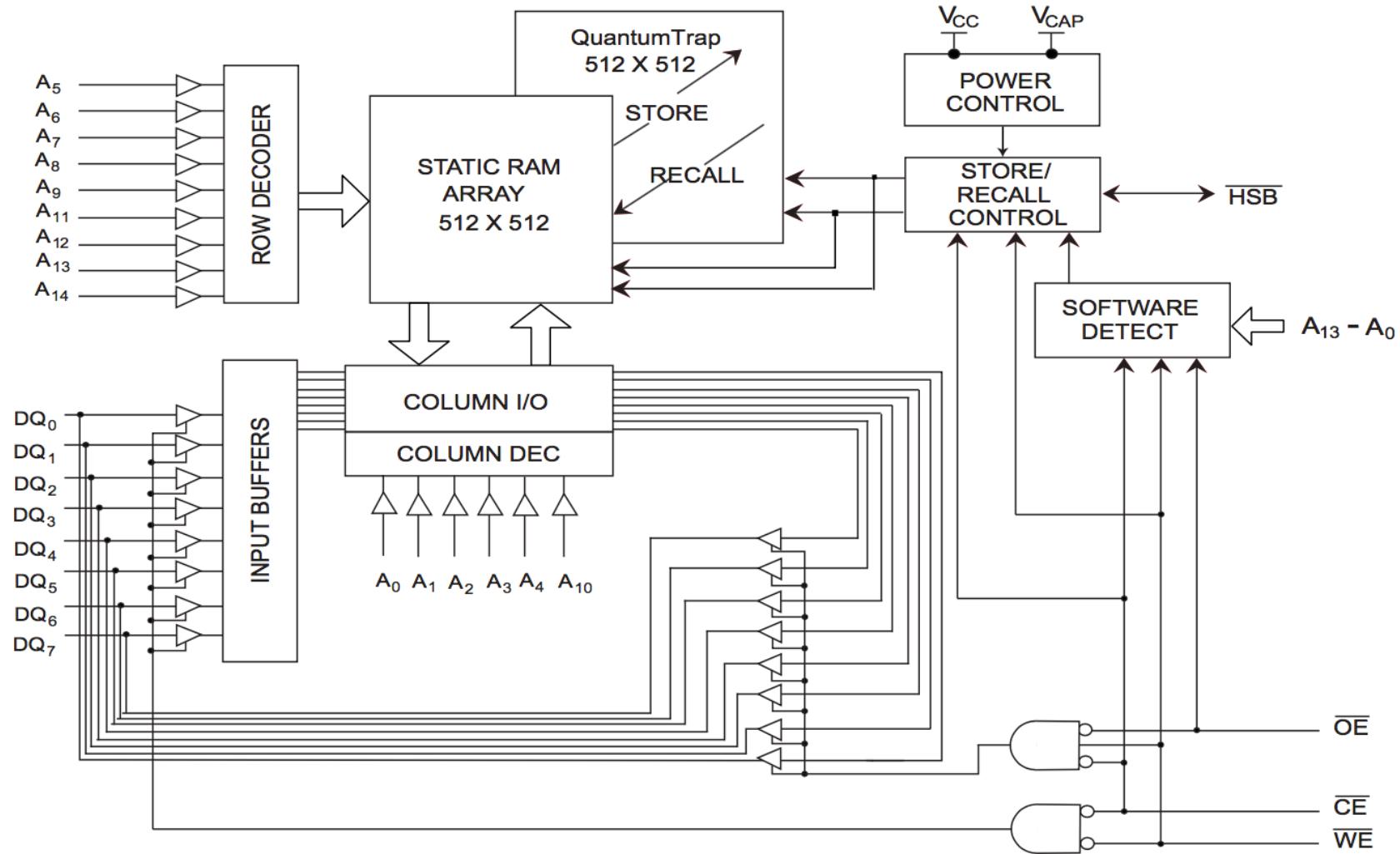
- How many address bits?

- $32\text{K} = 32 \times 1024 = 32768$ (locations)
 - $\log_2 32768 = 15$

$$2^5 \times 2^{10} = 2^{15}$$




Logic Block Diagram



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For a complete list of related documentation, click [here](#).

Datasheet

<https://www.cypress.com/documentation/datasheets/cy14e256la-256-kbit-32-k-8-nvsram>



Summary

- Basic memory concepts
- Static vs dynamic memory
 - Static: holds data as long as power is applied (SRAM)
 - Dynamic: must be refreshed periodically (DRAM)
- Memory arrangement
 - How to determine memory capacity
 - How many address bits
- Commercial datasheet



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In this lecture

Foundations

- Data representation, logic, Boolean algebra.

Building blocks

- Transistors, transistor based logic, simple devices, storage.

Modules

- **Memory**, simple controllers, FSMs, processors and execution.

Programming

- Machine code, assembly, high-level languages, compilers.

Wrap-up

- Operating systems, energy aware computing.



In the next lecture

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