LAB1:
Introduction to tools and simple gates:

Introduction:

As instructed in the lab manual, I have designed four different gates AND, OR, NOT and XOR using VHDL expressions.

In the code, I have taken two inputs (a, b) and four outputs (c, f, h, k) for four different gates AND, OR, NOT and XOR respectively.

As the first input (a) I have taken a clock input for the time period 1000ns and a constant for input (b) in MultiSim. In Quartus I have just taken two constant inputs.

WAVEFORM:

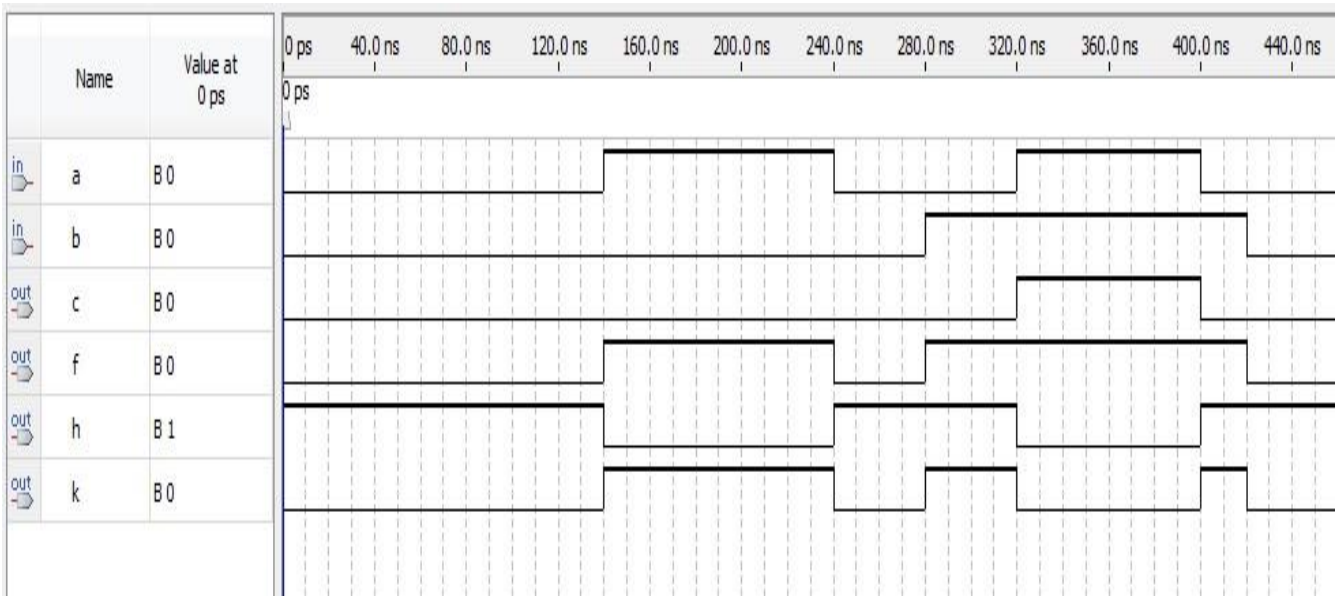


Figure 1: Waveform using Quartus.

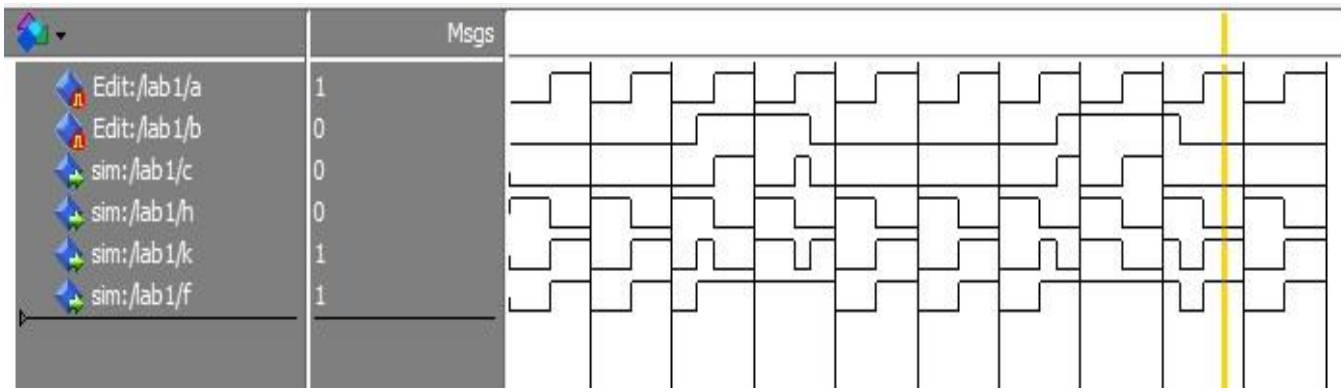
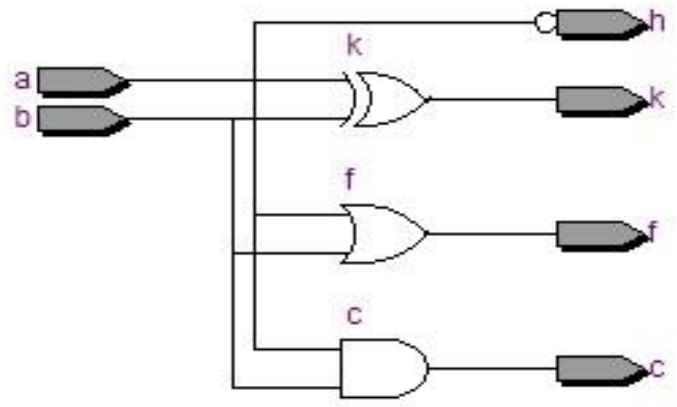


Figure 1: Waveform using ModelSim.

RTL VIEW:



CODE:

```
library ieee;
use ieee.std_logic_1164.all;
entity lab1 is
port
(a,b : in std_logic;
c,h,k,f : out std_logic);
end entity;
architecture rt1 of lab1 is
begin
c <= a and b;
f <= a or b;
h <= not a;
k <= a xor   b;
end rt1;
```

CONCLUSION:

In this lab I have learned how to use simple gates using VHDL.