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Reg. No. : 2021-EE-1 Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_

**Lab Manual 4b**

**Combinational Circuit design using K-Maps**

(Seven Segment Display)

Truth table for seven segments is given in the manual.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | 0 | 1 | 0 | 0 |
| **01** | 1 | 0 | 0 | 0 |
| **11** | 0 | 1 | 0 | 0 |
| **10** | 0 | 0 | 1 | 0 |

a = (~num[0] & ~num[1] & ~num[2] & num[3]) | (~num[0] & num[1] & ~num[2] & ~num[3]) | (num[0] & num[1] & ~num[2] & num[3]) | (num[0] & ~num[1] & num[2] & num[3])

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | 0 | 0 | 0 | 0 |
| **01** | 0 | 1 | 0 | 1 |
| **11** | 1 | 0 | 1 | 1 |
| **10** | 0 | 0 | 1 | 0 |

b = (num[1] & num[2] & ~num[3]) | (num[0] & num[2] & num[3]) | (~num[0] & num[1] & ~num[2] & num[3]) | (num[0] & num[1] & ~num[3])

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | 0 | 0 | 0 | 1 |
| **01** | 0 | 0 | 0 | 0 |
| **11** | 1 | 0 | 1 | 1 |
| **10** | 0 | 0 | 0 | 0 |

c = (num[0] & num[1] & num[2]) | (num[0] & num[1] & ~num[3]) | (~num[0] & ~num[1] & num[2] & ~num[3])

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | 0 | 0 | 0 | 0 |
| **01** | 1 | 0 | 1 | 0 |
| **11** | 0 | 0 | 1 | 0 |
| **10** | 0 | 0 | 0 | 1 |

d = (num[1] & num[2] & num[3]) | (num[0] & ~num[1] & num[2] & ~num[3]) | (~num[0] & num[1] & ~num[2] & ~num[3]) | (~num[0] & ~num[1] & ~num[2] & num[3])

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | 0 | 1 | 1 | 0 |
| **01** | 1 | 1 | 1 | 0 |
| **11** | 0 | 0 | 0 | 0 |
| **10** | 0 | 1 | 0 | 0 |

e = (~num[0] & num[3]) | (~num[0] & num[1] & ~num[2]) | (~num[1] & ~num[2] & num[3])

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | 0 | 1 | 1 | 1 |
| **01** | 0 | 0 | 1 | 0 |
| **11** | 0 | 1 | 0 | 0 |
| **10** | 0 | 0 | 0 | 0 |

f = (~num[0] & num[2] & num[3]) | (~num[0] & ~num[1] & num[2]) | (~num[0] & ~num[1] & num[3]) | (num[0] & num[1] & ~num[2] & num[3])

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | 1 | 1 | 0 | 0 |
| **01** | 0 | 0 | 1 | 0 |
| **11** | 1 | 0 | 0 | 0 |
| **10** | 0 | 0 | 0 | 0 |

g = (~num[0] & ~num[1] & ~num[2]) | (~num[0] & num[1] & num[2] & num[3]) | (num[0] & num[1] & ~num[2] & ~num[3])

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a[0] | a[1] | a[2] | Anode0 | Anode1 | Anode2 | Anode3 | Anode4 | Anode5 | Anode6 | Anode7 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 0 | 1 | 1 | 1 |
| **1** | 1 | 1 | 1 | 1 |

an0 = sel[0] | sel[1] | sel[2]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 1 | 0 | 1 | 1 |
| **1** | 1 | 1 | 1 | 1 |

an1 = sel[0] | sel[1] | ~sel[2]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 1 | 1 | 1 | 0 |
| **1** | 1 | 1 | 1 | 1 |

an2 = sel[0] | ~sel[1] | sel[2]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 1 | 1 | 0 | 1 |
| **1** | 1 | 1 | 1 | 1 |

an3 = sel[0] | ~sel[1] | ~sel[2]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 1 | 1 | 1 | 1 |
| **1** | 0 | 1 | 1 | 1 |

an4 = ~sel[0] | sel[1] | sel[2]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 1 | 1 | 1 | 1 |
| **1** | 1 | 0 | 1 | 1 |

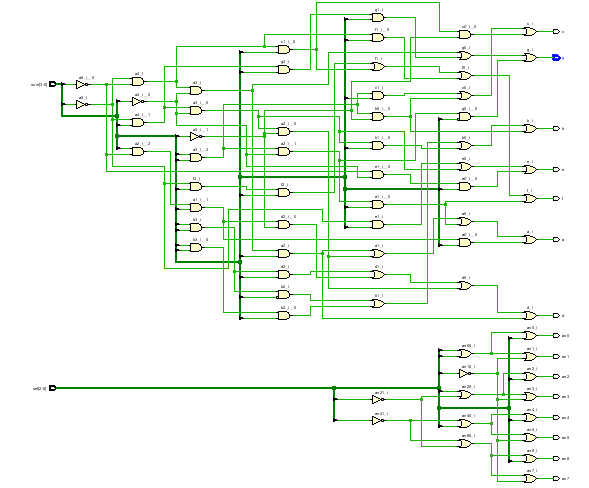
an4 = ~sel[0] | sel[1] | sel[2]

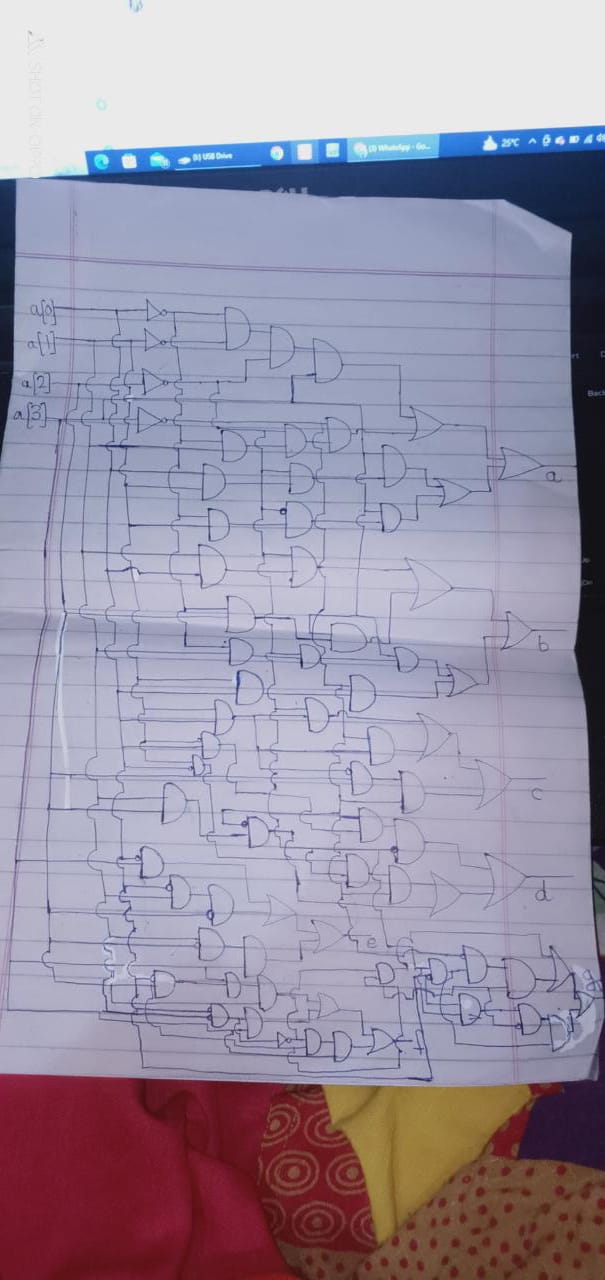
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 1 | 1 | 1 | 1 |
| **1** | 1 | 1 | 1 | 0 |

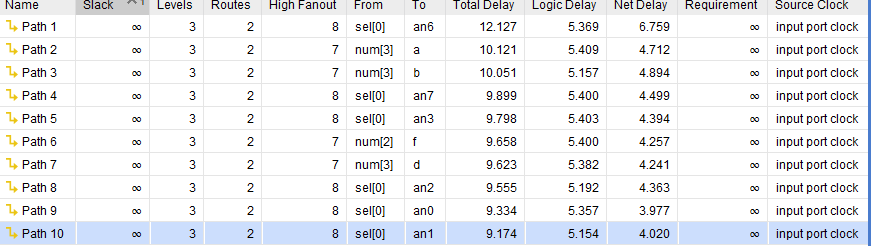
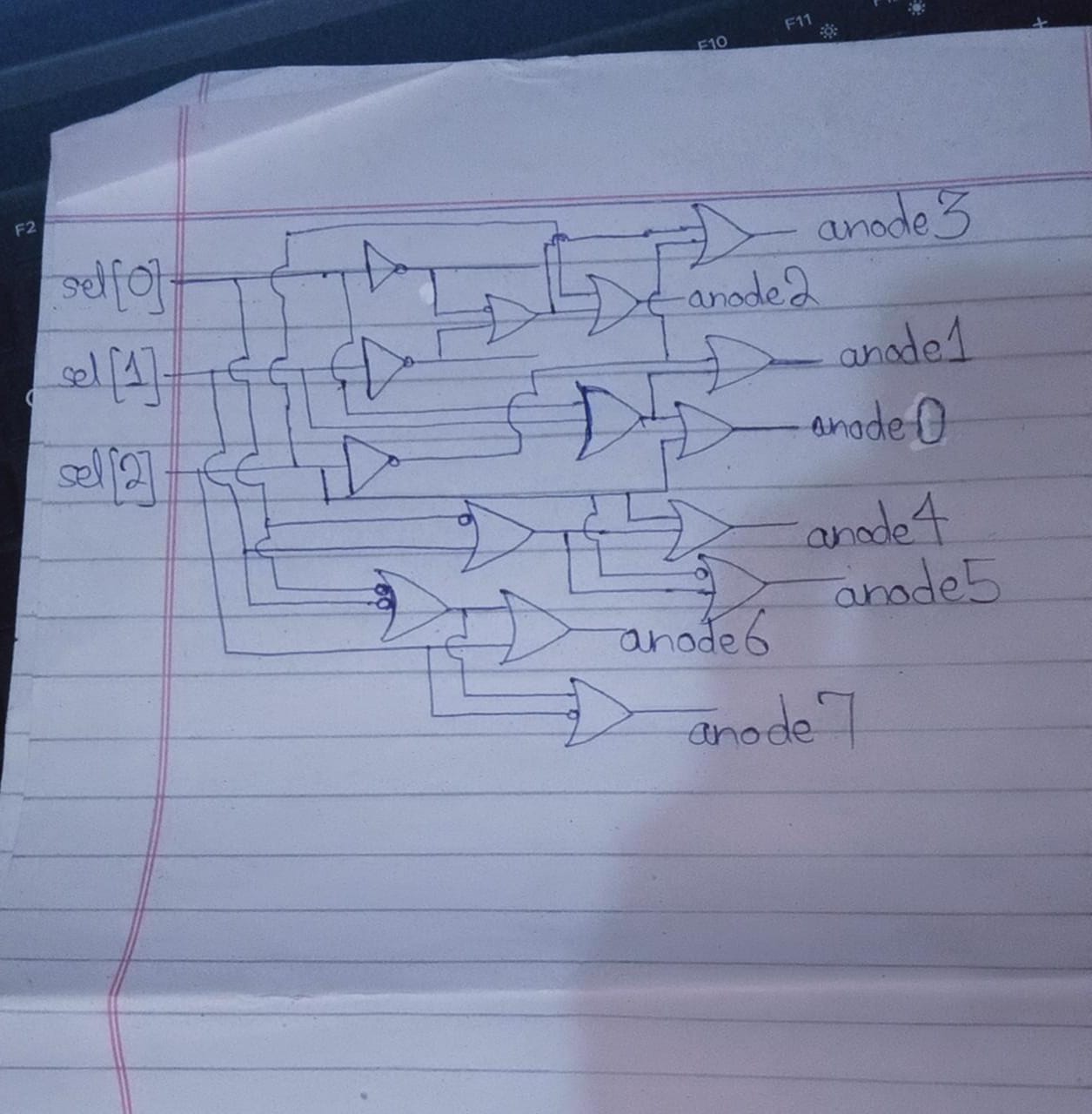
an6 = ~sel[0] | ~sel[1] | sel[2]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **0** | 1 | 1 | 1 | 1 |
| **1** | 1 | 1 | 0 | 1 |

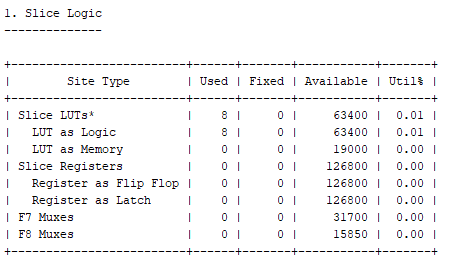
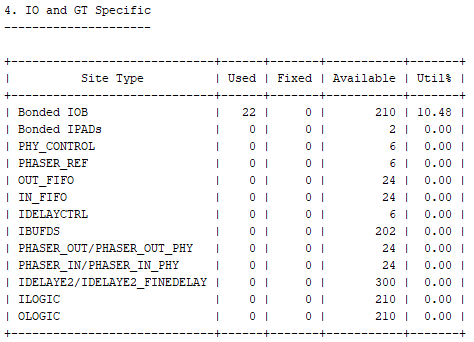
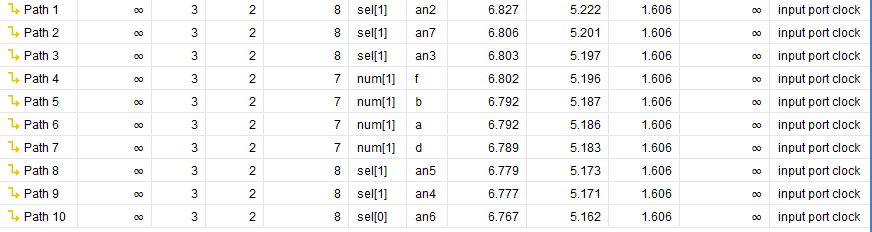
an7 = ~sel[0] | ~sel[1] | ~sel[2]







**Delay in case of implemented circuit**

**Delay in case of Synthesized design**