```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3
4  -- Uncomment the following library declaration if using
5  -- arithmetic functions with Signed or Unsigned values
6  --USE ieee.numeric_std.ALL;
7
8  ENTITY ADD8_test IS
9  END ADD8_test;
10
11 ARCHITECTURE behavior OF ADD8_test IS
12
13     -- Component Declaration for the Unit Under Test (UUT)
14
15     COMPONENT ADD8
16     PORT(
17          A : IN  std_logic_vector(7 downto 0);
18          B : IN  std_logic_vector(7 downto 0);
19          Cin : IN  std_logic;
20          Sum : OUT  std_logic_vector(7 downto 0);
21          Cout : OUT  std_logic
22         );
23     END COMPONENT;
24
25
26    --Inputs
27    signal A : std_logic_vector(7 downto 0) := (others => '0');
28    signal B : std_logic_vector(7 downto 0) := (others => '0');
29    signal Cin : std_logic := '0';
30
31     --Outputs
32    signal Sum : std_logic_vector(7 downto 0);
33    signal Cout : std_logic;
34
35 BEGIN
36
37     -- Instantiate the Unit Under Test (UUT)
38    uut: ADD8 PORT MAP (
39           A => A,
40           B => B,
41           Cin => Cin,
42           Sum => Sum,
43           Cout => Cout
```

```
        );


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 100 ns;

      A <= "10101010";
      B <= "00000000";
      Cin <= '0';
      wait for 10 ns;

      B <= "01010101";
      wait for 10 ns;

      Cin <= '1';
      wait for 10 ns;
        wait;
   end process;

END;
```