```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3
4  ENTITY ALU_8bit_test IS
5  END ALU_8bit_test;
6
7  ARCHITECTURE behavior OF ALU_8bit_test IS
8
9      -- Component Declaration for the Unit Under Test (UUT)
10
11     COMPONENT ALU_8bit
12     PORT(
13          DR1 : IN  std_logic_vector(7 downto 0);
14          DR2 : IN  std_logic_vector(7 downto 0);
15          Cin : IN  std_logic;
16          OPCODE : IN  std_logic_vector(3 downto 0);
17          AC : OUT  std_logic_vector(7 downto 0);
18          Cout : OUT  std_logic
19         );
20     END COMPONENT;
21
22
23    --Inputs
24    signal DR1 : std_logic_vector(7 downto 0) := (others => '0');
25    signal DR2 : std_logic_vector(7 downto 0) := (others => '0');
26    signal Cin : std_logic := '0';
27    signal OPCODE : std_logic_vector(3 downto 0) := (others => '0');
28
29     --Outputs
30    signal AC : std_logic_vector(7 downto 0);
31    signal Cout : std_logic;
32    -- No clocks detected in port list. Replace <clock> below with
33    -- appropriate port name
34
35 BEGIN
36
37     -- Instantiate the Unit Under Test (UUT)
38    uut: ALU_8bit PORT MAP (
39           DR1 => DR1,
40           DR2 => DR2,
41           Cin => Cin,
42           OPCODE => OPCODE,
43           AC => AC,
44           Cout => Cout
45         );
46
47
48    -- Stimulus process
49    stim_proc: process
50    begin
51       -- hold reset state for 100 ns.
52       wait for 100 ns;
53         DR1 <= "11110000";
54         DR2 <= "00111100";
55
56       OPCODE <= "0000";
57         wait for 20ns;
58
59       OPCODE <= "0100";
60       wait for 20ns;
61
```

```
62        OPCODE <= "0101";
63        wait for 20ns;
64
65        OPCODE <= "0110";
66        wait for 20ns;
67
68          OPCODE <= "0111";
69        wait for 20ns;
70
71          wait;
72     end process;
73
74  END;
```