

Title			ADC (FPGA Development Boards)		
Size	A4	Number	Revision		
Date:	2012/12/13	90/04/08	Sheet of	6	6
File:	E:\JDEVS\...\TSK002-01(ADC).SchDoc	Drawn By:	Design: M.SH		

A

B

C

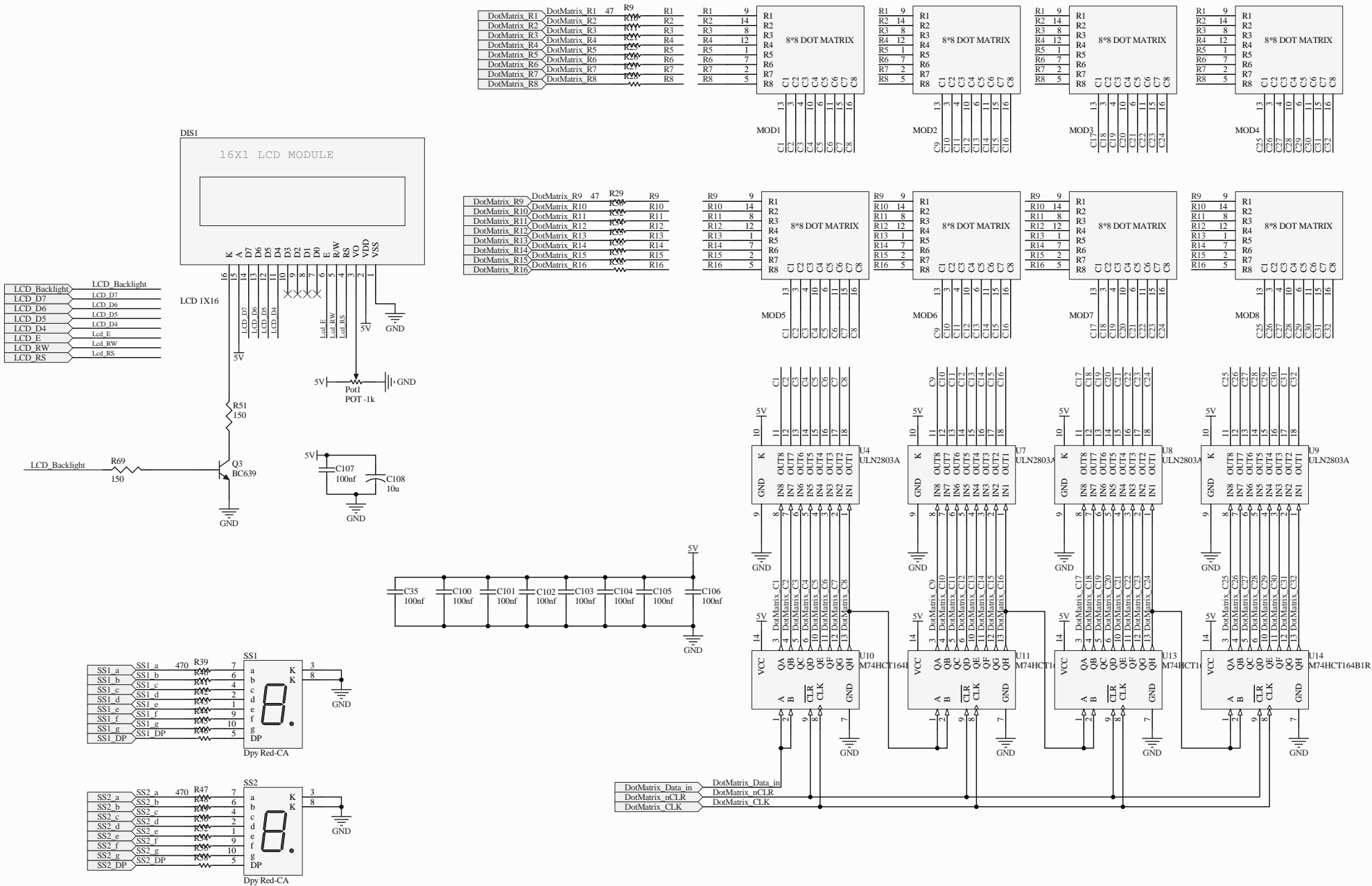
D

A

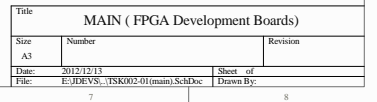
B

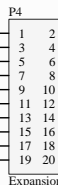
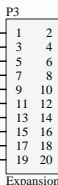
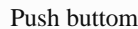
C

D

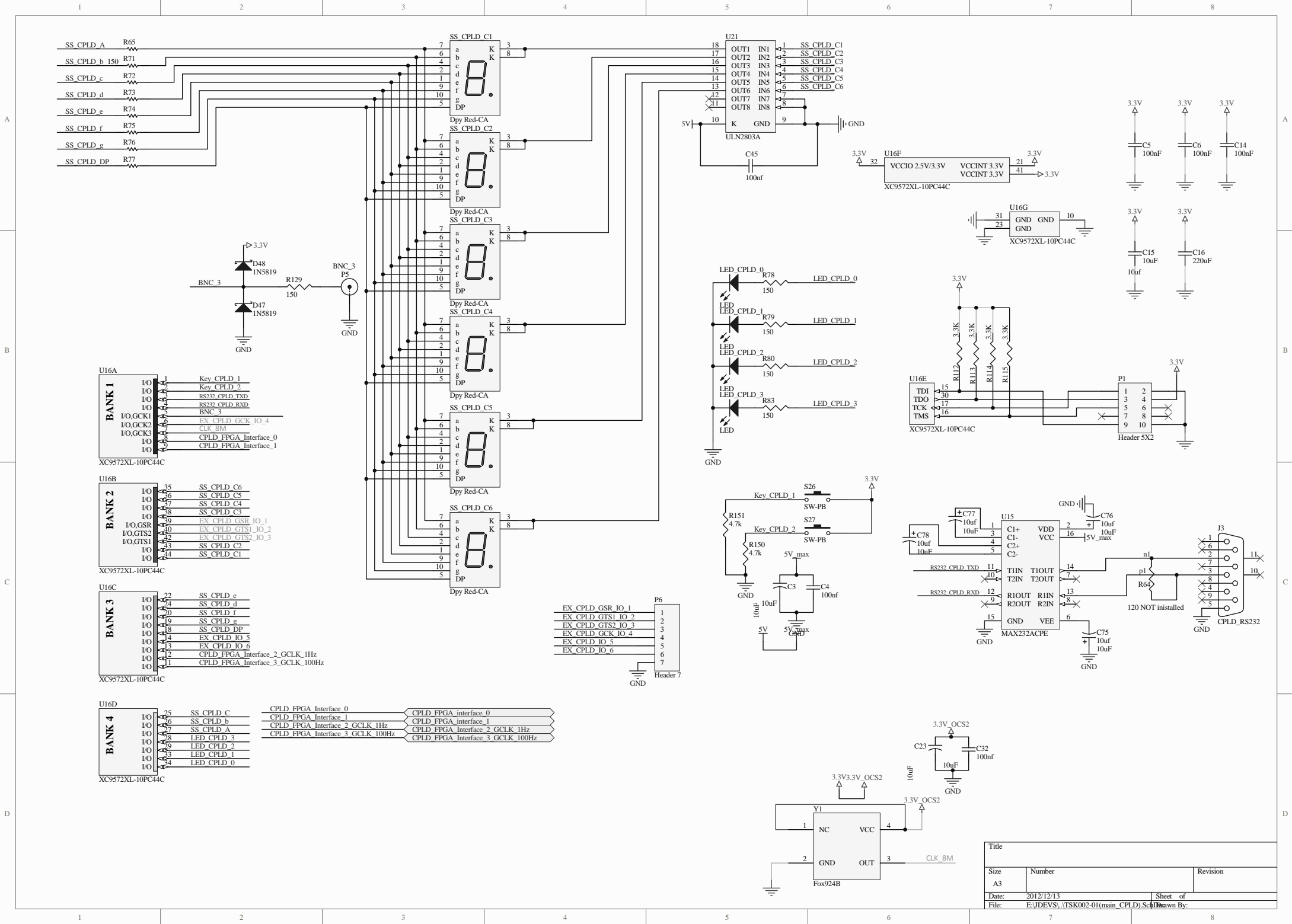


Title		
Size	Number	Revision
A3		
Date:	2012/12/13	Sheet of
File:	E:\DEVSV\...\TISK002-01(Display)\SchDoc	Drawn By:

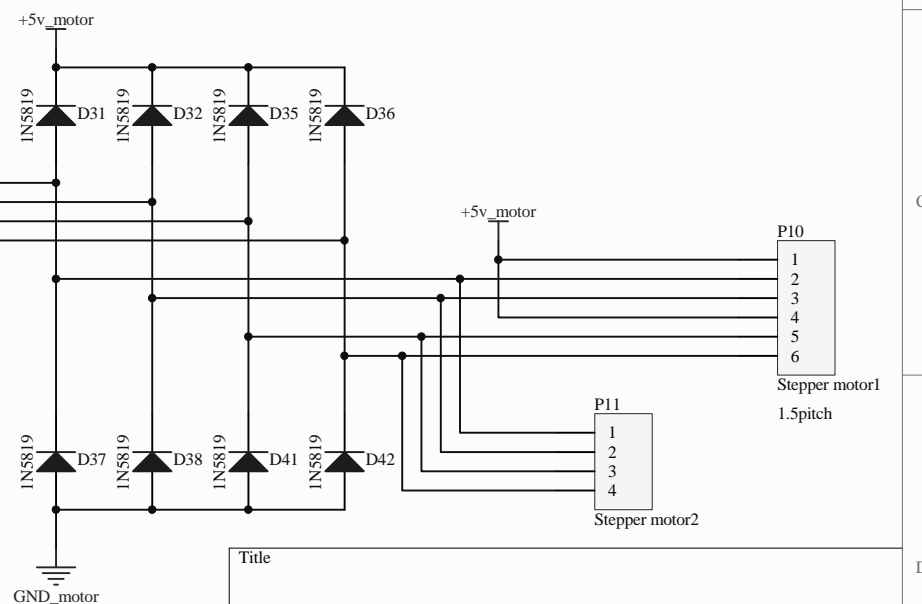
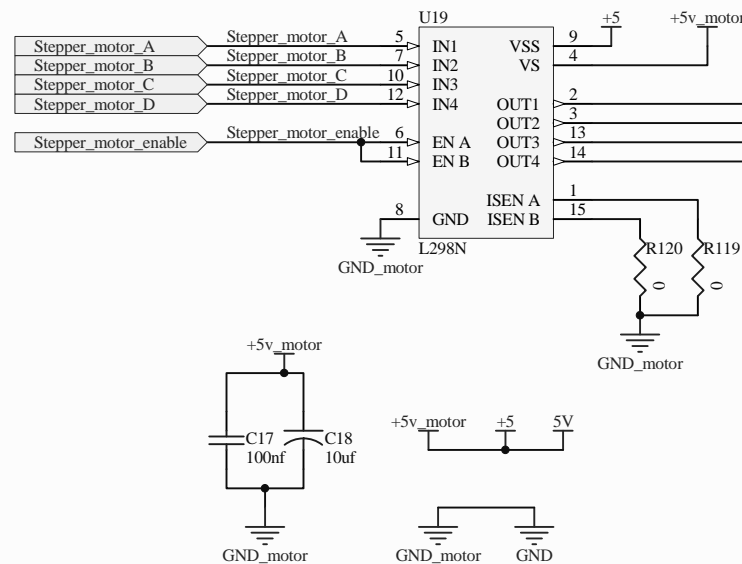
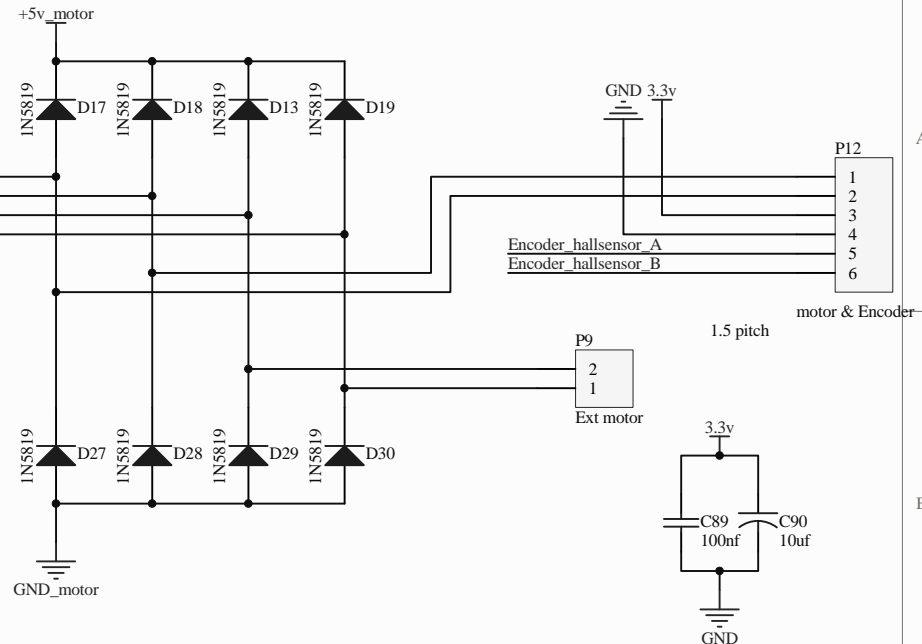
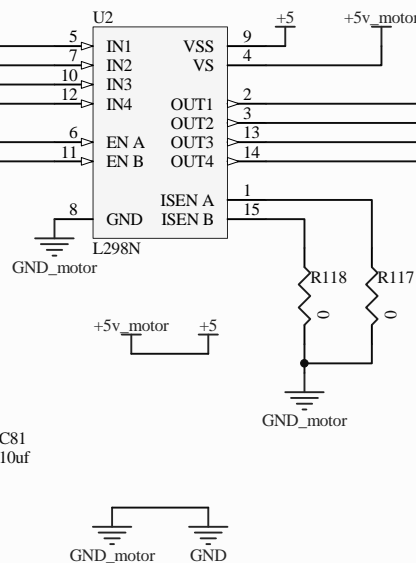
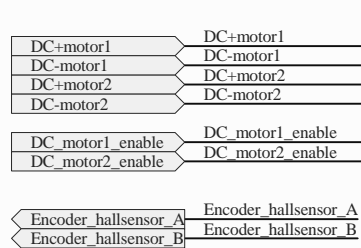




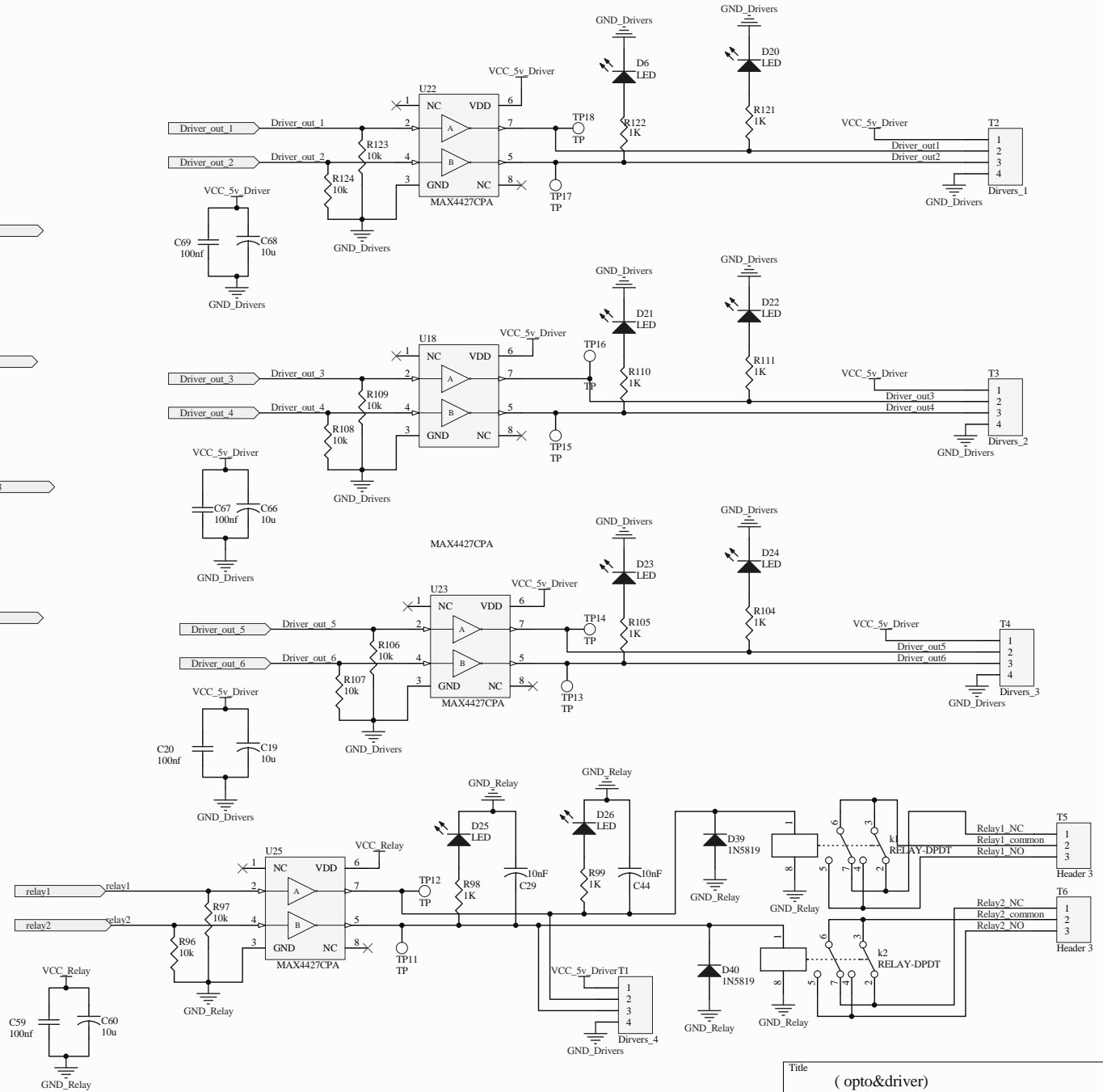
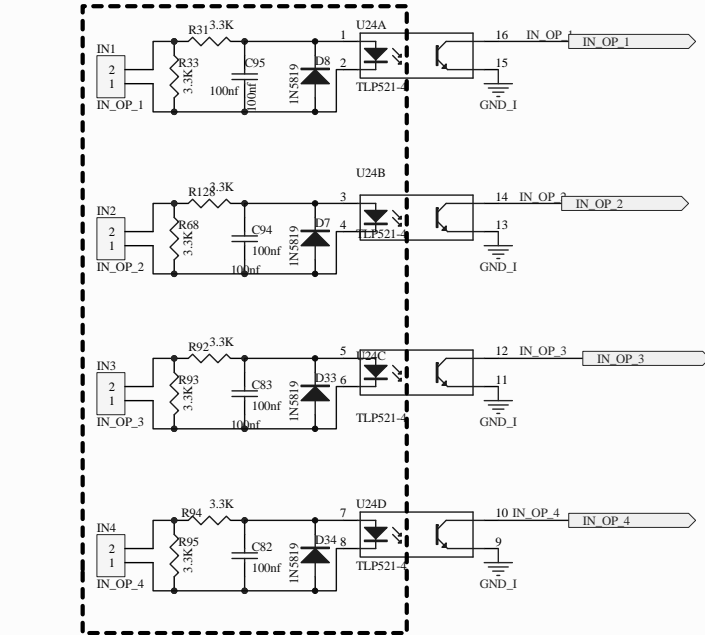
Title				interface (FPGA Development Boards)			
Size		Number				Revision	
A3							
Date:		90/04/08		Sheet 5 of 6			
File:		E:\JDEVS\...TSK002-01(interface).SchDoc		Drawn By:		Design: M.SH	



Title		
Size	Number	Revision
A3		
Date:	2012/12/13	Sheet of
File:	E:\JDEVSI\JTSK002-01(main_CPLD).Sch	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2012/12/13	Sheet of
File:	E:\JDEVS\...\TSK002-01(Motor Drivers).Sch	
	Drawn By:	



Title (opto&driver)				
Size A3	Number 90	01	Revision	
Date: 2012/12/13	90/05/20	8	9	
File: E:\JDEVSV\TSK002-01(OPTO),SchDoc	Shed Design: M.S.H		Drawn By:	