```vhdl
 1 library IEEE;
 2 use IEEE.STD_LOGIC_1164.ALL;
 3 use IEEE.NUMERIC_STD.ALL;
 4
 5
 6 entity ComBus is
 7     Port ( Sel : in  STD_LOGIC_VECTOR (2 downto 0);
 8            RW : in  STD_LOGIC;
 9            ALU: inout STD_LOGIC_VECTOR (7 downto 0);
10            AX : inout  STD_LOGIC_VECTOR (7 downto 0);
11            BX : inout  STD_LOGIC_VECTOR (7 downto 0);
12            CX : inout  STD_LOGIC_VECTOR (7 downto 0);
13            DX : inout  STD_LOGIC_VECTOR (7 downto 0);
14            RAM : inout  STD_LOGIC_VECTOR (7 downto 0);
15            BUS_DATA : inout  STD_LOGIC_VECTOR (7 downto 0));
16 end ComBus;
17
18 architecture Behavioral of ComBus is
19 signal R: STD_LOGIC_VECTOR (7 downto 0);
20 signal W: STD_LOGIC_VECTOR (7 downto 0) := "00000010";
21 begin
22
23     with Sel select
24         R <=    ALU when "000",
25                 AX  when "001",
26                 BX  when "010",
27                 CX  when "011",
28                 DX  when "100",
29                 RAM when "101",
30                 "ZZZZZZZZ" when others;
31
32     with RW select
33         BUS_DATA <= R when '1',
34                 "ZZZZZZZZ" when others;
35
36     with RW select
37         W <=    BUS_DATA when '0',
38                 "ZZZZZZZZ" when others;
39
40     ALU <=  W when (Sel = "000") else "ZZZZZZZZ";
41     AX  <=  W when (Sel = "001") else "ZZZZZZZZ";
42     BX  <=  W when (Sel = "010") else "ZZZZZZZZ";
43     CX  <=  W when (Sel = "011") else "ZZZZZZZZ";
```

```
44     DX  <=  W when (Sel = "100") else "ZZZZZZZZ";
45     RAM <=  W when (Sel = "101") else "ZZZZZZZZ";
46
47 end Behavioral;
```