```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3  USE ieee.numeric_std.ALL;
4
5  ENTITY ALU_test IS
6  END ALU_test;
7
8  ARCHITECTURE behavior OF ALU_test IS
9
10     -- Component Declaration for the Unit Under Test (UUT)
11
12     COMPONENT ALU
13     PORT(
14          A : IN  std_logic_vector(7 downto 0);
15          B : IN  std_logic_vector(7 downto 0);
16          F : OUT  std_logic_vector(7 downto 0);
17          Cin : IN  std_logic;
18          OPCODE : IN  std_logic_vector(3 downto 0);
19          Cout : OUT  std_logic
20         );
21     END COMPONENT;
22
23
24    --Inputs
25    signal A : std_logic_vector(7 downto 0) := (others => '0');
26    signal B : std_logic_vector(7 downto 0) := (others => '0');
27    signal Cin : std_logic := '0';
28    signal OPCODE : std_logic_vector(3 downto 0) := (others => '0');
29
30     --Outputs
31    signal F : std_logic_vector(7 downto 0);
32    signal Cout : std_logic;
33
34 BEGIN
35
36     -- Instantiate the Unit Under Test (UUT)
37    uut: ALU PORT MAP (
38           A => A,
39           B => B,
40           F => F,
41           Cin => Cin,
42           OPCODE => OPCODE,
43           Cout => Cout
```

```
44          );
45
46     -- Stimulus process
47     stim_proc: process
48     begin
49        A <= "11000000";
50        B <= "00000011";
51        Cin <= '1';
52
53        OPCODE <= "0000";
54        wait for 10 ns;
55
56        OPCODE <= "0001";
57        wait for 10 ns;
58
59        OPCODE <= "1010";
60        wait for 10 ns;
61
62        wait;
63     end process;
64
65  END;
```