```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity ADD8 is
5      Port ( A : in        STD_LOGIC_VECTOR (7 downto 0);
6             B : in        STD_LOGIC_VECTOR (7 downto 0);
7             Cin : in      STD_LOGIC;
8             Sum : out     STD_LOGIC_VECTOR (7 downto 0);
9             Cout : out    STD_LOGIC);
10 end ADD8;
11
12 architecture Behavioral of ADD8 is
13     signal c: STD_LOGIC_VECTOR (6 downto 0);
14
15     COMPONENT FA
16     PORT(
17         A : IN      std_logic;
18         B : IN      std_logic;
19         Cin : IN    std_logic;
20         Sum : OUT   std_logic;
21         Cout : OUT  std_logic
22         );
23     END COMPONENT;
24 begin
25
26 -- FA 0
27 Inst_FA0: FA PORT MAP (
28         A => A(0),
29         B => B(0),
30         Cin => Cin,
31         Sum => Sum(0),
32         Cout => c(0)
33     );
34
35 -- FA from 1 to 6
36 gen : for i in 1 to 6 generate
37     Inst_FA: FA PORT MAP (
38         A => A(i),
39         B => B(i),
40         Cin => c(i-1),
41         Sum => Sum(i),
42         Cout => c(i)
43     );
```

```
44 end generate ; -- gen
45
46 -- FA 7
47 Inst_FA7: FA PORT MAP (
48         A => A(7),
49         B => B(7),
50         Cin => c(6),
51         Sum => Sum(7),
52         Cout => Cout
53     );
54
55 end Behavioral;
```