```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity FA is
5      Port ( A : in        STD_LOGIC;
6             B : in        STD_LOGIC;
7             Cin : in      STD_LOGIC;
8             Sum : out     STD_LOGIC;
9             Cout : out    STD_LOGIC);
10 end FA;
11
12 architecture Behavioral of FA is
13 begin
14     Sum <= A xor B xor Cin;
15    Cout <= (A and B) or (B and Cin) or (A and Cin);
16
17 end Behavioral;
```