Three Phase Pre-Driver with Dual Current Shunt Amplifiers and Buck Regulator – Hardware Controlled

Check for Samples: DRV8302

FEATURES

- **Operating Supply Voltage 8V–60V**
- **2.3A Sink and 1.7A Source Gate Drive Current Capability**
- **Integrated Dual Shunt Current Amplifiers With Adjustable Gain and Offset**
- **Integrated Buck Converter to Support up to 1.5A External Load**
- **Independent Control of 3 or 6 PWM Inputs**
- **Bootstrap Gate Driver With 100% Duty Cycle Support**
- **Programmable Dead Time to Protect External FETs from Shoot Through**
- **Programmable Overcurrent Protection of External MOSFETs**
- **Thermally Enhanced 56-Pin TSSOP Pad Down DCA Package**

APPLICATIONS

- **3-Phase Brushless DC Motor and Permanent Magnet Synchronous Motor**
- **CPAP and Pump**
- **E-bike, Hospital Bed, Wheel Chair**
- **Power Drill, Blender, Chopper**

DESCRIPTION

The DRV8302 is a gate driver IC for three phase motor drive applications. It provides three half bridge drivers, each capable of driving two N-type MOSFETs, one for the high-side and one for the low side. It supports up to 2.3A sink and 1.7A source peak current capability and only needs a single power supply with a wide range from 8 to 60V. The DRV8302 uses bootstrap gate drivers with trickle charge circuitry to support 100% duty cycle. The gate driver uses automatic hand shaking when high side FET or low side FET is switching to prevent current shoot through. Vds of FETs is sensed to protect external power stage during overcurrent conditions.

The DRV8302 includes two current shunt amplifiers for accurate current measurement. The current amplifiers support bi-directional current sensing and provide an adjustable output offset of up to 3V.

The DRV8302 also has an integrated switching mode buck converter with adjustable output and switching frequency to support MCU or additional system power needs. The buck is capable to drive up to 1.5A load.

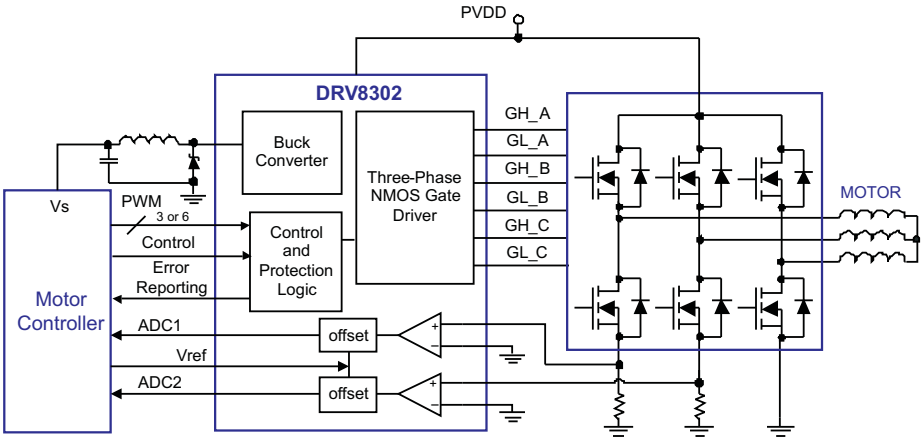


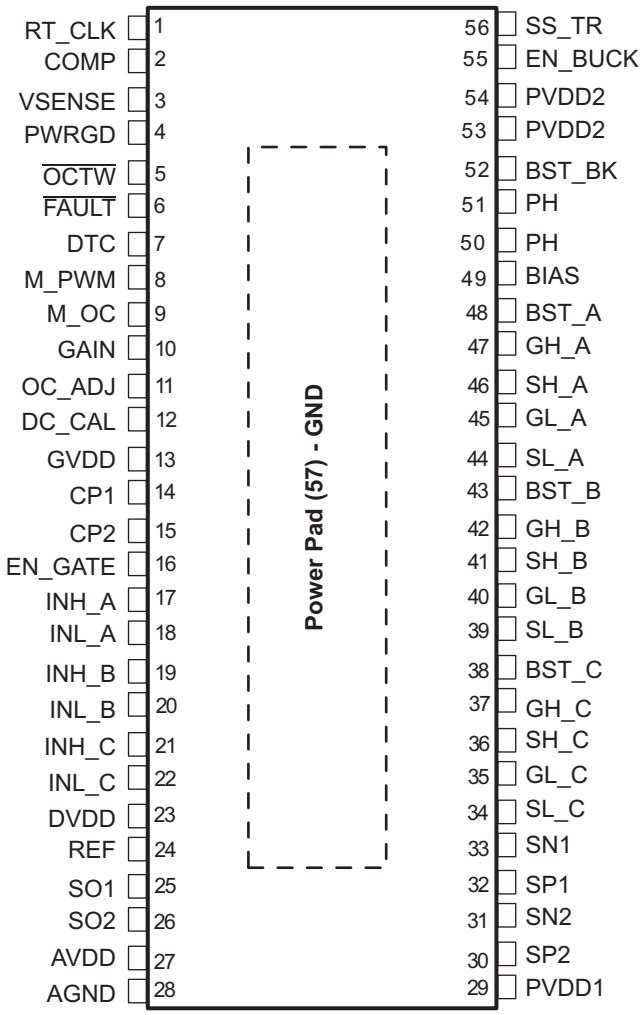
Figure 1. DRV8302 Simplified Application Schematic

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

PIN ASSIGNMENT

The DRV8302 is designed to fit the 56pin DCA package. Here is the pinout of the device.



PIN FUNCTIONS

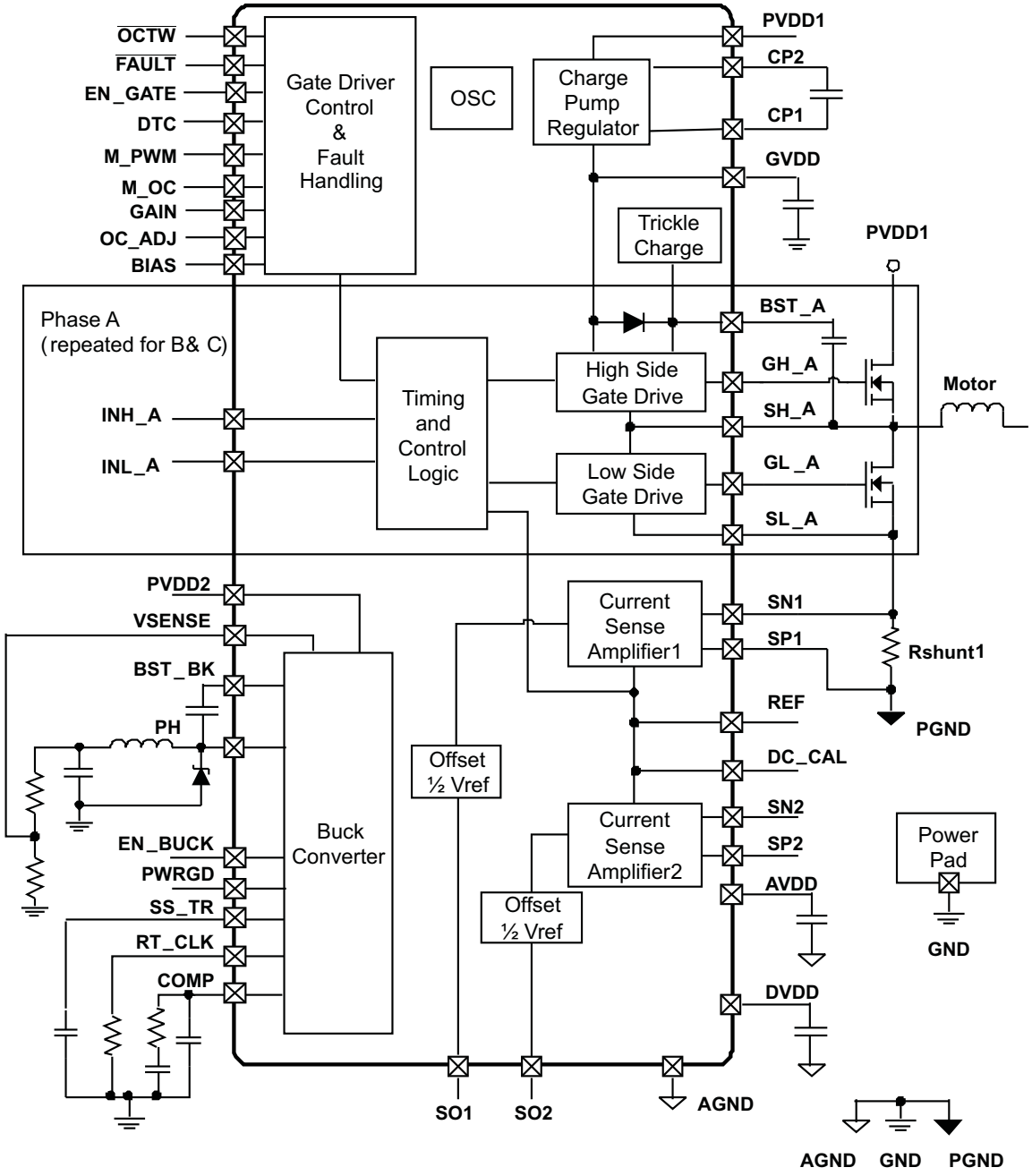
PIN		I/O(1)	DESCRIPTION
NAME	NO.		
RT_CLK	1	I	Resistor timing and external clock for buck regulator. Resistor should connect to GND (power pad) with very short trace to reduce the potential clock jitter due to noise.
COMP	2	O	Buck error amplifier output and input to the output switch current comparator.
VSENSE	3	I	Buck output voltage sense pin. Inverting node of error amplifier.
PWRGD	4	I	An open drain output with external pull-up resistor required. Asserts low if buck output voltage is low due to thermal shutdown, dropout, over-voltage, or EN_BUCK shut down
$\overline{\text{OCTW}}$	5	O	Over current and over temperature warning indicator. This output is open drain with external pull-up resistor required.
$\overline{\text{FAULT}}$	6	O	Fault report indicator. This output is open drain with external pull-up resistor required.
DTC	7	I	Dead-time adjustment with external resistor to GND
M_PWM	8	I	Mode selection pin for PWM input configuration. If M_PWM = LOW, the device supports 6 independent PWM inputs. When M_PWM = HIGH, the device must be connected to ONLY 3 PWM input signals on INH_x. The complementary PWM signals for low side signaling will be internally generated from the high side inputs.
M_OC	9	I	Mode selection pin for over-current protection options. If M_OC = LOW, the gate driver will operate in a cycle-by-cycle current limiting mode. If M_OC = HIGH, the gate driver will shutdown the channel which detected an over-current event.
GAIN	10	O	Gain selection for integrated current shunt amplifiers. If GAIN = LOW, the internal current shunt amplifiers have a gain of 10V/V. If GAIN = HIGH, the current shunt amplifiers have a gain of 40V/V.
OC_ADJ	11	I	Over-current trip set pin. Apply a voltage on this pin to set the trip point for the internal over-current protection circuitry. A voltage divider from DVDD is recommended.
DC_CAL	12	I	When DC_CAL is high, device shorts inputs of shunt amplifiers and disconnects loads. DC offset calibration can be done through external microcontroller.
GVDD	13	P	Internal gate driver voltage regulator. GVDD cap should connect to GND
CP1	14	P	Charge pump pin 1, ceramic cap should be used between CP1 and CP2
CP2	15	P	Charge pump pin 2, ceramic cap should be used between CP1 and CP2
EN_GATE	16	I	Enable gate driver and current shunt amplifiers. Control buck via EN_BUCK pin.
INH_A	17	I	PWM Input signal (high side), half-bridge A
INL_A	18	I	PWM Input signal (low side), half-bridge A
INH_B	19	I	PWM Input signal (high side), half-bridge B
INL_B	20	I	PWM Input signal (low side), half-bridge B
INH_C	21	I	PWM Input signal (high side), half-bridge C
INL_C	22	I	PWM Input signal (low side), half-bridge C
DVDD	23	P	Internal 3.3V supply voltage. DVDD cap should connect to AGND. This is an output, but not specified to drive external circuitry.
REF	24	I	Reference voltage to set output of shunt amplfiiers with a bias voltage which equals to half of the voltage set on this pin. Connect to ADC reference in microcontroller.
SO1	25	O	Output of current amplifier 1
SO2	26	O	Output of current amplifier 2
AVDD	27	P	Internal 6V supply voltage, AVDD cap should connect to AGND. This is an output, but not specified to drive external circuitry.
AGND	28	P	Analog ground pin
PVDD1	29	P	Power supply pin for gate driver and current shunt amplifier. PVDD1 is independent of buck power supply, PVDD2. PVDD1 cap should connect to GND
SP2	30	I	Input of current amplifier 2 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best commom mode rejection.
SN2	31	I	Input of current amplifier 2 (connecting to negative input of amplifier).
SP1	32	I	Input of current amplifier 1 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best commom mode rejection.
SN1	33	I	Input of current amplifier 1 (connecting to negative input of amplifier).

(1) KEY: I =Input, O = Output, P = Power

PIN FUNCTIONS (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
SL_C	34	I	Low-Side MOSFET source connection, half-bridge C. Low-side V_{DS} measured between this pin and SH_C.
GL_C	35	O	Gate drive output for Low-Side MOSFET, half-bridge C
SH_C	36	I	High-Side MOSFET source connection, half-bridge C. High-side V_{DS} measured between this pin and PVDD1.
GH_C	37	O	Gate drive output for High-Side MOSFET, half-bridge C
BST_C	38	P	Bootstrap cap pin for half-bridge C
SL_B	39	I	Low-Side MOSFET source connection, half-bridge B. Low-side V_{DS} measured between this pin and SH_B.
GL_B	40	O	Gate drive output for Low-Side MOSFET, half-bridge B
SH_B	41	I	High-Side MOSFET source connection, half-bridge B. High-side V_{DS} measured between this pin and PVDD1.
GH_B	42	O	Gate drive output for High-Side MOSFET, half-bridge B
BST_B	43	P	Bootstrap cap pin for half-bridge B
SL_A	44	I	Low-Side MOSFET source connection, half-bridge A. Low-side V_{DS} measured between this pin and SH_A.
GL_A	45	O	Gate drive output for Low-Side MOSFET, half-bridge A
SH_A	46	I	High-Side MOSFET source connection, half-bridge A. High-side V_{DS} measured between this pin and PVDD1.
GH_A	47	O	Gate drive output for High-Side MOSFET, half-bridge A
BST_A	48	P	Bootstrap cap pin for half-bridge A
BIAS	49	I	Bias pin. Connect 1MΩ resistor to GND, or 0.1 µF capacitor to GND.
PH	50, 51	O	The source of the internal high side MOSFET of buck converter
BST_BK	52	P	Bootstrap cap pin for buck converter
PVDD2	53,54	P	Power supply pin for buck converter, PVDD2 cap should connect to GND.
EN_BUCK	55	I	Enable buck converter. Internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors
SS_TR	56	I	Buck soft-start and tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. Cap should connect to GND
GND (POWER PAD)	57	P	GND pin. The exposed power pad must be electrically connected to ground plane through soldering to PCB for proper operation and connected to bottom side of PCB through vias for better thermal spreading.

FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

			VALUE		UNITS
			MIN	MAX	
PVDD	Supply voltage range including transient	Relative to PGND	–0.3	70	V
$PVDD_{RAMP}$	Maximum supply voltage ramp rate	Voltage rising up to $PVDD_{MAX}$	50		V/mS
V_{PGND}	Maximum voltage between PGND and GND		±0.3		V
I_{IN_MAX}	Maximum current, all digital and analog input pins except $\overline{FAULT}$ and $\overline{OCTW}$ pins		±1		mA
$I_{IN\_OD\_MAX}$	Maximum sinking current for open drain pins ($\overline{FAULT}$ and $\overline{OCTW}$ Pins)		7		mA
V_{OPA_IN}	Voltage range for SPx and SNx pins		±0.6		V
V_{LOGIC}	Input voltage range for logic/digital pins (INH_A, INL_A, INH_B, INL_B, INH_C, INL_C, EN_GATE, M_PWM, M_OC, OC_ADJ, GAIN, DC_CAL)		-0.3	7	V
V_{GVDD}	Maximum voltage for GVDD Pin		13.2		V
V_{AVDD}	Maximum voltage for AVDD Pin		8		V
V_{DVDD}	Maximum voltage for DVDD Pin		3.6		V
V_{REF}	Maximum reference voltage for current amplifier		7		V
I_{REF}	Maximum current for REF Pin		100		µA
T_J	Maximum operating junction temperature range		–40	150	°C
$T_{STORAGE}$	Storage temperature range		–55	150	°C
	Capacitive discharge model		500		V
	Human body model		2000		V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8302 DCA (56) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.5	
θ_{JB}	Junction-to-board thermal resistance	17.5	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	7.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNITS
PVDD1	DC supply voltage PVDD1 for normal operation	Relative to PGND	8		60	V
PVDD2	DC supply voltage PVDD2 for buck converter		3.5		60	V
C_{AVDD}	External capacitance on AVDD pin (ceramic cap) 20% tolerance			1		µF
C_{DVDD}	External capacitance on DVDD pin (ceramic cap) 20% tolerance			1		µF
C_{GVDD}	External capacitance on GVDD pin (ceramic cap) 20% tolerance			2.2		µF
C_{CP}	Flying cap on charge pump pins (between CP1 and CP2) (ceramic cap) 20% tolerance			22		nF
C_{BST}	Bootstrap cap (ceramic cap)			100		nF
I_{DIN_EN}	Input current of digital pins when EN_GATE is high				100	µA
I_{DIN_DIS}	Input current of digital pins when EN_GATE is low				1	µA
C_{DIN}	Maximum capacitance on digital input pin				10	pF
C_{O_OPA}	Maximum output capacitance on outputs of shunt amplifier				20	pF
R_{DTC}	Dead time control resistor range. Time range is 50ns (-GND) to 500ns (150kΩ) with a linear approximation.		0		150	kΩ
I_{FAULT}	$\overline{\text{FAULT}}$ pin sink current. Open-drain	V = 0.4 V			2	mA
I_{OCTW}	$\overline{\text{OCTW}}$ pin sink current. Open-drain	V = 0.4 V			2	mA
V_{REF}	External voltage reference voltage for current shunt amplifiers		2		6	V
f_{gate}	Operating switching frequency of gate driver	Qg(TOT) = 25 nC or total 30 mA gate drive average current			200	kHz
T_A	Ambient temperature		–40		125	°C

ELECTRICAL CHARACTERISTICS

PVDD = 8-60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT PINS: INH_X, INL_X, M_PWM, M_OC, GAIN, EN_GATE, DC_CAL						
V_{IH}	High input threshold		2			V
V_{IL}	Low input threshold				0.8	V
R_{EN_GATE}	Internal pull down resistor for EN_GATE			100		kΩ
R_{INH_X}	Internal pull down resistor for high side PWMs (INH_A, INH_B, and INH_C)	EN_GATE high		100		kΩ
R_{INH_X}	Internal pull down resistor for low side PWMs (INL_A, INL_B, and INL_C)	EN_GATE high		100		kΩ
R_{M_PWM}	Internal pull down resistor for M_PWM	EN_GATE high		100		kΩ
R_{M_OC}	Internal pull down resistor for M_OC	EN_GATE high		100		kΩ
R_{DC_CAL}	Internal pull down resistor for DC_CAL	EN_GATE high		100		kΩ
OUTPUT PINS: $\overline{\text{FAULT}}$ AND $\overline{\text{OCTW}}$						
V_{OL}	Low output threshold	I_O = 2 mA			0.4	V
V_{OH}	High output threshold	External 47 kΩ pull up resistor connected to 3-5.5 V	2.4			V
I_{OH}	Leakage Current on Open Drain Pins When Logic High ($\overline{\text{FAULT}}$ and $\overline{\text{OCTW}}$)				1	µA

ELECTRICAL CHARACTERISTICS (continued)

PVDD = 8-60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVE OUTPUT: GH_A, GH_B, GH_C, GL_A, GL_B, GL_C						
V_{GX_NORM}	Gate driver Vgs voltage	PVDD = 8–60V	9.5		11.5	V
I_{oso1}	Maximum source current setting 1, peak	Vgs of FET equals to 2 V. REG 0x02		1.7		A
I_{osi1}	Maximum sink current setting 1, peak	Vgs of FET equals to 8 V. REG 0x02		2.3		A
R_{gate_off}	Gate output impedence during standby mode when EN_GATE low (pins GH_x, GL_x)		1.6		2.4	kΩ
SUPPLY CURRENTS						
I_{PVDD1_STB}	PVDD1 supply current, standby	EN_GATE is low. PVDD1 = 8V.		20	50	µA
I_{PVDD1_OP}	PVDD1 supply current, operating	EN_GATE is high, no load on gate drive output, switching at 10 kHz, 100 nC gate charge		15		mA
I_{PVDD1_HIZ}	PVDD1 Supply current, HiZ	EN_GATE is high, gate not switching	2	5	11	mA
INTERNAL REGULATOR VOLTAGE						
A_{VDD}	AVDD voltage		6	6.5	7	V
D_{VDD}	DVDD voltage		3	3.3	3.6	V
VOLTAGE PROTECTION						
V_{PVDD_UV}	Under voltage protection limit, PVDD				6	V
V_{GVDD_UV}	Under voltage protection limit, GVDD				8	V
V_{GVDD_OV}	Over voltage protection limit, GVDD			16		V
CURRENT PROTECTION, (VDS SENSING)						
V_{DS_OC}	Drain-source voltage protection limit		0.125		2.4	V
T_{oc}	OC sensing response time			1.5		µs
T_{OC_PULSE}	$\overline{\text{OCTW}}$ pin reporting pulse stretch length for OC event			64		µs

GATE TIMING AND PROTECTION CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING, OUTPUT PINS						
$t_{pd,lf-O}$	Positive input falling to GH_x falling	CL=1nF, 50% to 50%		45		ns
$t_{pd,lr-O}$	Positive input rising to GL_x falling	CL=1nF, 50% to 50%		45		ns
T_{d_min}	Minimum dead time after hand shaking (1)				50	ns
T_{dtp}	Dead Time	With R_{DTC} set to different values	50		500	ns
t_{GDr}	Rise time, gate drive output	CL=1nF, 10% to 90%		25		ns
t_{GDF}	Fall time, gate drive output	CL=1nF, 90% to 10%		25		ns
T_{ON_MIN}	Minimum on pulse	Not including handshake communication. Hiz to on state, output of gate driver			50	ns
T_{pd_match}	Propagation delay matching between high side and low side				5	ns
T_{dt_match}	Deadtime matching				5	ns
TIMING, PROTECTION AND CONTROL						
$t_{pd,R\_GATE-OP}$	Start up time, from EN_GATE active high to device ready for normal operation	PVDD is up before start up, all charge pump caps and regulator caps as in recommended condition		5	10	ms
$t_{pd,R\_GATE-Quick}$	If EN_GATE goes from high to low and back to high state within quick reset time, it will only reset all faults and gate driver without powering down charge pump, current amp, and related internal voltage regulators.	Maximum low pulse time			10	us
$t_{pd,E-L}$	Delay, error event to all gates low			200		ns
$t_{pd,E-FAULT}$	Delay, error event to $\overline{FAULT}$ low			200		ns
OTW_CLR	Junction temperature for resetting over temperature warning			115		°C
OTW_SET/OTSD_CLR	Junction temperature for over temperature warning and resetting over temperature shut down			130		°C
OTSD_SET	Junction temperature for over temperature shut down			150		°C

(1) Dead time programming definition: Adjustable delay from GH_x falling edge to GL_X rising edge, and GL_X falling edge to GH_X rising edge. This is a minimum dead-time insertion. It is not added to the value set by the microcontroller externally.

CURRENT SHUNT AMPLIFIER CHARACTERISTICS

T_C = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G1	Gain option 1	(GAIN = 0V)	9.5	10	10.5	V/V
G2	Gain Option 2	(GAIN = 2V)	38	40	42	V/V
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 10, Vstep = 2 V		300		ns
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 40, Vstep = 2 V		1.2		µs
Vswing	Output swing linear range		0.3		5.7	V
Slew Rate		G = 10		10		V/µs
DC_offset	Offset error RTI	G = 10 with input shorted			4	mV
Drift_offset	Offset drift RTI			10		µV/C
Ibias	Input bias current				100	µA
Vin_com	Common input mode range		–0.15		0.15	V
Vin_dif	Differential input range		–0.3		0.3	V
Vo_bias	Output bias	With zero input current, Vref up to 6 V	–0.5%	0.5×Vref	0.5%	V
CMRR_OV	Overall CMRR with gain resistor mismatch	CMRR at DC, gain = 10	70	85		dB

BUCK CONVERTER CHARACTERISTICS

T_C = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
$I_{SD(PVDD2)}$	Shutdown supply current	EN = 0 V, 25°C, 3.5 V ≤ VIN ≤ 60 V		1.3	4	µA
$I_{NON\_SW(PVDD2)}$	Operating: nonswitching supply current	VSENSE = 0.83 V, VIN = 12 V		116	136	µA
V_{EN_BUCK}	Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	0.9	1.25	1.55	V
R_{DS_ON}	On-resistance	VIN = 12 V, BOOT-PH = 6 V		200	410	mΩ
I_{LIM}	Current limit threshold	VIN = 12 V, T_J = 25°C	1.8	2.7		A
OTSD_BK	Thermal shutdown			150		°C
F_{sw}	Switching frequency	RT = 200 kΩ	450	581	720	kHz
PWRGD	VSENSE threshold	VSENSE falling		92%		
		VSENSE rising		94%		
		VSENSE rising		109%		
		VSENSE falling		107%		
	Hysteresis	VSENSE falling		2%		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω

FUNCTIONAL DESCRIPTION

THREE-PHASE GATE DRIVER

The DRV8302 provides three half bridge drivers, each capable of driving two N-type MOSFETs, one for the high-side and one for the low side.

Gate driver has following features:

- Internal hand shake between high side and low side FETs during switching transition to prevent current shoot through.
- Support up to 200kHz switching frequency with Qg(TOT)=25nC or total 30mA gate drive average current
- Provide cycle-by-cycle current limiting and latch over-current (OC) shut down of external FETs. Current is sensed through FET drain-to-source voltage and the over-current level is programmable through OC_ADJ pin
- High side gate drive will survive negative output from half bridge up to –10V for 10ns
- During EN_GATE pin low and fault conditions, gate driver will keep external FETs in high impedance mode.
- Programmable dead time through DTC pin. Dead time control range: 50ns to 500ns. Short DTC pin to ground will provide minimum dead time (50ns). External dead time will override internal dead time as long as the time is longer than the dead time setting (minimum hand shake time cannot be reduced in order to prevent shoot through current).
- Bootstraps are used in high side FETs of three-phase pre-gate driver. Trickle charge circuitry is used to replenish current leakage from bootstrap cap and support 100% duty cycle operation.

CURRENT SHUNT AMPLIFIERS

The DRV8302 includes two high performance current shunt amplifiers for accurate current measurement. The current amplifiers provide output offset up to 3V to support bi-directional current sensing.

Current shunt amplifier has following features:

- Programmable gain: 2 gain settings through GAIN pin
- Programmable output offset through reference pin (half of the Vref)
- Minimize DC offset and drift over temperature with dc calibrating through DC_CAL pin. When DC calibration is enabled, device will short input of current shunt amplifier and disconnect the load. DC calibrating can be done at anytime even when FET is switching since the load is disconnected. For best result, perform the DC calibrating during switching off period when no load is present to reduce the potential noise impact to the amplifier.

The output of current shunt amplifier can be calculated as:

$$V_O = \frac{V_{REF}}{2} - G \times (SN_X - SP_X) \quad (1)$$

Where Vref is the reference voltage, G is the gain of the amplifier; SNx and SPx are the inputs of channel x. SPx should connect to resistor ground for the best common mode rejection.

Figure 2 shows current amplifier simplified block diagram.

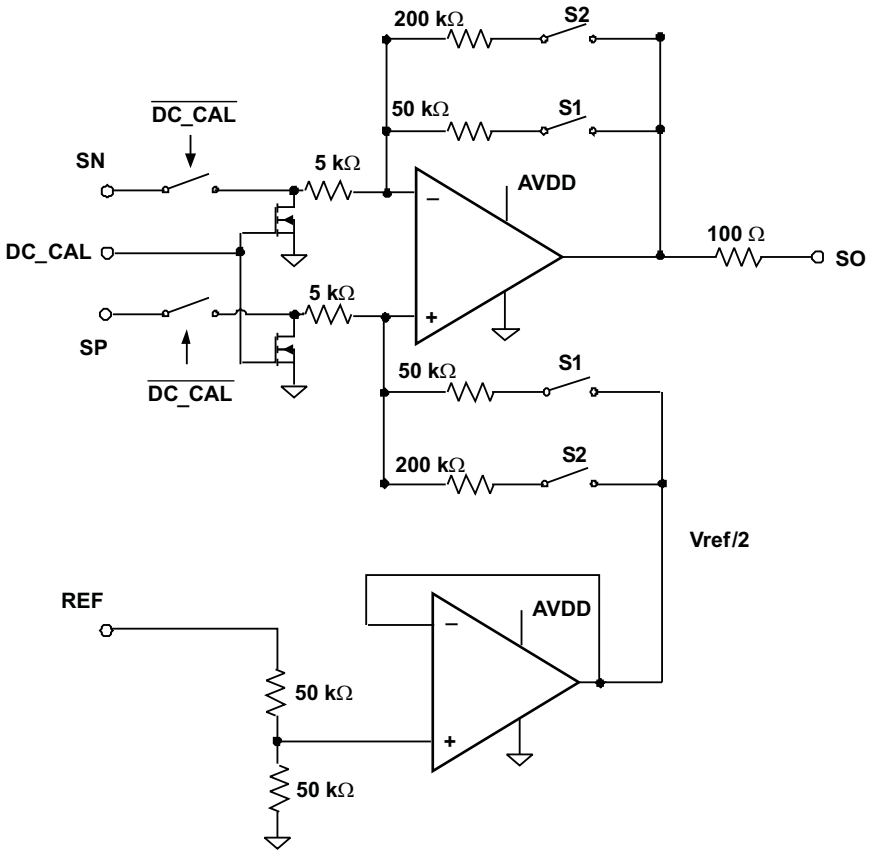


Figure 2. Current Shunt Amplifier Simplified Block Diagram

BUCK CONVERTER

Although integrated in the same device, buck converter is designed completely independent of rest of the gate driver circuitry. Since buck will support external MCU or other external power need, the independency of buck operation is very critical for a reliable system; this will give buck minimum impact from gate driver operations. Some examples are: when gate driver shuts down due to any failure, buck will still operate unless the fault is coming from buck itself. The buck keeps operating at much lower PVDD of 3.5V, this will assure the system to have a smooth power up and power down sequence when gate driver is not able to operate due to a low PVDD.

The buck has an integrated high side n-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The wide switching frequency of 450kHz to 720kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT_CLK pin.

The buck converter has a default start up voltage of approximately 2.5V. The EN_BUCK pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) threshold with two external resistors. In addition, the pull up current provides a default condition. When the EN_BUCK pin is floating the device will operate. The operating current is 116μA when not switching and under no load. When the device is disabled, the supply current is 1.3μA.

The integrated 200mΩ high side MOSFET allows for high efficiency power supply designs capable of delivering 1.5 amperes of continuous current to a load. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The buck can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8V reference.

The buck has a power good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open drain output which deasserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage allowing the pin to transition high when a pull-up resistor is used.

The buck minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power good comparator. When the OV comparator is activated, the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS_TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin to adjust the slow start time. A resistor divider can be coupled to the pin for critical power supply sequencing requirements. The SS_TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an over-temperature fault,

The buck, also, discharges the slow start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit will slow start the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

PROTECTION FEATURES

Power Stage Protection

The DRV8302 provides over-current and under-voltage protection for the MOSFET power stage. During fault shut down conditions, all gate driver outputs will be kept low to ensure external FETs at high impedance state.

Over-Current Protection (OCP) and Reporting

To protect the power stage from damage due to high currents, a V_{DS} sensing circuitry is implemented in the DRV8302. Based on $R_{DS(on)}$ of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated which, when exceeded, triggers the OC protection feature. This voltage threshold level is programmable through the OC_ADJ terminal (see next section) by applying an external reference voltage with a DAC or resistor divider from DVDD.

There are a total of 2 OC_MODE settings selectable with the M_OC pin.

1. Current Limit Mode (M_OC = LOW)

   When current limit mode is enabled, device operates current limiting instead of OC shut down during OC event. During OC event, the FET that detected OC will turn off until next PWM cycle. The over-current event is reported through $\overline{\text{OCTW}}$ pin. $\overline{\text{OCTW}}$ reporting should hold low during same PWM cycle or for a max 64µs period (internal timer) so external controller has enough time to sample the warning signal. If in the middle of reporting, other FET(s) gets OC, then OCTW reporting will hold low and recount another 64µS unless PWM cycles on both FETs are ended.
2. OC latch shut down mode (M_OC = HIGH)

   When OC occurs, device will turn off both high side and low side FETs in the same phase if any of the FETs in that phase has OC.

OC_ADJ

When external MOSFET is turned on, the output current flows through the on resistance, $RD_{S(on)}$ of the MOSFET, which creates a voltage drop V_{DS}. The over current protection event will be enabled when the V_{DS} exceeds a pre-set value. The voltage on OC_ADJ pin will be used to pre-set the OC tripped value. The OC tripped value I_{OC} has to meet following equations:

$$\frac{R2}{(R1 + R2)} \times DVDD = V_{DS} \quad (2)$$

$$I_{OC} = \frac{V_{DS}}{R_{DS(on)}} \quad (3)$$

Where

R1 + R2 ≥ 100 KΩ

DVDD = 3.3 V

Connect OC_ADJ pin to DVDD to disable the over-current protection feature.

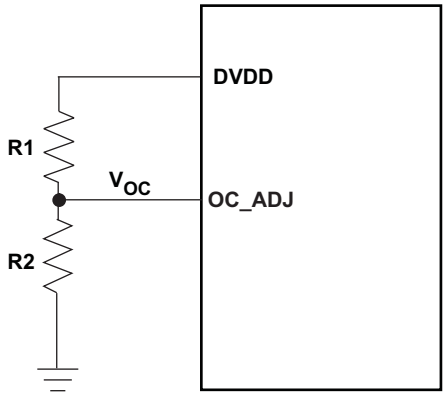


Figure 3. OC_ADJ Current Programming Pin Connection

Under-Voltage Protection (UVP)

To protect the power output stage during startup, shutdown and other possible under-voltage conditions, the DRV8302 provides power stage under-voltage protection by driving its outputs low whenever PVDD is below 6V (PVDD_UV) or GVDD is below 8V (GVDD_UV). When UVP is triggered, the DRV8302 outputs are driven low and the external MOSFETs will go to a high impedance state.

Over-Voltage Protection (GVDD_OV)

Device will shut down both gate driver and charge pump if GVDD voltage exceeds 16V to prevent potential issue related to GVDD or charge pump (e.g. short of external GVDD cap or charge pump). The fault is a latched fault and can only be reset through a transition on EN_GATE pin.

Over-Temperature Protection

A two-level over-temperature detection circuit is implemented:

- Level 1: over temperature warning (OTW)
  OTW is reported through $\overline{\text{OCTW}}$ pin.
- Level 2: over temperature (OT) latched shut down of gate driver and charge pump (OTSD_GATE)
  Fault will be reported to $\overline{\text{FAULT}}$ pin. This is a latched shut down, so gate driver will not be recovered automatically even if OT condition is not present anymore. An EN_GATE reset through pin is required to recover gate driver to normal operation after temperature goes below a preset value, t_{OTSD_CLR}.

Fault and Protection Handling

The $\overline{\text{FAULT}}$ pin indicates an error event with shut down has occurred such as over-current, over-temperature, over-voltage, or under-voltage. Note that $\overline{\text{FAULT}}$ is an open-drain signal. $\overline{\text{FAULT}}$ will go high when gate driver is ready for PWM signal (internal EN_GATE goes high) during start up.

The $\overline{\text{OCTW}}$ pin indicates an over temperature or over current event that is not necessarily related to shut down.

Following is the summary of all protection features and their reporting structure:

Table 1. Fault and Warning Reporting and Handling

EVENT	ACTION	LATCH	REPORTING ON $\overline{\text{FAULT}}$ PIN	REPORTING ON $\overline{\text{OCTW}}$ PIN
PVDD undervoltage	External FETs HiZ; Weak pull down of all gate driver output	N	Y	N
DVDD undervoltage	External FETs HiZ; Weak pull down of all gate driver output; When recovering, reset all status registers	N	Y	N
GVDD undervoltage	External FETs HiZ; Weak pull down of all gate driver output	N	Y	N
GVDD overvoltage	External FETs HiZ; Weak pull down of all gate driver output Shut down the charge pump Won't recover and reset through SPI reset command or quick EN_GATE toggling	Y	Y	N
OTW	None	N	N	Y
OTSD_GATE	Gate driver latched shut down. Weak pull down of all gate driver output to force external FETs HiZ Shut down the charge pump	Y	Y	Y
OTSD_BUCK	OTSD of Buck	Y	N	N
Buck output undervoltage	UVLO_BUCK: auto-restart	N	Y, in PWRGD pin	N
Buck overload	Buck current limiting (HiZ high side until current reaches zero and then auto-recovering)	N	N	N
External FET overload – current limit mode	External FETs current Limiting (only OC detected FET)	N	N	Y
External FET overload – Latch mode	Weak pull down of gate driver output and PWM logic "0" of LS and HS in the same phase. External FETs HiZ	Y	Y	Y
External FET overload – reporting only mode	Reporting only	N	N	Y

PIN CONTROL FUNCTIONS

EN_GATE

EN_GATE low is used to put gate driver, charge pump, current shunt amplifier, and internal regulator blocks into a low power consumption mode to save energy. Device will put the MOSFET output stage to high impedance mode as long as PVDD is still present.

When EN_GATE pin goes to high, it will go through a power up sequence, and enable gate driver, current amplifiers, charge pump, internal regulator, etc and reset all latched faults related to gate driver block. All latched faults can be reset when EN_GATE is toggled after an error event unless the fault is still present.

When EN_GATE goes from high to low, it will shut down gate driver block immediately, so gate output can put external FETs in high impedance mode. It will then wait for 10us before completely shutting down the rest of the blocks. A quick fault reset mode can be done by toggling EN_GATE pin for a very short period (less than 10µS). This will prevent device to shut down other function blocks such as charge pump and internal regulators and bring a quicker and simple fault recovery.

One exception is to reset a GVDD_OV fault. A quick EN_GATE quick fault reset won't work with GVDD_OV fault. A complete EN_GATE with low level holding longer than 10 µs is required to reset GVDD_OV fault. It is highly recommended to inspect the system and board when GVDD_OV occurs.

EN_BUCK

Buck enable pin, internal pull-up current source. Pull below 1.2 V to disable. Float to enable.

DTC

Dead time can be programmed through DTC pin. A resistor should be connected from DTC to ground to control the dead time. Dead time control range is from 50ns to 500ns. Short DTC pin to ground will provide minimum dead time (50ns). Resistor range is 0 to 150kΩ. Dead time is linearly set over this resistor range.

Current shoot through prevention protection will be enabled in the device all time independent of dead time setting and input mode setting.

DC_CAL

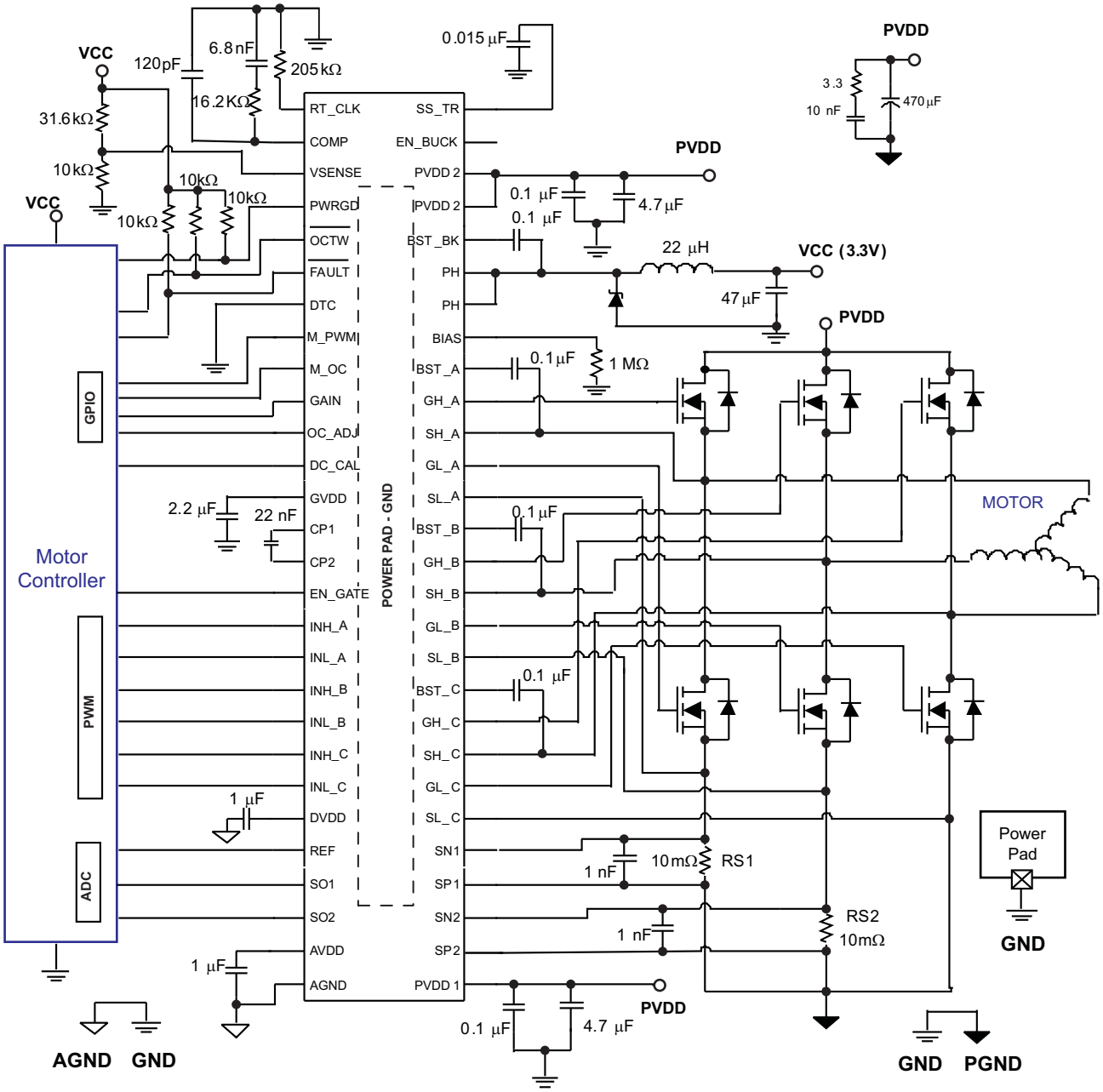
When DC_CAL is enabled, device will short inputs of shunt amplifier and disconnect from the load, so external microcontroller can do a DC offset calibration.

STARTUP AND SHUTDOWN SEQUENCE CONTROL

During power-up all gate drive outputs are held low. Normal operation of gate driver and current shunt amplifiers can be initiated by toggling EN_GATE from a low state to a high state. If no errors are present after a 10-ms wait time, the DRV8302 is ready to accept PWM inputs. Gate driver always has control of the power FETs even in gate disable mode as long as PVDD is within functional region.

APPLICATION SCHEMATIC EXAMPLE

Example:
Buck: PVDD= 3.5V – 40V, Iout_max = 1.5A, Vo = 3.3V, Fs = 570 kHz



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV8302DCA	ACTIVE	HTSSOP	DCA	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8302	Samples
DRV8302DCAR	ACTIVE	HTSSOP	DCA	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8302	Samples

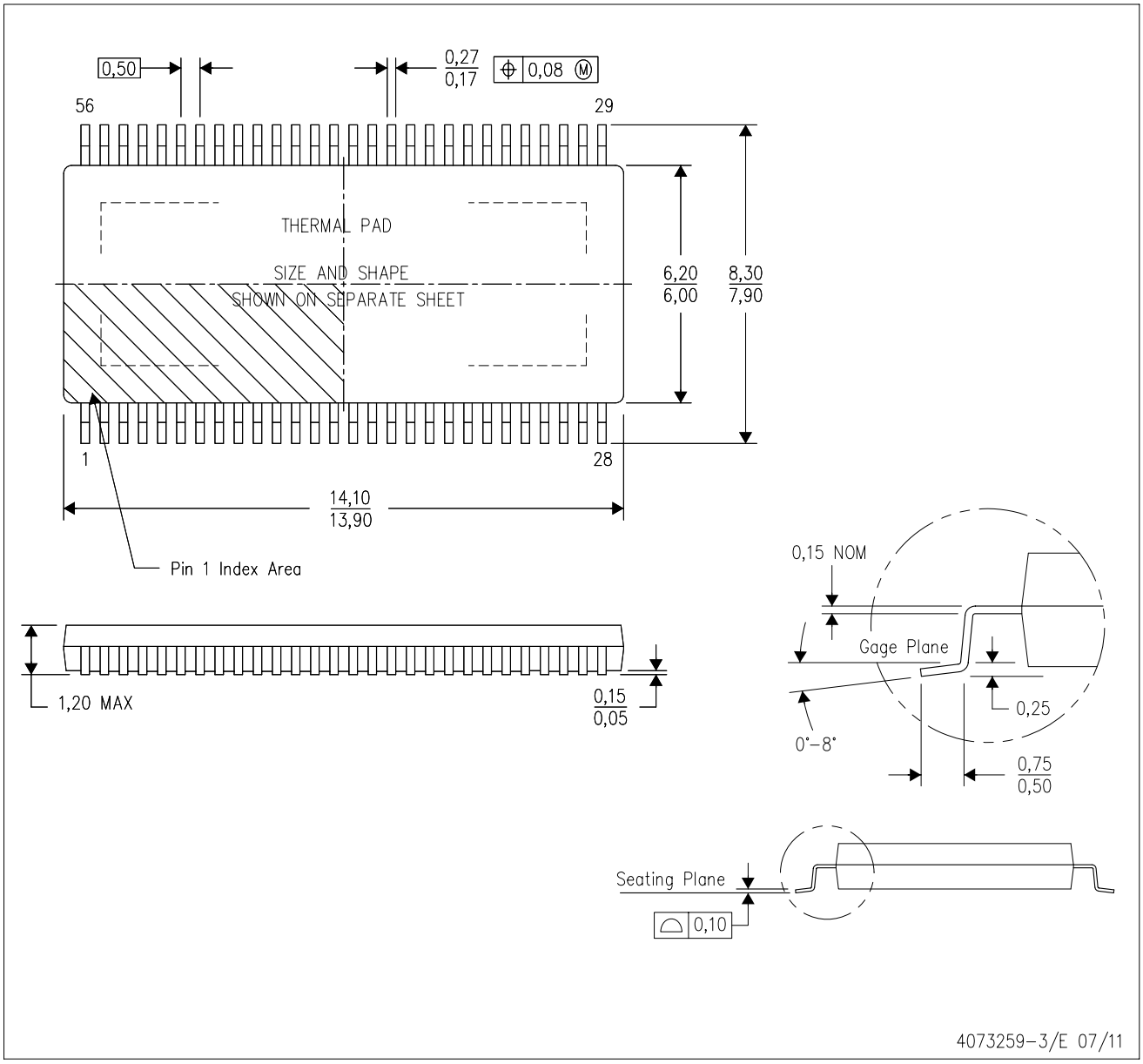
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

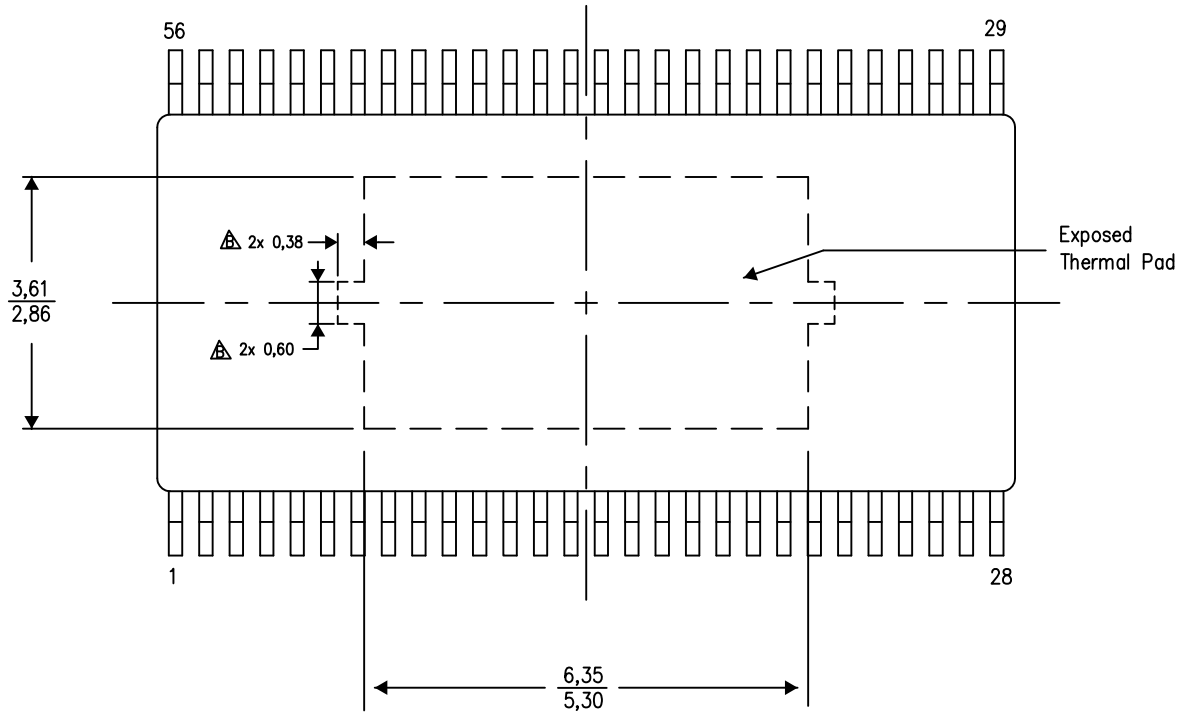
DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

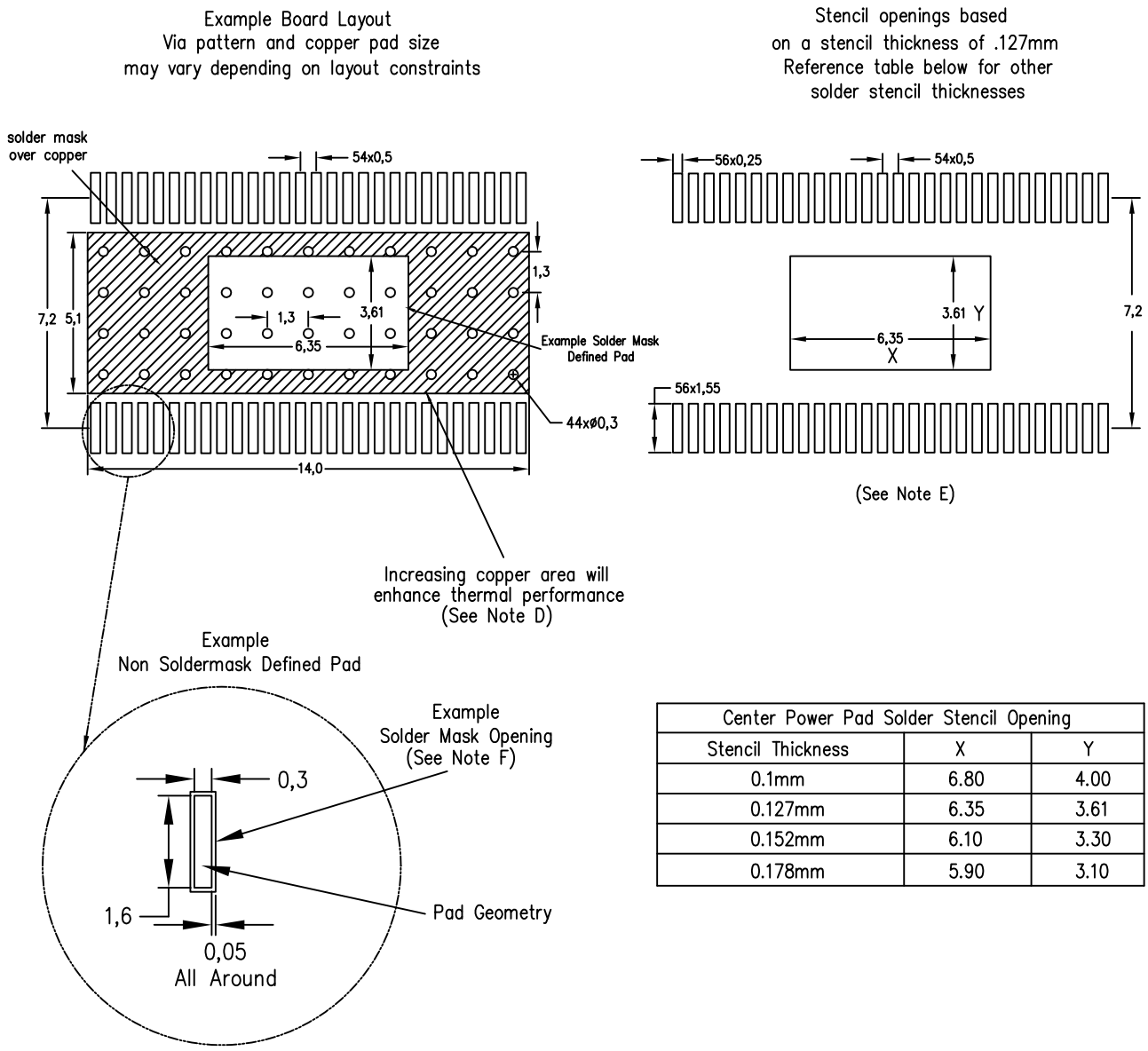
4206320–15/R 03/13

NOTES: A. All linear dimensions are in millimeters

B. Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.80	4.00
0.127mm	6.35	3.61
0.152mm	6.10	3.30
0.178mm	5.90	3.10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments:

DRV8302DCA DRV8302DCAR