Massine **BITAM**

Hardware Engineer · Front-end Asic

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Work Experience

NXP Semiconductors

Nice (Sophia Antipolis), France

Final-year Internship, Digital Power Optimization

March. 2016 - Exp. Aug. 2016

- Working on power consumption optimisation on the digital part of a mixed signal IC (Audio Amplifier).
- Gate level simulation and TCF dumping for power comsumption analysis, indentification of power bugs and huge power wastage of different blocks on the design.
- Exploring power saving opportunity, clock gating insertion, implementation of Self gating technique on blocks with asynchronious events.
- implementation of Dynamic frequency scaling (DFS) based on running mode of the circuit.
- Low Power synthesis and logic equivqlence checking after RTL update.
- study of advanced power reduction techniques such as PSO, DVFS, Power partitioning...
- Agressive power reduction using common Power Format (CPF) on the design flow.
- Possible change of the PLL IP and redesign clock deviders on the CGU.
- Tools Used : Cadence..., Power-Artist.
- Environement: Linux (Redhat), VHDL, VERILOG, TCL.

LIP6 Center for Scientific Research

Paris, France

Summer Intern (RTL Designer)

June. 2015 - Aug. 2015

- Study and profiling of a SystemC (CABA) model of a VCI AHCI SDCard controller component.
- Description, modeling and implementation with VHDL as part of the TSAR project.
- Functional verification, cosimulation (SystemC/VHDL) using ModelSim in a virtual prototype architecture with Soclib components and the GIET_VM operating system.

Tutored Projects

Tutored Project

Univ P & M Curie

VLSI - Synthesis, Place and route of a five stage pipeline MIPS32

Feb. 2015, May. 2015

- Full VLSI process: Synthesis, P&R, floor planning, static timing analysis will be carried out on the VHDL code of a MIPS32 using Cadence tools.

Tutored Project

Univ P & M Curie

Implementation of a cache coherency protocol

Feb. 2015, May. 2015

- Modeling, and implementation of two cache coherency protocols using Java in a multi-processor system.
- Implementation of Write Through Invalidate and Write Back MESI protocols for the L1 and Memory controllers.i

Tutored Project

Univ P & M Curie

Real-Time audio compression wit SocKit SoC

Feb. 2015, May. 2015

- Cross-compiling and porting the Vorbis audio codec and Linux kernel on a SoC platform (SocKit board) targeting an ARM Cortex A9 architecture.
- Synthesis of the Altera audio codec IP on the FPGA (Cyclone V).
- Memory mapping redefinition of a baremetal code that runs under Linux to read an input stream, compress it and store it on the file system.i

Tutored Project

Univ P & M Curie

Design and implementation of a DCC controller

Mar. 2015, May. 2015

- Cross-compiling and porting the Vorbis audio codec and Linux kernel on a SoC platform (SocKit board) targeting an ARM Cortex A9 architecture.
- Synthesis of the Altera audio codec IP on the FPGA (Cyclone V).
- Memory mapping redefinition of a baremetal code that runs under Linux to read an input stream, compress it and store it on the file system.

Tutored Project

Univ P & M Curie

Implementation of an AMD2901 chip

Oct. 2014, Jan. 2014

- VHDL behavioural and structural description.
- Simulation and verification of the functional characteristics using GHDL.
- Synthesis, P&R using Alliance and Coriolis (open source tools for VLSI conception).
- Timing analysis and frequency optimization.

Education

University Pierre and Marie Curie

Paris, France

Master's Degree (Embedded Systems)

2014 - PRESENT

- Got a Chun Shin-Il Scholarship which is given to promising students in CSE Dept.

University of Oran — *Oran, Algeria*

Master's Degree, Network and Distributed Systems — *2013 - 2014, first year only*

University of Oran — *Oran, Algeria*

Bachelor's degree, Computer Science — *2010 - 2013, Graduated*

Skills

Programming	C/C++, VHDL, Verilog, SystemC, Mips Assembly, Java, Python, Shell script, Tcl, LaTeX
Tools	Cadence tools, ISE, Quartus, ModelSim, Git, Design-Sync, Makefile, Android Studio, vim, Office tools
Platform	Linux, Windows, Android
Platform	SocKit(Altera), Arduino
Protocols	VCI, DSPIN, DHCCP, AHCI, SdCard, JTAG, I2C, TCP/IP
Languages	Kabyle (Mother tongue), English, French and Arabic

Interest & Activities

- Sport: Football, Running trails.
- Music: Jazz, Pop-Rock, Alternative.
- Reading.

Miscellaneous

- Strong knowledge in low level programming and object oriented programming.
- Strong background in computer architecture: pipeline, cache-subsytems, coherence protocols, virtual memory, out-of-order execution, branch prediction, compilation optimization, network on chip, GALS systems, SMP/ccNUMA architectures.
- Strong background in Digital Design, RTL coding, FPGA prototyping, VLSI Design and IP block implementation.
- Self-educated in SoC verification using System-Verilog (on going), following a course on Udemy, cadence training (introduction to UVM for System-verilog) and Mentor Graphics verification academy courses (on going).
- Deep knowledge in Unix/Linux systems.
- Ability to work independently as well as in a team environment.