HARDWARE DESIGN VERIFICATION CHECKLIST				
TASKS / SUBTASKS	12/4/2014	12/9/2014	12/11/2014	12/16/2014
Subunits compile and simulate clean				
VCS compile for each subunit without unexpected warnings				
DC compile (elaborate and check) for each subunit without unexpected warnings				
Subunits with their own testbench should sim clean				
Unit compiles clean				
VCS compile for unit without unexpected warnings				
DC compile (elaborate and check) for unit without unexpected warnings				
Reset tests				
Basic reset (beginning of simulation)				
Dynamic reset (middle of simulation)				
Commission order				
The commission order should be the same as the order in the instruction queue				
Commission number				
Verify commission number without data dependency				
Verify commission number with complete data dependency				
Verify numbers of load/store instructions committed (should be only one for each)				
Verify numbers of jump/branch instructions feedbacks (should be only one for each)				
Verify commission number with mixed dependency randomly				
Fullness of the ROB				
Verify ROB_full with complete dependent instruction sequences				
Instruction arithmetic/logical instructions				
Verify consecutive addition/subtraction instructions with independent registers				
Verify consecutive addition/subtraction instructions with dependent registers				
Verify consecutive logical instructions with independent registers				
Verify consecutive logical instructions with dependent registers				
Verify consecutive shifting instructions with independent registers				
Verify consecutive shifting instructions with dependent registers				
Verify consecutive comparison instructions with independent registers				

Verify consecutive comparison instructions with dependent registers				
Verify mixed arithmetic/logical instructions with independent registers				
Verify mixed arithmetic/logical instructions with dependent registers				
Load/Store instructions				
Verify consecutive loads with independent addresses				
Verify consecutive loads with the same/limited addresses				
Verify consecutive stores with independent addresses				
Verify consecutive stores with the same/limited addresses				
Verify consecutive interleaved loads/stores with independent addresses				
Verify consecutive interleaved loads/stores with the same/limited addresses				
Jump				
Verify jump target PC				
Verify jump flush PC (branch_PC)				
Branch when misprediction				
Verify branch decision				
Verify branch target PC				
Verify branch flush PC (jump_PC)				
Random halts and related events				
Randomly halt and resume				
Randomly halt, do cache flush, and resume				
Final random testing and coverage assessment				
Randomize the testbench parameters				
Run at least 10 thousands cycles of random simulation				
Performance validation				
Exception event hit rate				
Performance gains				
Overall bandwidth				
Overall latency				